



# STP3NK80Z - STF3NK80Z STD3NK80Z - STD3NK80Z-1

N-channel 800V - 3.8Ω - 2.5A - TO-220/TO-220FP/DPAK/IPAK  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>
STP3NK80Z	800 V	< 4.5 Ω	2.5 A
STF3NK80Z	800 V	< 4.5 Ω	2.5 A
STD3NK80Z	800 V	< 4.5 Ω	2.5 A
STD3NK80Z-1	800 V	< 4.5 Ω	2.5 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

## Description

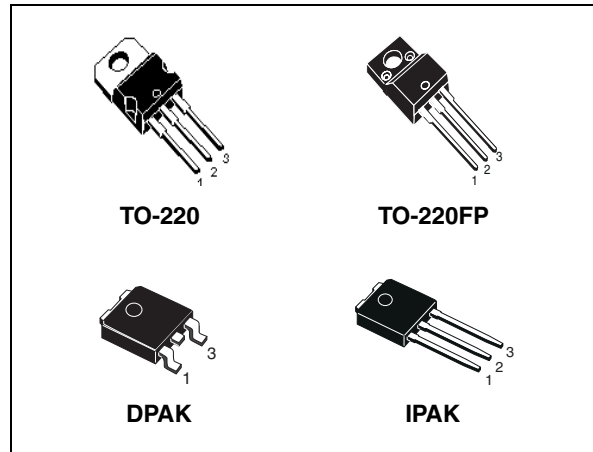
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## Applications

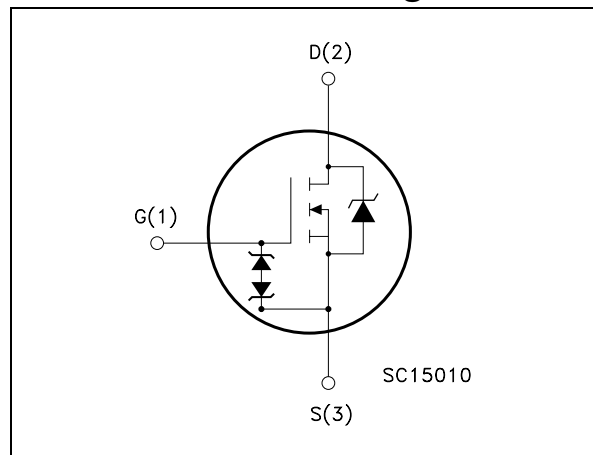
- Switching application

## Order codes

Part number	Marking	Package	Packaging
STP3NK80Z	P3NK80Z	TO-220	Tube
STF3NK80Z	F3NK80Z	TO-220FP	Tube
STD3NK80ZT4	D3NK80Z	DPAK	Tape & reel
STD3NK80Z-1	D3NK80Z	IPAK	Tube



## Internal schematic diagram



# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
1.1	Protection features of gate-to-source zener diodes .....	4
<b>2</b>	<b>Electrical characteristics</b> .....	<b>5</b>
2.1	Electrical characteristics (curves) .....	7
<b>3</b>	<b>Test circuit</b> .....	<b>10</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>11</b>
<b>5</b>	<b>Packing mechanical data</b> .....	<b>16</b>
<b>6</b>	<b>Revision history</b> .....	<b>17</b>

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220 / DPAK IPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	800		V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20K\Omega$ )	800		V
$V_{GS}$	Gate-source voltage	$\pm 30$		V
$I_D$	Drain current (continuous) at $T_C = 25^\circ C$	2.5	2.5 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ C$	1.57	1.57 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	10	10 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ C$	70	25	W
	Derating factor	0.56	0.2	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5K $\Omega$ )	2		V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
$V_{ISO}$	Insulation withstand voltage (DC)	-	2500	V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 2.5A$ ,  $di/dt \leq 200A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	DPAK IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.78	5	1.78	°C/W
$R_{thj-a}$	Thermal resistance junction-ambient max	62.5		100	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300			°C

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	170	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

## 1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1mA, V_{GS} = 0$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating},$ $T_c = 125^{\circ}C$			1 50	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{GS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 10$	$\mu A$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 50\mu A$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 1.25 A$		3.8	4.5	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 1.25A$		2.1		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		485		pF
$C_{oss}$	Output capacitance			57		pF
$C_{rss}$	Reverse transfer capacitance			11		pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 640V$		22		pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400V, I_D = 1.25A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see <a href="#">Figure 18</a> )		17		ns
$t_r$	Rise time			27		ns
$t_{d(off)}$	Off-voltage rise time			36		ns
$t_f$	Fall time			40		ns
$Q_g$	Total gate charge	$V_{DD} = 640V, I_D = 2.5A$ $V_{GS} = 10V$		19		nC
$Q_{gs}$	Gate-source charge			3.2		nC
$Q_{gd}$	Gate-drain charge			10.8		nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.  $C_{oss \text{ eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				10	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=2.5\text{ A}$ , $V_{GS}=0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD}=2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=50\text{ V}$ , $T_j=25^\circ\text{C}$ (see <a href="#">Figure 20</a> )		384		ns
$Q_{rr}$	Reverse recovery charge			1600		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			8.4		A
$t_{rr}$	Reverse recovery time	$I_{SD}=2.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=50\text{ V}$ , $T_j=150^\circ\text{C}$ (see <a href="#">Figure 20</a> )		474		ns
$Q_{rr}$	Reverse recovery charge			2100		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			8.8		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220/DPAK/IPAK

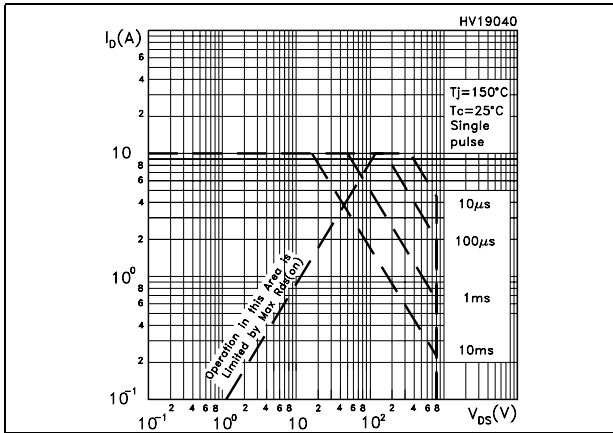


Figure 2. Thermal impedance for TO-220/DPAK/IPAK

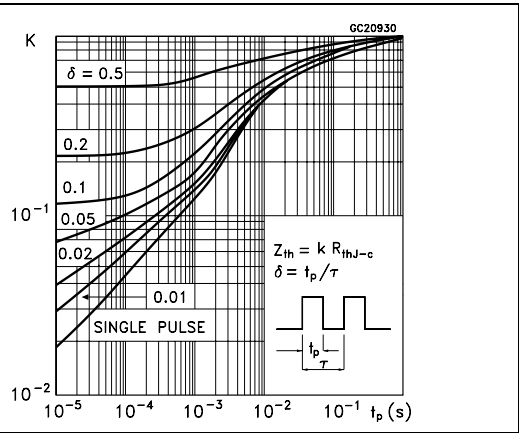


Figure 3. Safe operating area for TO-220FP (HV19050)

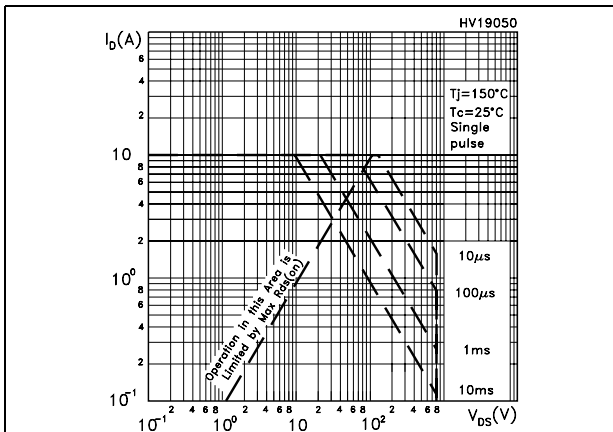


Figure 4. Thermal impedance for TO-220FP

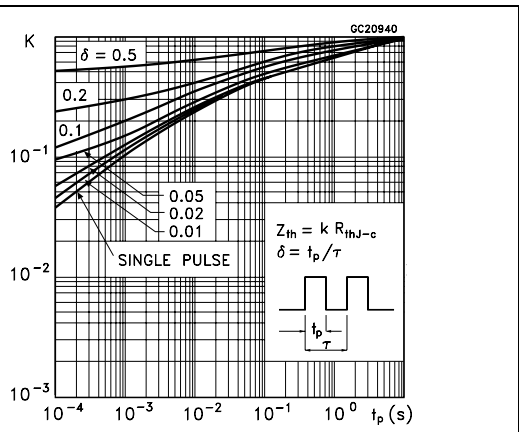


Figure 5. Output characteristics

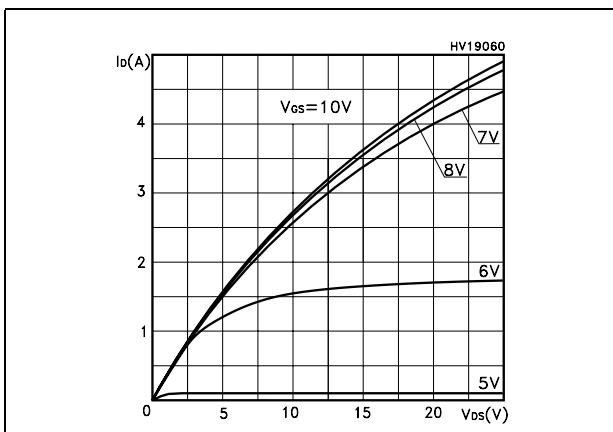


Figure 6. Transfer characteristics

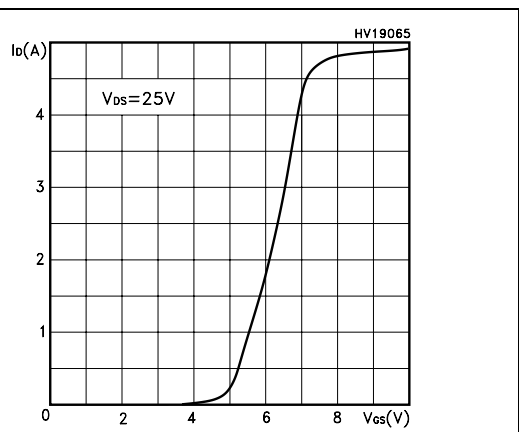


Figure 7. Transconductance

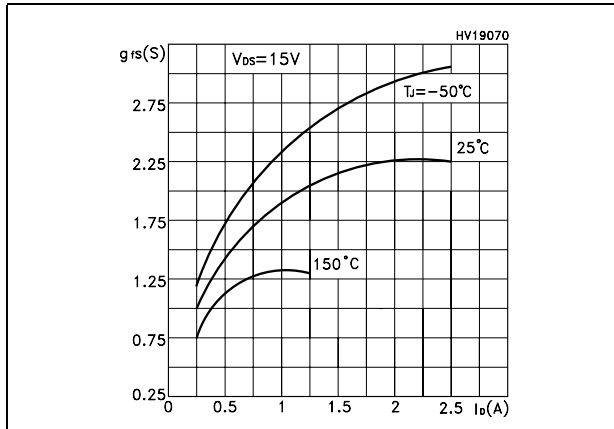


Figure 8. Static drain-source on resistance

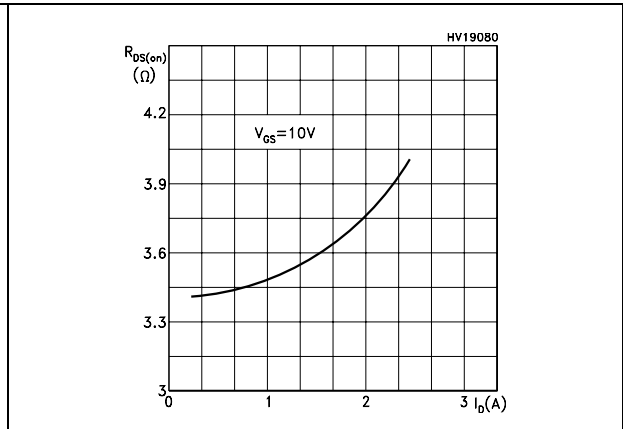


Figure 9. Gate charge vs gate-source voltage

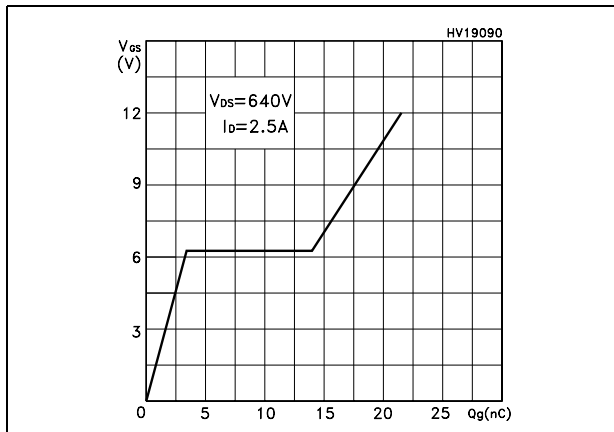


Figure 10. Capacitance variations

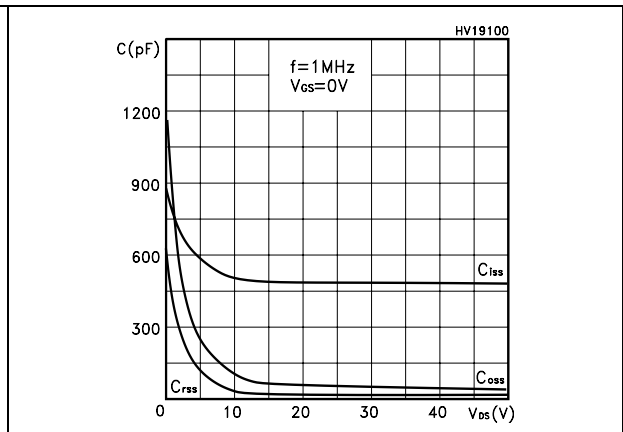


Figure 11. Normalized gate threshold voltage vs temperature

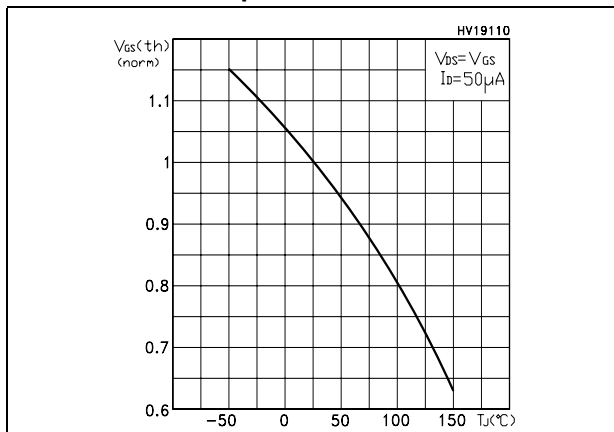


Figure 12. Normalized on resistance vs temperature

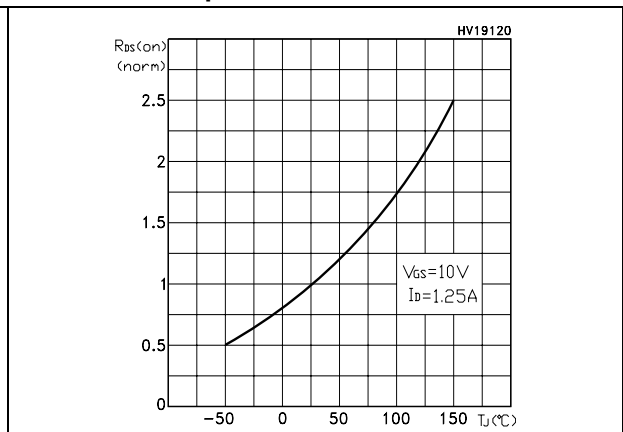




Figure 13. Source-drain diode forward characteristics

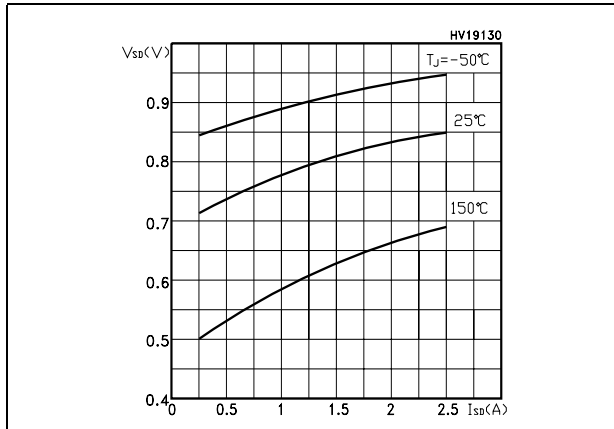


Figure 14. Normalized  $B_{VDSS}$  vs temperature

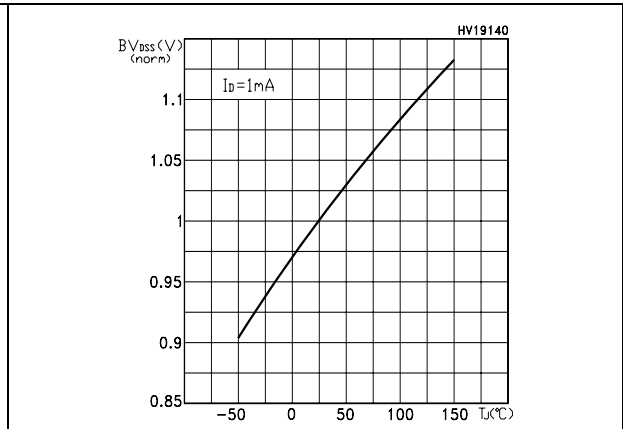
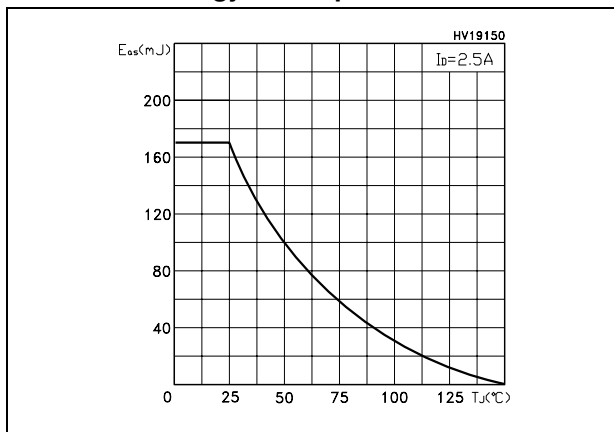


Figure 15. Maximum avalanche energy vs temperature



### 3 Test circuit

Figure 16. Unclamped Inductive load test circuit

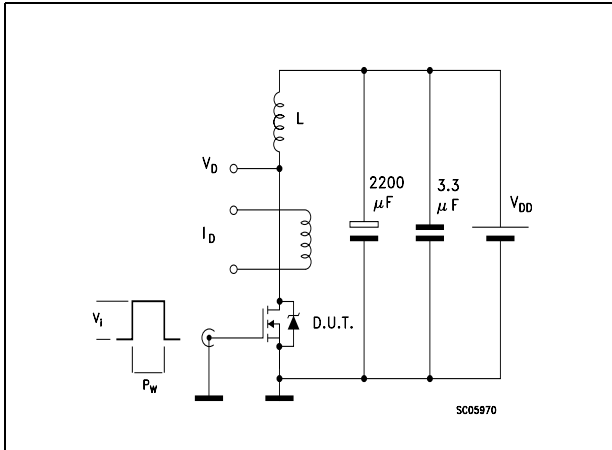


Figure 17. Unclamped Inductive waveform

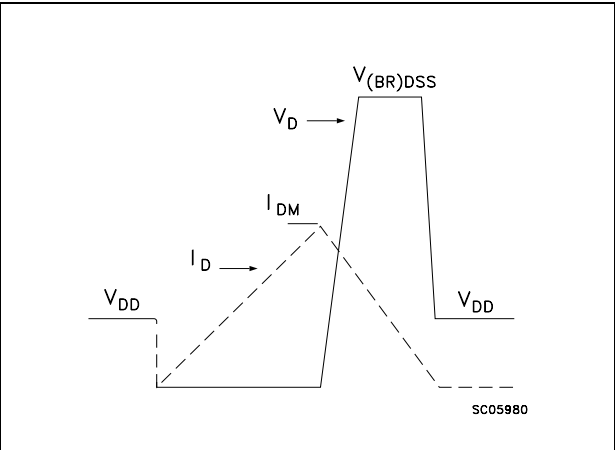


Figure 18. Switching times test circuit for resistive load

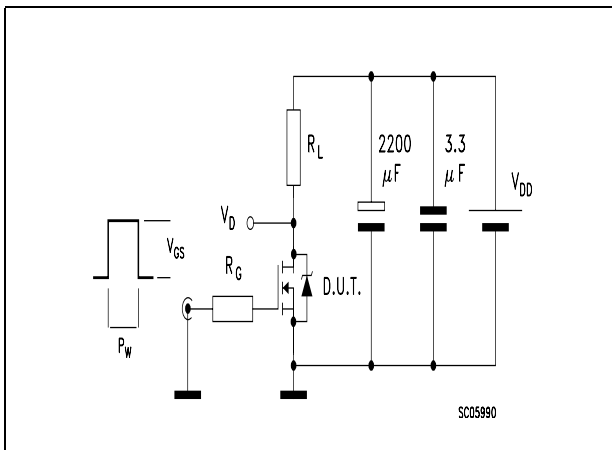


Figure 19. Gate charge test circuit

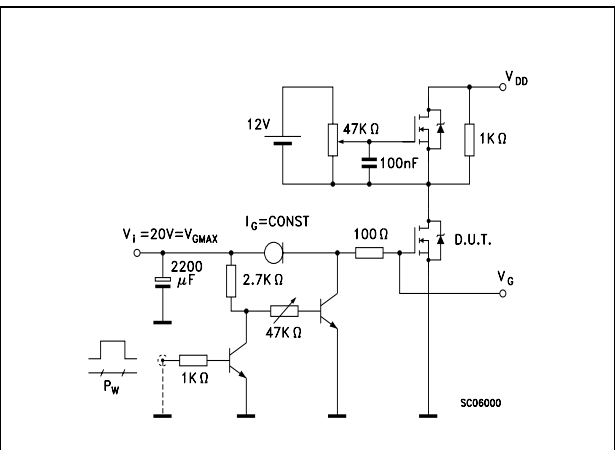
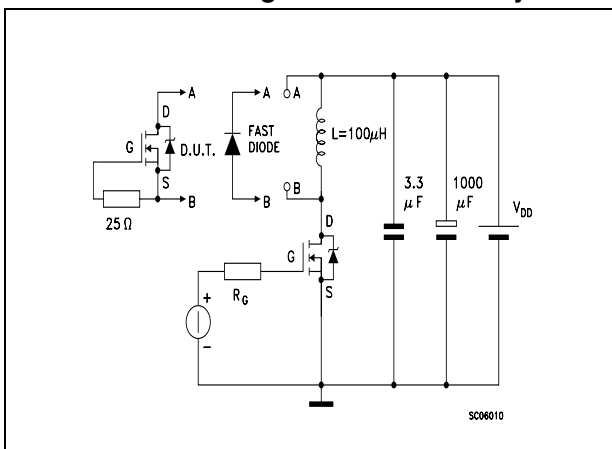


Figure 20. Test circuit for inductive load switching and diode recovery times

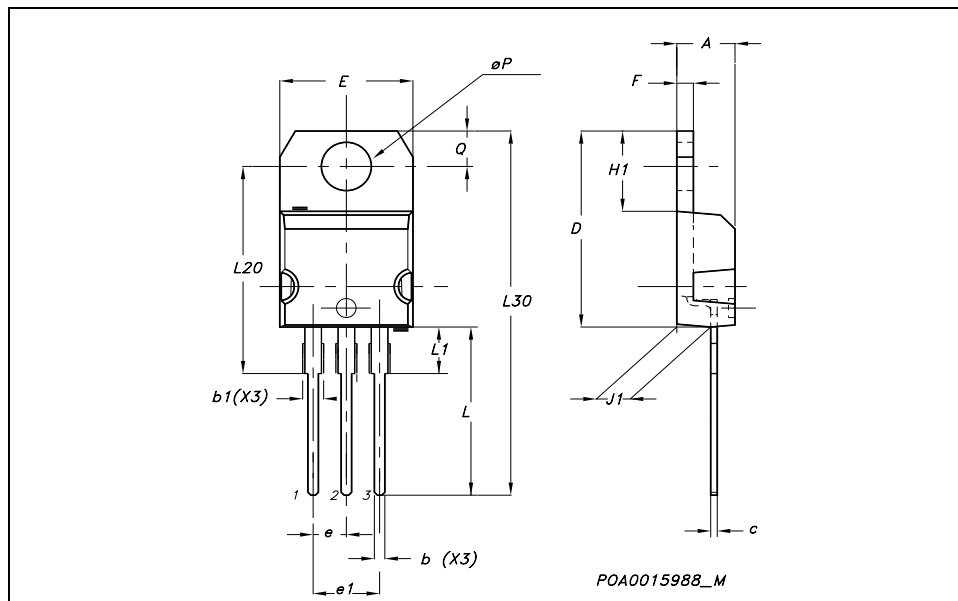


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

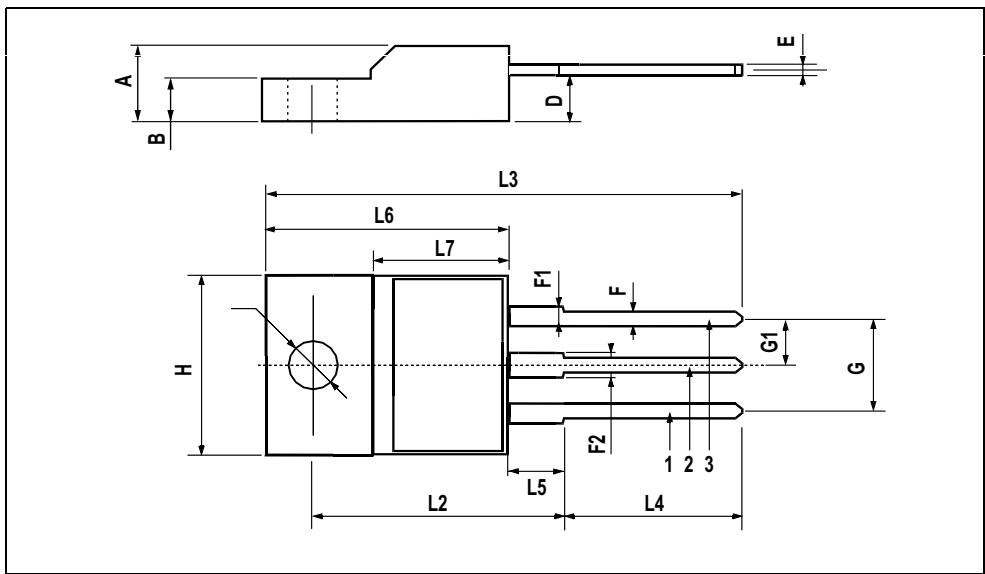
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



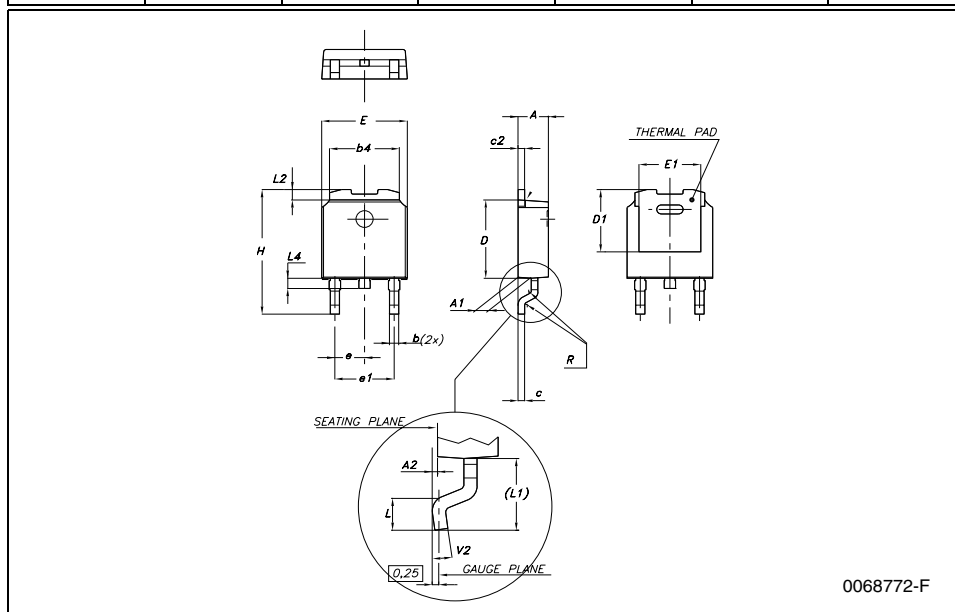
**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



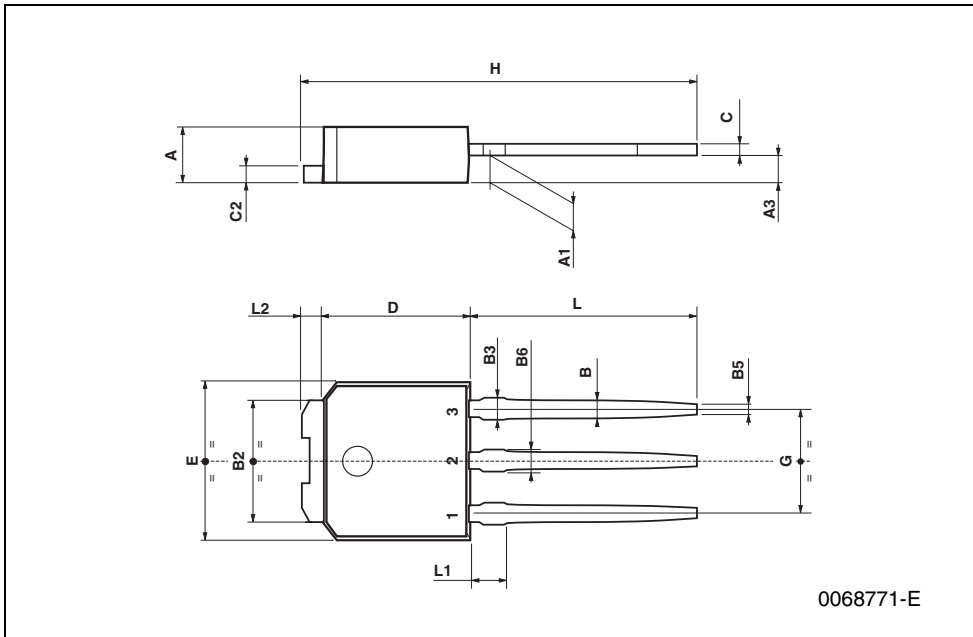
**DPAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



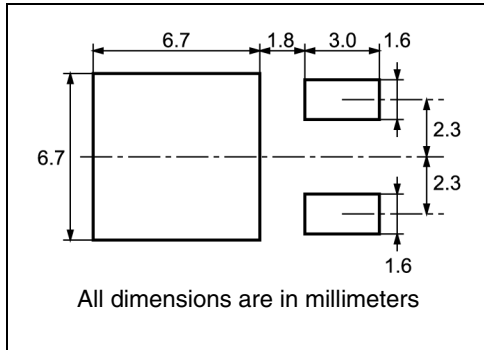
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



# 5 Packing mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

### REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

TRL

FEED DIRECTION

Bending radius R min.

For machine ref. only including draft and radii concentric around B0