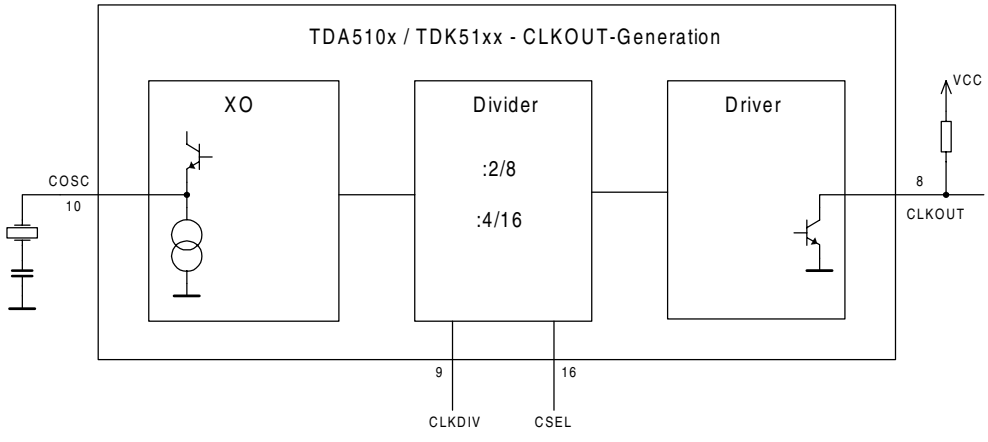
1 CLKOUT-Output at startup of the Crystal-Oscillator

Blockdiagram of the CLKOUT-Generation:



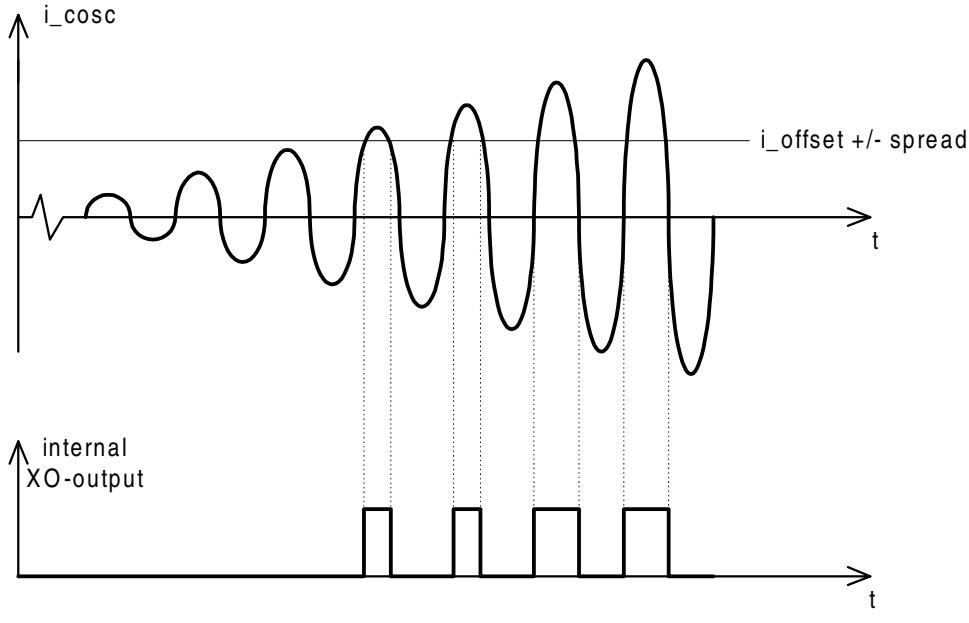
CLKOUT-Generation.wmf

Figure 1 CLKOUT-Generation

When the IC is switched from power-down-mode into PLL-enable-mode, the crystal oscillator initially starts oscillation by the noise current. During startup the amplitude of the oscillator current rises exponentially until, due to the nonlinear transfer characteristic of the oscillator, its stable final value is reached.

The clock input of the following divider chain comprises an offset. If the crystal oscillator output current overcomes this offset, the divider starts toggling. This built in offset is stable (production tolerance a few % and a very small temperature coefficient), but has superimposed a statistical component due to nonideal component matching. So, the absolut value of this offset varies over the production spread and as a result the CLKOUT shows up toggling for different values of the instantaneous increasing oscillator current.

The principle is shown in the next figure.



timing_simplified_v003.wmf

Figure 2 Timing simplified

It is clear, that the starting point of toggling varies with the spread of the offset-current and the instantaneous crystal oscilllator current.

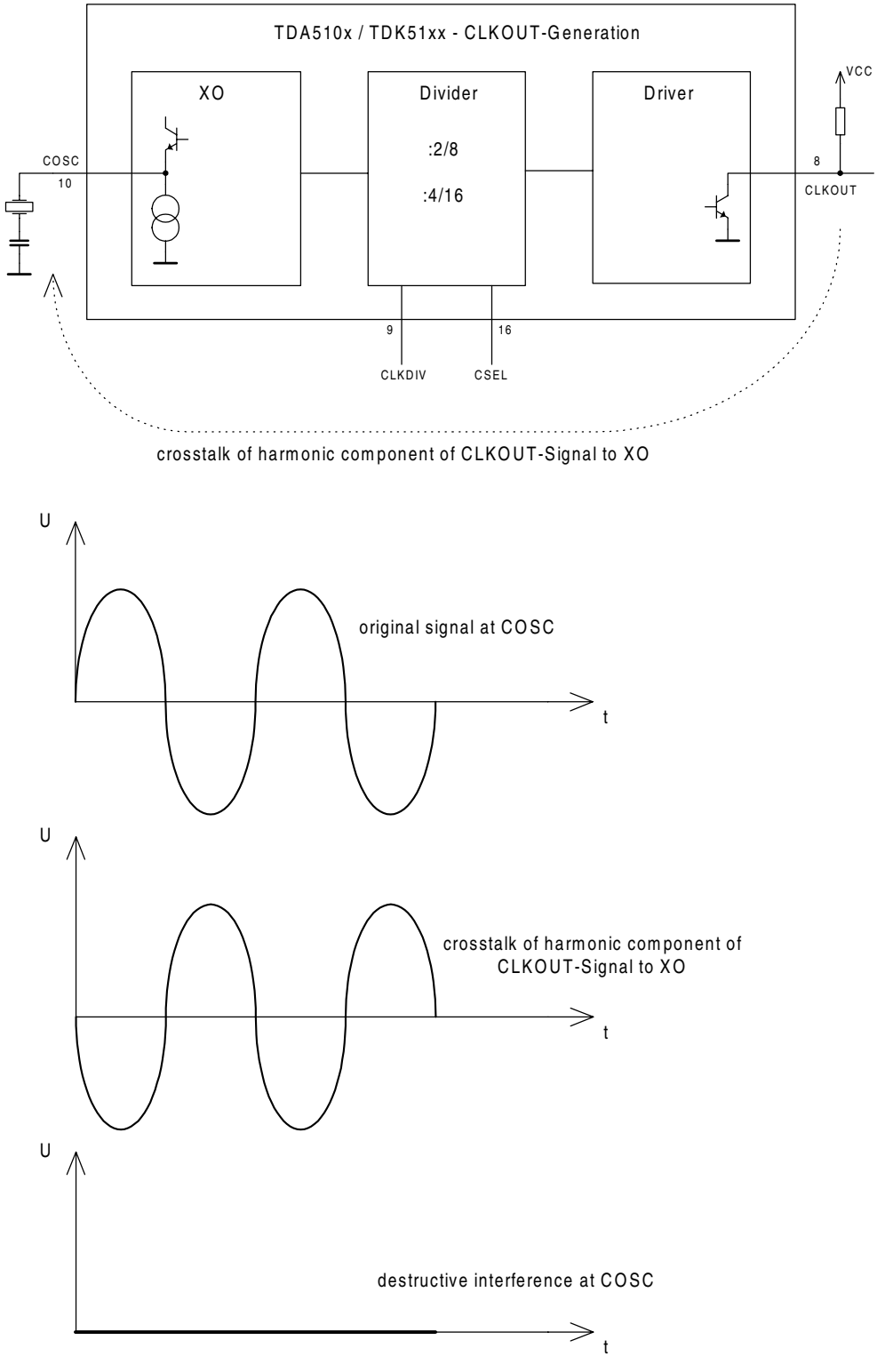
2 Coupling between CLKOUT and XO

Ideally the CLKOUT signal is a symmetrical rectangular waveform, which contains no even harmonics, and the divider factor is an even number, so the CLKOUT spectrum should have no component at the crystal oscillator frequency.

Considering a resistive/capacitive load at the asymmetrical CLK output the rising and falling edges of the waveform are not symmetrical any longer. Also the duty cycle is different from 50 %. For such a realistic application the even harmonics are not equal zero. Depending on the divider factor, we find a small spectrum component at the crystal oscillator frequency. Due to the parasitic coupling between the CLKOUT and COSC input a destructive interference can occur, which degrades the instantaneous gain factor of the oscillator circuit. If this gain becomes smaller than one, the oscillator stops oscillation.

This only can happen, if the **gain and phase** conditions are fulfilled. So a lot of external parameters, like load resistor and capacitor, groundplane and most important PCB layout are involved. On chip the built in offset of the crystal-oscillator plays the major role. The **smaller** the offset, the **more sensitive** the complete system.

The absolute worstcase is illustrated in the next figure.



Interference.wmf

Figure 3 Interference

3 Testing of existing Applications

If the isolation between CLKOUT and COSC is high enough, the startup of the XO is no problem.

If the isolation between CLKOUT and COSC is **critical**, the function of the IC depends on the internal offset-current of the crystal-oscillator. This offset is different for each IC and also varies slightly over temperature.

With an external forced offset current, the offset can be altered for testing purposes.

Whether the isolation between COSC and CLKOUT is high enough or not can be tested with following test-setup:

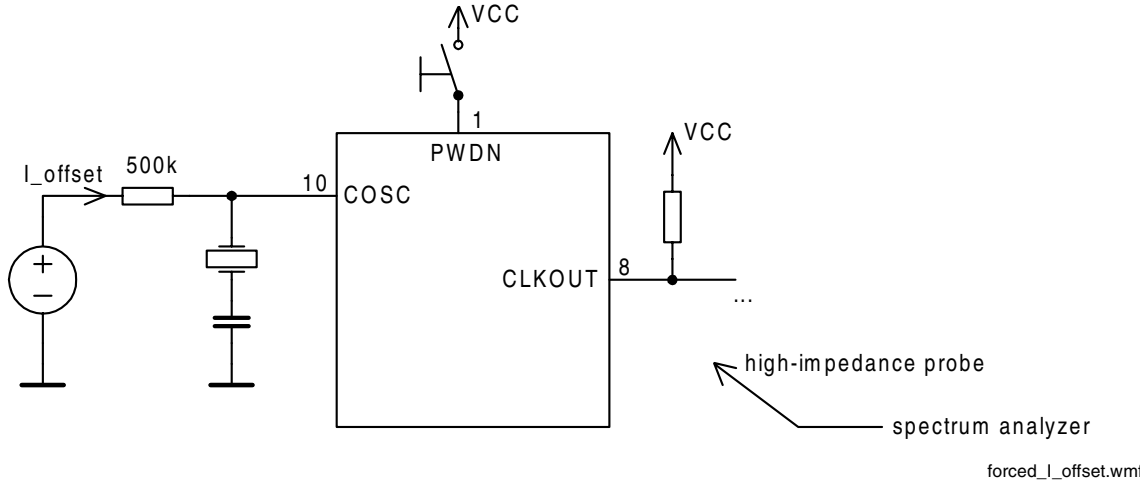


Figure 4 Forced Offset

Since the coupling between CLKOUT and COSC is only a problem at startup, the PLL-Enable-Mode has to be triggered each time for testing. This is done with a push-button from pin PWDN to VCC. A logic high at PWDN activates the PLL-enable-mode.

A spectrum analyzer with a high impedance probe near the CLKOUT-PCB-trace is used to monitor the CLKOUT-signal. The probe should not touch the trace, so the circuit is not influenced by the probe. After triggering the PLL-enable-mode, there should be a CW-signal on the spectrum analyzer at 3.39MHz (CLKDIV=low) or 847.5kHz (CLKDIV=high). If this is not the case, the XO did not start up properly. This has to be tested at different I_offset at pin COSC. (+/- a few uA) In the schematic above this is done by using a variable voltage source and a high resistance. If your PCB fails at any I_offset, the layout of the PCB is not OK and a redesign is recommended (see **Chapter 4**).

If your PCB does not fail at any I_offset, another test is required to take care of variations of capactive/resistive loading at the CLKOUT over production, which incfluences the phase/amplitude at the harmonic component of the CLKOUT-signal. This will cause a different intereference-scenario at the XO. Before this test can be performed, the offset of the XO has to be tuned to zero for simulation of a worst case scenario, where the offset of the IC is zero. This can be done with following test-setup:

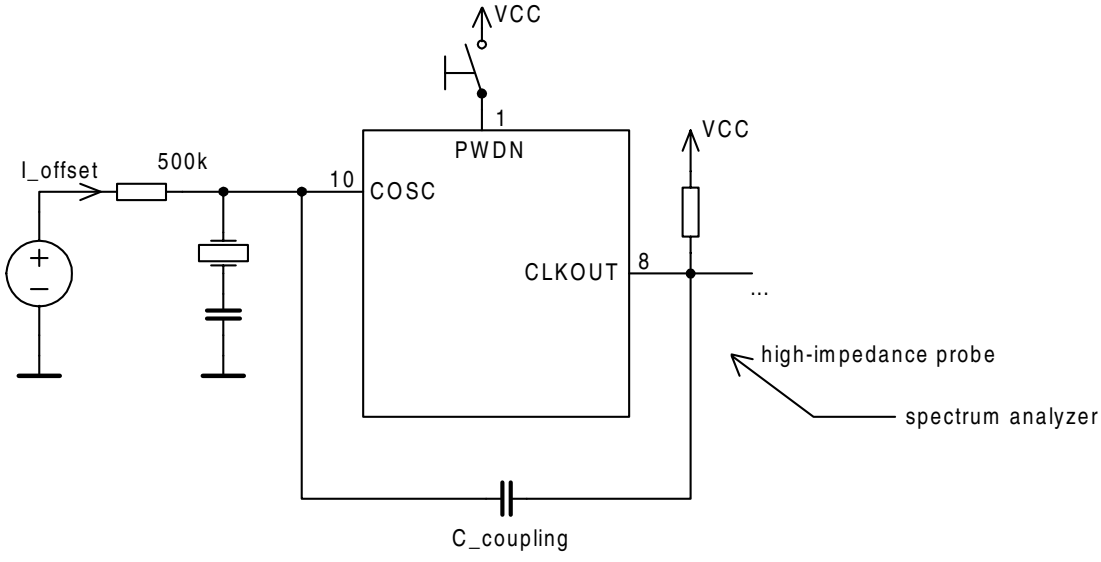


Figure 5 Nulling

C_coupling is a discrete capacitor, which has to be soldered on your PCB. This capacitor is simulating a bad PCB with significant coupling between CLKOUT and COSC. So this capacitor should be very small (0.5pF). Now I_offset has to be variied until the application fails. Then the offset of the XO is tuned to zero.

Next step of this test is the variation of the phase/magnitude of the CLKOUT-signal to take care of tolerances over production. This is done most easily by variing the pull-up-resistor of the CLKOUT. See next figure:

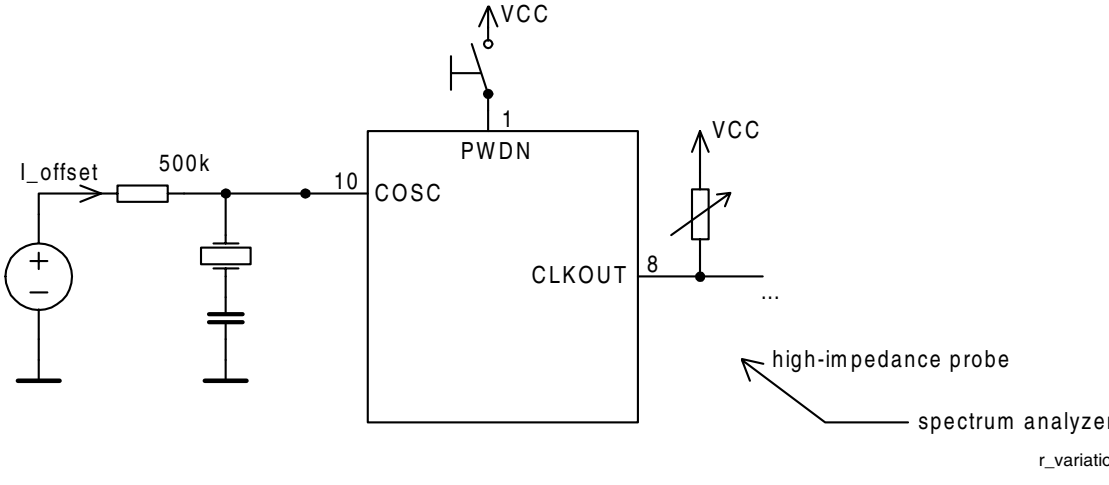


Figure 6 R_variation

The range of variation of the CLKOUT-resistor should be large enough to cover all tolerances. Assuming a tolerance of the parasitic capacitive loading of the CLKOUT of +/-20% and a tolerance of the pull-up-resistor of +/-10%, the CLKOUT-resistor should be varied by about +/-30% minimum. The resistor should be varied in small steps due to the fact that the phase of the harmonic comonent of the CLKOUT is strongly dependant on the time-constant. If the application starts up without any problem, the layout of the PCB is OK and no redesign is necessary.

4 Solutions

There are 2 possible solutions to get rid of the coupling-problem between CLKOUT and the XO on your PCB:

4.1 Better Layout

A better layout will decrease the coupling between CLKOUT and COSC. Separate the CLKOUT-trace and the parts at the XO as good as possible. Also use a good groundplane. For ASK-systems it is also possible to exchange the positions of crystal and series-tuning-capacitor. This might decrease coupling due to the smaller area of sensitive PCB-traces at the XO.

4.2 Delay of CLKOUT

Without the CLKOUT-interferer, the XO will start up without any problems. After the XO has started up, the signal at the XO is strong. If the CLKOUT is acitvated AFTER the startup of the XO, the crosstalk of the CLKOUT to the XO will have no influence any more due to the strong XO-signal. Without a pull-up at the CLKOUT-open-collector-output, there will be no signal. So a switch between the pull-up and VCC with some delay between triggering the PLL-Enable-Mode of the IC and activation of the CLKOUT will work.