Integrated Circuit Systems, Inc.

ICS9112-06/07

Low Skew Output Buffer

General Description

The **ICS9112** is a high performance, low skew, low jitter clock driver. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in PC systems operating at speeds from 25 to 75 MHz (30 to 90mHz for 5V operation).

ICS9112 is a zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

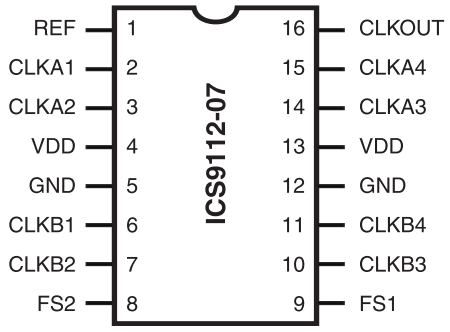
The **ICS9112** comes in with two different options; dash 06 and dash 07. The dash 07 is available in a 16 pin 150 mil SOIC package. It has two banks of four outputs controlled by two address lines. Depending on the selected address line, bank B or both banks can be put in a tri-state mode. In this mode, the PLL is still running and only the output buffers are put in a high impedance mode. The test mode shuts off the PLL and connects the input directly to the output buffers (see table below for functionality).

The dash 06 is an eight pin 150 mil SOIC package. It has five output clocks. In the absence of REF input, both **ICS9112-06** and **-07** will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

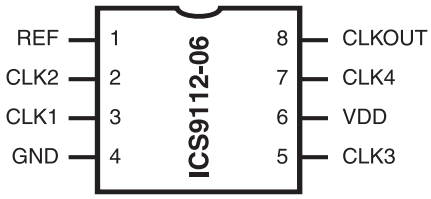
Features

- Zero input - output delay
- Frequency range 25 - 75 MHz (3.3V), 30-90MHz (5.0V)
- Less than 200 ps Jitter between outputs
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 8 or 16 pin versions, 150 mil SOIC packages
- 3.3V ±10%, 5.0V±10% operation

Pin Configuration

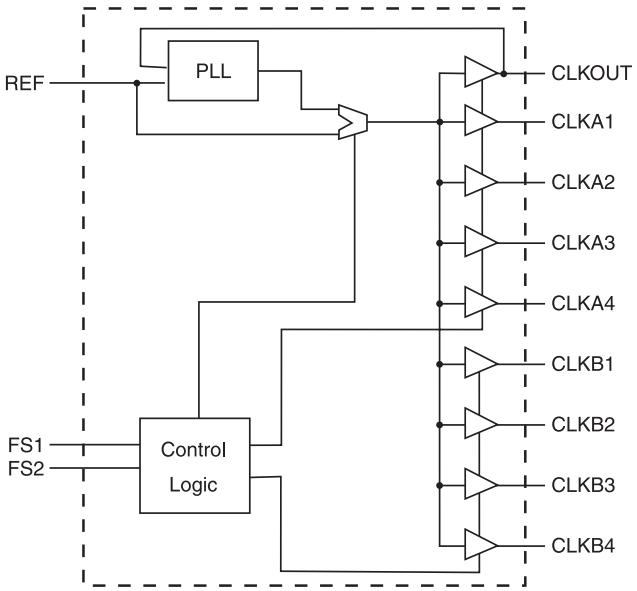


16 pin SOIC



8 pin SOIC

Block Diagram



Functionality (-07)

FS2	FS1	CLKA (1, 4)	CLKB (1, 4)	CLKOUT	Output Source	PLL Shutdown
0	0	Tristate	Tristate	Driven	PLL	N
0	1	Driven	Tristate	Driven	PLL	N
1	0	Test Mode	Test Mode	Test Mode	REF	Y
1	1	Driven	Driven	Driven	PLL	N

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF[2]	IN	Input reference frequency. 5V tolerant input
2	CLKA2[3]	OUT	Buffered clock output, Bank A
3	CLKA1[3]	OUT	Buffered clock output, Bank A
4, 13	VDD	PWR	3.3V supply
5, 12	GND	PWR	Ground
6	CLKB1[3]	OUT	Buffered clock output. Bank B
7	CLKB2[3]	OUT	Buffered clock output. Bank B
8	FS2[4]	IN	Select input, bit 2
9	FS1[4]	IN	Select input, bit 1
10	CLKB3[3]	OUT	Buffered clock output. Bank B
11	CLKB4[3]	OUT	Buffered clock output. Bank B
14	CLKA2[3]	OUT	Buffered clock output, Bank A
15	CLKA3[3]	OUT	Buffered clock output, Bank A
16	CLKOUT[3]	OUT	Buffered clock output, internal feedback on this pin

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF[2]	IN	Input reference frequency. 5V tolarant input
2	CLK2[3]	OUT	Buffered clock output
3	CLK3[3]	OUT	Buffered clock output
4	GND	PWR	Ground
5	CLK3[3]	OUT	Buffered clock output
6	VDD	PWR	3.3v Supply
7	CLK4[3]	OUT	Buffered clock output
8	CLK6 (CLKOUT)[3]	OUT	Buffered clock output. Internal feedback on this pin

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. Weak pull-down
3. Weak pull-down on all outputs
4. Weak pull-ups on these inputs

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V		19	50.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}		0.10	100.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL} = 8mA		0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = 8mA	2.4	2.9		V
Power Down Supply Current	I_{DD}	REF = 0 MHz		37.0	75.0	µA
Supply Current	I_{DD}	Unloaded oututs at 66.66 MHz SEL inputs at V_{DD} or GND		16.0	40.0	mA

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. All Skew specifications are mesured with a 50Ω transmission line, load teminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

Switching Characteristics (3.3V Continued)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output period	t1	With CL=30pF	40.00 (25)		20.00 (50)	ns (MHz)
Output period	t1	With CL=20pF	40.00 (25)		13.33 (75)	ns (MHz)
Duty Cycle[1]	Dt1	Measured at 1.4V; CL=30pF	40.0	49.1	60.0	%
Rise Time[1]	tr1	Measured between 0.8V and 2.0V: CL=30pF		1.70	2.50	ns
Rise Time[1]	tr2	Measured between 0.8V and 2.0V: CL=20pF		1.4	2.0	ns
Fall Time[1]	tf1	Measured between 2.0V and 0.8V; CL=30pF		1.50	2.50	ns
Fall Time[1]	tf2	Measured between 2.0V and 0.8V; CL=20pF		1.3	2.0	ns
Delay, REF Rising Edge to CLKOUT Rising Edge[1, 2]	Dr1	Measured at VDD/2		0	±350	ps
Output to Output Skew[1]	Tskew	All outputs equally loaded, CL=20pF			250	ps
Device to Device Skew[1]	Tdsk-Tdsk	Measured at VDD/2 on the CLKOUT pins of devices		0	700	ps
Cycle to Cycle Jitter[1]	Tcyc-Tcyc	Measured at 66.66 MHz, loaded outputs			200	
PLL Lock Time[1]	tLOCK	Stable power supply, valid clock presented on REF pin			1.0	ms
Jitter; Absolute Jitter[1]	Tjabs	@ 10,000 cycles CL=30pF F=20 - 50MHz	-100	70	100	ps
Jitter; 1 - Sigma[1]	Tj1s	@ 10,000 cycles CL=30pF F=20 - 50MHz		14	30	ps

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. REF input has a threshold voltage of VDD/2
3. All parameters expected with loaded outputs

Electrical Characteristics at 5.0V

V_{DD} = 4.5 – 5.5 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V	-100	-19		µA
Input High Current	I_{IH}	V_{IN}=V_{DD}		0.10	100.0	µA
Output Low Voltage[1]	V_{OL}	I_{OL} = 10mA		0.25	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = 10mA	3.4	4.0		V
Power Down Supply Current	I_{DD}	REF = 0 MHz		48	150	µA
Supply Current	I_{DD}	Unloaded oututs at 66.66 MHz SEL inputs at V_{DD} or GND		24	65	mA

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. All Skew specifications are mesured with a 50Ω transmission line, load teminated with 50Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.

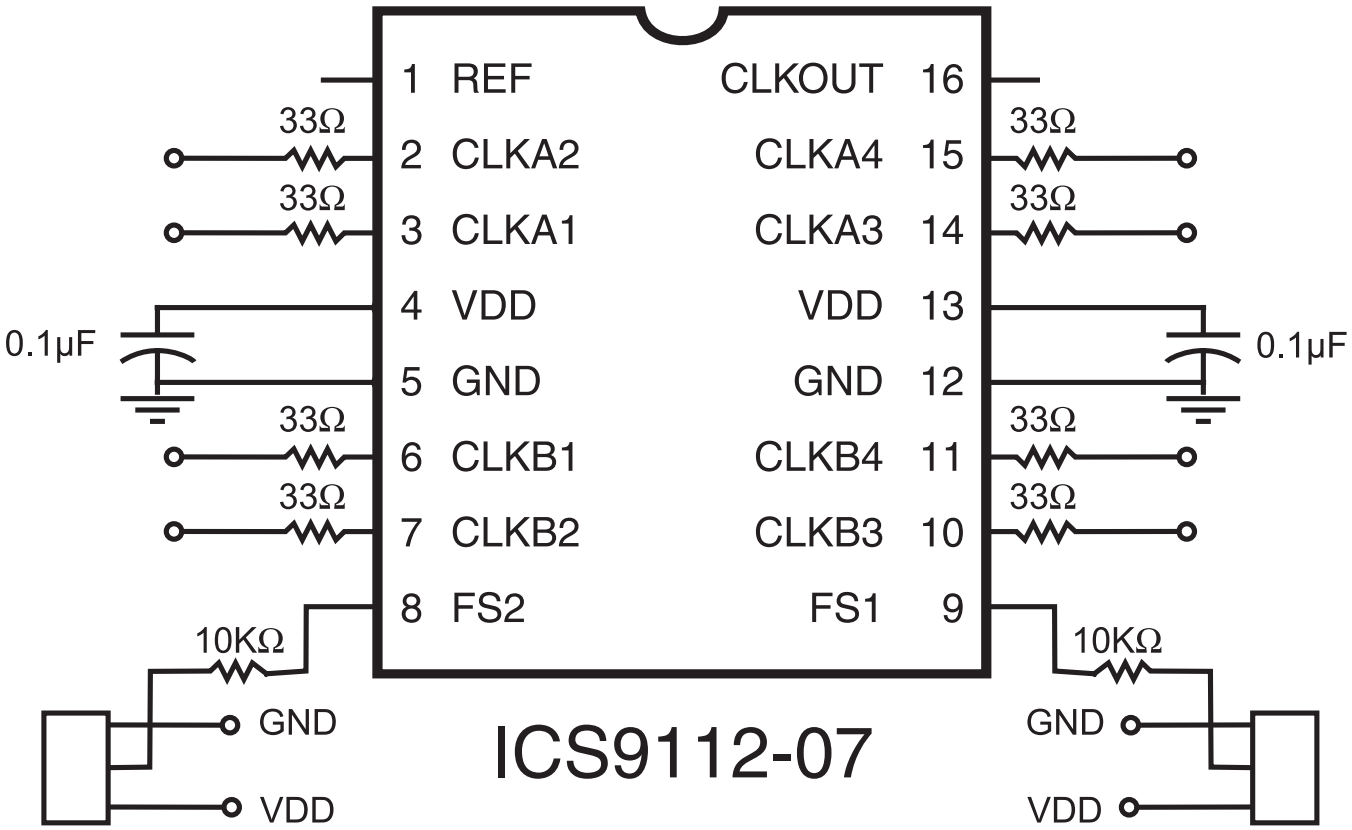
Switching Characteristics (5.0V Continued)

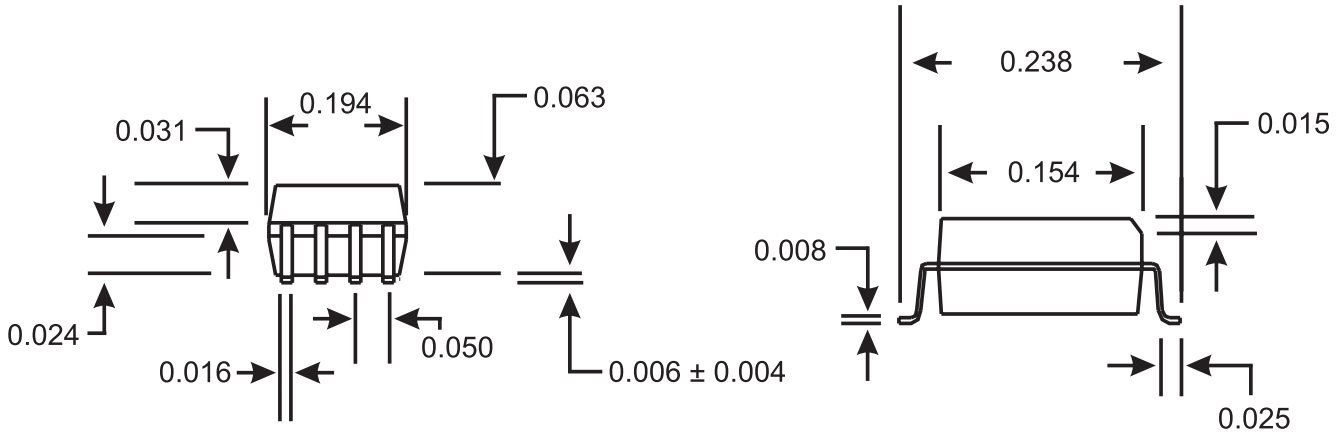
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output period	t1	With CL=30pF	60.00 (30)		20.00 (50)	ns (MHz)
Output period	t1	With CL=20pF	60.00 (30)		16.11 (90)	ns (MHz)
Duty Cycle[1]	Dt1	Measured at 1.4V; CL=30pF	40.0	49.1	60	%
Rise Time[1]	tr1	Measured between 0.8V and 2.0V: CL=30pF		1.5	2.3	ns
Rise Time[1]	tr2	Measured between 0.8V and 2.0V: CL=20pF		0.7	1.8	ns
Fall Time[1]	tf1	Measured between 2.0V and 0.8V; CL=30pF		1.2	2.3	ns
Fall Time[1]	tf2	Measured between 2.0V and 0.8V; CL=20pF		0.9	1.8	ns
Delay, REF Rising Edge to CLKOUT Rising Edge[1, 2]	Dr1	Measured at VDD/2	-400	0	+400	ps
Output to Output Skew[1]	Tskew	All outputs equally loaded, CL=20pF		80	250	ps
Device to Device Skew[1]	Tdsk-Tdsk	Measured at VDD/2 on the CLKOUT pins of devices		0	700	ps
Cycle to Cycle Jitter[1]	Tcyc-Tcyc	Measured at 66.66 MHz, loaded outputs			300	
PLL Lock Time[1]	tLOCK	Stable power supply, valid clock presented on REF pin			1.5	ms
Jitter; Absolute Jitter[1]	Tjabs	@ 10,000 cycles CL=30pF F=20 - 50MHz	-200	80	100	ps
Jitter; 1 - Sigma[1]	Tj1s	@ 10,000 cycles CL=30pF F=20 - 50MHz		14	30	ps

Notes:
1. Guaranteed by design and characterization. Not subject to 100% test.
2. REF input has a threshold voltage of VDD/2
3. All parameters expected with loaded outputs

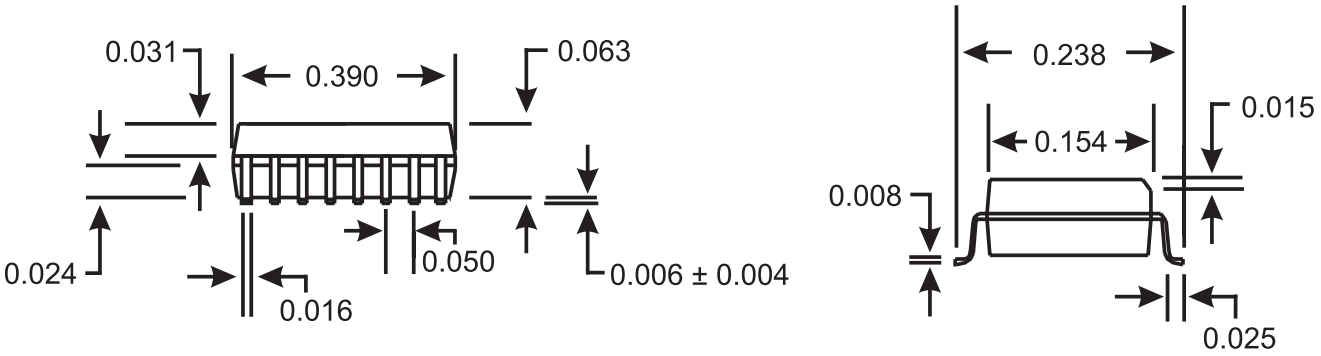
Application Suggestion:

ICS9112 is a mixed analog/digital product. The analog portion of the PLL is very sensitive to any random noise generated by charging or discharging of internal or external capacitor on the power supply pins. This type of noise will cause excess jitter to the outputs of ICS9112. Below is a recommended lay out to alleviate any addition noise. Figure below depicts only ICS9112-07, but similar techniques could be used for dash 06. For additional information on FT. layout, please refer to our AN07. The 0.1 uF capacitors should be connected as close as possible to power pins (4 & 13). An Isolated power plane with a 2.2 uF capacitor to ground will enhance the power line stability.





8 pin SOIC Package



16-Pin SOIC Package

Ordering Information

ICS9112M-06

ICS9112M-07

Example:

ICS XXXX M- PPP

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Package Type
M=SOIC

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV = Standard Device