Application Note AN-3004

Applications of Zero Voltage Crossing Optically Isolated Triac Drivers

Introduction

The zero-cross family of optically isolated triac drivers is an inexpensive, simple and effective solution for interface applications between low current dc control circuits such as logic gates and microprocessors and ac power loads (120, 240 or 380 volt, single or 3-phase).

These devices provide sufficient gate trigger current for high current, high voltage thyristors, while providing a guaranteed 7.5 kV dielectric withstand voltage between the line and the control circuitry. An integrated, zero-crossing switch on the detector chip eliminates current surges and the resulting electromagnetic interference (EMI) and reliability problems for many applications. The high transient immunity of 5000 V/µs, combined with the features of low coupling capacitance, high isolation resitance and up to 800 volt specified V_{DRM} ratings qualify this triac driver family as the ideal link between sensitive control circuitry and the ac power system environment.

Optically isolated triac drivers are not intended for stand alone service as are such devices as solid state relays. They will, however, replace costly and space demanding discrete drive circuitry having high component count consisting of standard transistor optoisolators, support components including a full wave rectifier bridge, discrete transistor, trigger SCRs and various resistor and capacitor combinations.

This paper describes the operation of a basic driving circuit and the determination of circuit values needed for proper implementation of the triac driver. Inductive loads are discussed along with the special networks required to use triacs in their presence. Brief examples of typical applications are presented.

Construction

The zero-cross family consists of a liquid phase EPI, infrared, light emitting diode which optically triggers a silicon detector chip. A schematic representation of the triac driver is shown in Figure 1. Both chips are housed in a small, 6-pin dual-in-line (DIP) package which provides mechanical integrity and protection for the semiconductor chips from external impurities. The chips are insulated by an infrared transmissive medium which reliably isolates the LED input drive circuits from the environment of the ac power load. This insulation system meets the stringent requirements for isolation set forth by regulatory agencies such as UL and VDE.

The Detector Chip

The detector chip is a complex monolithic IC which contains two infrared sensitive, inverse parallel, high voltage SCRs which function as a light sensitive triac. Gates of the individual SCRs are connected to high speed zero crossing detection circuits. This insures that with a continuous forward current through the LED, the detector will not switch to the conducting state until the applied ac voltage passes through a point near zero. Such a feature not only insures lower generated noise (EMI) and inrush (Surge) currents into resistive loads and moderate inductive loads but it also provides high noise immunity (several thousand V/µs) for the detection circuit.

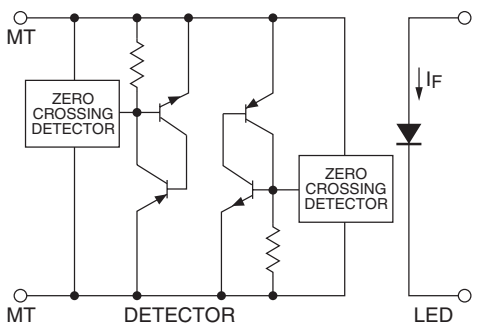


Figure 1. Schematic of Zero Crossing Optically Isolated Triac Driver

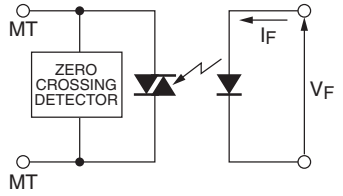


Figure 2. Simplified Schematic of Isolator

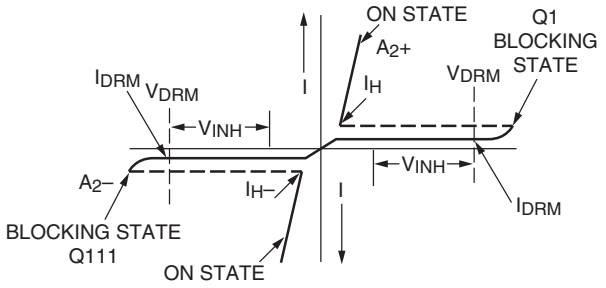


Figure 3. Triac Voltage-Current Characteristic

Electrical Characteristics

A simplified schematic of the optically isolated triac driver is shown in Figure 2. This model is sufficient to describe all important characteristics. A forward current flow through the LED generates infrared radiation which triggers the detector. This LED trigger current (I_{FT}) is the maximum guaranteed current necessary to latch the triac driver and ranges from 5 mA for the MOC3063 to 15 mA for the MOC3061. The LED's forward voltage drop at I_F = 30 mA is 1.5 V maximum. Voltage-current characteristics of the triac are identified in Figure 3.

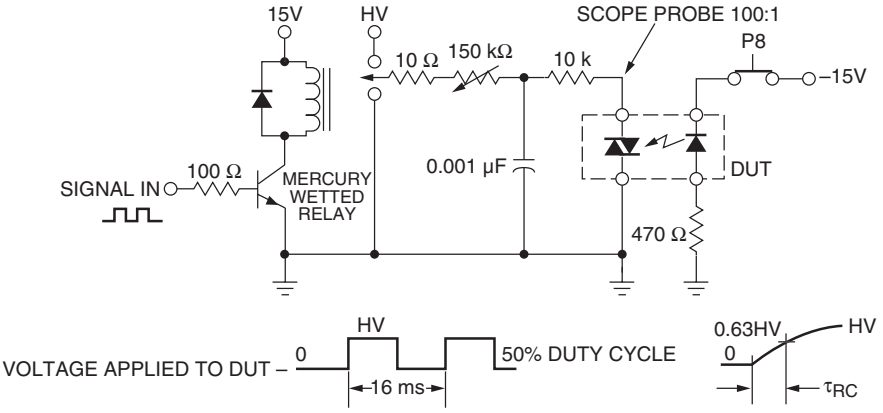
Once triggered, the detector stays latched in the "on state" until the current flow through the detector drops below the holding current (I_H) which is typically 100 µA. At this time, the detector reverts to the "off" (non-conducting) state. The detector may be triggered "on" not only by I_{FT} but also by exceeding the forward blocking voltage between the two main terminals (MT1 and MT2) which is a minimum of 600 volts for all MOC3061 family members. Also, voltage ramps (transients, noise, etc.) which are common in ac power lines may trigger the detector accidentally if they exceed the static dV/dt rating. Since the fast switching, zero-crossing switch provides a minimum dV/dt of 500 V/µs even at an ambient temperature of 70°C, accidental triggering of the triac driver is unlikely. Accidental triggering of the main triac is a more likely occurrence. Where high dV/dt transients on the ac line are anticipated, a form of suppression network commonly called a "snubber" must be used to prevent false "turn on" of the main triac. A detailed discussion of a "snubber" network is given under the section "Inductive and Resistive Loads."

Figure 4 shows a static dV/dt test circuit which can be used to test triac drivers and power triacs. The proposed test method is per EIA/NARM standard RS-443.

Tests on the MOC3061 family of triac drivers using the test circuit of Figure 4 have resulted in data showing the effects of temperature and voltage transient amplitude on static dV/dt. Figure 5 is a plot of dV/dt versus ambient temperature while Figure 6 is a similar plot versus transient amplitude.

Basic Driving Circuit

Assuming the circuit shown in Figure 7 is in the blocking or "off" state (which means I_F is zero), the full ac line voltage appears across the main terminals of both the triac and the triac driver. When sufficient LED current (I_{FT}) is supplied and the ac line voltage is below the inhibit voltage (V_{INH} in Figure 3), the triac driver latches "on." This action introduces a gate current in the main triac triggering it from the blocking



Test Procedure-

Turn the D.U.T. on, while applying sufficient dV/dt to ensure that it remains on, even after the trigger current is removed. Then decrease dV/dt until the D.U.T. turns off. Measure τ_{RC}, the time it takes to rise to 0.63 HV, and divide 0.63 HV by τ_{RC} to get dV/dt.

Figure 4. Static dV/dt Test Circuit

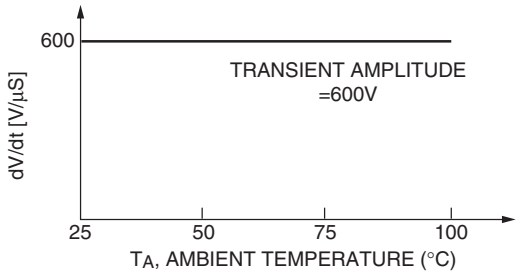


Figure 5. Static dV/dt versus Temperature

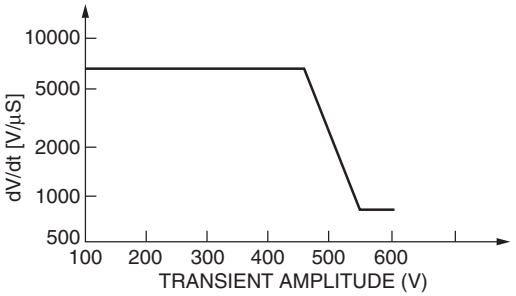


Figure 6. Static dV/dt versus Transient Amplitude

state into full conduction. Once triggered, the voltage across the main terminals collapses to a very low value which results in the triac drive output current decreasing to a value lower than its holding current, thus forcing the triac driver into the "off" state, even when I_{FT} is still applied.

The power triac remains in the conducting state until the load current drops below the power triac's holding current, a situation that occurs every half cycle. The actual duty cycle for the triac drive is very short (in the 1 to 3 µs region). When I_{FT} is present, the power triac will be retriggered every half cycle of the ac line voltage until I_{FT} is switched "off" and the power triac has gone through a zero current point. (See Figure 8).

Resistor R (shown in Figure 7) is not mandatory when R_L is a resistive load since the current is limited by the gate trigger current (I_{GT}) of the power triac. However, resistor R (in combination with R-C snubber networks that are described in the section "Inductive and Resistive Loads") prevents possible destruction of the triac drive in applications where the load is highly inductive.

Unintentional phase control of the main triac may happen if the current limiting resistor R is too high in value. The function of this resistor is to limit the current through the triac driver in case the main triac is forced into the non-conductive state close to the peak of the line voltage and the energy stored in a "snubber" capacitor is discharged into the triac driver. A calculation for the current limiting resistor R is shown below for a typical 220 volt application: Assume the line voltage is 220 volts RMS. Also assume the maximum peak repetitive drive current (normally for a 10 micro second maximum time interval is 1 ampere. Then

$$R = \frac{V_{peak}}{I_{peak}} = \frac{220\sqrt{2}\ \text{volts}}{1\ \text{amp}} = 311\,\text{ohms}$$

One should select a standard resistor value >311 ohms → 330 ohms.

The gate resistor R_G (also shown in Figure 7) is only necessary when the internal gate impedance of the triac or SCR is very high which is the case with sensitive gate thyristors. These devices display very poor noise immunity and thermal stability without R_G. The value of the gate resistor in this case should be between 100 and 500. The circuit designer should be aware that use of a gate resistor increases the required trigger current (I_{GT}) since R_G drains off part of I_{GT}. Use of a gate resistor combined with the current limiting resistor R can result in an unintended delay or phase shift between the zero-cross point and the time the power triac triggers.

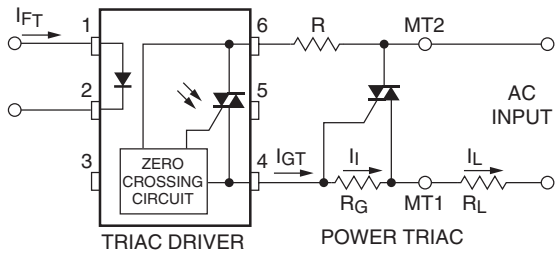


Figure 7. Basic Driving Circuit – Triac Driver, Triac and Load

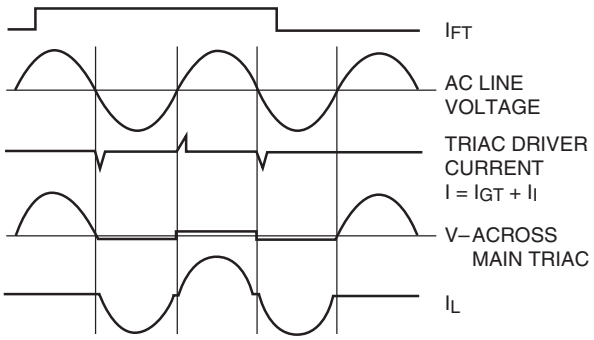


Figure 8. Waveforms of a Basic Driving Circuit

Unintended Trigger Delay Time

To calculate the unintended time delay, one must remember that power triacs require a specified trigger current (I_{GT}) and trigger voltage (V_{GT}) to cause the triac to become conductive. This necessitates a minimum line voltage V_T to be present between terminal MT1 and MT2 (see Figure 7), even when the triac driver is already triggered "on." The value of minimum line voltage V_T is calculated by adding all the voltage drops in the trigger circuit:

$V_T = V_R + V_{TM} + V_{GT}$.

Current I in the trigger circuit consists not only of I_{GT} but also the current through R_G:

$I = I_{RG} + I_{GT}$.

Likewise, I_{RG} is calculated by dividing the required gate trigger voltage V_{GT} for the power triac by the chosen value of gate resistor R_G:

$I_{RG} = V_{GT}/R_G$

Thus, $I = V_{GT}/R_G + I_{GT}$.

All voltage drops in the trigger circuit can now be determined as follows:

$V_R = I \times R = V_{GT}/R_G \times R + I_{GT} \times R = R(V_{GT}/R_G + I_{GT})$
V_{TM} = From triac driver data sheet.
V_{GT} = From power triac data sheet.
I_{GT} = From power triac data sheet.

With V_{TM}, V_{GT} and I_{GT} taken from data sheets, it can be seen that V_T is only dependent on R and R_G.

Knowing the minimum voltage between MT1 and MT2 (line voltage) required to trigger the power triac, the unintended phase delay angle θ_d (between the ideal zero crossing of the ac line voltage and the trigger point of the power triac) and the trigger delay time t_d can be determined as follows:

$$\theta_d = \sin^{-1} V_T/V_{peak}$$

$$= \sin^{-1} \frac{R(V_{GT}/R_G + I_{GT}) + V_{TM} + V_{GT}}{V_{peak}}$$

The time delay t_d is the ratio of θ_d to θ_{Vpeak} (which is 90 degrees) multiplied by the time it takes the line voltage to go from zero voltage to peak voltage (simply 1/4f, where f is the line frequency). Thus

$T_d = \theta_d/90 \times 1/4f$.

Figure 9 shows the trigger delay of the main triac versus the value of the current limiting resistor R for assumed values of I_{GT}. Other assumptions made in plotting the equations for t_d are that line voltage is 220 V RMS which leads to V_{peak} = 311 volts; R_G = 300 ohms; V_{GT} = 2 volts and f = 60 Hz. Even though the triac driver triggers close to the zero cross point of the ac voltage, the power triac cannot be triggered until the voltage of the ac line rises high enough to create enough current flow to latch the power triac in the "on" state. It is apparent that significant time delays from the zero crossing point can be observed when R is a large value along with a high value of I_{GT} and/or a low value of R_G. It should be remembered that low values of the gate resistor improve the dV/dt ratings of the power triac and minimize self latching problems that might otherwise occur at high junction temperatures.

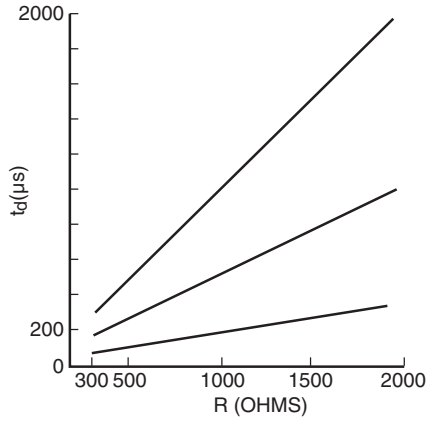


Figure 9. Time Delay t_d versus Current Limiting Resistor R

Switching Speed

The switching speed of the triac driver is a composition of the LED's turn on time and the detector's delay, rise and fall times. The harder the LED is driven the shorter becomes the LED's rise time and the detector's delay time. Very short I_{FT} duty cycles require higher LED currents to guarantee "turn on" of the triac driver consistent with the speed required by the short trigger pulses.

Figure 10 shows the dependency of the required LED current normalized to the dc trigger current required to trigger the triac driver versus the pulse width of the LED current. LED trigger pulses which are less than 100 µs in width need to be higher in amplitude than specified on the data sheet in order to assure reliable triggering of the triac driver detector.

The switching speed test circuit is shown in Figure 11. Note that the pulse generator must be synchronized with the 60 Hz line voltage and the LED trigger pulse must occur near the zero cross point of the ac line voltage. Peak ac current in the curve tracer should be limited to 10 mA. This can be done by setting the internal load resistor to 3k ohms.

Fairchild isolated triac drivers are triggered devices and designed to work in conjunction with triacs or inverse parallel SCRs which are able to take rated load current. However, as soon as the power triac is triggered there is no current flow through the triac driver. The time to turn the triac driver "off" depends on the switching speed of the triac, which is typically on the order of 1-2 µs.

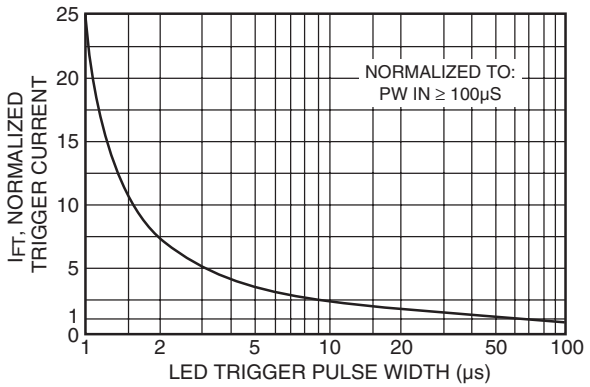


Figure 10. I_{FT} Normalized to I_{FT} dc as Specified on the Data Sheet

Inductive and Resistive Loads

Inductive loads (motors, solenoids, etc.) present a problem for the power triac because the current is not in phase with the voltage. An important fact to remember is that since a triac can conduct current in both directions, it has only a brief interval during which the sine wave current is passing through zero to recover and revert to its blocking state. For inductive loads, the phase shift between voltage and current means that at the time the current of the power handling triac falls below the holding current and the triac ceases to conduct, there exists a certain voltage which must appear across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with certain inductive loads, the rate of rise in voltage (dV/dt) must be limited by a series RC network placed in parallel with the power triac. The capacitor C_S will limit the dV/dt across the triac.

The resistor R_S is necessary to limit the surge current from C_S when the triac conduct and to damp the ringing of the capacitance with the load inductance L_L. Such an RC network is commonly referred to as a "snubber."

Figure 12 shows current and voltage wave forms for the power triac. Commutating dV/dt for a resistive load is typically only 0.13 V/µs for a 240 V, 50 Hz line source and 0.063 V/µs for a 120 V, 60 Hz line source. For inductive loads the "turn off" time and commutating dV/dt stress are more difficult to define and are affected by a number of variables such as back EMF of motors and the ratio of inductance to resistance (power factor). Although it may appear from the inductive load that the rate or rise is extremely fast, closer circuit evaluation reveals that the commutating dV/dt generated is restricted to some finite value which is a function of the load reactance L_L and the device capacitance C but still may exceed the triac's critical commuting dV/dt rating which is about 50 V/µs. It is generally good practice to use an RC snubber network across the triac to limit the rate of rise (dV/dt) to a value below the maximum allowable rating. This snubber network not only limits the voltage rise during commutation but also suppresses transient voltages that may occur as a result of ac line disturbances.

There are no easy methods for selecting the values for R_S and C_S of a snubber network. The circuit of Figure 13 is a damped, tuned circuit comprised of R_S, C_S, R_L and L_L, and to a minor extent the junction capacitance of the triac. When the triac ceases to conduct (this occurs every half cycle of the line voltage when the current falls below the holding current), the load current receives a step impulse of line voltage which depends on the power factor of the load. A given load fixes R_L and L_L; however, the circuit designer

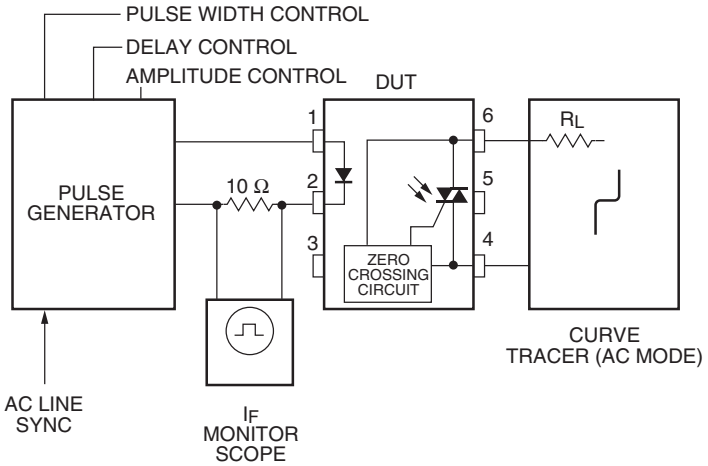


Figure 11. Test Circuit for LED Forward Trigger Current versus Pulse Width

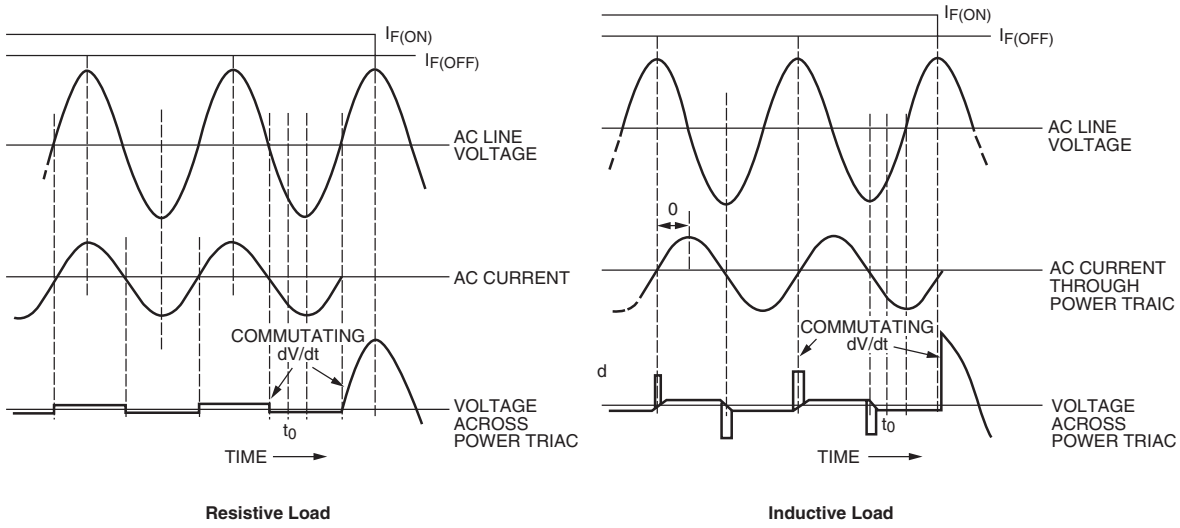


Figure 12. Current and Voltage Waveforms During Commutation

can vary R_S and C_S. Commutating dV/dt can be lowered by increasing C_S while R_S can be increased to decrease resonant "over ringing" of the tuned circuit. Generally this is done experimentally beginning with values calculated as shown in the next section and, then, adjusting R_S and C_S values to achieve critical damping and a low critical rate of rise of voltage.

Less sensitive to commutating dV/dt are two SCRs in an inverse parallel mode often referred to as a back-to-back SCR pair (see Figure 15). This circuit uses the SCRs in an alternating mode which allows each device to recover and turn "off" during a full half cycle. Once in the "off" state, each SCR can resist dV/dt to the critical value of about 100 V/µs. Optically isolated triac drivers are ideal in this application since both gates can be triggered by one triac driver which also provides isolation between the low voltage control circuit and the ac power line.

It should be mentioned that the triac driver detector does not see the commutating dV/dt generated by the inductive load during its commutation; therefore, the commutating dV/dt appears as a static dV/dt across the two main terminals of the triac driver.

Snubber Design - The Resonant Method

If R, L and C are chosen to resonate, the voltage waveform on dV/dt will look like Figure 14. This is the result of a damped quarter-cycle of oscillation. In order to calculate the components for snubbing, the dV/dt must be related to frequency. Since, for a sine wave,

$$V(t) = V_P \sin \omega t$$
$$dV/dt = V_P\, \omega \cos \omega t$$
$$dV/dt_{(max)} = V_P\, \omega = V_P 2\pi f$$

$$f = \frac{dV/dt}{2\pi V_{P(max)}}$$

Where dV/dt is the maximum value of off state dV/dt specified by the manufacturer.

From:

$$f = \frac{1}{2\pi\sqrt{LC}}$$
$$C = \frac{1}{(2\pi f)^2 L}$$

We can choose the inductor for convenience. Assuming the resistor is chosen for the usual 30% overshoot:

$$R = \sqrt{\frac{L}{C}}$$

Assuming L is 50 µH, then:

$$f = \frac{(dV/dt)_{min}}{2\pi V_P} = \frac{50 V/\mu s}{2\pi(294\ V)} = 27\ kHz$$

$$C = \frac{1}{(2\pi f)^2 L} = 0.69\ \mu F$$

$$R = \sqrt{\frac{L}{C}} = \sqrt{\frac{50\ \mu H}{0.69\ \mu F}} = 8.5\ \Omega$$

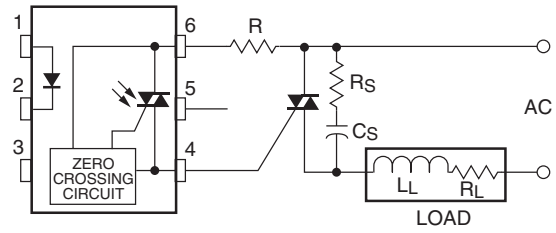


Figure 13. Triac Driving Circuit - with Snubber

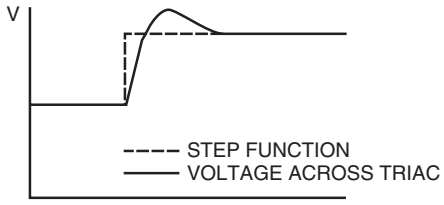


Figure 14. Voltage Waveform After Step Voltage Rise - Resonant Snubbing

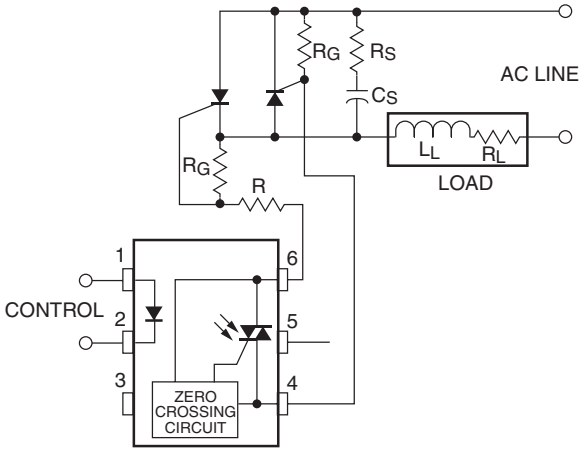


Figure 15. A Circuit Using Inverse Parallel SCRs

Inrush (Surge) Currents

The zero crossing feature of the triac driver insures lower generated noise and sudden inrush currents on resistive loads and moderate inductive loads. However, the user should be aware that many loads even when started at close to the ac zero crossing point presents very low impedance. For example, incandescent lamp filaments when energized at the zero crossing may draw ten to twenty times the steady state current that is drawn when the filament is hot. A motor when started pulls a “locked rotor” current of, perhaps, six times its running current. This means the power triac switching these loads must be capable of handling current surges without junction overheating and subsequent degradation of its electrical parameter.

Almost pure inductive loads with saturable ferromagnetic cores may display excessive inrush currents of 30 to 40 times the operating current for several cycles when switched “on” at the zero crossing point. For these loads, a random phase triac driver (MOC3051 family) with special circuitry to provide initial “turn on” of the power triac at ac peak voltage may be the optimized solution.

Zero Cross, Three Phase Control

The growing demand for solid state switching of ac power heating controls and other industrial applications has resulted in the increased use of triac circuits in the control of three phase power. Isolation of the dc logic circuitry from the ac line, the triac and the load is often desirable even in single phase power control applications. In control circuits for poly phase power systems, this type of isolation is mandatory because the common point of the dc logic circuitry cannot be referred to a common line in all phases. The MOC3061 family's characteristics of high off-state blocking voltage and high isolation capability make the isolated triac drivers devices for a simplified, effective control circuit with low component count as shown in Figure 16. Each phase is controlled individually by a power triac with optional snubber network (R_S, C_S) and an isolated triac driver with current limiting resistor R. All LEDs are connected in series and can be controlled by one logic gate or controller. An example is shown in Figure 17.

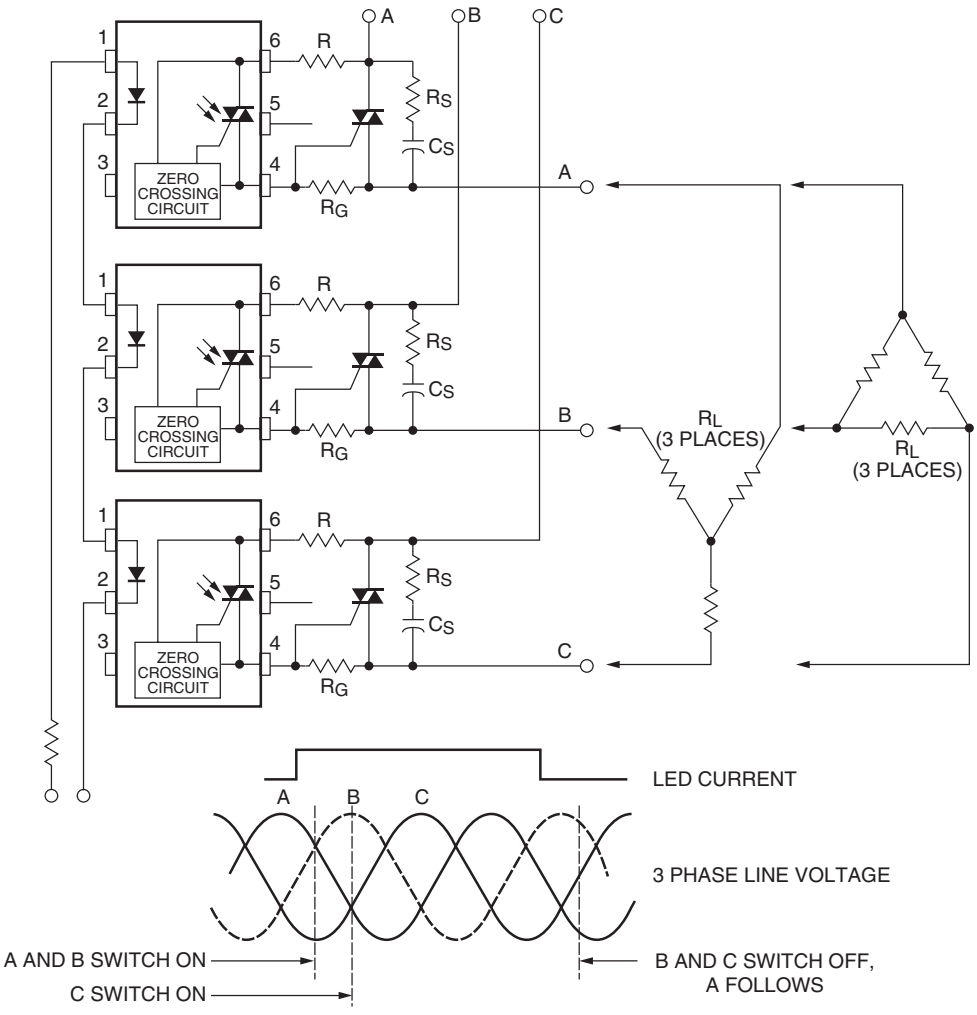


Figure 16. 3 Phase Control Circuit

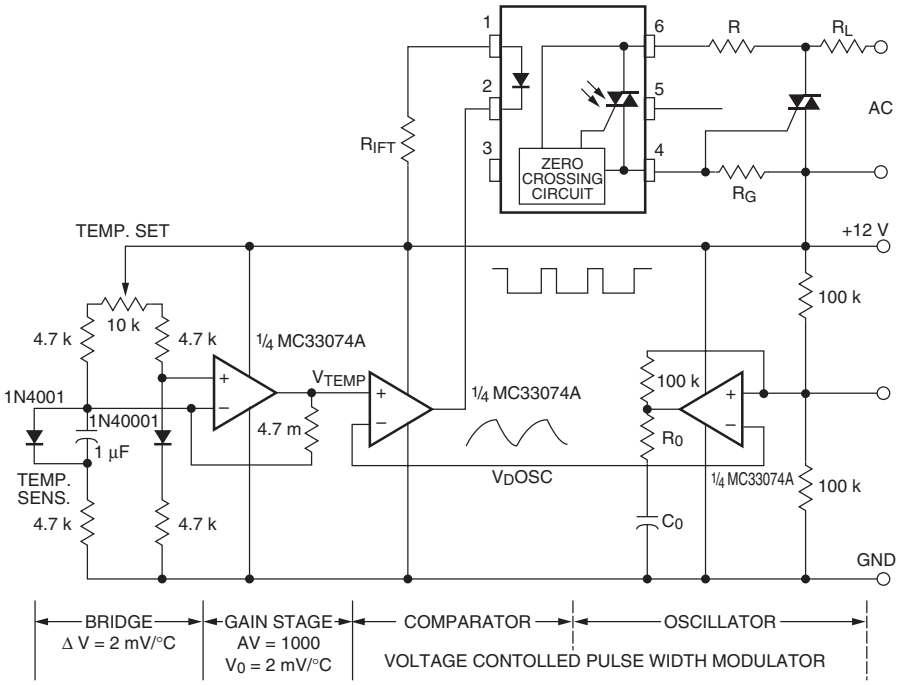


Figure 17. Proportional Zero Voltage Switching Temperature Controller

At startup, by applying I_F, the two triac drivers which see zero voltage differential between phase A and B or A and C or C and B (which occurs every 60 electrical degrees of the ac line voltage) will switch "on" first. The third driver (still in the "off" state) switches "on" when the voltage difference between the phase to which it is connected approaches the same voltage (superimposed voltage) of the phases already switched "on." This guarantees zero current "turn on" of all three branches of the load which can be in Y or Delta configuration. When the LEDs are switched "off," all phases switch "off" when the current (voltage difference) between any two of the three phases drops below the holding current of the power triacs. Two phases switched "off" create zero current. In the remaining phase, the third triac switches "off" at the same time.

Proportional Zero Voltage Switching

The built-in zero voltage switching feature of the zero-cross triac drivers can be extended to applications in which it is desirable to have constant control of the load and a minimization of system hysteresis as required in industrial heater applications, oven controls, etc. A closed loop heater control in which the temperature of the greater element or the chamber is sensed and maintained at a particular value is a good example of such applications. Proportional zero voltage switching provides accurate temperature control, minimizes overshoots and reduces the generation of line noise transients.

Figure 17 shows a low cost MC33074 quad op amp which provides the task of temperature sensing, amplification, voltage controlled pulse width modulation and triac drive LED control. One of the two 1N4001 diodes (which are in a Wheatstone bridge configuration) senses the temperature in the oven chamber with an output signal of about 2 mV/°C. This signal is amplified in an inverting gain stage by a factor of 1000 and compared to a triangle wave generated by an oscillator. The comparator and triangle oscillator form a voltage controlled pulse width modulator which controls the triac driver. When the temperature in the chamber is below the desired value, the comparator output is low, the triac driver and the triac are in the conducting state and full power is applied to the load. When the oven temperature comes close to the desired value (determined by the "temp set" potentiometer), a duty cycle of less than 100% is introduced providing the heater with proportionally less power until equilibrium is reached. The proportional band can be controlled by the amplification of the gain stage - more gain provides a narrow band; less gain a wider band. Typical waveforms are shown in Figure 18.

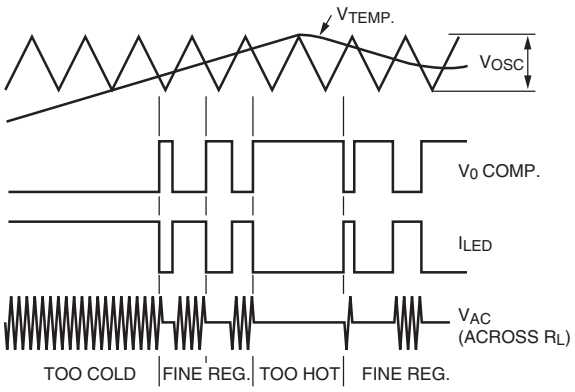


Figure 18. Typical Waveforms of Temperature Controller

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