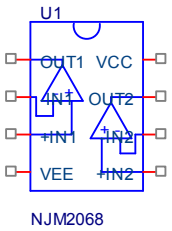
Device Modeling Report

COMPONENTS:MOSFET: OPERATIONAL AMPLIFIER
PART NUMBER:NJM2068
MANUFACTURER: NEW JAPAN RADIO CO.,LTD

Bee Technologies Inc.

SPice Model

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*$
* PART NUMBER:NJM2068
* MANUFACTURER: NEW JAPAN RADIO
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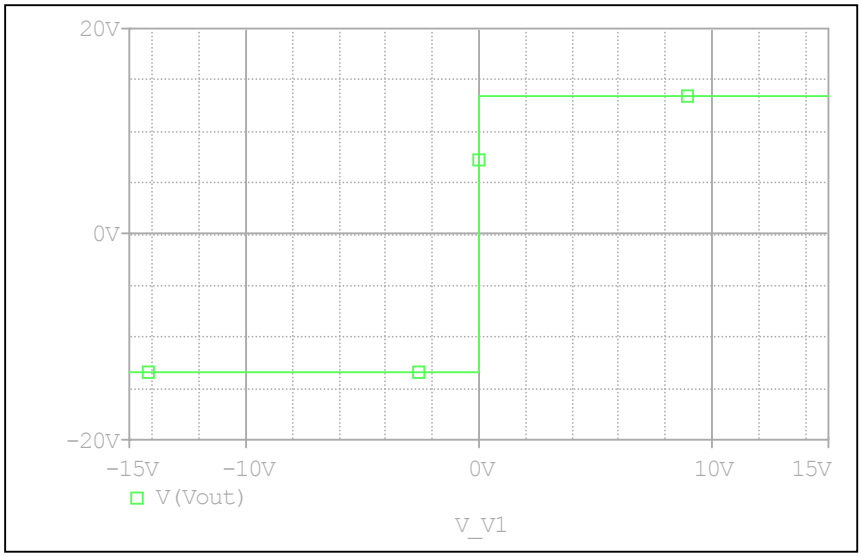
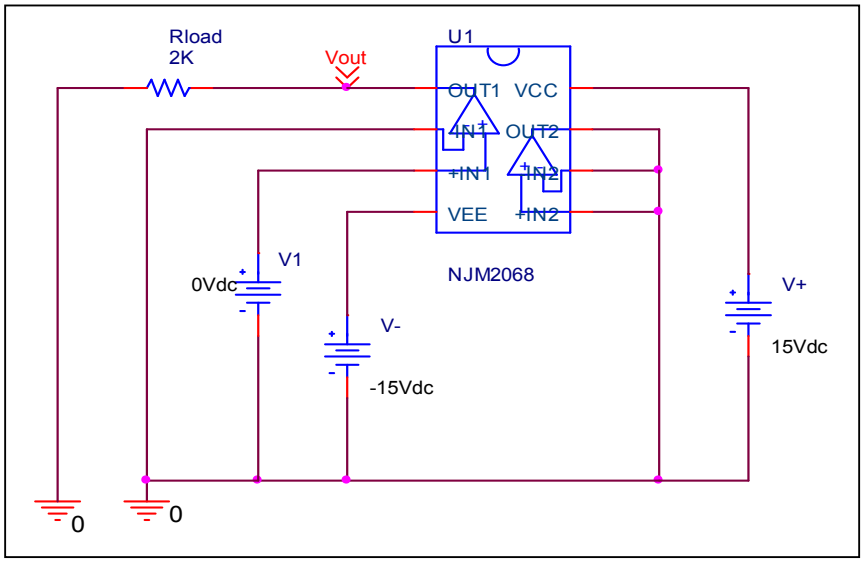
.Subckt NJM2068 OUT1 -IN1 +IN1 VEE +IN2 -IN2 OUT2 VCC
X_U1     +IN1 -IN1 VCC VEE OUT1 NJM2068_SUB
X_U2     +IN2 -IN2 VCC VEE OUT2 NJM2068_SUB
.ends  NJM2068
.subckt NJM2068_SUB  1 2 3 4 5
  c1   11 12 8.6603E-12
  c2    6  7 30.000E-12
  dc    5 53 dy
  de   54  5 dy
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 35.357E6 -1E3 1E3 35E6 -35E6
  ga    6  0 11 12 1.1924E-3
  gcm   0  6 10 99 3.6134E-9
  iee   3 10 dc 185.58E-6
  hlim 90  0 vlim 1K
  q1   11  2 13 qx1
  q2   12  1 14 qx2
  r2    6  9 100.00E3
  rc1   4 11 838.63
  rc2   4 12 838.63
  re1  13 10 558.53
  re2  14 10 558.53
  ree  10 99 1.0777E6
  ro1   8  5 50
  ro2   7 99 25
  rp    3  4 1.8203E3
  vb    9  0 dc 0
  vc    3 53 dc 2.2550
  ve   54  4 dc 2.2550
  vlim  7  8 dc 0
  vlp  91  0 dc 10
  vln   0 92 dc 10
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=603.91)
.model qx2 PNP(Is=809.2394E-18 Bf=626.80)
.ends
*$
```

Output Voltage Swing

Simulation result



Evaluation circuit

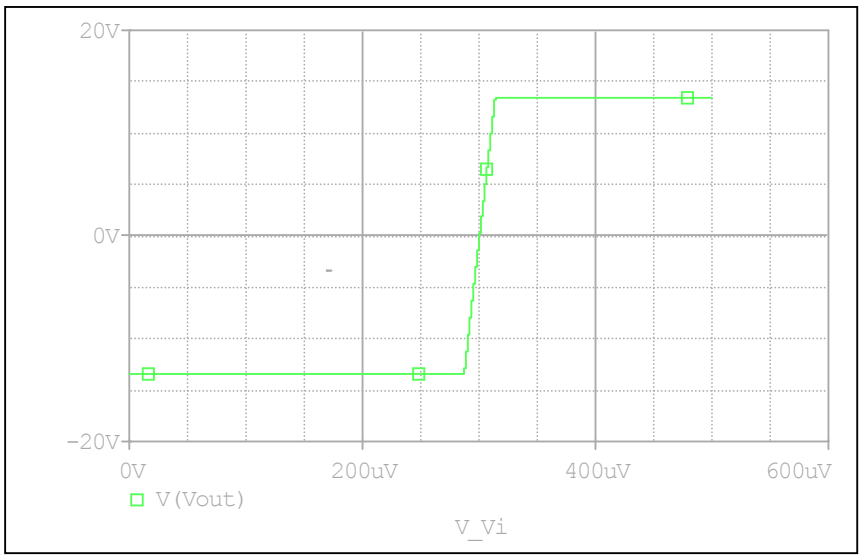


Comparison table

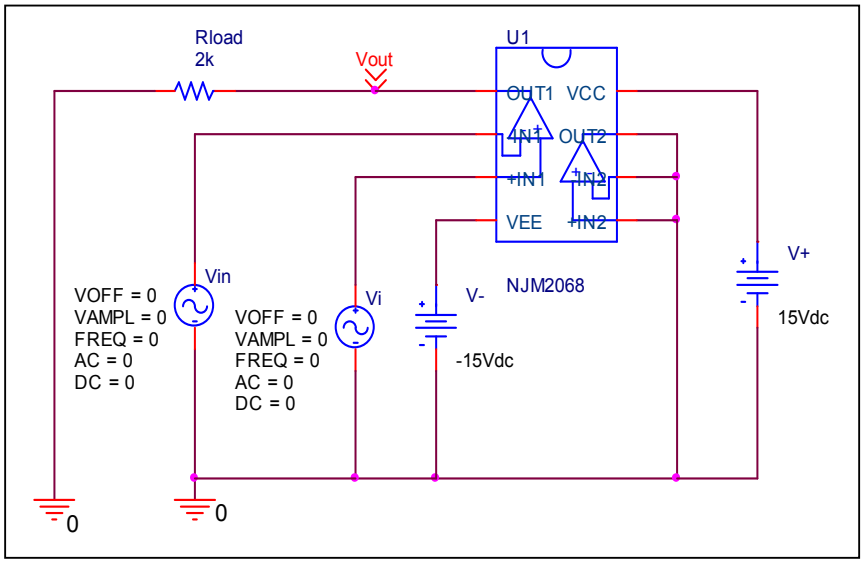
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	+13.5	+13.501	0.007
-Vout(V)	-13.5	-13.501	0.007

Input Offset Voltage

Simulation result



Evaluation circuit

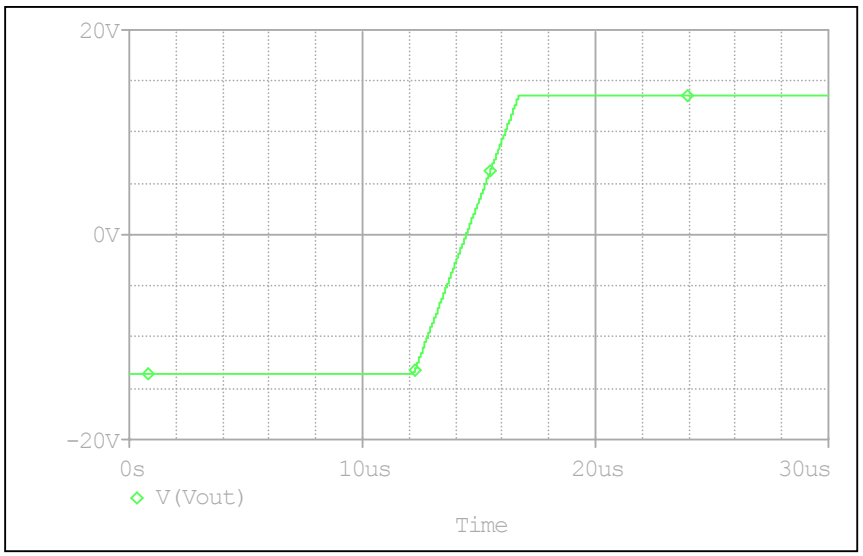


Comparison table

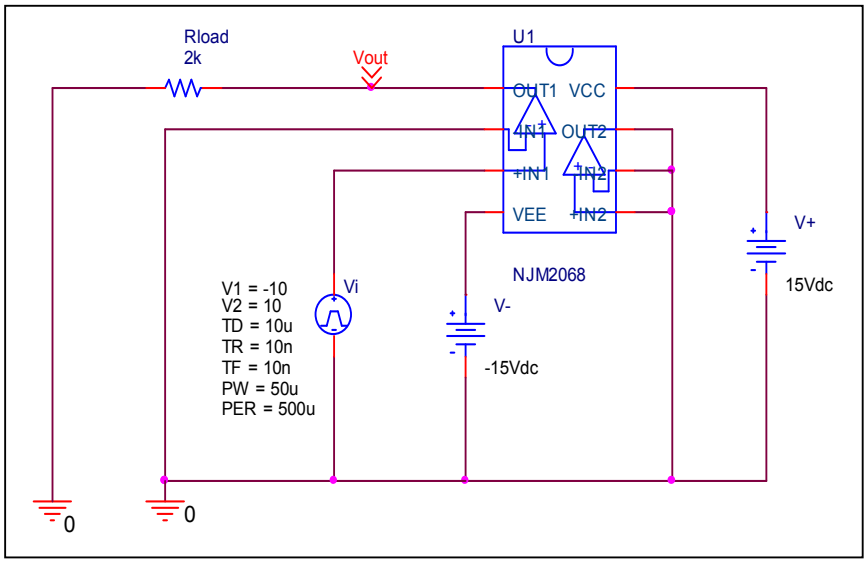
	Measurement	Simulation	%Error
Vos (mV)	0.3	0.302	0.667

Slew Rate

Simulation result



Evaluation circuit

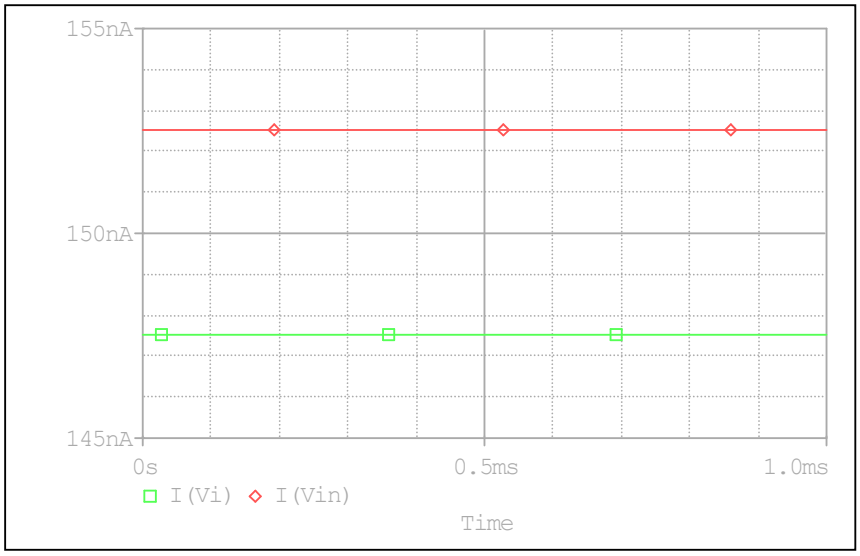


Comparison table

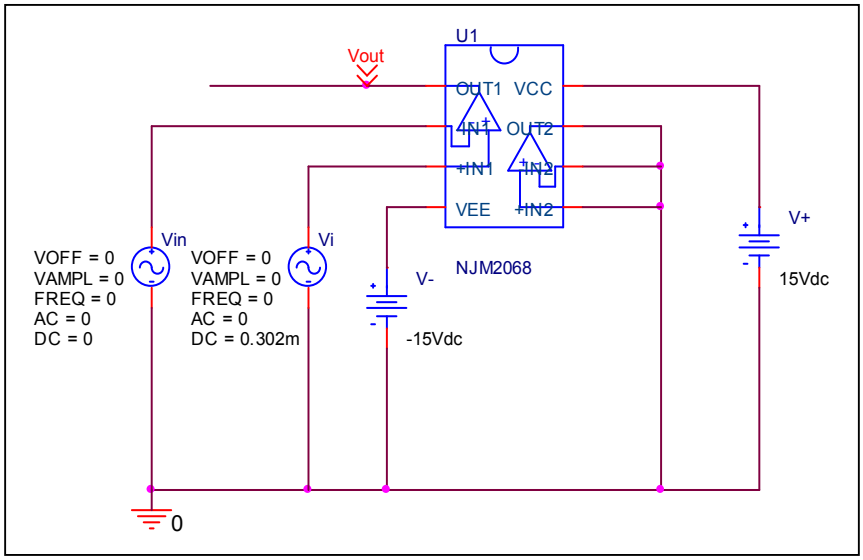
	Measurement	Simulation	%Error
Slew Rate(v/us)	6	6	0

Input current

Simulation result



Evaluation circuit

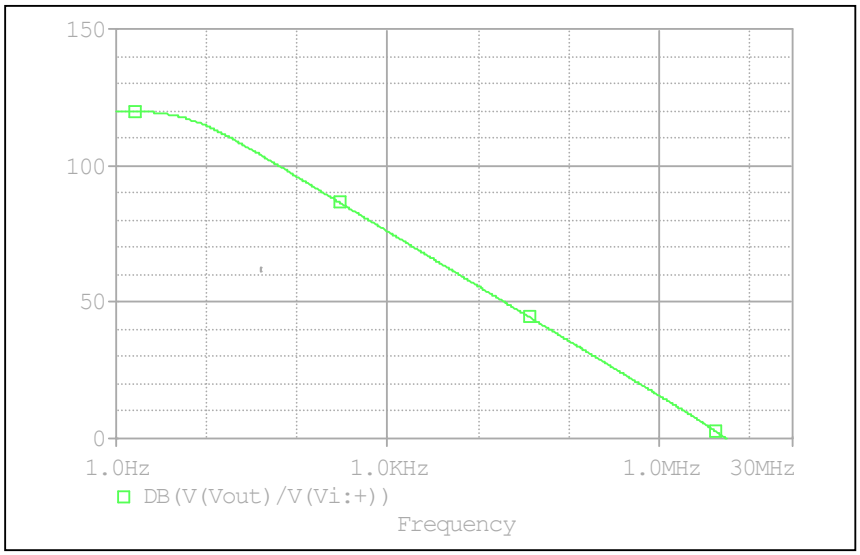


Comparison table

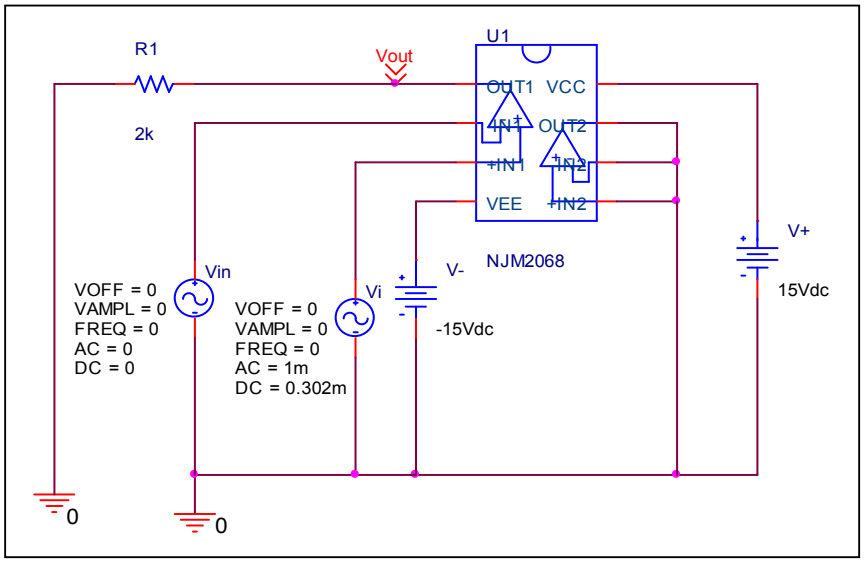
	Measurement	Simulation	%Error
Ib (nA)	150	150.043	0.029
Ibos (nA)	5	5.001	0.020

Open Loop Voltage Gain vs. Frequency

Simulation result



Evaluation circuit

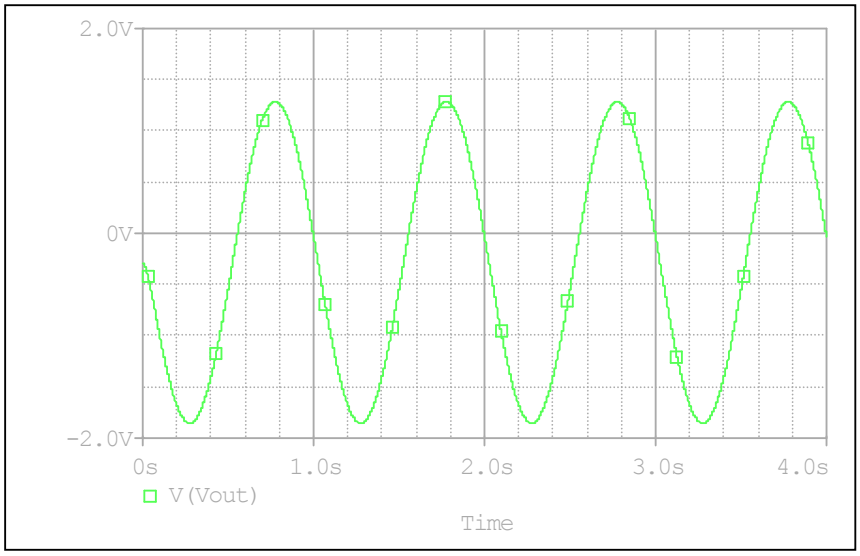


Comparison table

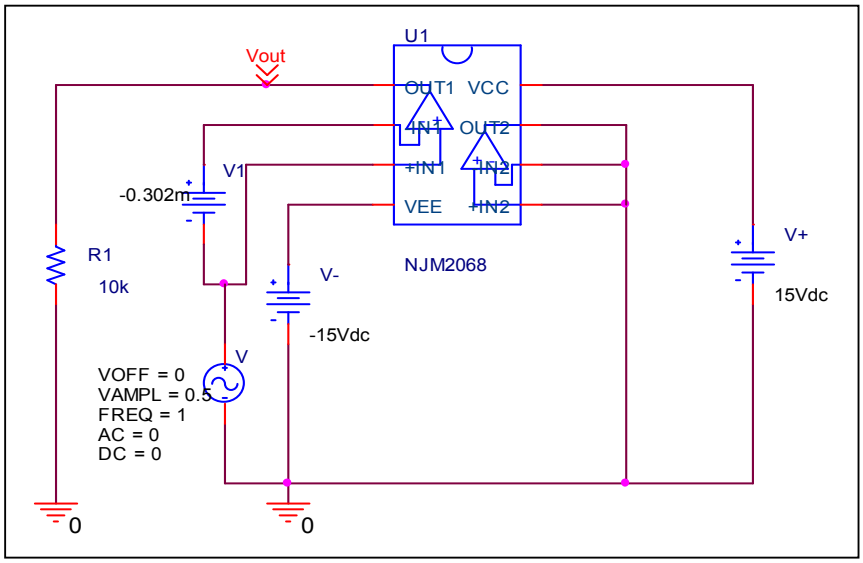
	Measurement	Simulation	%Error
f-0dB(MHz)	5.5	5.5077	0.140
Av-dc(dB)	120	120.011	0.009

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit



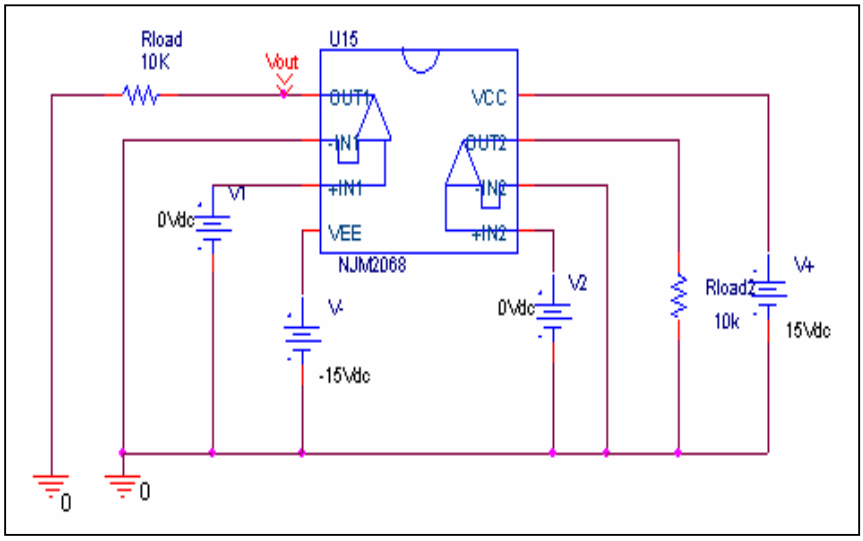
CMRR=20*LOG(1001267.224/3.1127) = 110.148 dB

Comparison table

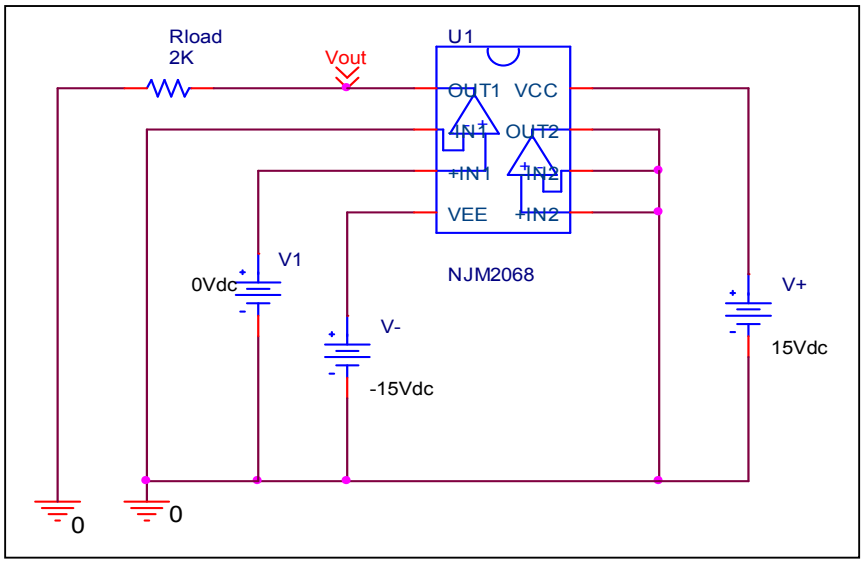
	Measurement	Simulation	%Error
CMRR(dB)	110	110.148	0.135

Remark Output Voltage Swing

Before

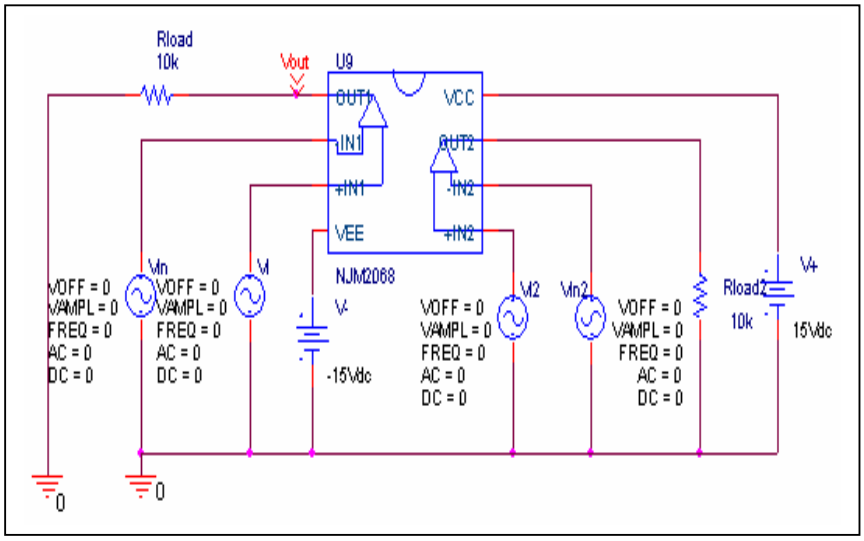


After

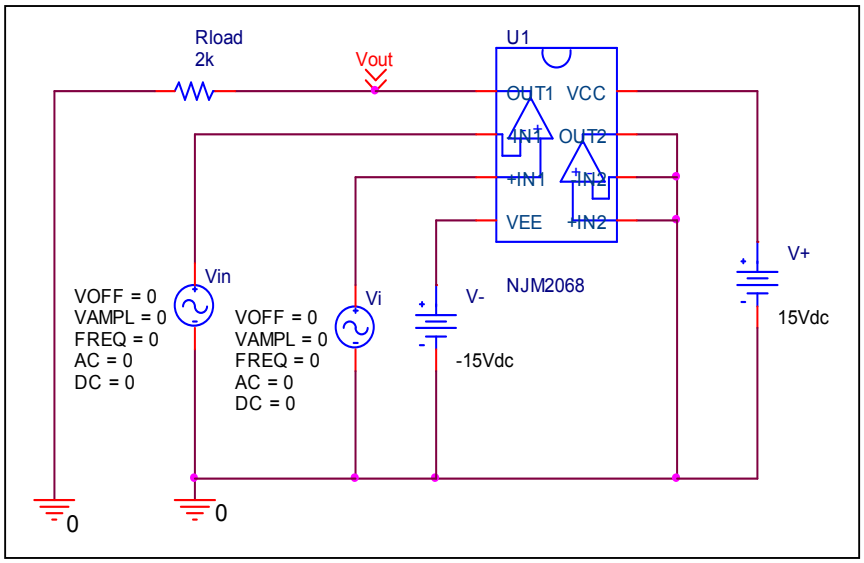


Remark Input Offset Voltage

Before

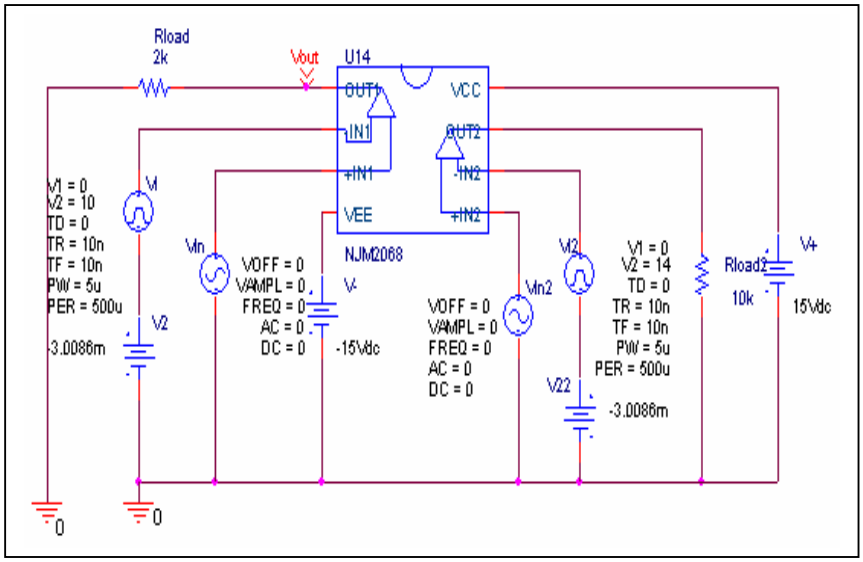


After

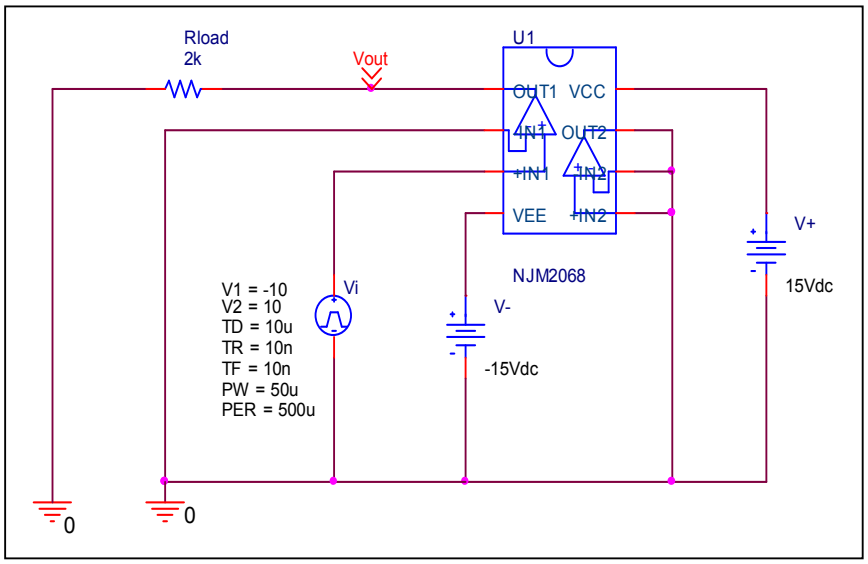


Remark Slew Rate

Before

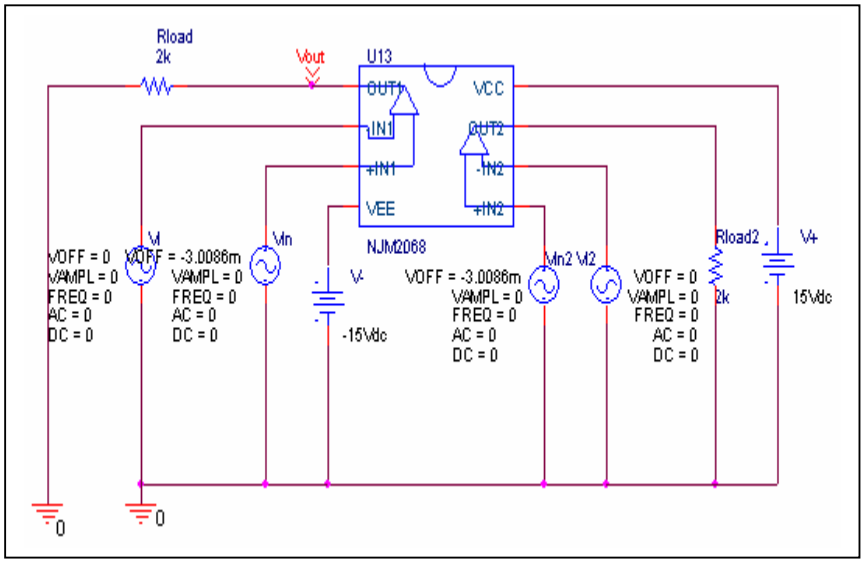


After

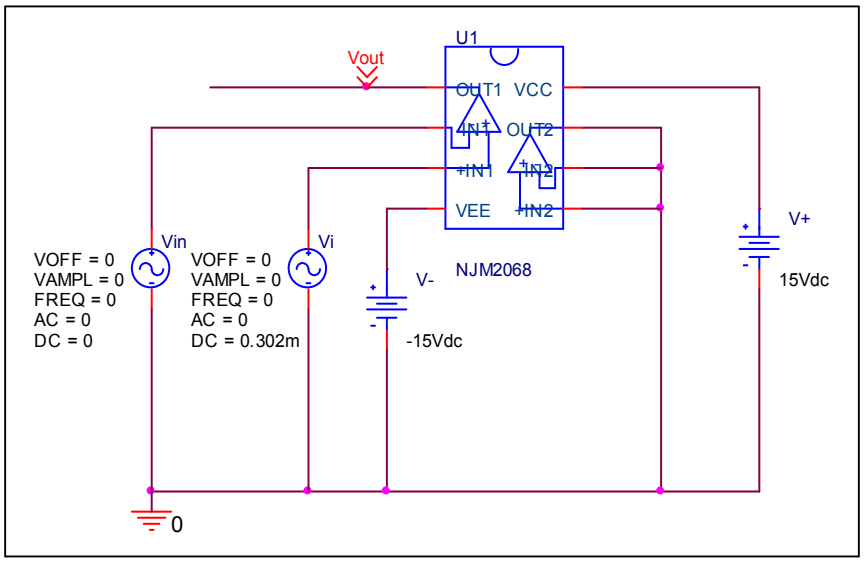


Remark Input current

Before

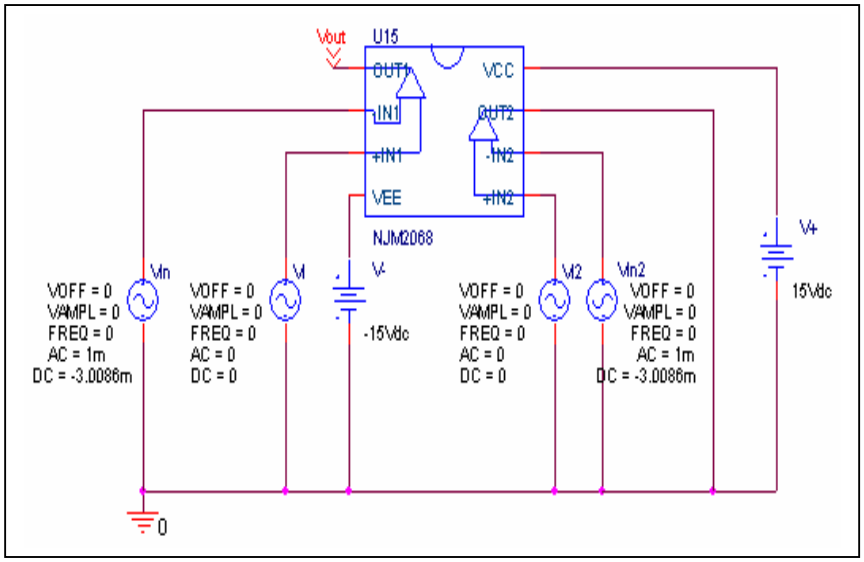


After

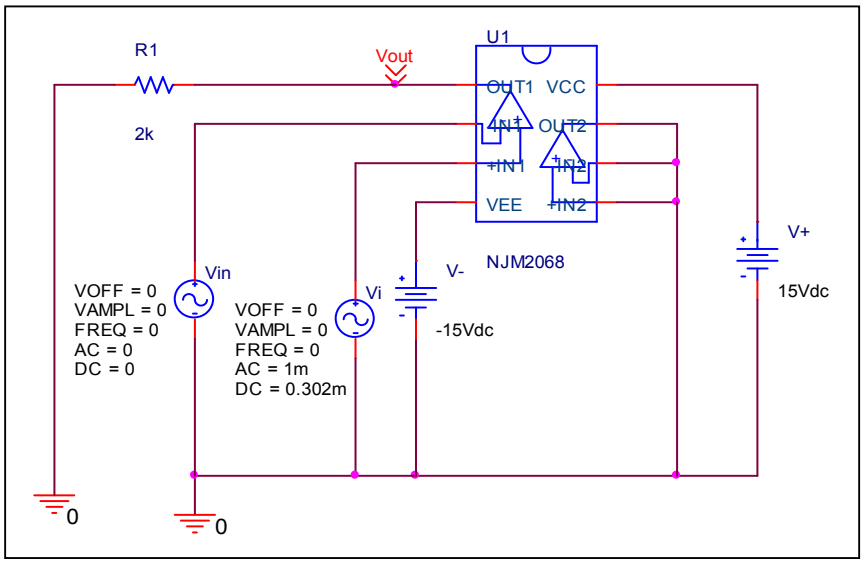


Remark Open Loop Voltage Gain vs. Frequency

Before

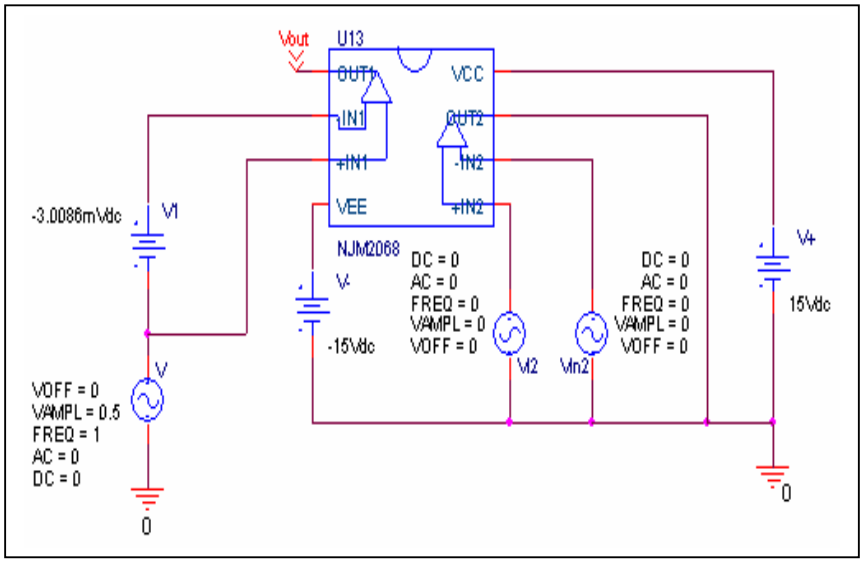


After



Remark Common-Mode Rejection Voltage gain

Before



After