

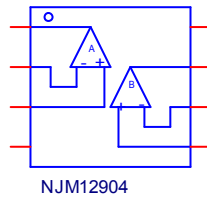
Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER
PART NUMBER: NJM12904
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

SPice Model



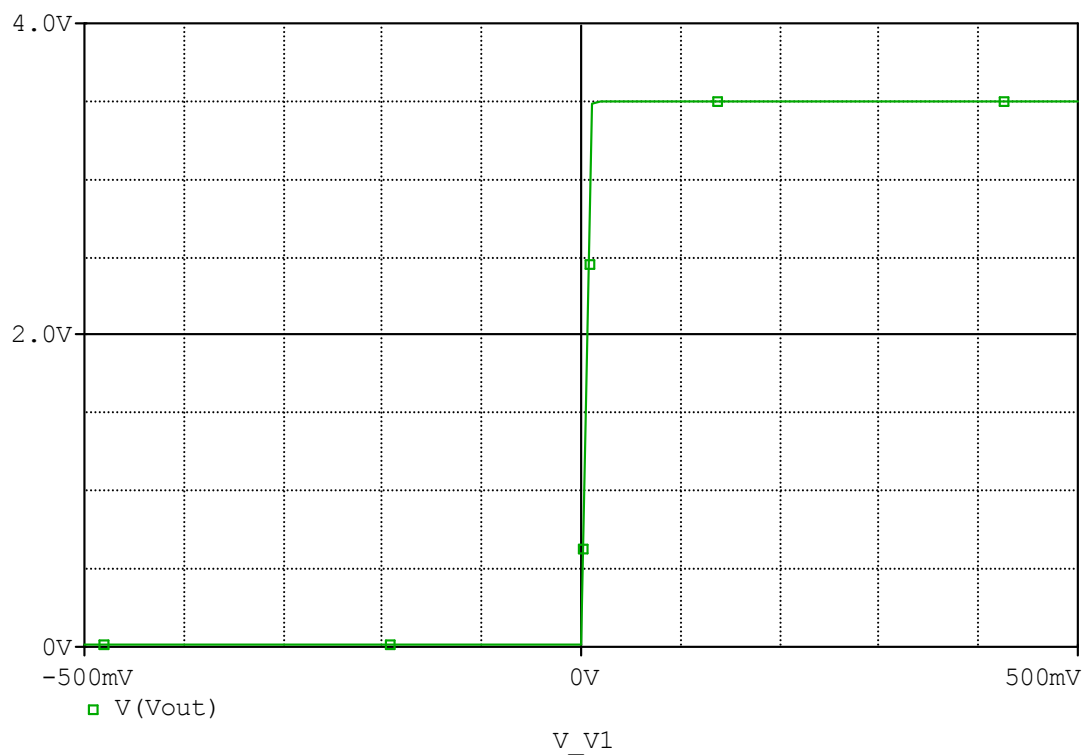
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*$
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM12904 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1  +IN1 -IN1 V+ V- OUT1 NJM12904_ME
X_U2  +IN2 -IN2 V+ V- OUT2 NJM12904_ME
.ends NJM12904
.subckt NJM12904_ME 1 2 3 4 5
c1  11 12 8.6603E-12
c2  6 7 30.000E-12
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 12.707E6 -1E3 1E3 13E6 -13E6
ga  6 0 11 12 314.79E-6
gcm 0 6 10 99 17.702E-9
iee 3 10 dc 21.940E-6
hlim 90 0 vlim 1K
q1  11 2 13 qx1
q2  12 1 14 qx2
r2  6 9 100.00E3
rc1 4 11 3.1767E3
rc2 4 12 3.1767E3
re1 13 10 813.26
re2 14 10 813.26
ree 10 99 9.1158E6
ro1 8 5 50
ro2 7 99 25
rp  3 4 50.011
vb  9 0 dc 0
vc  3 53 dc 2.3080
ve  54 4 dc .80796
vlim 7 8 dc 0
vlp 91 0 dc 29.500
vln 0 92 dc 29.500
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=480.26)
.model qx2 PNP(Is=835.0806E-18 Bf=636.63)
.ends
*$

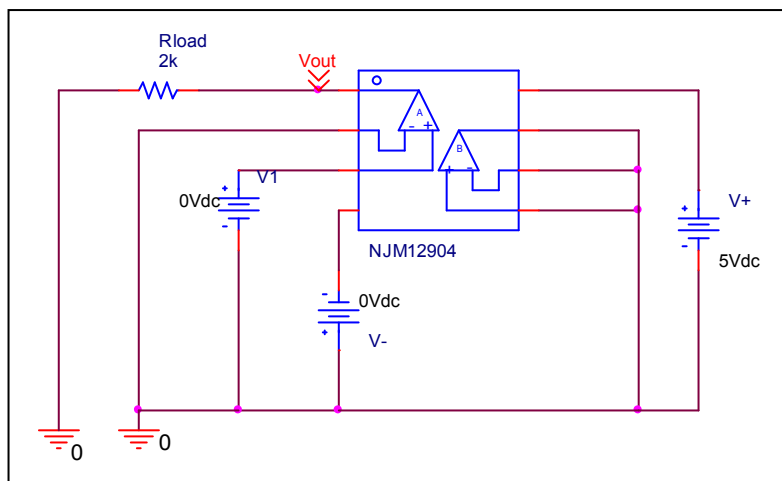
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Output Voltage Swing

Simulation result



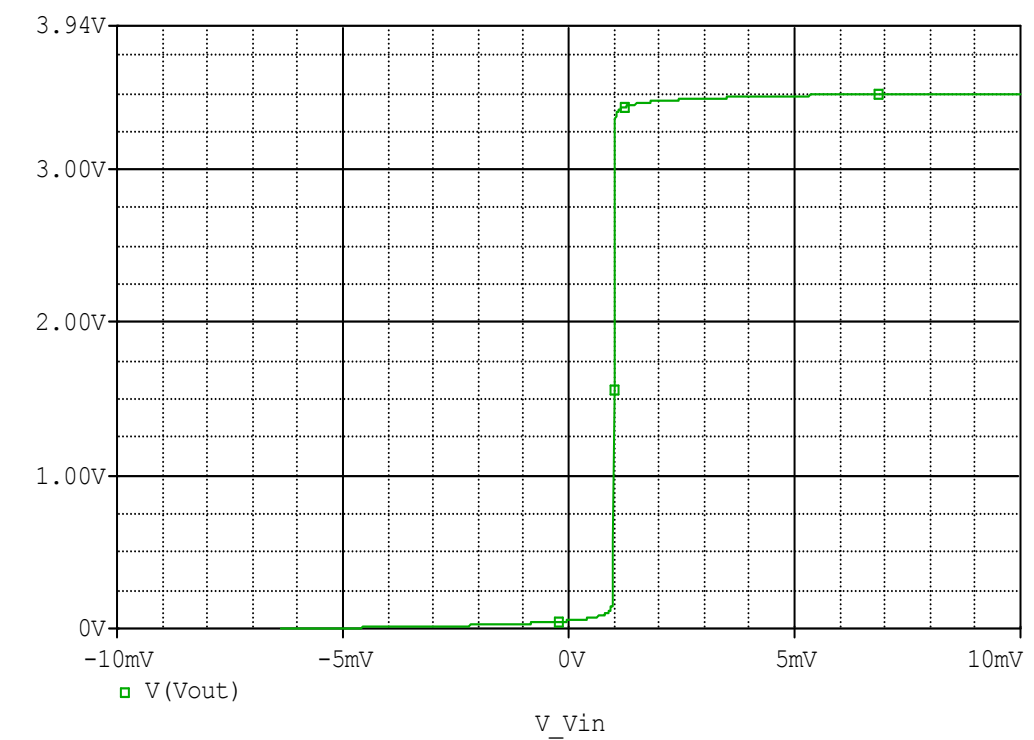
Evaluation circuit



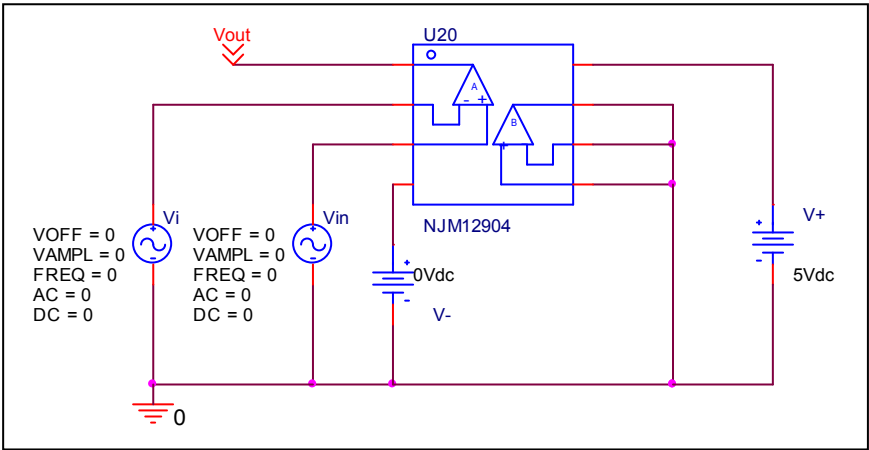
Output Voltage Swing	Measurement	Simulation	%Error
+Vout(V)	3.500	3.492	0.228

Input Offset Voltage

Simulation result



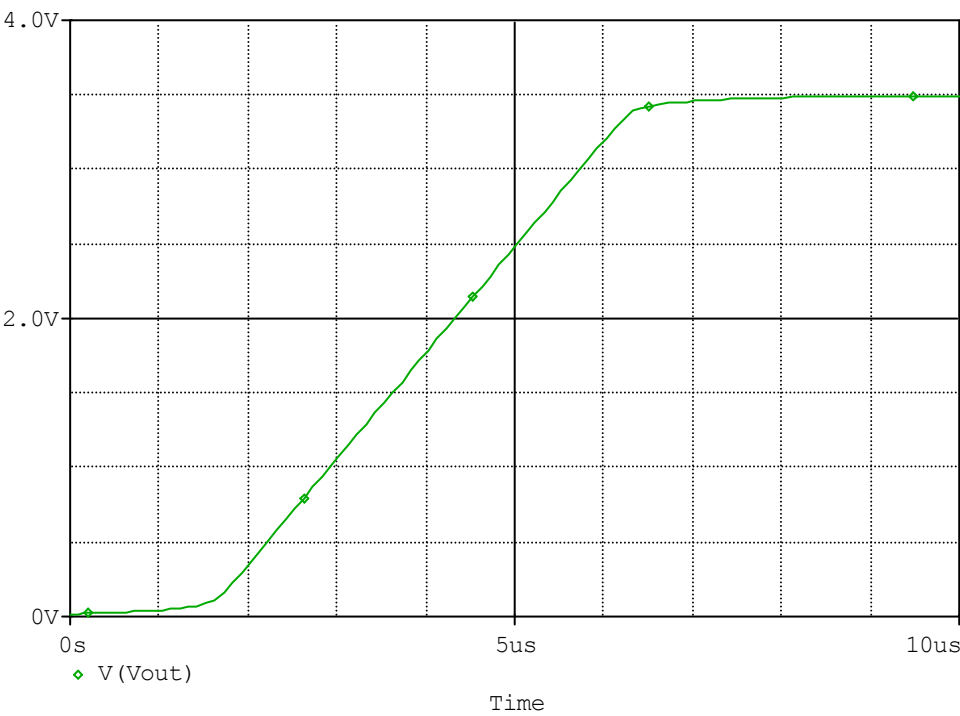
Evaluation circuit



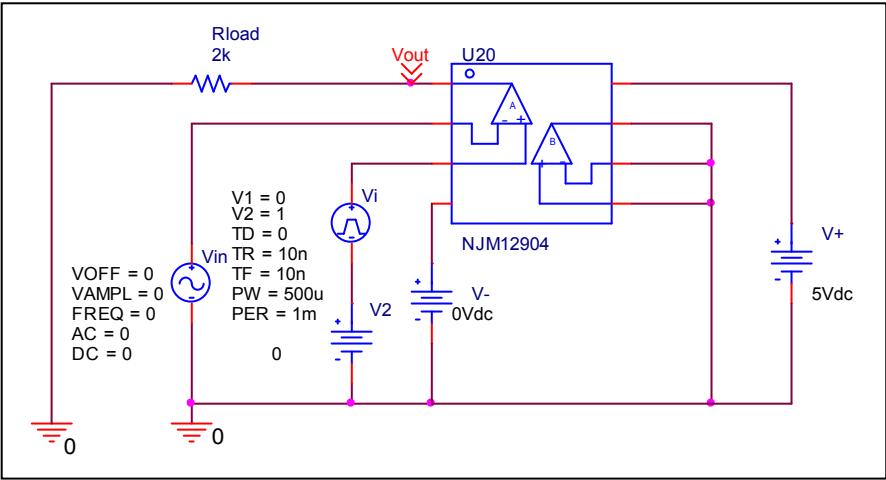
Vos(mV)	Measurement	Simulation	Error
	1	1	0

Slew Rate

Simulation result



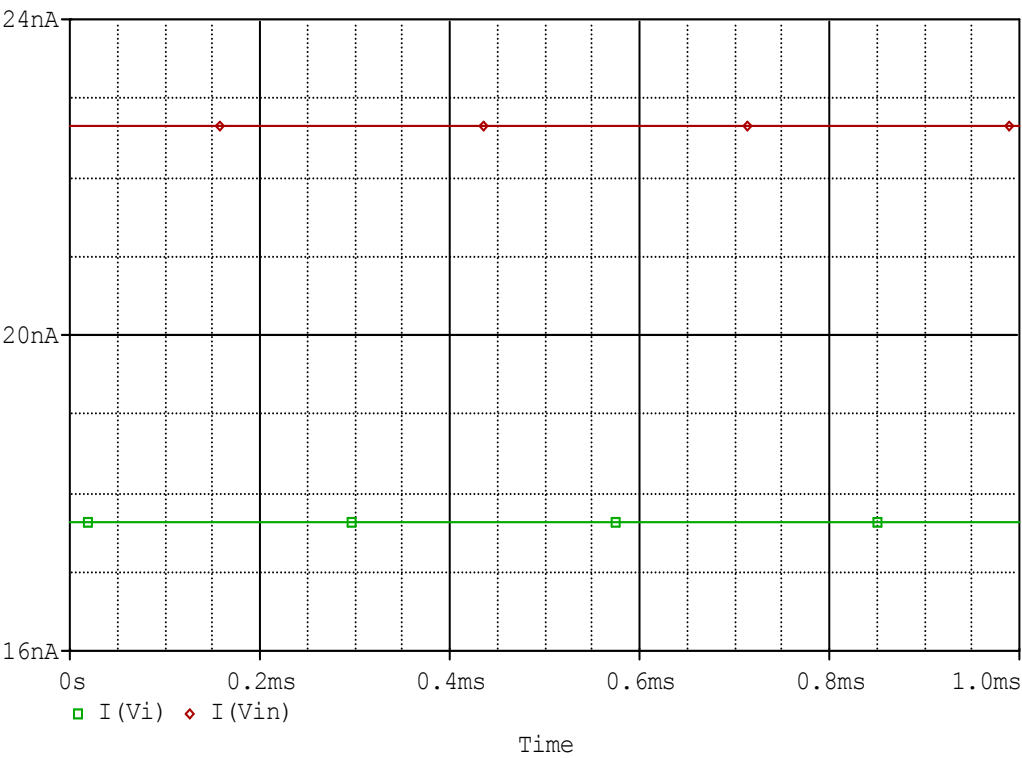
Evaluation circuit



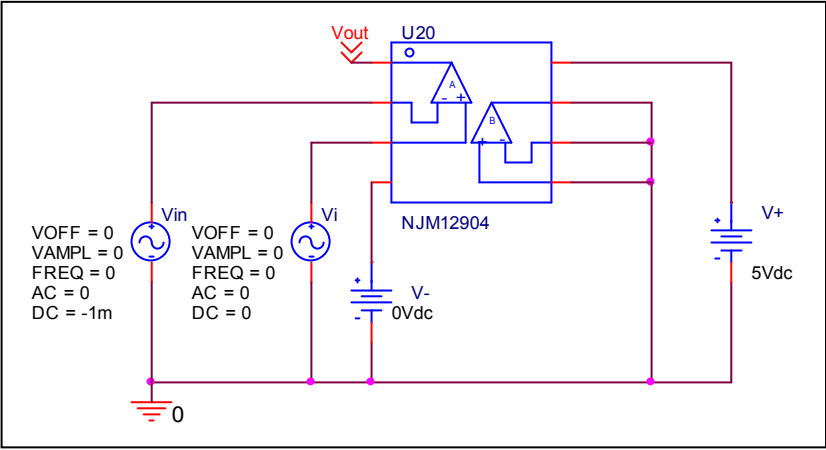
Slew Rate(v/us)	Measurement	Simulation	%Error
	0.700	0.72	2.857

Input current

Simulation result



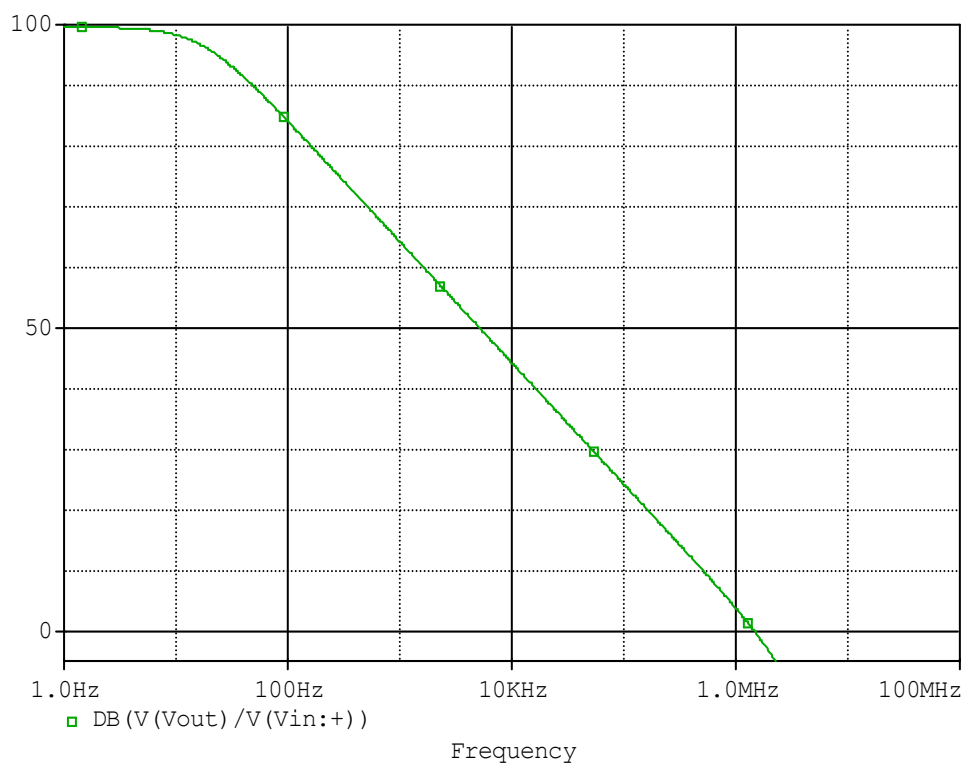
Evaluation circuit



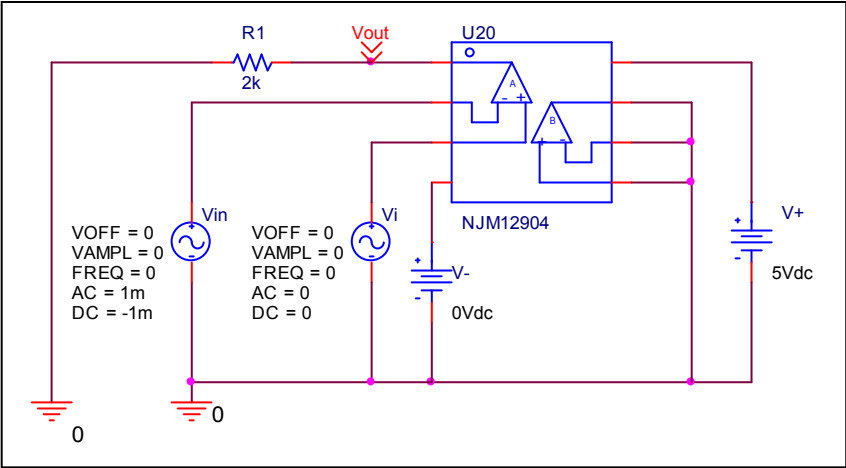
	Measurement	Simulation	%Error
Ib(nA)	20.000	20.100	0.500
Ibos(nA)	5.000	4.981	0.400

Open Loop Voltage Gain vs. Frequency

Simulation result



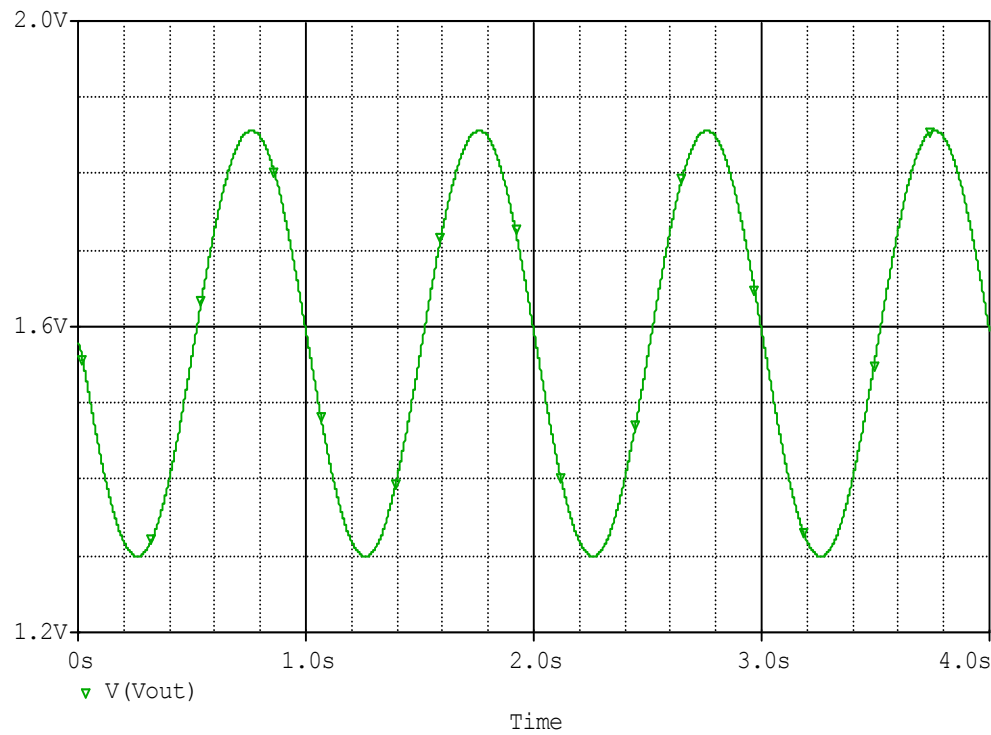
Evaluation circuit



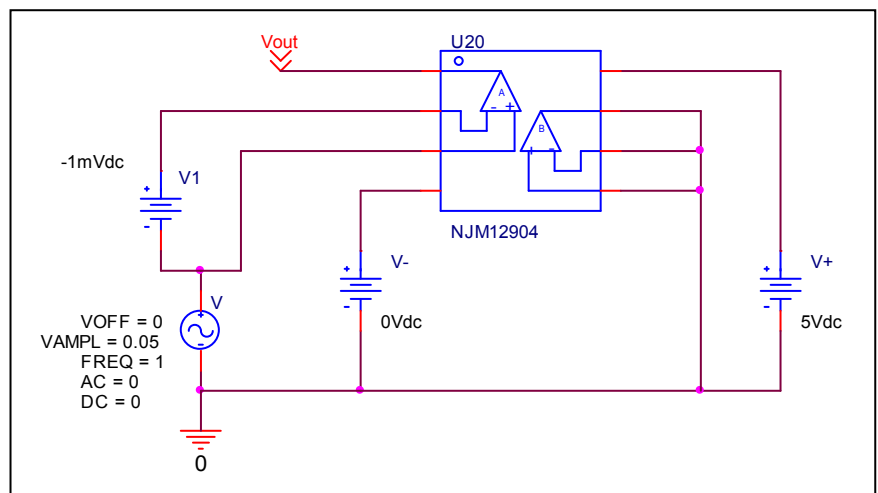
	Measurement	Simulation	%Error
f-0dB(MHz)	1.500	1.446	-3.600
Av-dc(dB)	100.000	99.615	-0.385

Common-Mode Rejection Voltage gain

Simulation result



Evaluation circuit

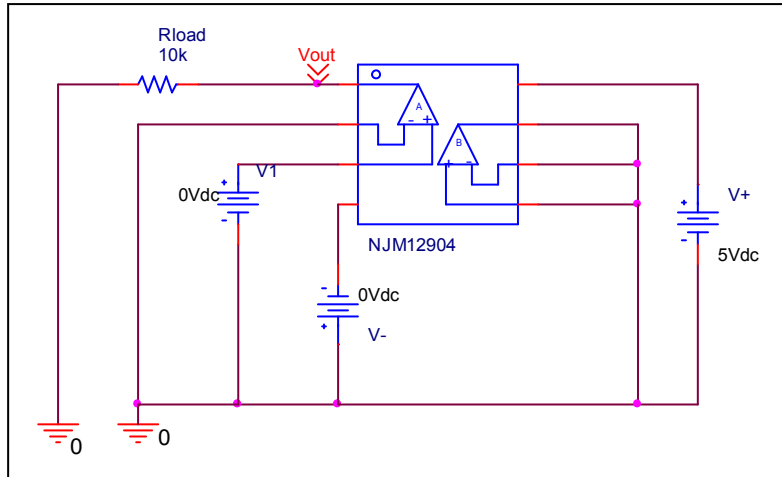


Common Mode Reject Ratio= $98809/5.55=17803$

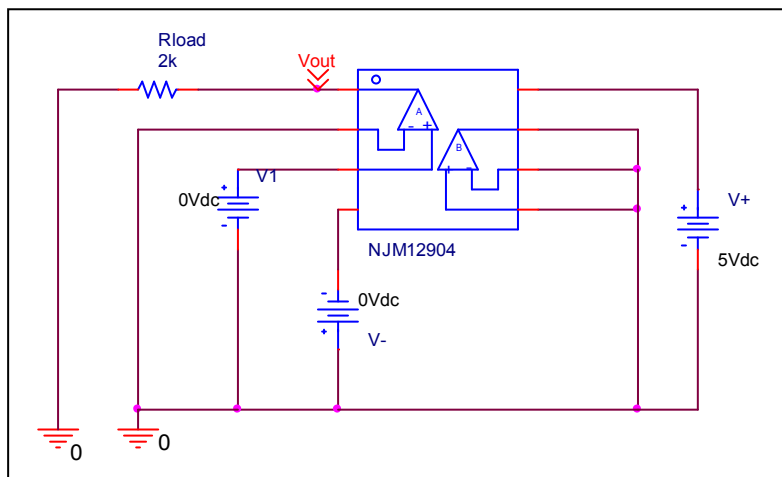
CMRR(dB)	Measurement	Simulation	%Error
	85.000	85.01	0.012

Remark Output Voltage Swing

Before

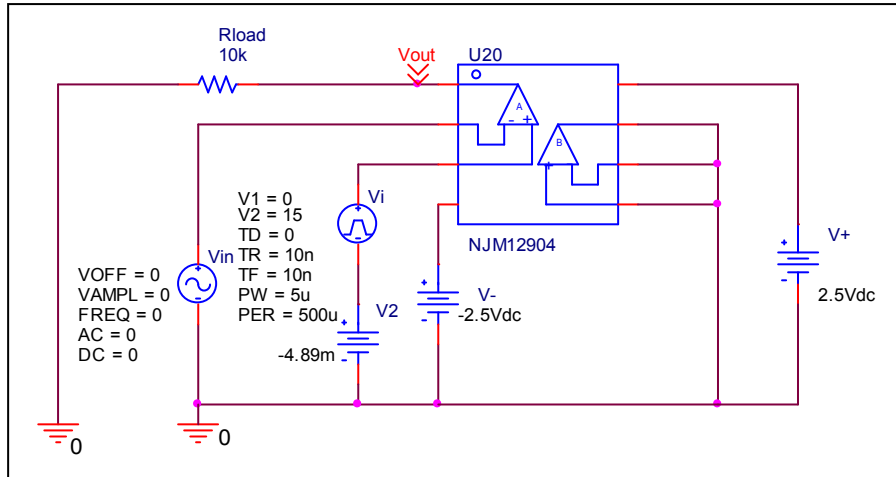


After

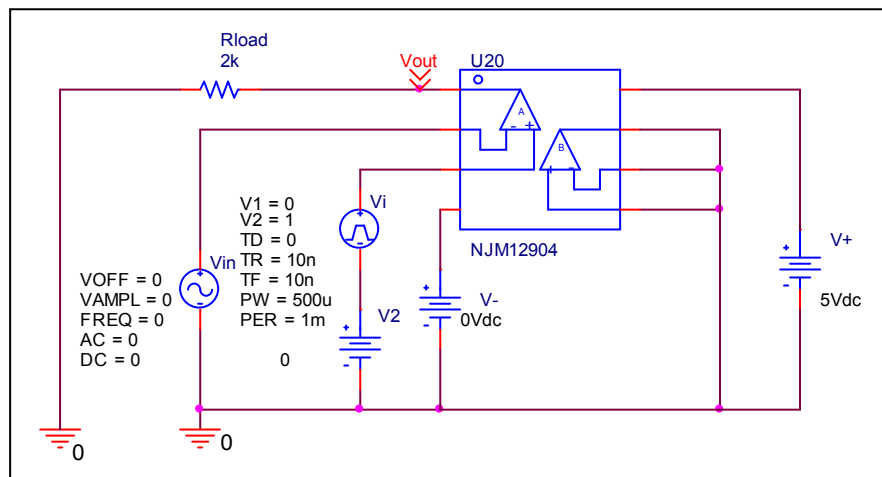


Remark Slew Rate

Before

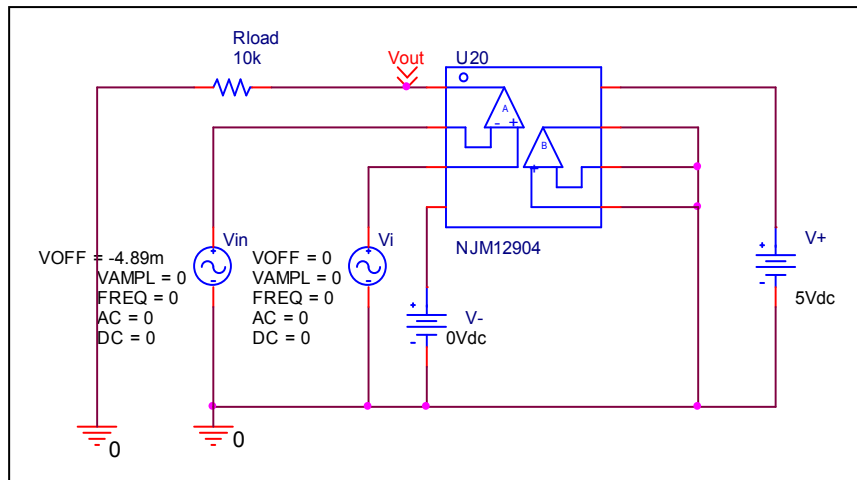


After

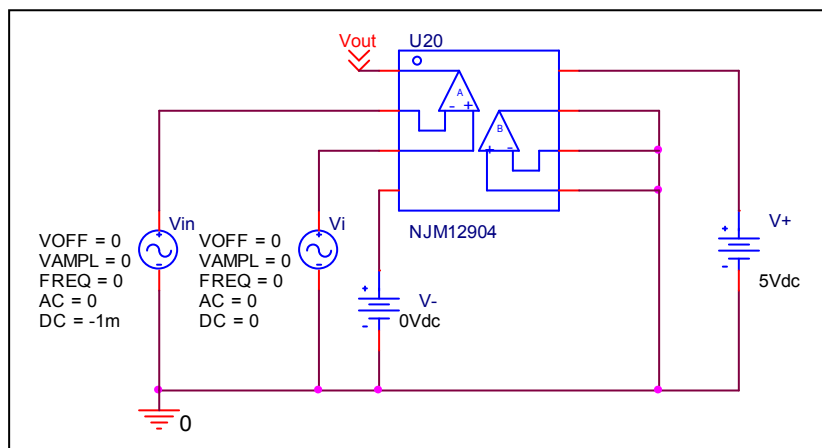


Remark Input current

Before

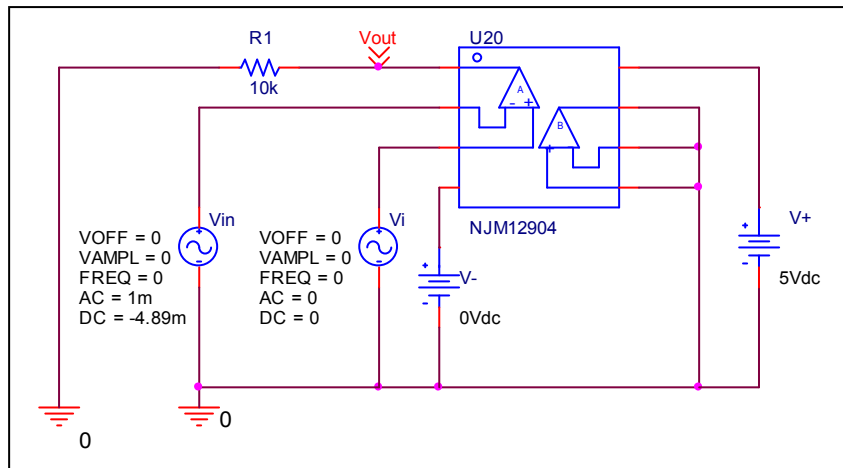


After

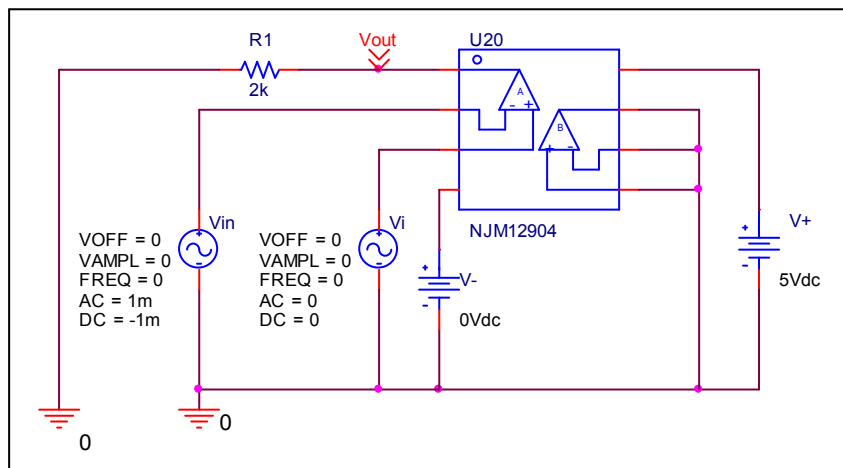


Remark Open Loop Voltage Gain vs. Frequency

Before

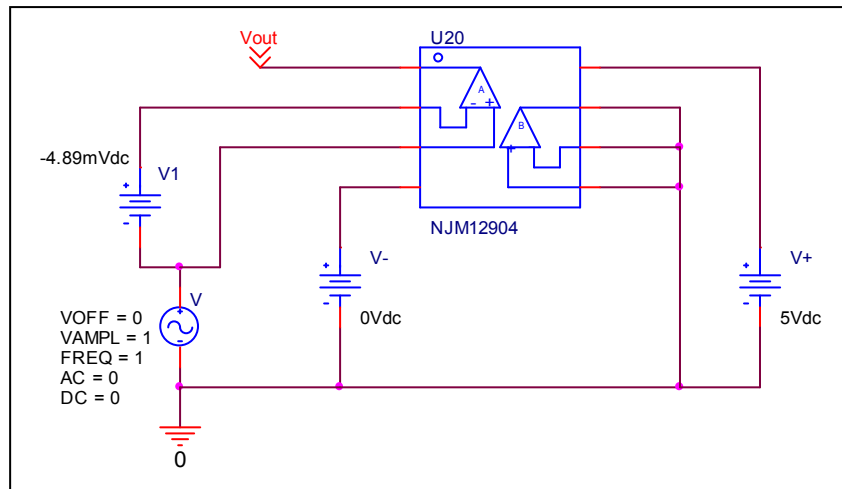


After



Remark Common-Mode Rejection Voltage gain

Before



After

