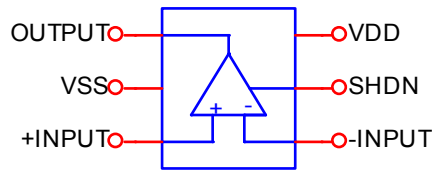


Device Modeling Report

COMPONENTS: CMOS OPERATIONAL AMPLIFIER
PART NUMBER: NJU7098
MANUFACTURER: NEW JAPAN RADIO
Remark:VDD=5.0V



Pin Configuration



Spice Model (1/2)

```

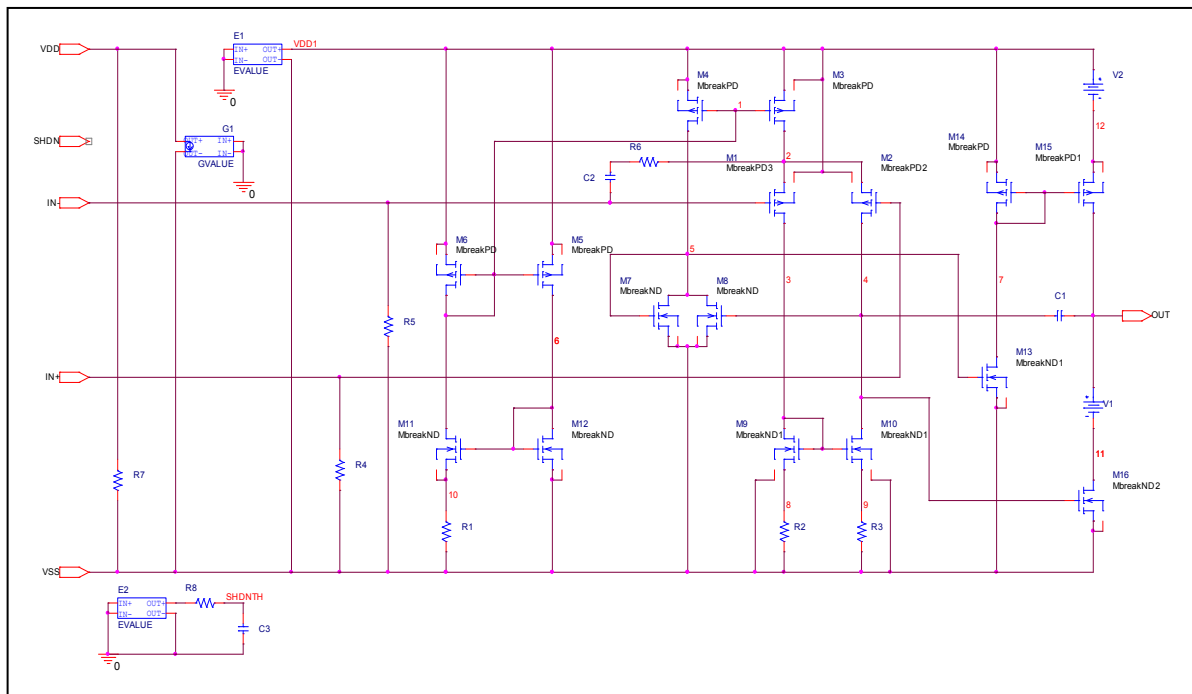
*$
*PART NUMBER: NJU7098
*MANUFACTURER: NEW JAPAN RADIO
*CMOS OPAMP
*All Rights Reserved Copyright (C) Bee Technologies Corporation 2009
*Remark: VDD=5.0V
.SUBCKT NJU7098 IN+ IN- VDD VSS OUT SHDN
M_M1      3 IN- 2 VDD1 MbreakPD3      L=6u W=19.89894m
M_M2      4 IN+ 2 VDD1 MbreakPD2      L=6u W=10.10106m
M_M3      2 1 VDD1 VDD1 MbreakPD
M_M4      5 1 VDD1 VDD1 MbreakPD
M_M5      6 1 VDD1 VDD1 MbreakPD
M_M6      1 1 VDD1 VDD1 MbreakPD
M_M7      5 5 VSS VSS MbreakND
M_M8      5 4 VSS VSS MbreakND
M_M9      3 3 8 VSS MbreakND1          L=6u W=12m
M_M10     4 3 9 VSS MbreakND1          L=6u W=5m
M_M11     1 6 10 10 MbreakND
M_M12     6 6 VSS VSS MbreakND
M_M13     7 5 VSS VSS MbreakND1
M_M14     7 7 VDD1 VDD1 MbreakPD
M_M15     OUT 7 12 12 MbreakPD1        L=6u W=203m
M_M16     11 4 VSS VSS MbreakND2       L=6u W=55.5m
R_R1      10 VSS 315
R_R2      8 VSS 2k
R_R3      9 VSS 3.99k
R_R4      IN+ VSS 10E12
R_R5      IN- VSS 25E9
R_R6      2 N675617 7k
R_R7      VDD VSS 333.333k
R_R8      N675675 SHDNTH 100
C_C1      OUT 4 7p
C_C2      IN- N675617 17p
C_C3      SHDNTH 0 100p
V_V1      OUT 11 0.00091
V_V2      VDD1 12 0.026
E_E1      VDD1 VSS VALUE {
+ IF(V(SHDN,VSS)>V(SHDNTH),V(VDD,VSS),0.01) }
E_E2      N675675 0 VALUE { IF(V(VDD1,VSS)>1,0.5,2.5) }
G_G1      VDD VSS VALUE { IF(V(SHDN,VSS)>V(SHDNTH),0.585m,0) }

```

Spice Model (2/2)

```
.model MbreakND NMOS ( LEVEL=3 L=6u W=3.2m VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=1.000E6 TOX=2.0E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakND1 NMOS (LEVEL=3 L=6u W=500m VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=10.000E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakND2 NMOS ( LEVEL=3 VTO=0 RS=10.000E-3 RD=10.000E-3
+ RDS=1.0000E6 TOX=2.0000E-6 CBD=23.5E-10 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakPD PMOS ( LEVEL=3 L=6u W=19.5m VTO=0 RS=10.000E-3
+ RD=10.00E-3 RDS=1.00E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=1E-6 )
.MODEL MbreakPD1 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.000E-3
+ RDS=1.00E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3 KP=1E-6 )
.MODEL MbreakPD2 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.00E-3
+ RDS=150E6 TOX=2.0000E-6 RG=5 RB=1.000E-3 KP=1E-6)
.MODEL MbreakPD3 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.00E-3
+ RDS=1.148E6 TOX=2.000E-6 RG=5 RB=1.000E-3 KP=1E-6 )
.ENDS NJU7098
*$
```

Equivalent Circuit

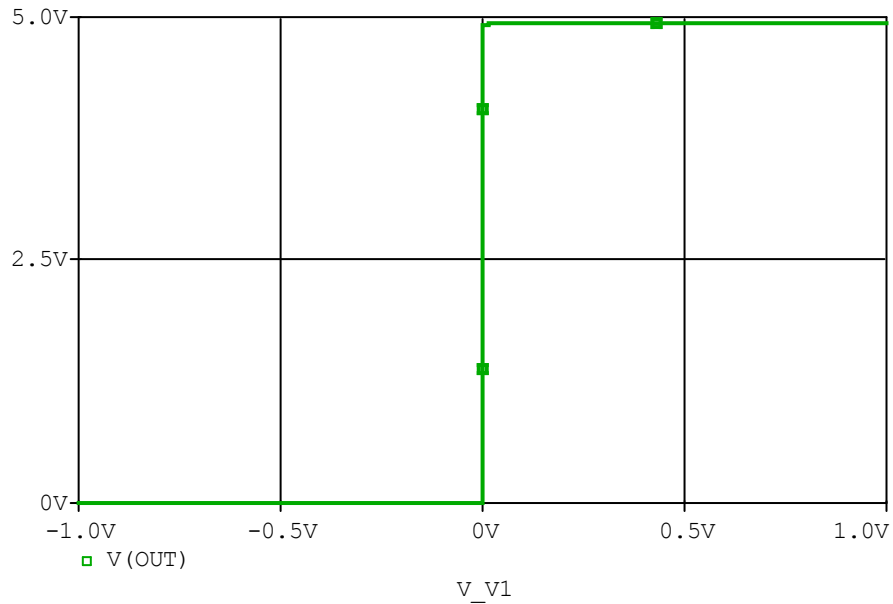


MOSFET MODEL

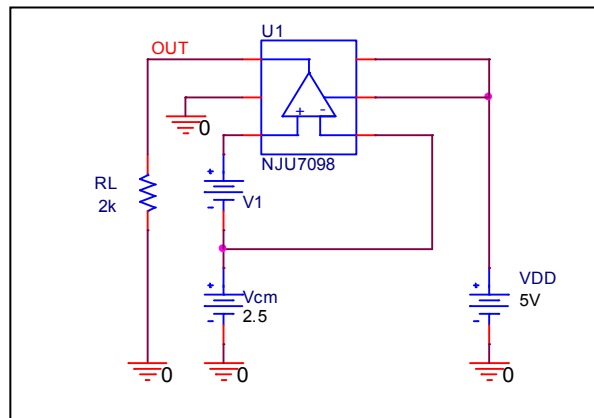
PSpice model parameter	Model description
LEVEL	
L	Channel Length
W	Channel Width
KP	Transconductance
RS	Source Ohmic Resistance
RD	Ohmic Drain Resistance
VTO	Zero-bias Threshold Voltage
RDS	Drain-Source Shunt Resistance
TOX	Gate Oxide Thickness
CGSO	Zero-bias Gate-Source Capacitance
CGDO	Zero-bias Gate-Drain Capacitance
CBD	Zero-bias Bulk-Drain Junction Capacitance
MJ	Bulk Junction Grading Coefficient
PB	Bulk Junction Potential
FC	Bulk Junction Forward-bias Capacitance Coefficient
RG	Gate Ohmic Resistance
IS	Bulk Junction Saturation Current
N	Bulk Junction Emission Coefficient
RB	Bulk Series Resistance
PHI	Surface Inversion Potential
GAMMA	Body-effect Parameter
DELTA	Width effect on Threshold Voltage
ETA	Static Feedback on Threshold Voltage
THETA	Mobility Modulation
KAPPA	Saturation Field Factor
VMAX	Maximum Drift Velocity of Carriers
XJ	Metallurgical Junction Depth
UO	Surface Mobility

Output Voltage Swing - VOH, VOL

Simulation result



Evaluation circuit



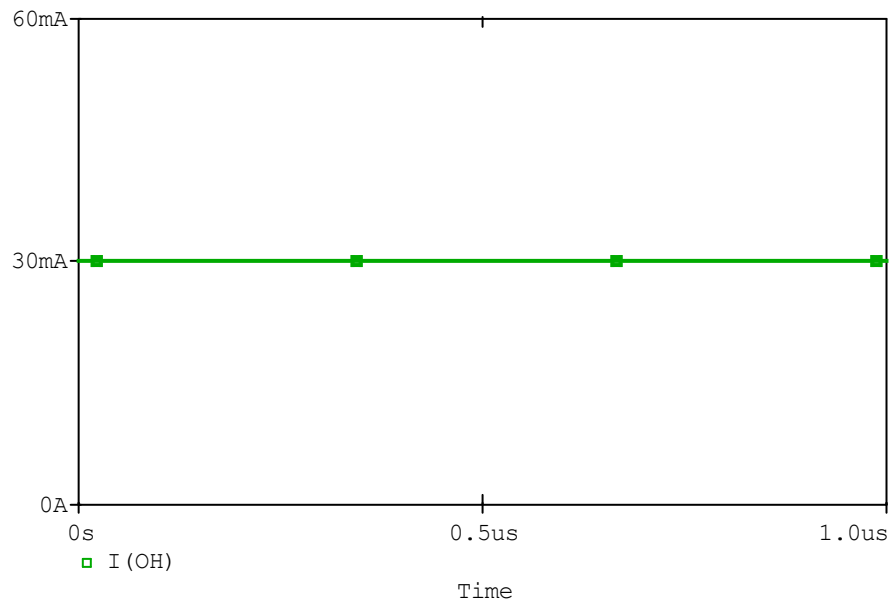
Comparison table

(RL=2KΩ to GND)

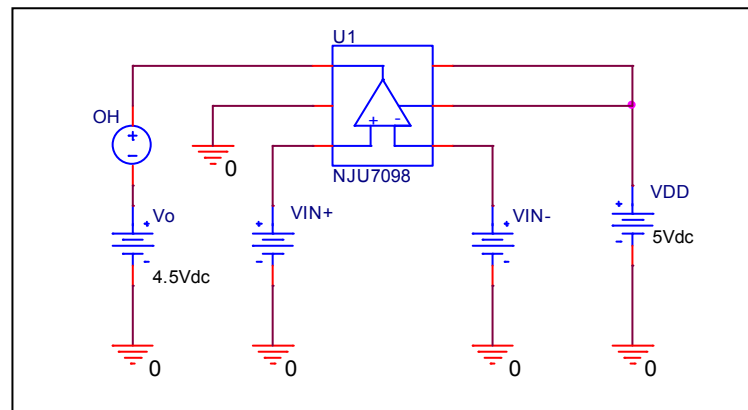
Parameter	Measurement	Simulation	%Error
VOH[V]	4.940	4.939	-0.020
VOL[mV]	1.000	1.000	0.000

Output Source Current - IOH

Simulation result



Evaluation circuit



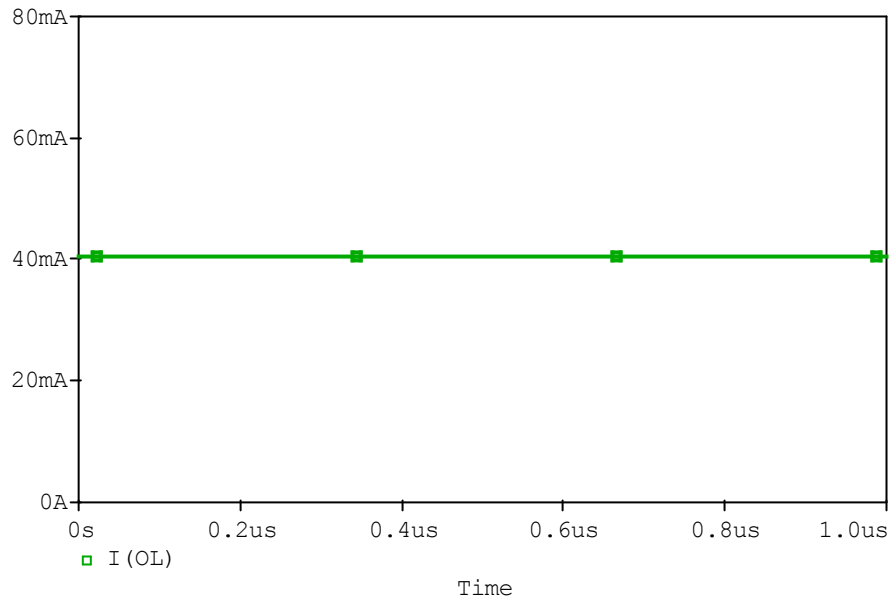
Comparison table

(Vo=4.5V)

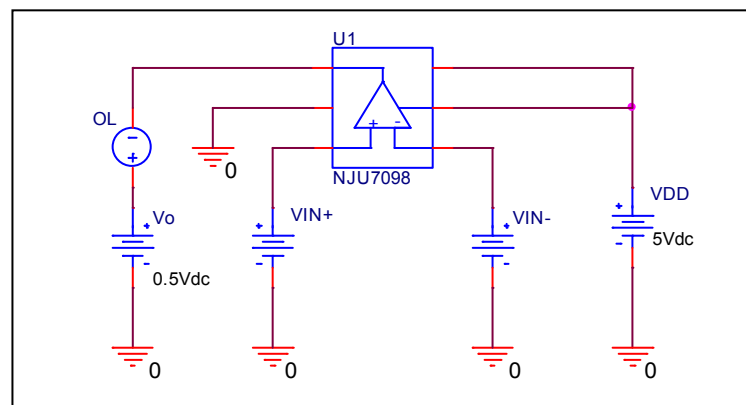
Parameter	Measurement	Simulation	%Error
IOH[mA]	30.000	30.239	0.797

Output Sink Current - IOL

Simulation result



Evaluation circuit



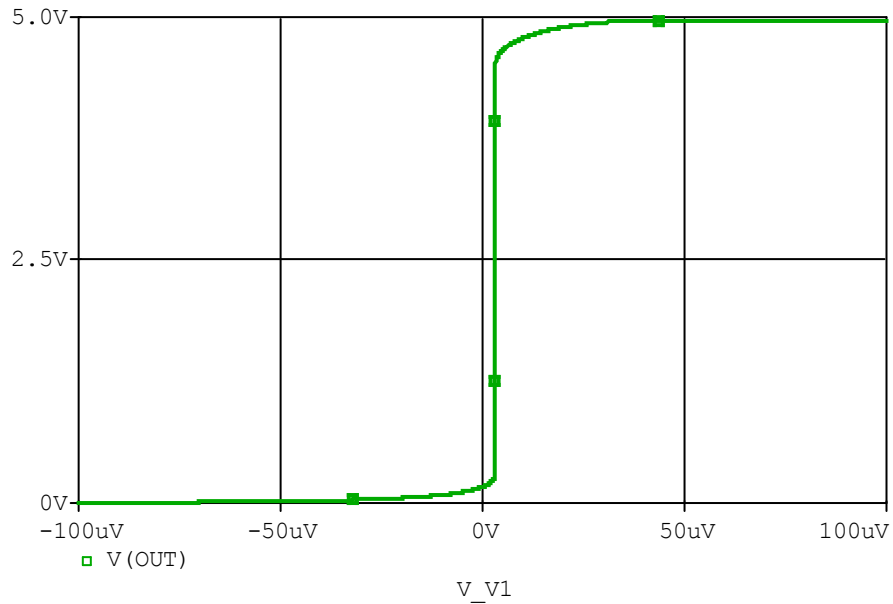
Comparison table

($V_o=0.5V$)

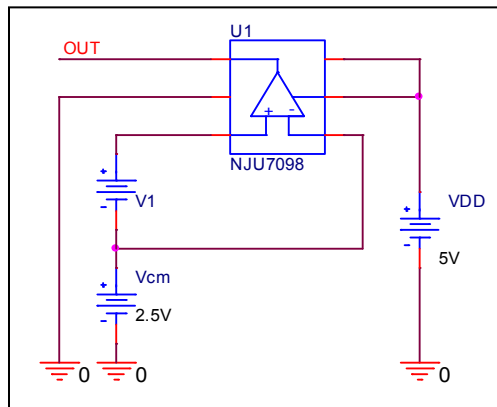
Parameter	Measurement	Simulation	%Error
IOL[mA]	40.000	40.368	0.920

Input Offset Voltage - VOS

Simulation result



Evaluation circuit

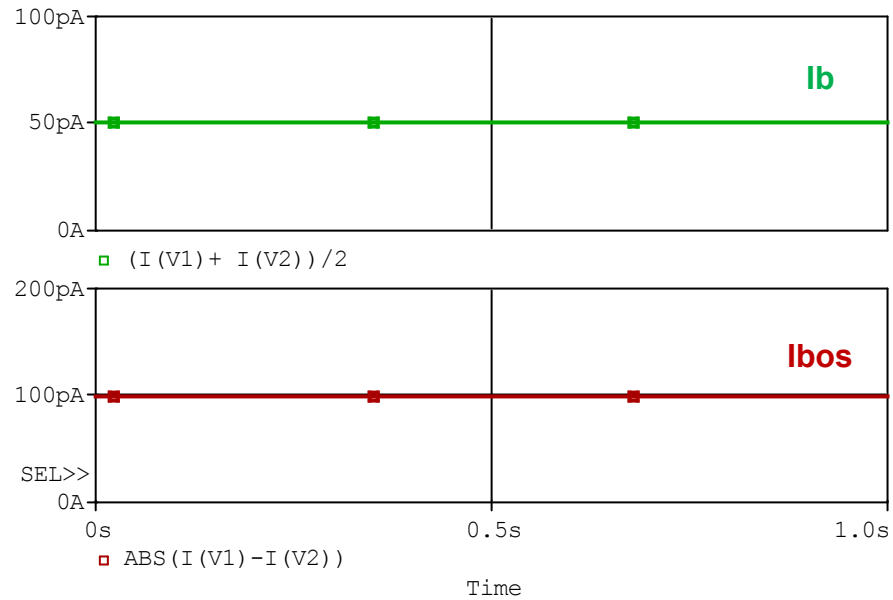


Comparison table

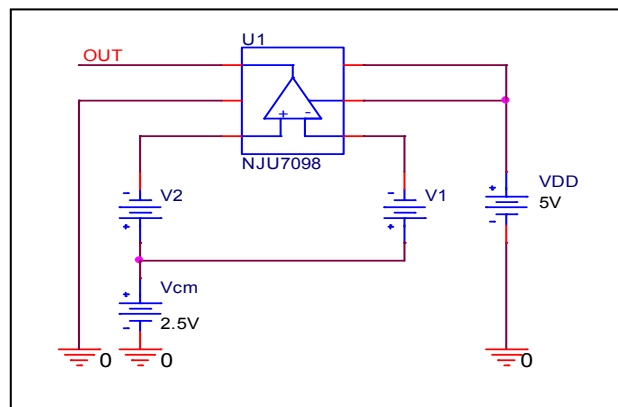
Parameter	Measurement	Simulation	%Error
VOS[μ V]	3.000	3.078	2.600

Input Current - Ib, Ibos

Simulation result



Evaluation circuit

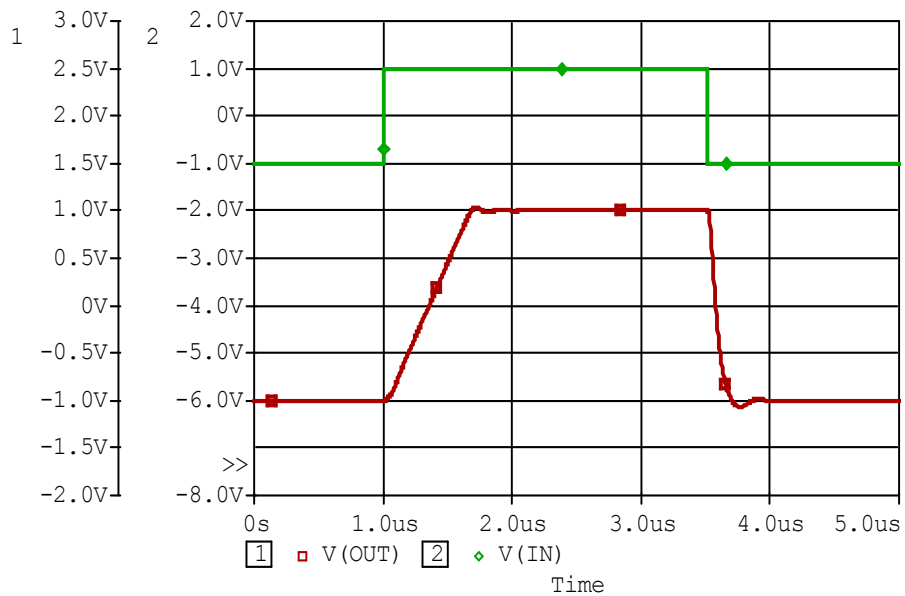


Comparison table

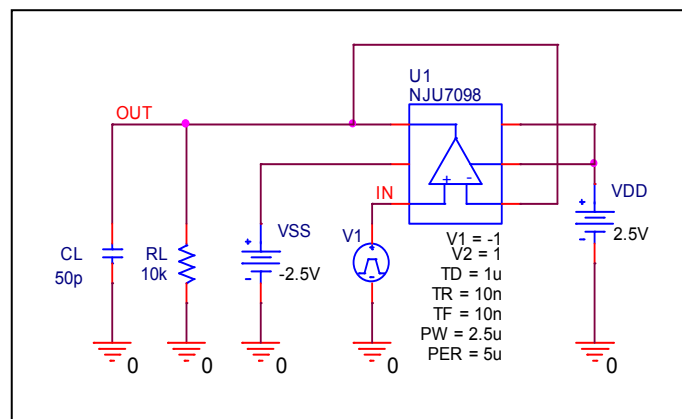
Parameter	Measurement	Simulation	%Error
I_b [pA]	50.000	50.125	0.250
I_{bos} [pA]	100.000	99.750	-0.250

Slew rate - SR

Simulation result



Evaluation circuit



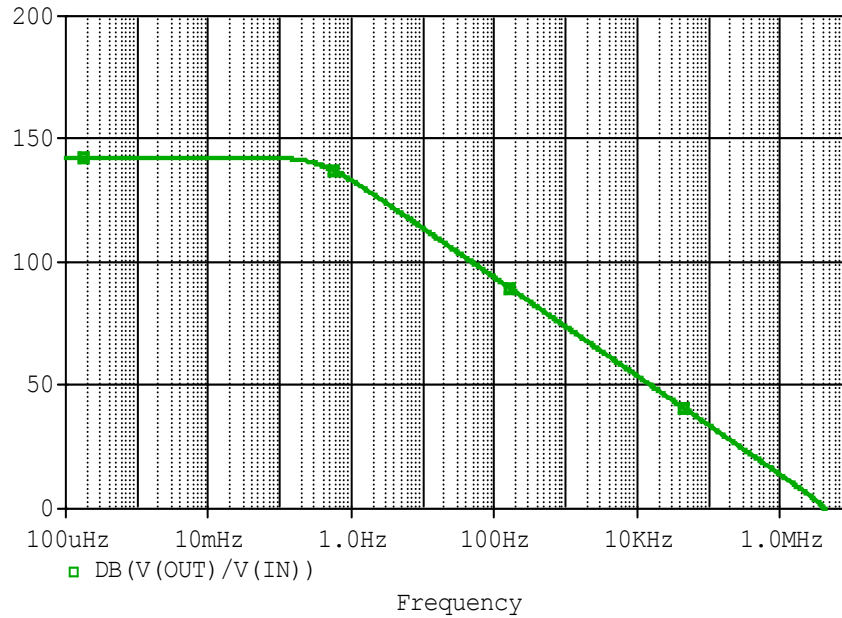
Comparison table

(AV=1, VIN=2Vp-p, RL=10KΩ)

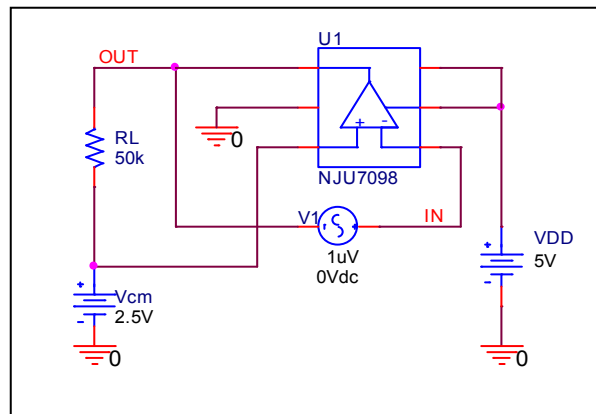
Parameter	Measurement	Simulation	%Error
+SR[V/us]	3.000	3.123	4.100
-SR[V/us]	12.000	12.442	3.683

Open loop voltage gain - AV

Simulation result



Evaluation Circuit



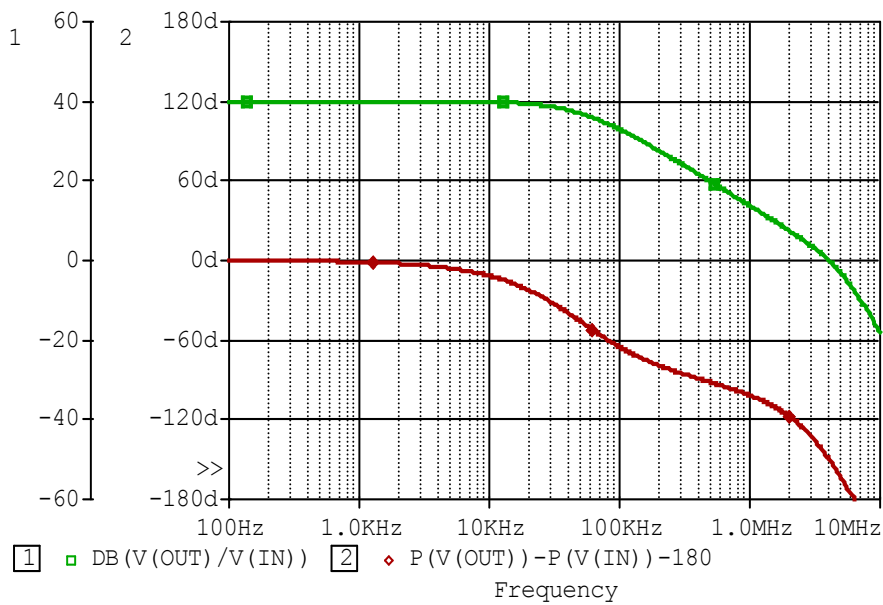
Comparison Table

($R_L \geq 10K\Omega$)

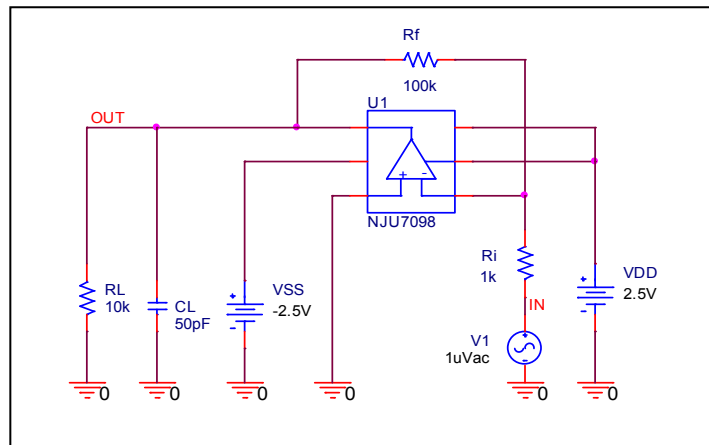
Parameter	Measurement	Simulation	%Error
AV[dB]	140.000	142.644	1.889

Gain Bandwidth Product - FT

Simulation result



Evaluation Circuit



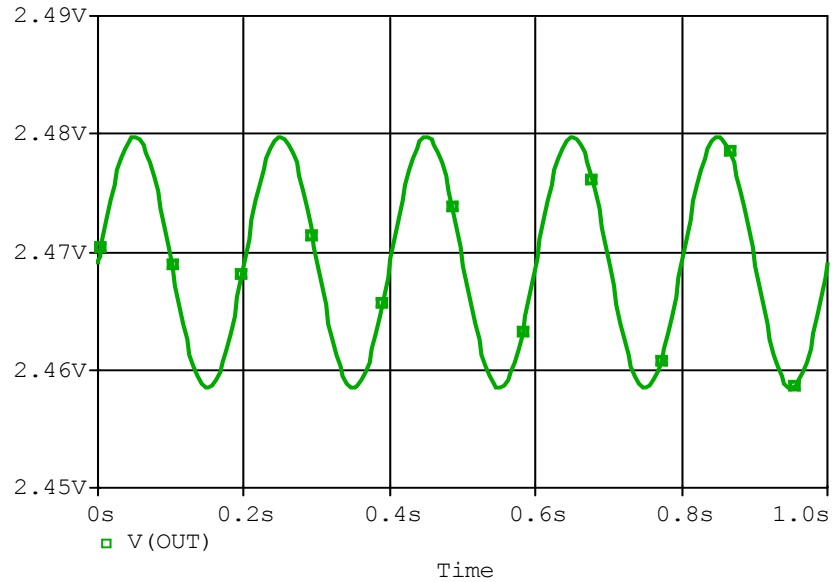
Comparison Table

(RL=10KΩ, CL=50pF)

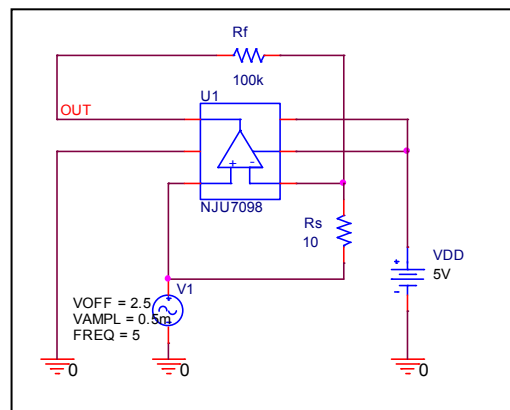
AV=40[dB]	Measurement	Simulation	%Error
GBWP[MHz]	4.000	4.089	2.225
Phase margin θ [°]	30.000	30.279	0.930

Common-mode rejection voltage gain - CMRR

Simulation result



Evaluation circuit



※ Common Mode Reject Ratio = $20 \times \text{LOG}(13558136.44/21.327) = 116.065\text{dB}$

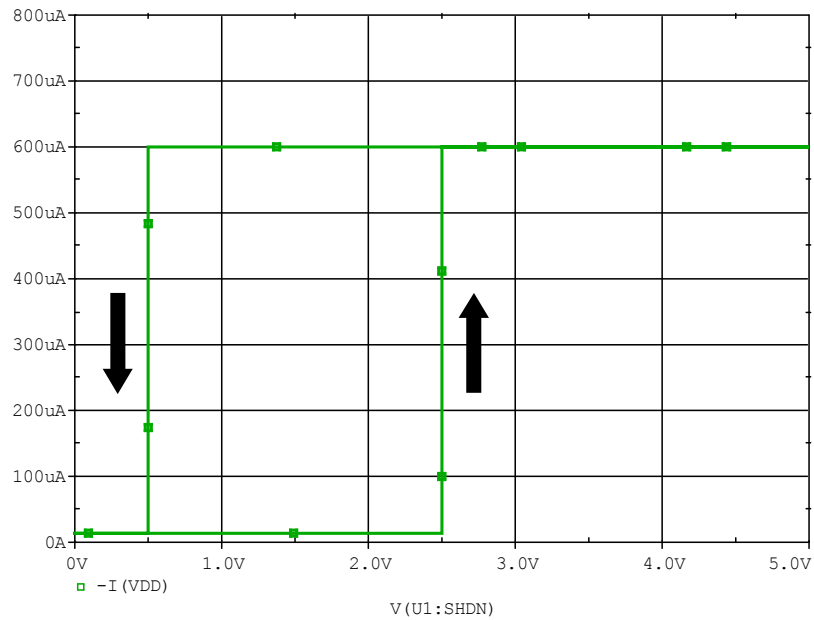
Comparison Table

(Vicm=0 ~3.5V)

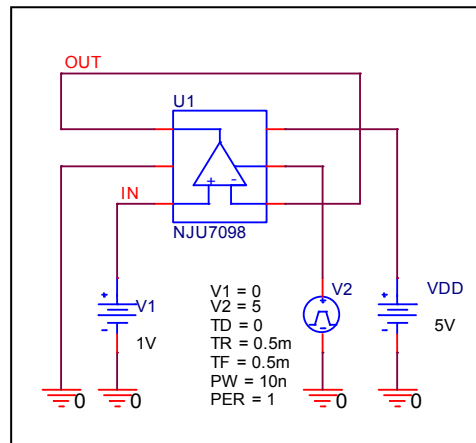
Parameter	Measurement	Simulation	%Error
CMRR[dB]	120.000	116.065	-3.279

Supply Current vs. Shutdown Pin Voltage

Simulation result



Evaluation Circuit



Comparison Table

(VDD=+5V, Gv=0dB,)

Parameter	Measurement	Simulation	%Error
V _{SHDNON} [V]	2.4	2.5	4.17
V _{SHDNOFF} [V]	0.5[Max.]	0.5	0