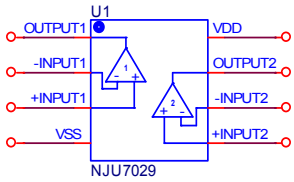
Device Modeling Report

COMPONENTS: CMOS OPERATIONAL AMPLIFIER
PART NUMBER: NJU7029
MANUFACTURER: NEW JAPAN RADIO

Bee Technologies Inc.

Pin Configuration



Spice Model (1/2)

```
*$
*PART NUMBER: NJU7029
*MANUFACTURER: NEW JAPAN RADIO
*CMOS OPAMP
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.SUBCKT NJU7029 1 2 3 4 5 6 7 8
X_U1    3 4 2 1 8       NJU7029_SUB
X_U2    5 4 6 7 8       NJU7029_SUB
.ENDS
.SUBCKT NJU7029_SUB INPUT+ VSS INPUT- OUTPUT VDD
M_M1      3 INPUT- 2 VDD        MbreakPD3     L=6u W=2.5m
M_M2       4 INPUT+ 2 VDD       MbreakPD2     L=6u W=2.5m
M_M3       2 1 VDD VDD          MbreakPD
M_M4       5 1 VDD VDD          MbreakPD
M_M5       6 1 VDD VDD          MbreakPD
M_M6       1 1 VDD VDD          MbreakPD
M_M7       5 5 VSS VSS          MbreakND
M_M8       5 4 VSS VSS          MbreakND
M_M9       3 3 8 VSS            MbreakND1     L=6u W=65m
M_M10      4 3 9 VSS            MbreakND1     L=6u W=85m
M_M11      1 6 10 10            MbreakND
M_M12      6 6 VSS VSS          MbreakND
M_M13      7 5 VSS VSS          MbreakND1
M_M14      7 7 VDD VDD          MbreakPD
M_M15      OUTPUT 7 12 12       MbreakPD1     L=2u W=50m
M_M16      11 4 VSS VSS         MbreakND2     L=2u W=15m
V_V1       OUTPUT 11            0.089
V_V2       VDD 12               0.099
R_R1       10 VSS               200k
R_R2       8 VSS                200
R_R3       9 VSS                200
R_R4       INPUT+ VSS           1.0E+12
R_R5       INPUT- VSS           3.0E+12
R_R6       VDD VSS              10.123E+3
C_C1       OUTPUT 4             0.415p
```
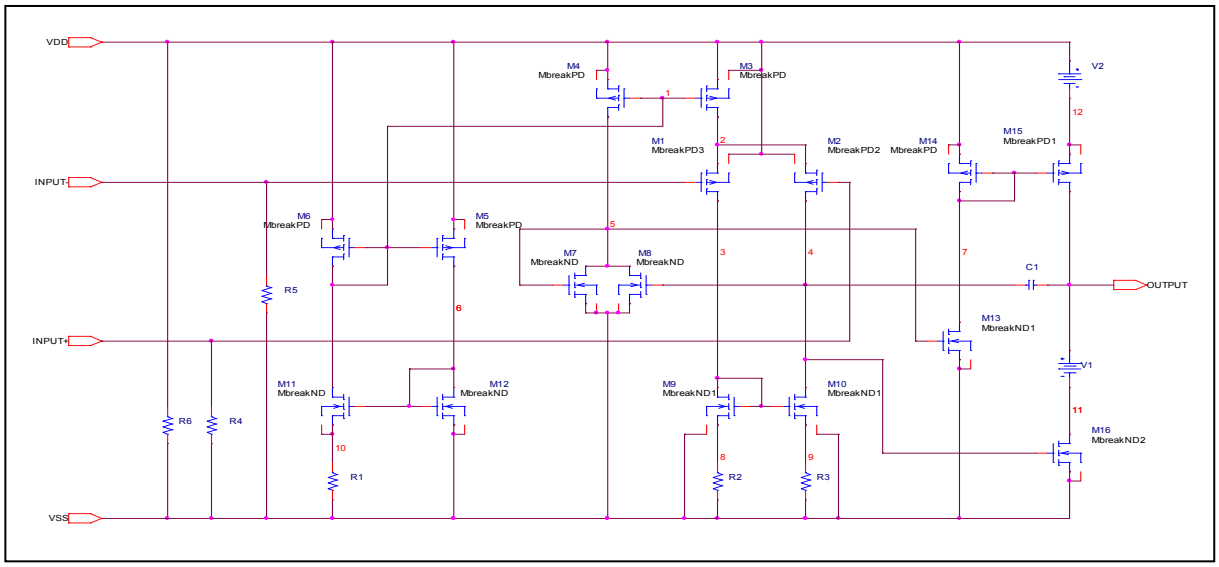

Spice Model (2/2)

```
.model MbreakND NMOS ( LEVEL=3 L=6u W=128u VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=10E6 TOX=2.0E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakND1 NMOS (LEVEL=3 L=6u W=200u VTO=0 RS=10.000E-3
+ RD=10.000E-3 RDS=2.4E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakND2 NMOS ( LEVEL=3 VTO=0 RS=10.000E-3 RD=10.000E-3
+ RDS=1.0000E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6)
.model MbreakPD PMOS ( LEVEL=3 L=6u W=27u VTO=0 RS=10.000E-3
+ RD=10.00E-3 RDS=1.00E9 TOX=2.0000E-6 RG=5 RB=1.0000E-3
+ KP=10E-6 )
.MODEL MbreakPD1 PMOS (LEVEL=3 VTO=-0.1 RS=10.000E-3 RD=10.000E-3
+ RDS=1.00E6 TOX=2.0000E-6 RG=5 RB=1.0000E-3 KP=50E-6 )
.MODEL MbreakPD2 PMOS (LEVEL=3 VTO=0 RS=10.000E-3 RD=10.00E-3
+ RDS=5E9 TOX=2.0000E-6 RG=5 RB=1.000E-3 KP=1E-6)
.MODEL MbreakPD3 PMOS (LEVEL=3 VTO=-5.25m RS=10.000E-3
RD=10.00E-3
+ RDS=5E9 TOX=2.000E-6 RG=5 RB=1.000E-3 KP=1E-6 )
.ENDS NJU7029_SUB
*$
```

Equivalent Circuit

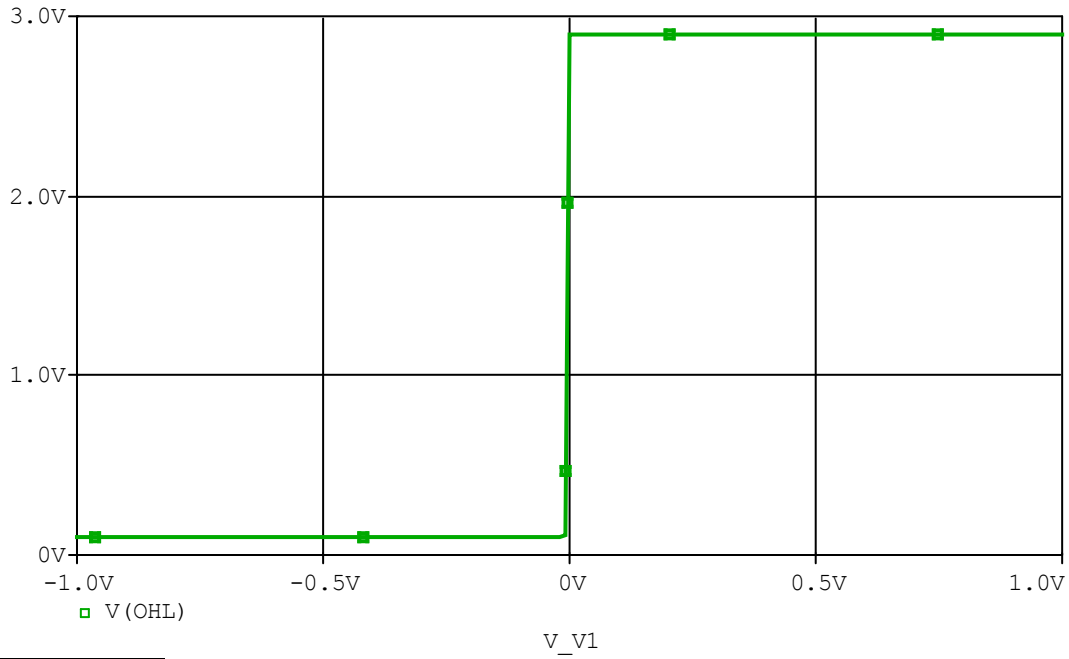


MOSFET MODEL

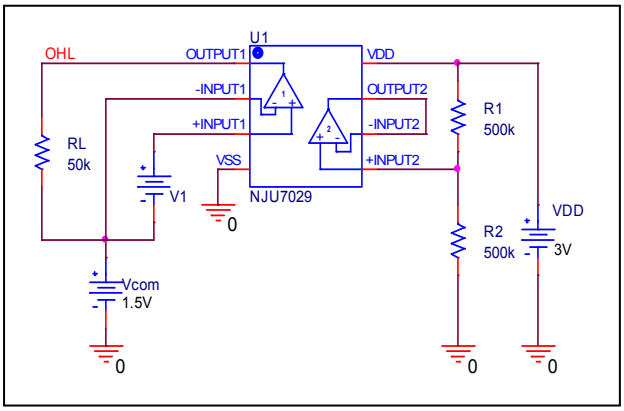
PSpice model parameter	Model description
LEVEL	
L	Channel Length
W	Channel Width
KP	Transconductance
RS	Source Ohmic Resistance
RD	Ohmic Drain Resistance
VTO	Zero-bias Threshold Voltage
RDS	Drain-Source Shunt Resistance
TOX	Gate Oxide Thickness
CGSO	Zero-bias Gate-Source Capacitance
CGDO	Zero-bias Gate-Drain Capacitance
CBD	Zero-bias Bulk-Drain Junction Capacitance
MJ	Bulk Junction Grading Coefficient
PB	Bulk Junction Potential
FC	Bulk Junction Forward-bias Capacitance Coefficient
RG	Gate Ohmic Resistance
IS	Bulk Junction Saturation Current
N	Bulk Junction Emission Coefficient
RB	Bulk Series Resistance
PHI	Surface Inversion Potential
GAMMA	Body-effect Parameter
DELTA	Width effect on Threshold Voltage
ETA	Static Feedback on Threshold Voltage
THETA	Mobility Modulation
KAPPA	Saturation Field Factor
VMAX	Maximum Drift Velocity of Carriers
XJ	Metallurgical Junction Depth
UO	Surface Mobility

Output Voltage Swing - V_{OH}, V_{OL}

Simulation result



Evaluation circuit



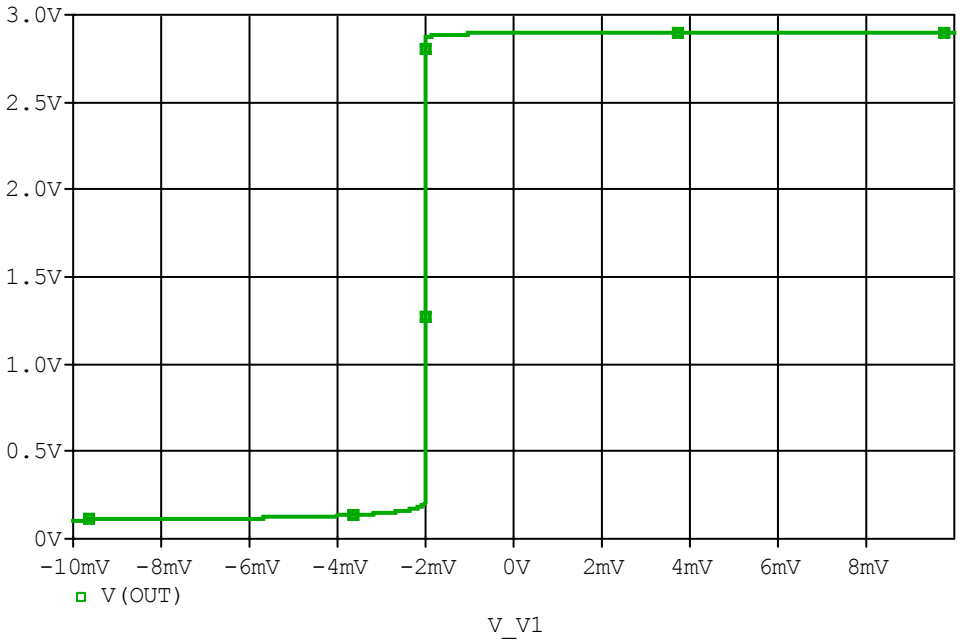
Comparison table

(Condition: R_L=50kΩ to 1.5V)

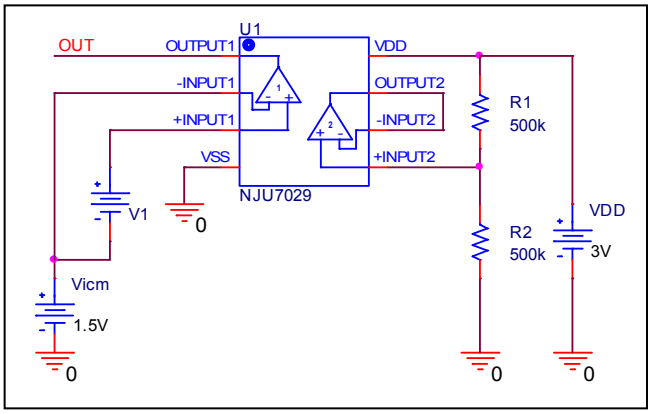
Parameter	Measurement	Simulation	%Error
V_{OH}[V]	**2.900**	**2.901**	**0.03**
V_{OL}[V]	**0.100**	**0.099**	**1.00**

Input Offset Voltage - V_{IO}

Simulation result



Evaluation circuit

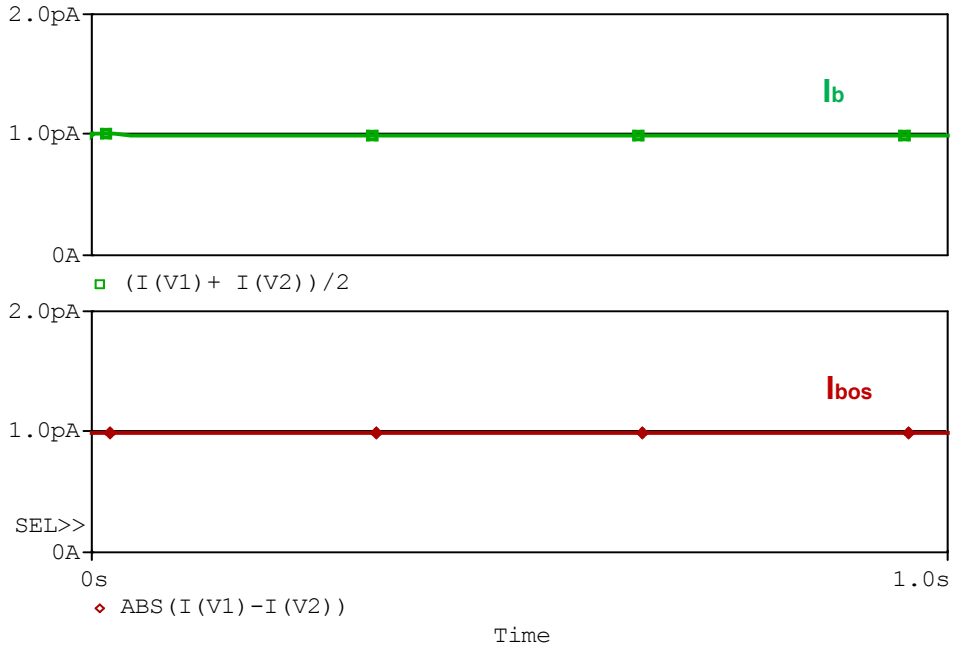


Comparison table

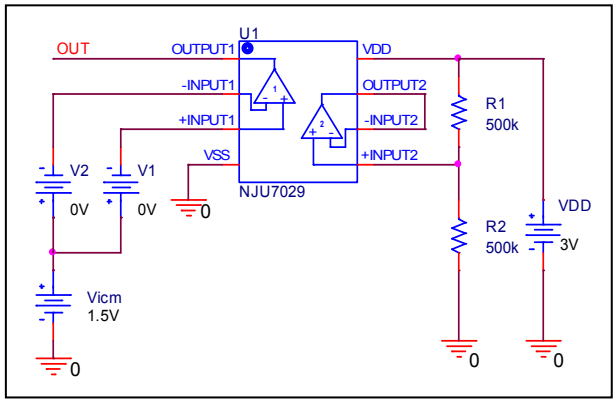
Parameter	Measurement	Simulation	%Error
$\|V_{IO}\|$ [mV]	2.000	2.0074	0.37

Input Current - I_b, I_{bos}

Simulation result



Evaluation circuit

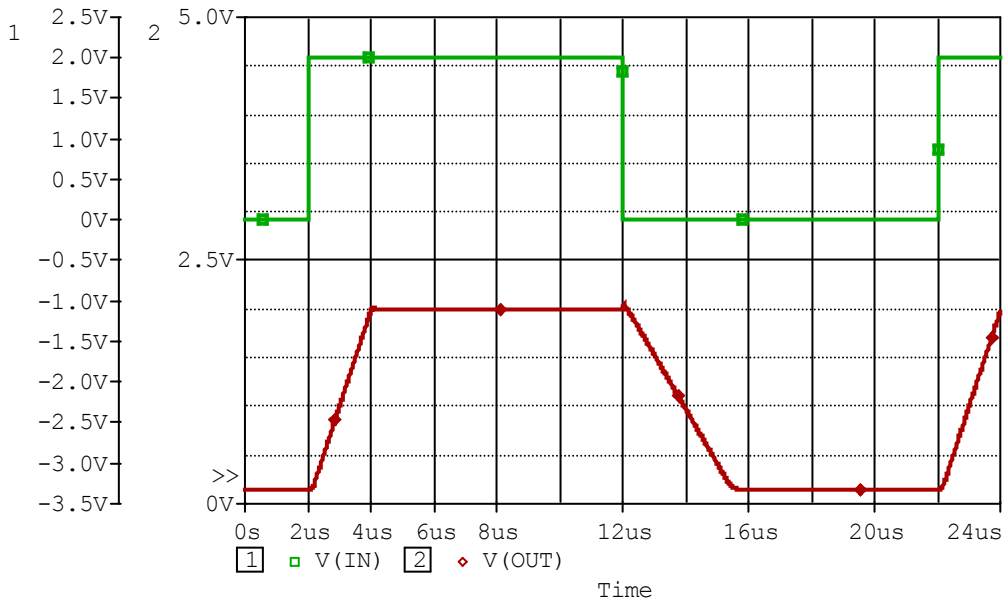


Comparison table

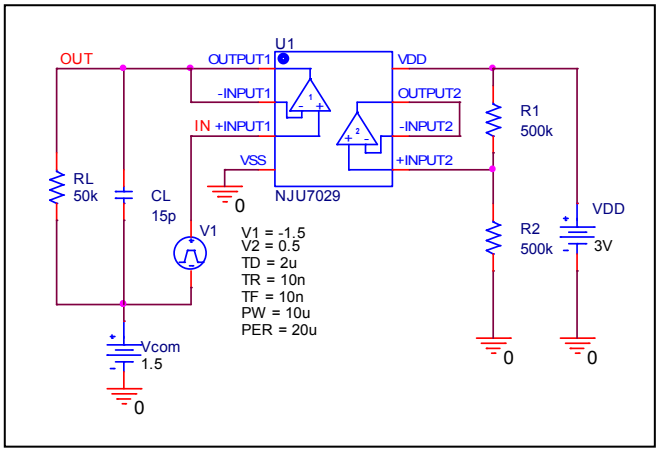
Parameter	Measurement	Simulation	%Error
I_b[pA]	**1.000**	**1.000**	**0**
I_{bos}[pA]	**1.000**	**1.000**	**0**

Slew Rate - SR

Simulation result



Evaluation circuit



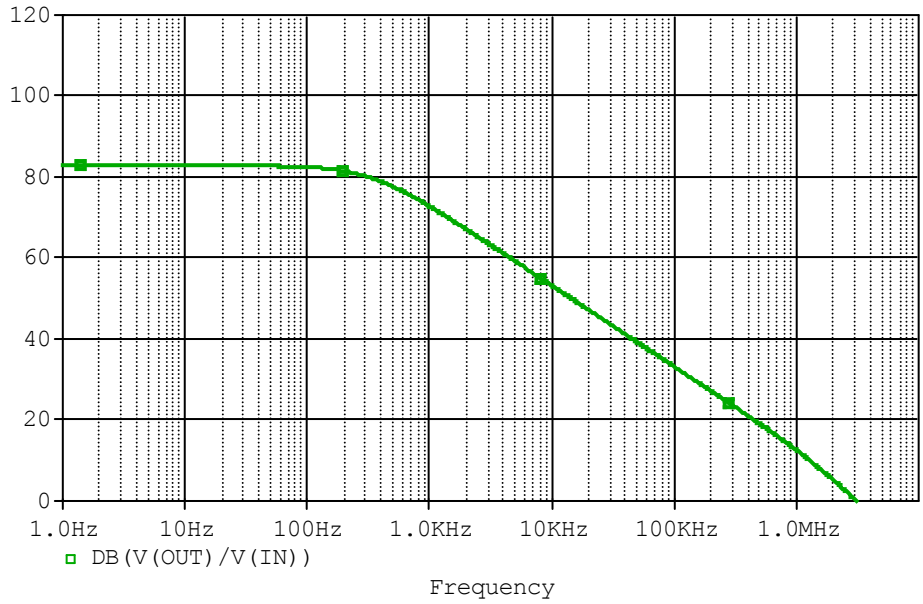
Comparison table

(Condition: GV=0dB, CL=15pF, RL=50kΩ to 1.5V)

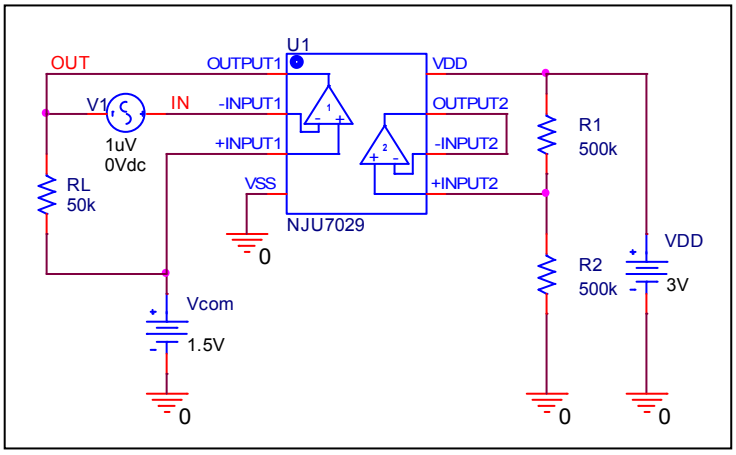
Parameter	Measurement	Simulation	%Error
SR[V/us]	1.000	0.992	0.8

Large Signal Voltage Gain - Av

Simulation result



Evaluation Circuit



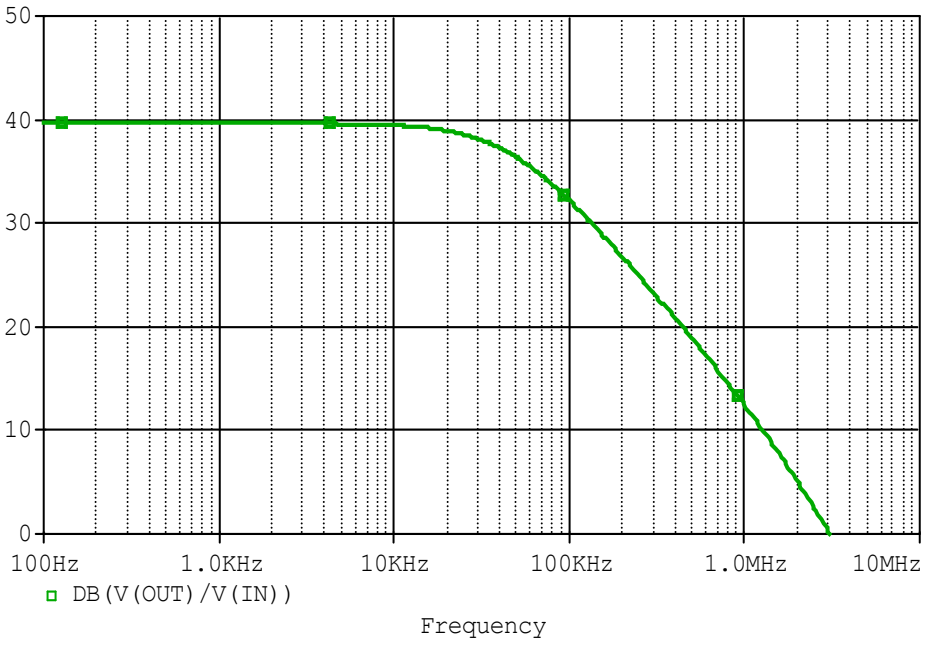
Comparison Table

(Condition: R_L=50kΩ to 1.5V, V_O=1.5V)

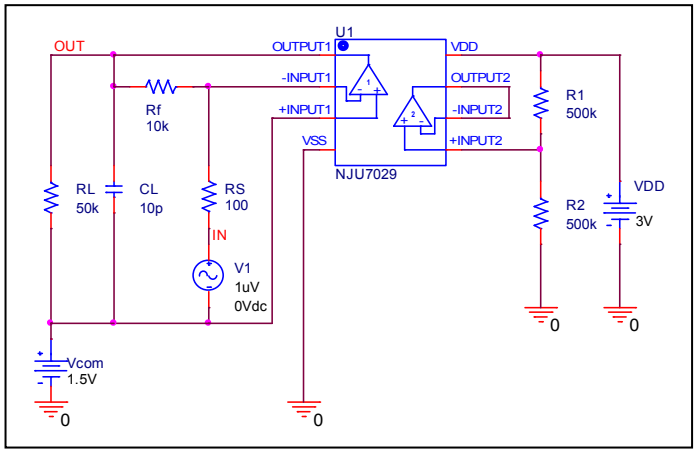
Parameter	Measurement	Simulation	%Error
Av[dB]	**80.000**	**82.846**	**3.56**

Unity Gain Frequency - f_T

Simulation result



Evaluation Circuit



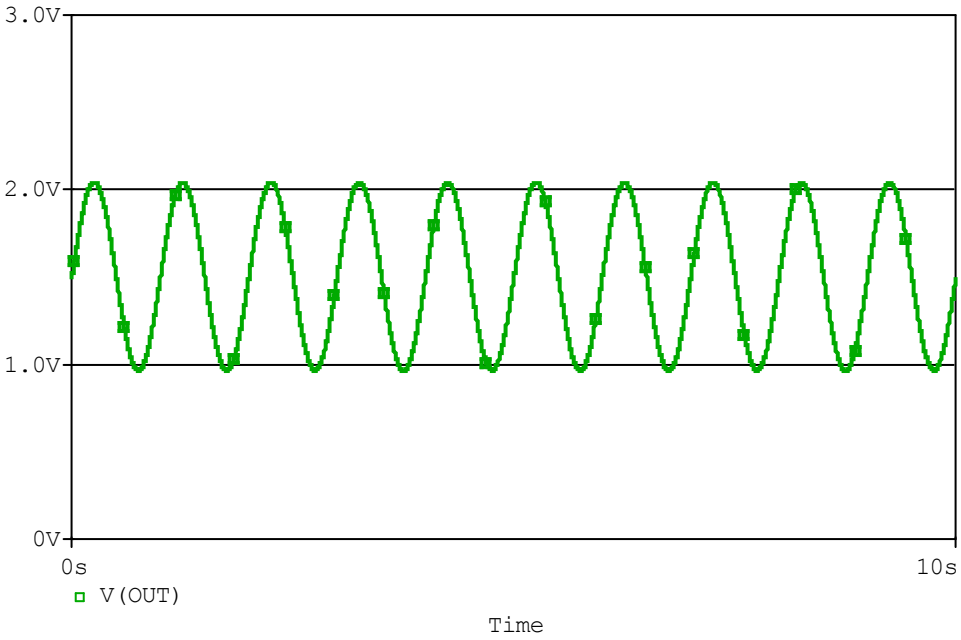
Comparison Table

(RL=50kΩ to 1.5V, C_L=10pF)

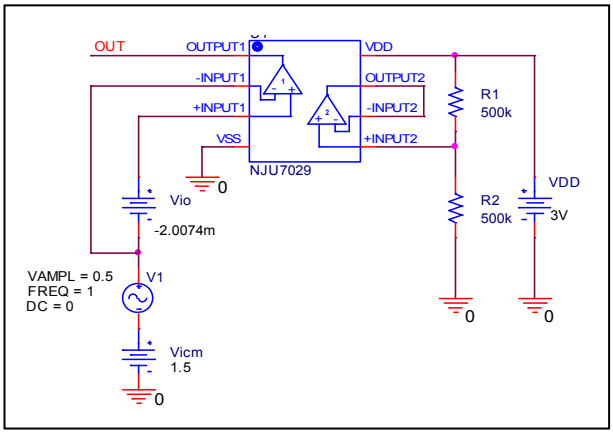
G_V=40[dB]	Measurement	Simulation	%Error
f_T [MHz]	3.000	3.086	2.87

Common Mode Rejection Ratio – CMR

Simulation result



Evaluation circuit



Comparison Table

(Condition: V_{icm}=0V~2.1V)

Parameter	Measurement	Simulation	%Error
CMR[dB]	80.000	82.214	-3.54

※ Common Mode Rejection Ratio =20*log(A_V/A_{VCM}) =20*log(13877/1.0755) =82.214dB