

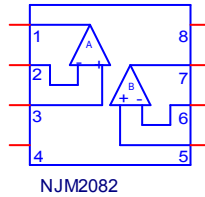
# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER  
PART NUMBER: NJM2082  
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

## SPice Model



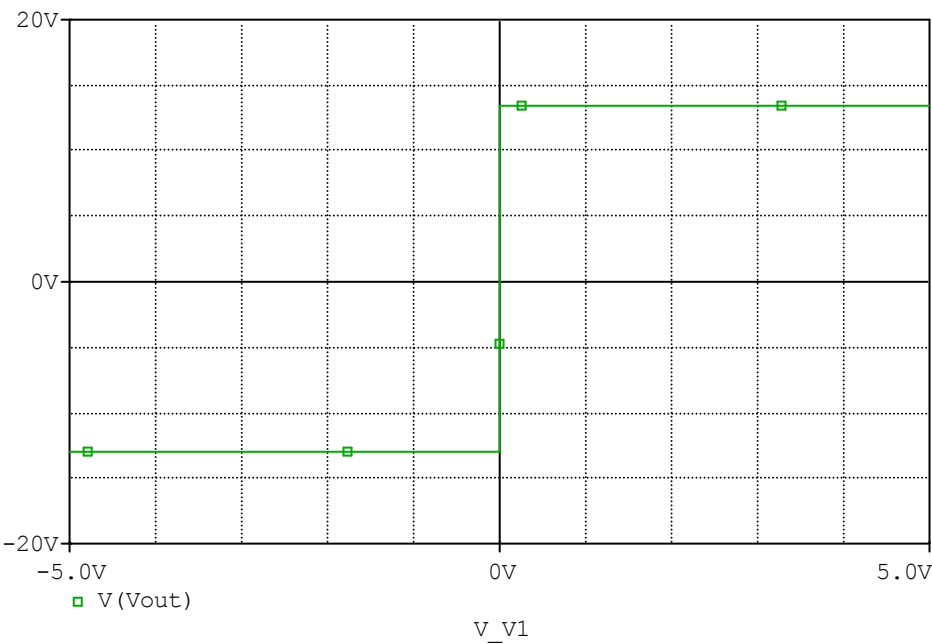
```

*$
* PART NUMBER: NJM2082
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.Subckt NJM2082 OUT1 -IN1 +IN1 V- +IN2 -IN2 OUT2 V+
X_U1  +IN1 -IN1 V+ V- OUT1 NJM2082_ME
X_U2  +IN2 -IN2 V+ V- OUT2 NJM2082_ME
.ends NJM2082
*$
.subckt NJM2082_ME 1 2 3 4 5
c1  11 12 8.6603E-12
c2  6 7 30.000E-12
css 10 99 1.0000E-30
dc  5 53 dy
de  54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp  4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb  7 99 poly(5) vb vc ve vlp vln 0 15.978E6 -1E3 1E3 16E6 -16E6
ga  6 0 11 12 791.68E-6
gcm 0 6 10 99 25.035E-9
iss 3 10 dc 600.00E-6
hlim 90 0 vlim 1K
j1  11 2 10 jx1
j2  12 1 10 jx2
r2  6 9 100.00E3
rd1 4 11 1.2631E3
rd2 4 12 1.2631E3
ro1 8 5 50
ro2 7 99 25
rp  3 4 1.8000E3
rss 10 99 333.33E3
vb  9 0 dc 0
vc  3 53 dc 2.2979
ve  54 4 dc 2.7979
vlim 7 8 dc 0
vlp 91 0 dc 20
vln 0 92 dc 20
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model jx1 PJF(Is=8.7500E-12 Beta=1.0446E-3 Vto=-.999)
.model jx2 PJF(Is=6.2500E-12 Beta=1.0446E-3 Vto=-1.001000)
.ends
*$

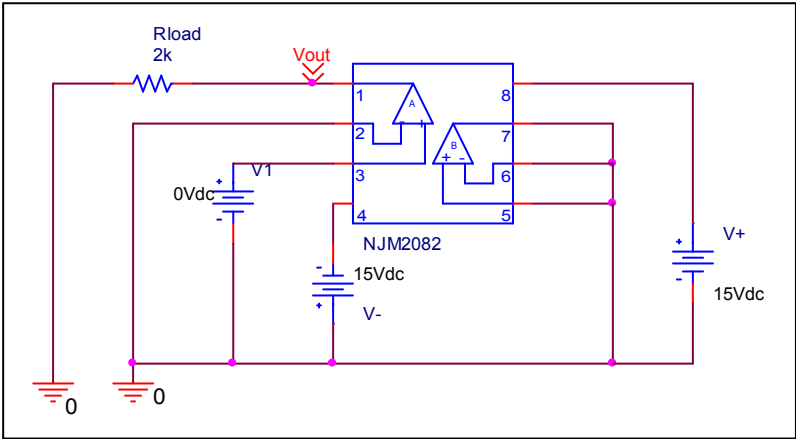
```

# Output Voltage Swing

## Simulation result



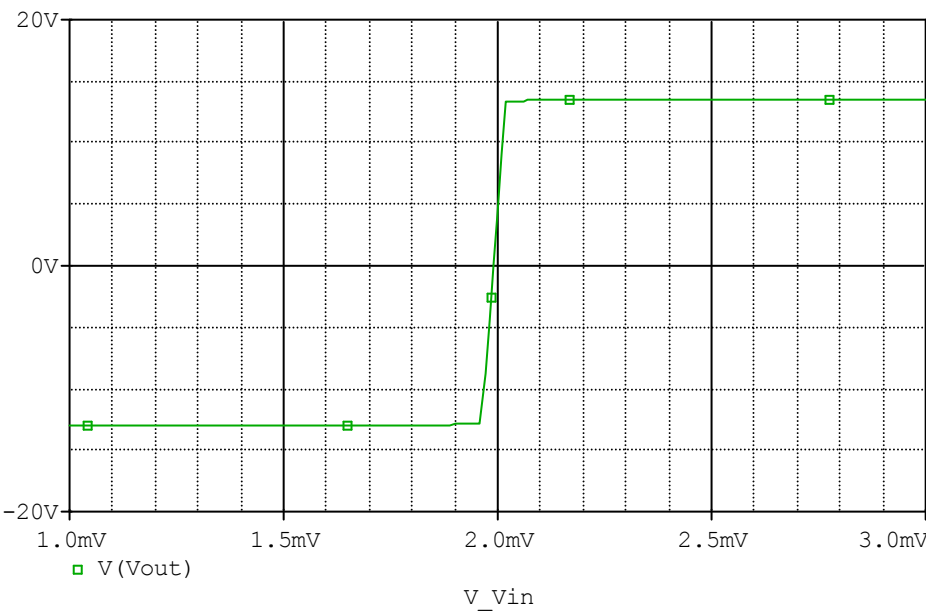
## Evaluation circuit



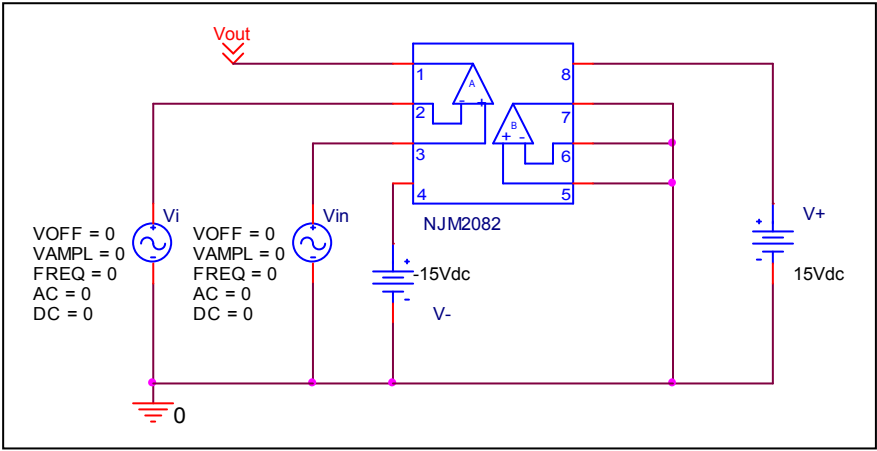
Output Voltage Swing	Measurement	Simulation	%Error
+ $V_{out}(V)$	+13.500	+13.491	-0.067
- $V_{out}(V)$	-13.000	-12.991	-0.069

# Input Offset Voltage

## Simulation result



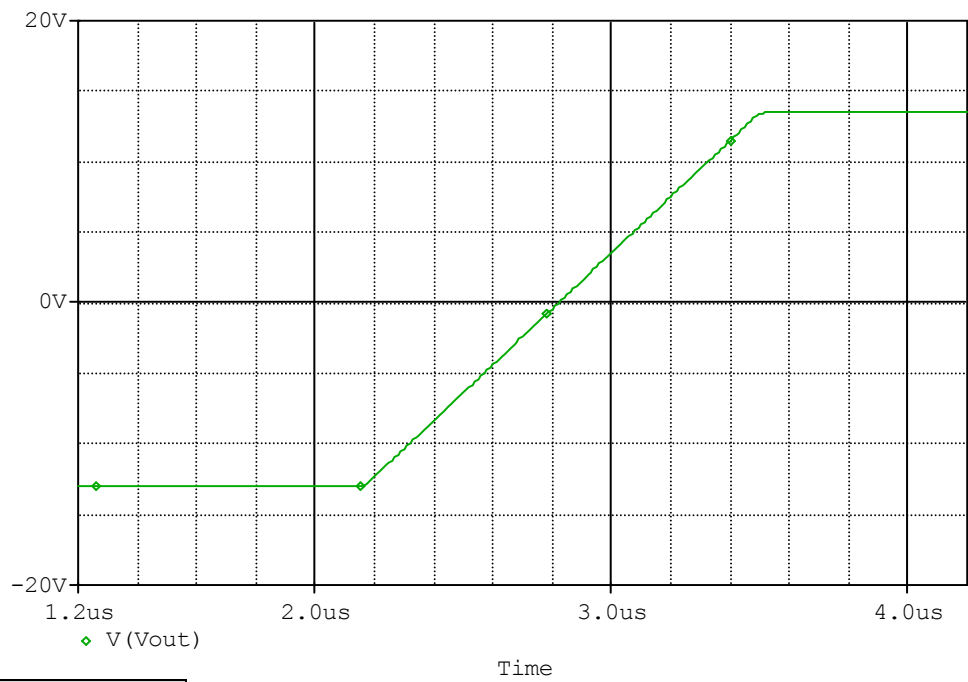
## Evaluation circuit



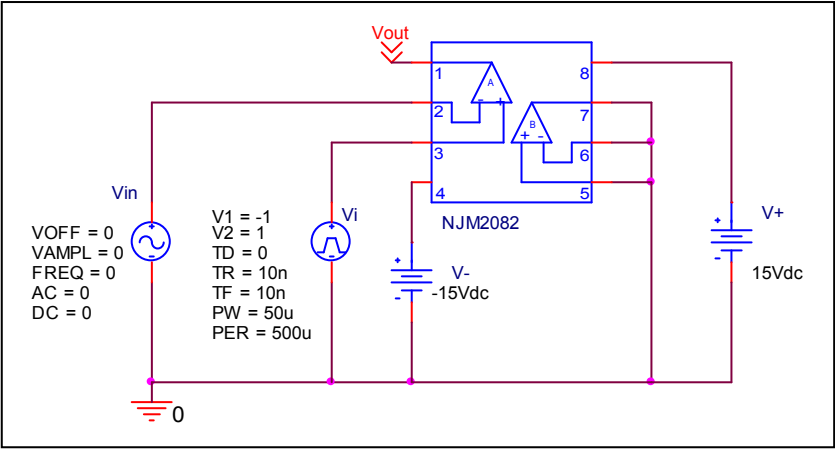
Vos	Measurement		Simulation		Error	
	2.000	mV	1.988	mV	-0.600	%

# Slew Rate

## Simulation result



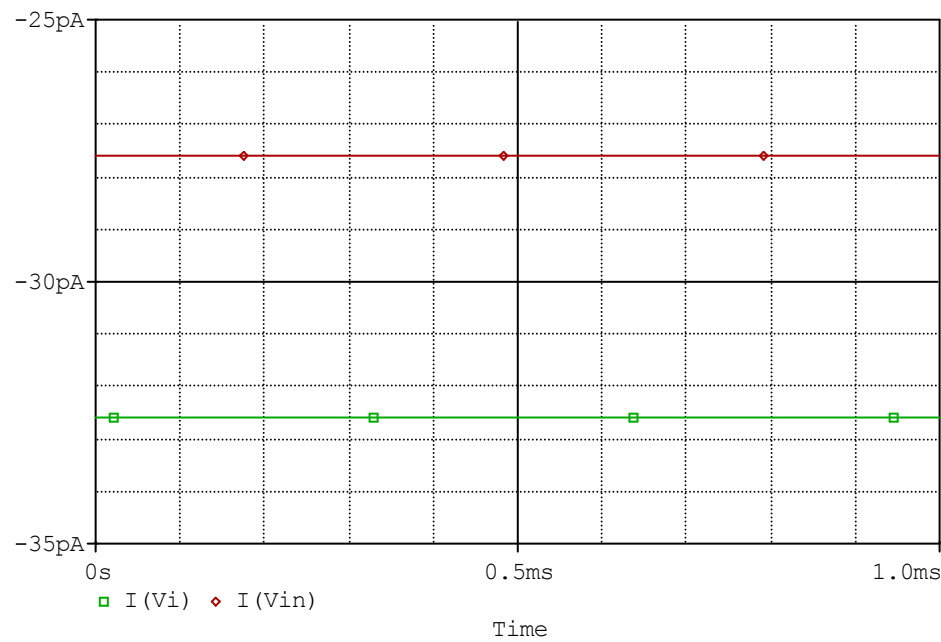
## Evaluation circuit



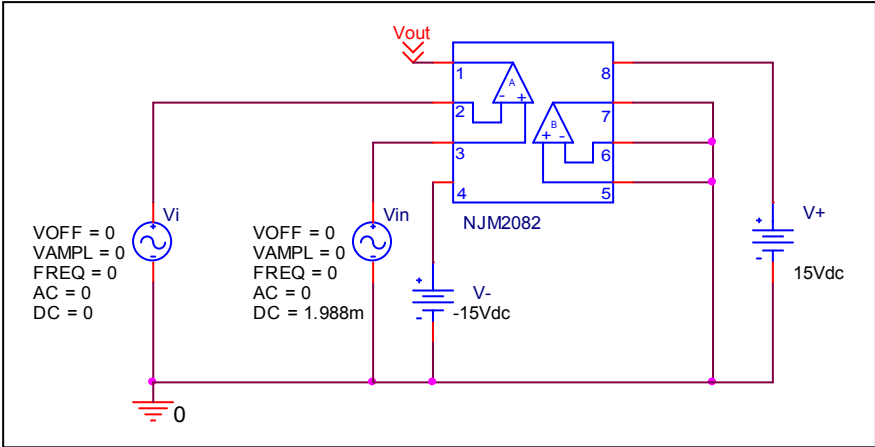
Slew Rate(v/us)	Measurement	Simulation	%Error
	20.000	19.916	-0.420

# Input current

## Simulation result



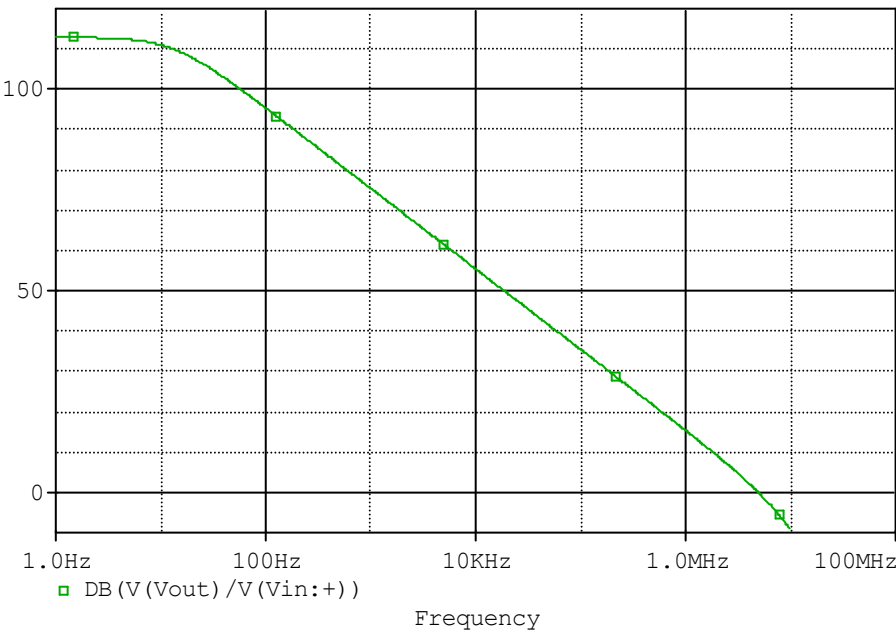
## Evaluation circuit



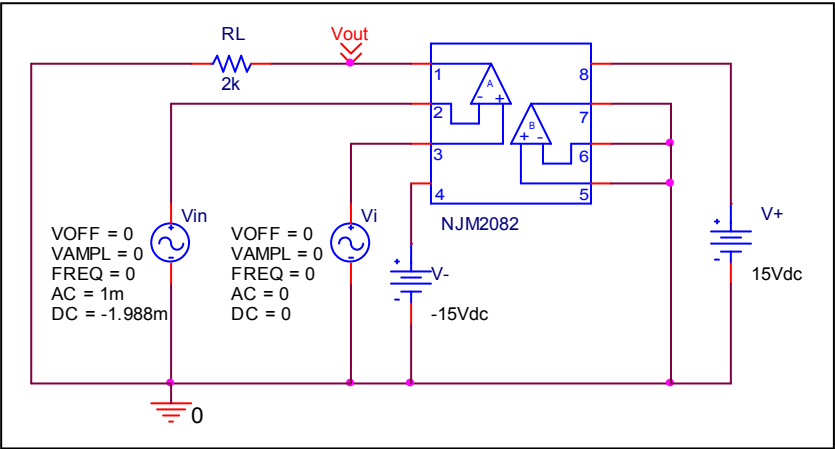
	Measurement	Simulation	%Error
Ib(pA)	30.000	30.000	0.000
Ibos(pA)	5.000	5.000	0.000

# Open Loop Voltage Gain vs. Frequency

## Simulation result



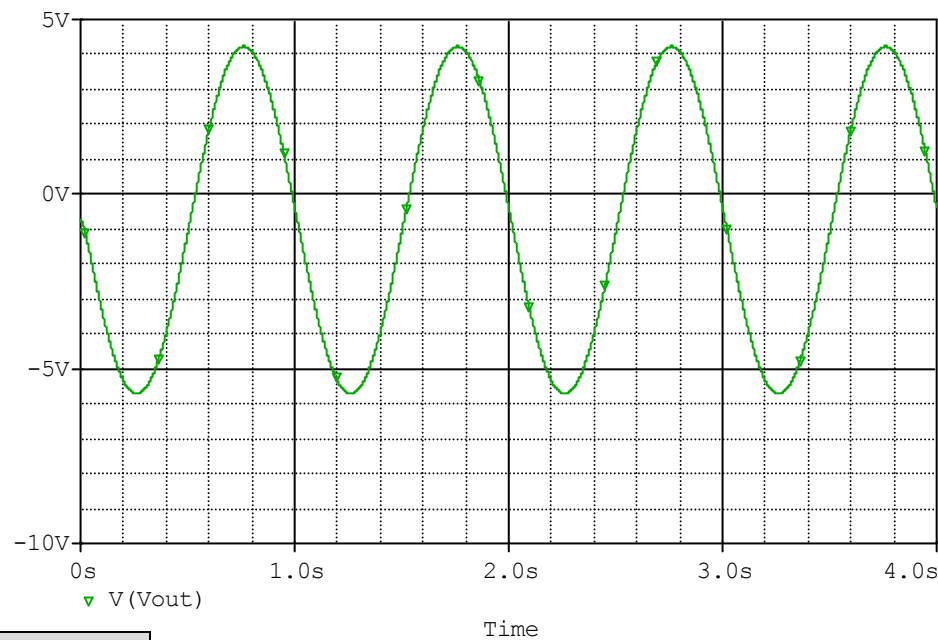
## Evaluation circuit



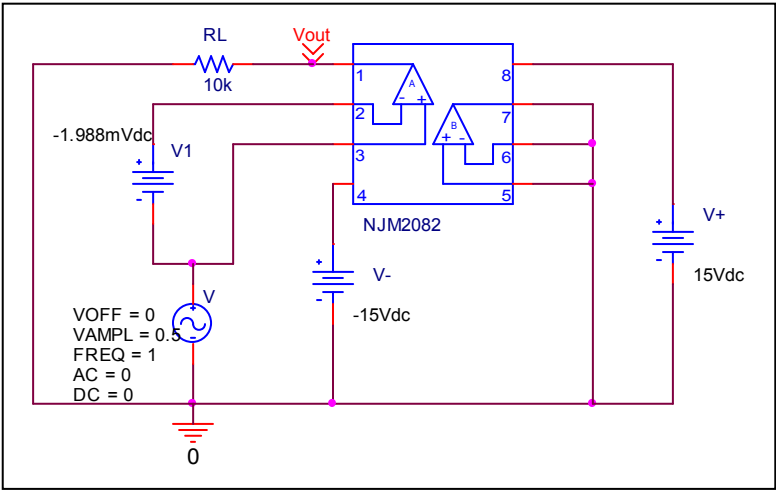
	Measurement	Simulation	%Error
<b>f-0dB(MHz)</b>	5.000	5.067	1.340
<b>Av-dc</b>	110.000	112.931	2.665

# Common-Mode Rejection Voltage gain

## Simulation result



## Evaluation circuit



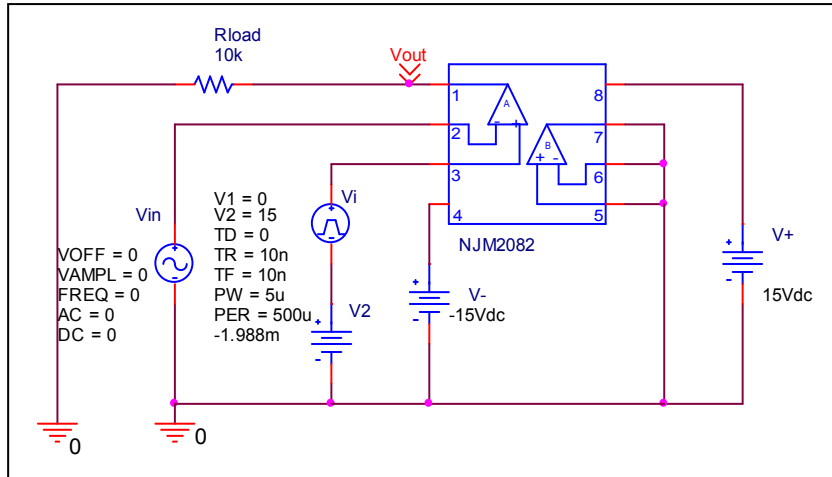
Common Mode Reject Ratio= $441570.447/9.945=44401.251$

CMRR	Measurement	Simulation	%Error
	90.000	92.947	3.274

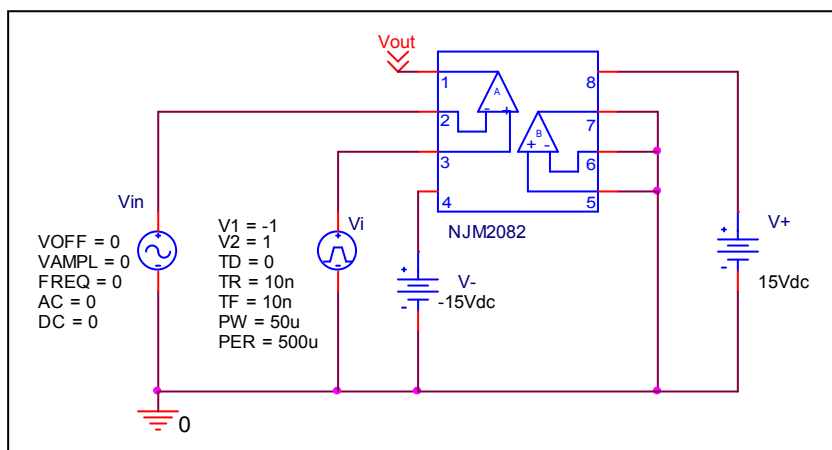


## Remark Slew Rate

### Before

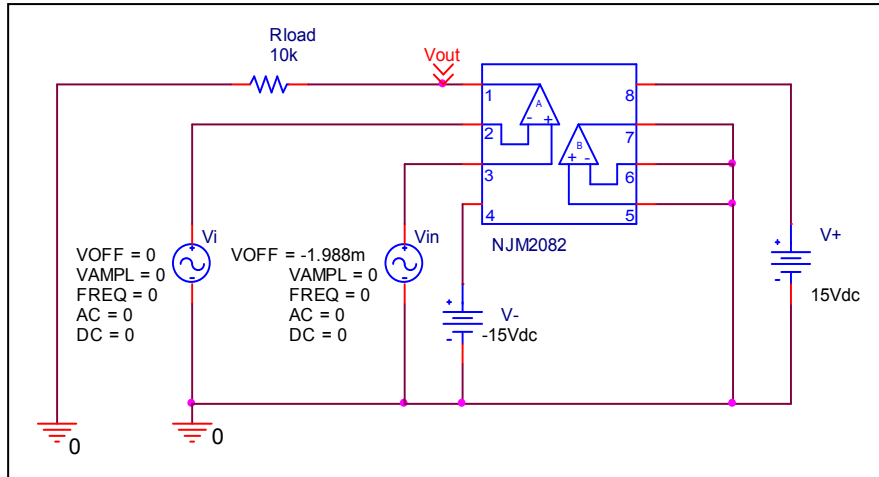


### After

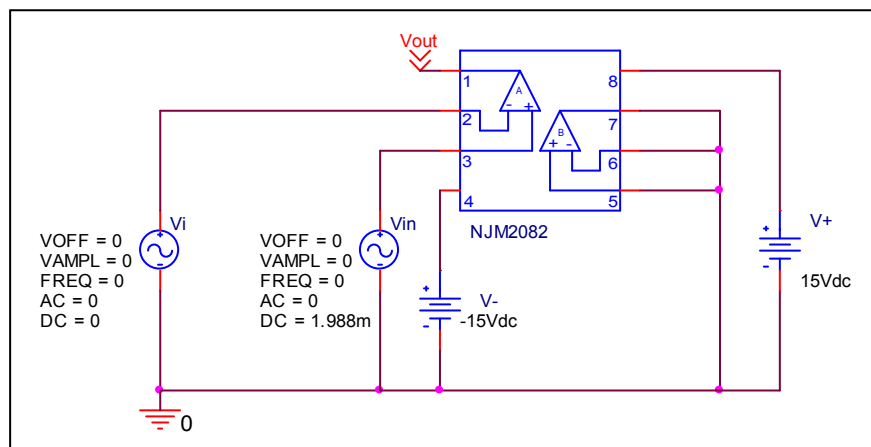


## Remark Input current

### Before

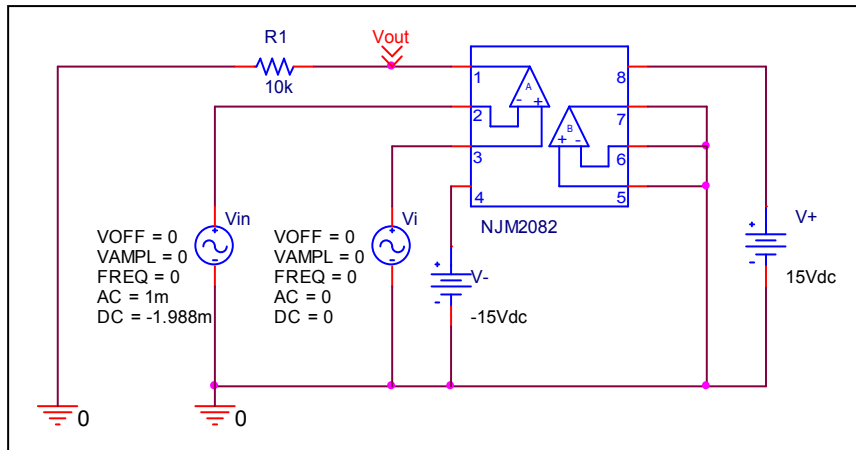


### After

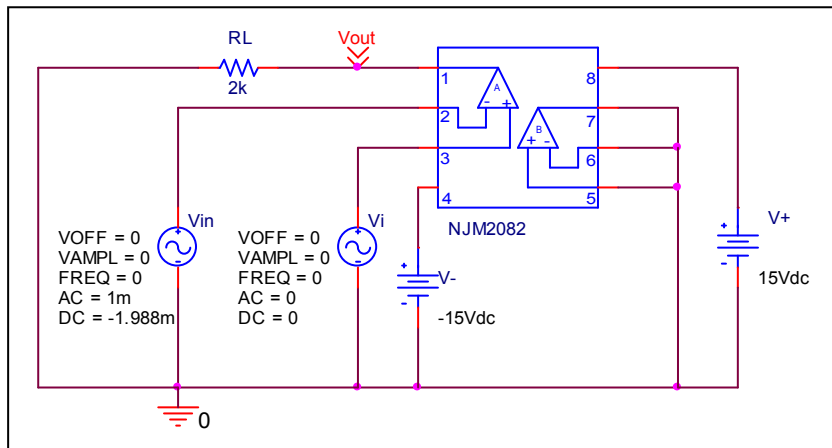


## Remark Open Loop Voltage Gain vs. Frequency

Before

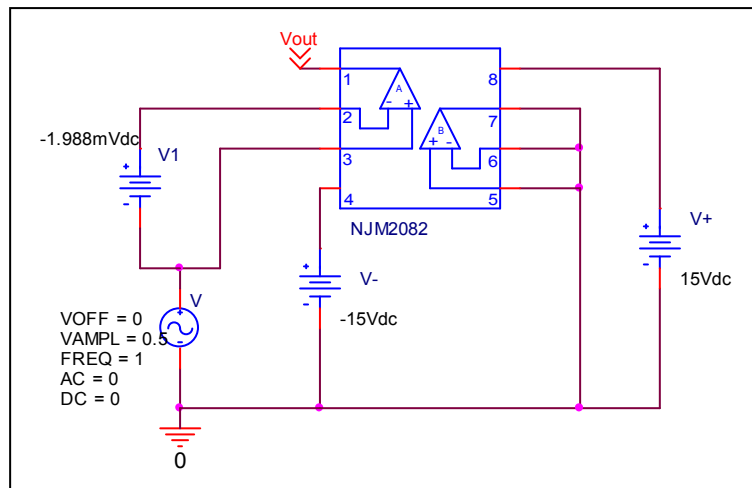


After



## Remark Common-Mode Rejection Voltage gain

Before



After

