

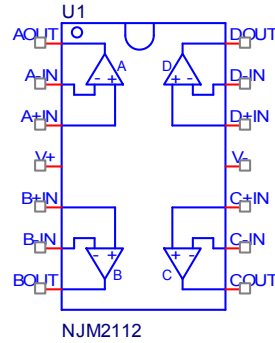
# Device Modeling Report

COMPONENTS: OPERATIONAL AMPLIFIER  
PART NUMBER: NJM2112  
MANUFACTURER: NEW JAPAN RADIO CO., LTD



Bee Technologies Inc.

## Spice Model



```

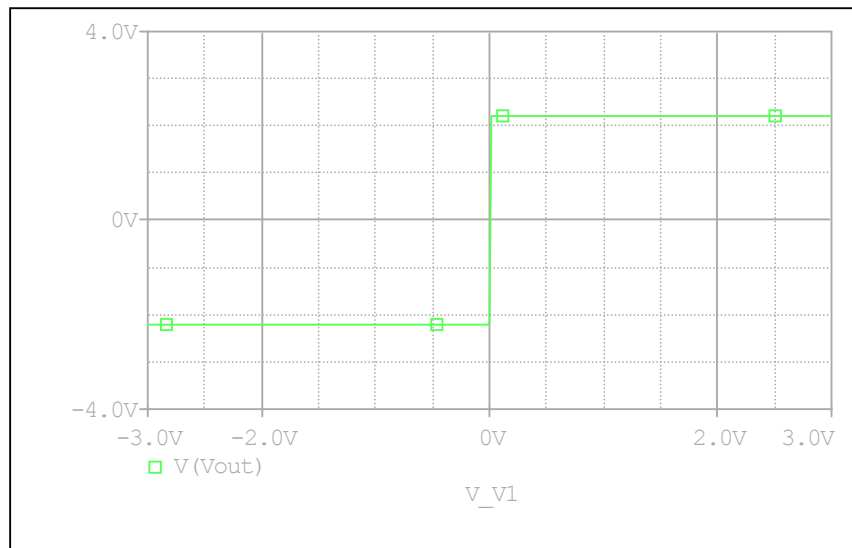
*$
* PART NUMBER:NJM2112
* MANUFACTURER: NEW JAPAN RADIO
* All Rights Reserved Copyright (c) Bee Technologies Inc. 2007
.SUBCKT NJM2112 OUT1 -IN1 +IN1 V+ +IN2 -IN2 OUT2 OUT3 -IN3 +IN3 V-
+ +IN4 -IN4 OUT4
X_U1  +IN1 -IN1 V+ V- OUT1 NJM2112_S
X_U2  +IN2 -IN2 V+ V- OUT2 NJM2112_S
X_U3  +IN3 -IN3 V+ V- OUT3 NJM2112_S
X_U4  +IN4 -IN4 V+ V- OUT4 NJM2112_S
.ENDS NJM2112
.SUBCKT NJM2112_S 1 2 3 4 5
c1 11 12 8.6603E-12
c2 6 7 29.500E-12
cee 10 99 1.0000E-30
dc 5 53 dy
de 54 5 dy
dlp 90 91 dx
dln 92 90 dx
dp 4 3 dx
egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
fb 7 99 poly(5) vb vc ve vlp vln 0 187.00E3 -1E3 1E3 190E3 -190E3
ga 6 0 11 12 2.4968E-3
gcm 0 6 10 99 431.78E-9
iee 3 10 dc 99.202E-6
hlim 90 0 vlim 1K
q1 11 2 13 qx1
q2 12 1 14 qx2
r2 6 9 100.00E3
rc1 4 11 400.52
rc2 4 12 400.52
re1 13 10 1
re2 14 10 1
ree 10 99 2.0161E6
ro1 8 5 50
ro2 7 99 25
rp 3 4 125.31
vb 9 0 dc 0
vc 3 53 dc 1.0309

```

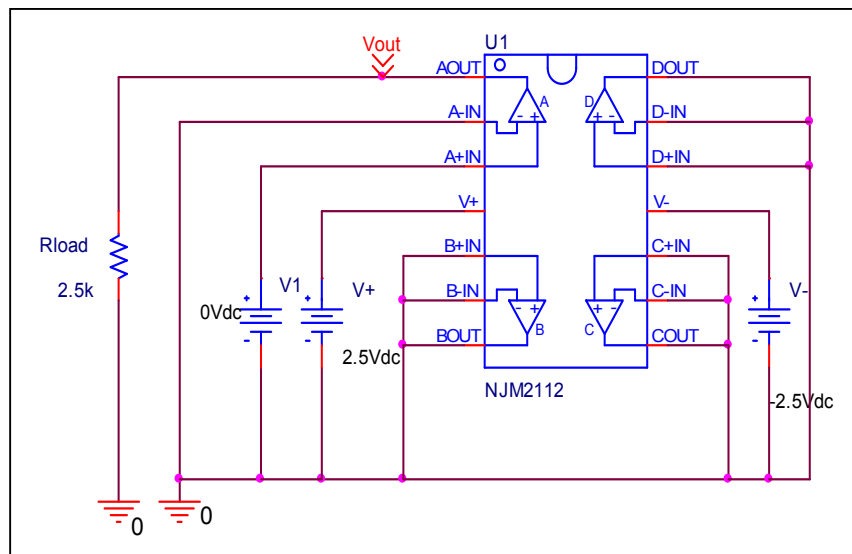
```
ve 54 4 dc 1.0309
vlim 7 8 dc 0
vlp 91 0 dc 1.5000
vln 0 92 dc 1.5000
.model dx D(Is=800.00E-18)
.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)
.model qx1 PNP(Is=800.00E-18 Bf=463.27)
.model qx2 PNP(Is=828.3277E-18 Bf=520.23)
.ends
*$
```

## Output Voltage Swing

### Simulation result



### Evaluation circuit

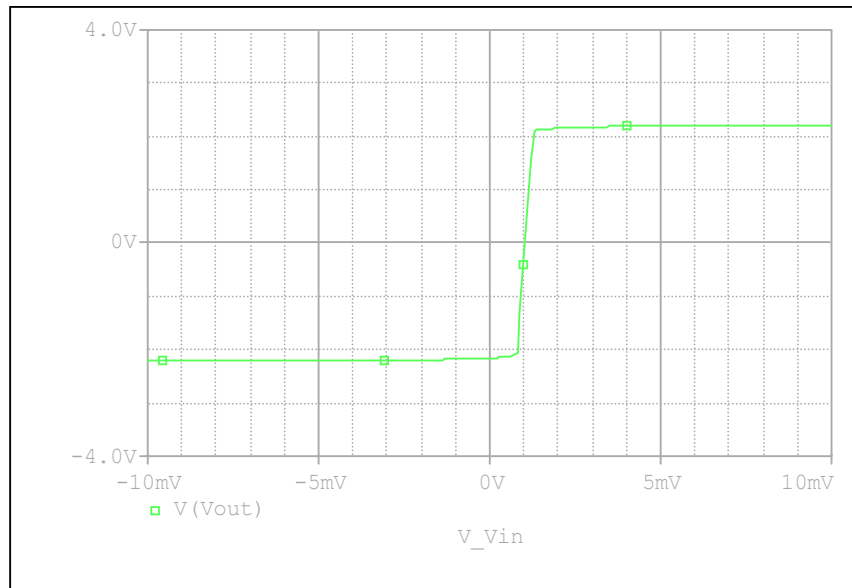


### Comparison table

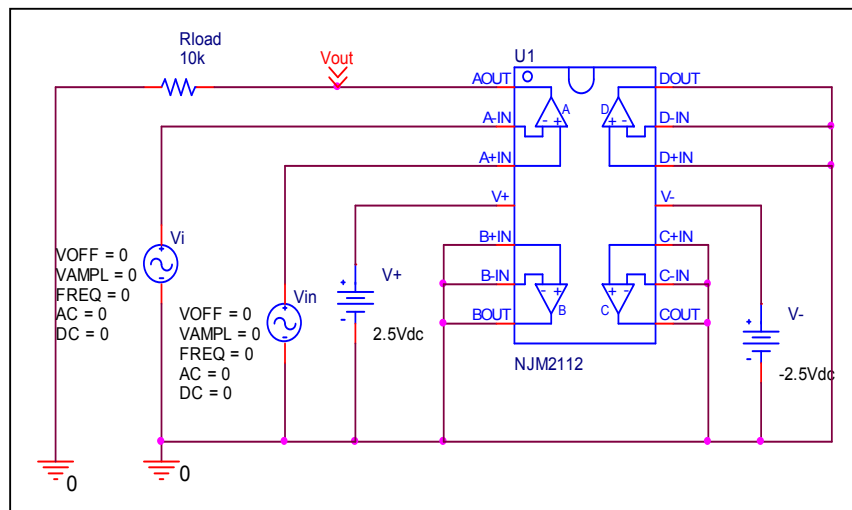
Output Voltage Swing	Measurement	Simulation	%Error
V+	+2.2	+2.1959	-0.186
V-	-2.2	-2.1959	-0.186

## Input Offset Voltage

### Simulation result



### Evaluation circuit

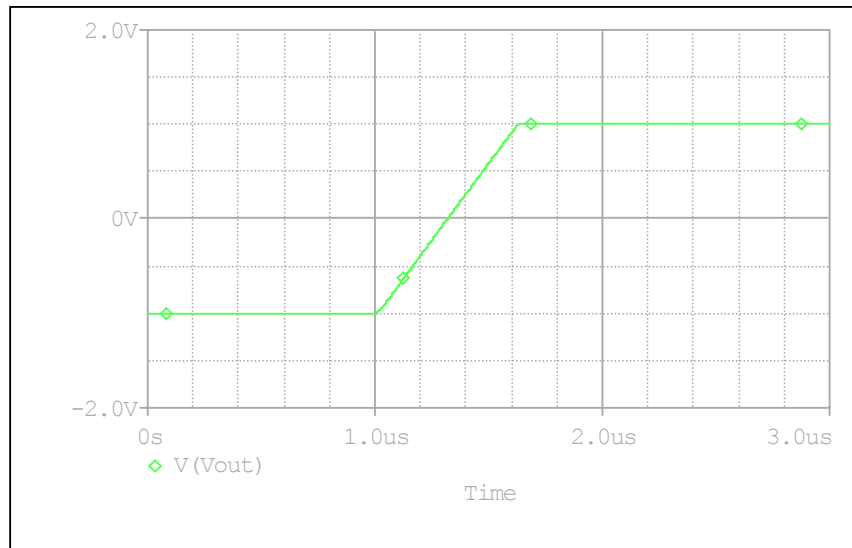


### Comparison table

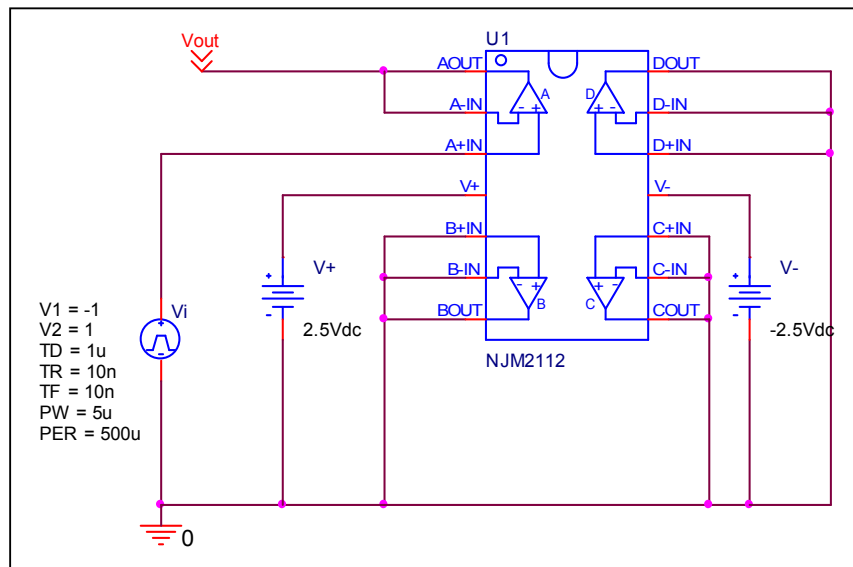
	Measurement	Simulation	%Error
<b>Vos (mV)</b>	1	1.0458	4.58

## Slew Rate

### Simulation result



### Evaluation circuit

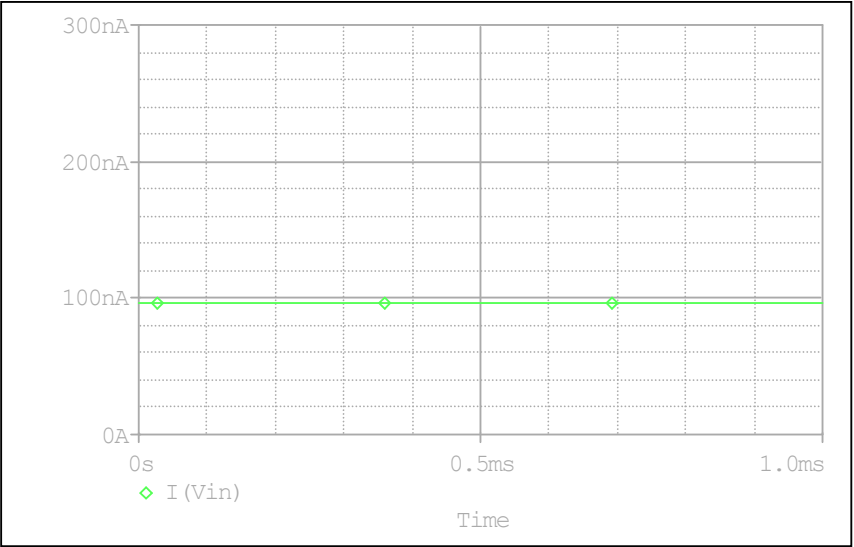


### Comparison table

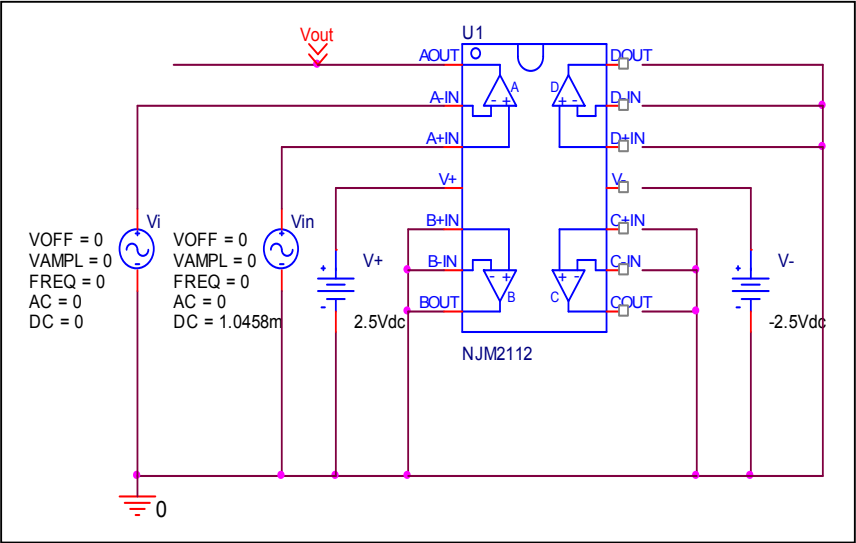
	Measurement	Simulation	%Error
<b>Slew Rate(v/us)</b>	3.2	3.286	2.688

Input current

Simulation result



Evaluation circuit

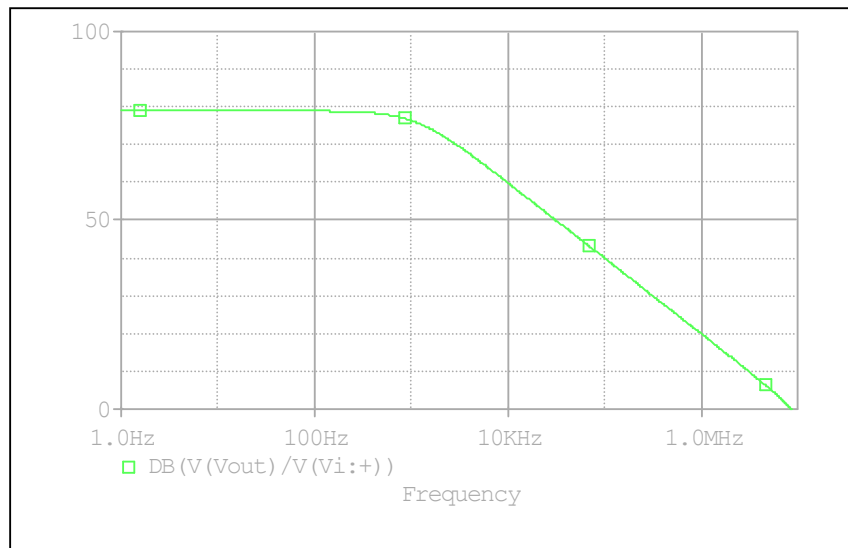


Comparison table

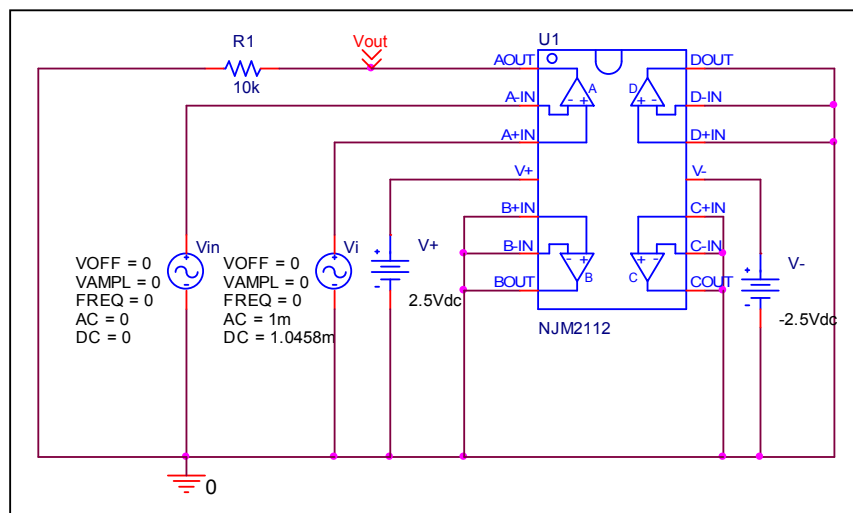
	Measurement	Simulation	%Error
Ib(nA)	100	96.489	-3.511

## Open Loop Voltage Gain vs. Frequency

### Simulation result



### Evaluation circuit



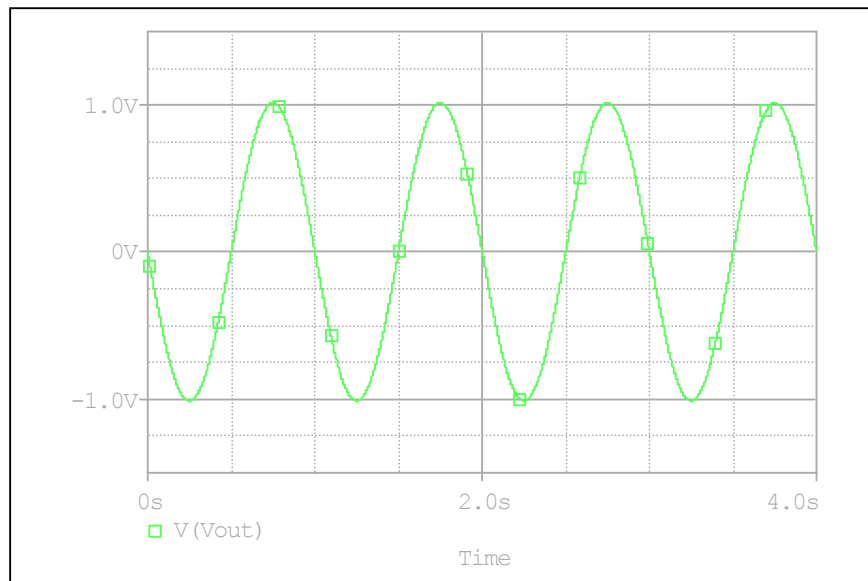
### Comparison table

	Measurement	Simulation	%Error
<b>f-0dB(MHz)</b>	9	8.6837	-3.514
<b>Av-dc</b>	80	78.924	-1.345

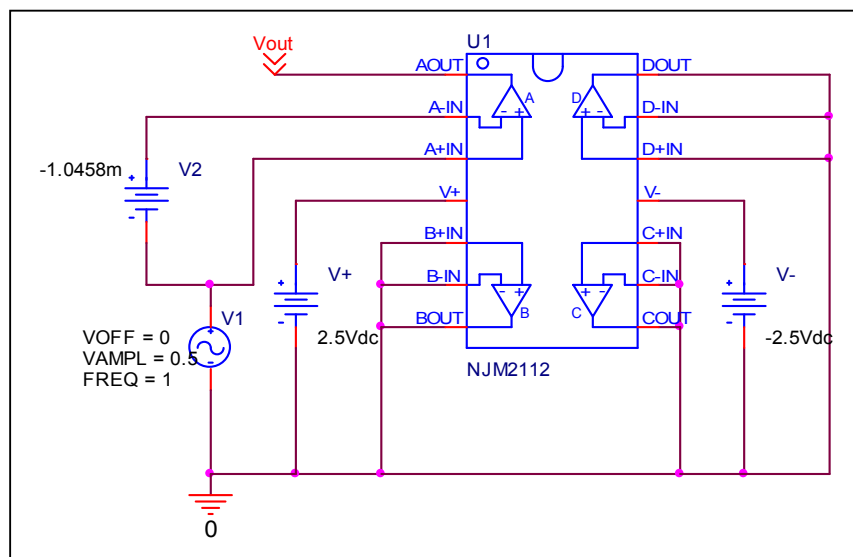


### Common-Mode Rejection Voltage gain

### Simulation result



## Evaluation circuit



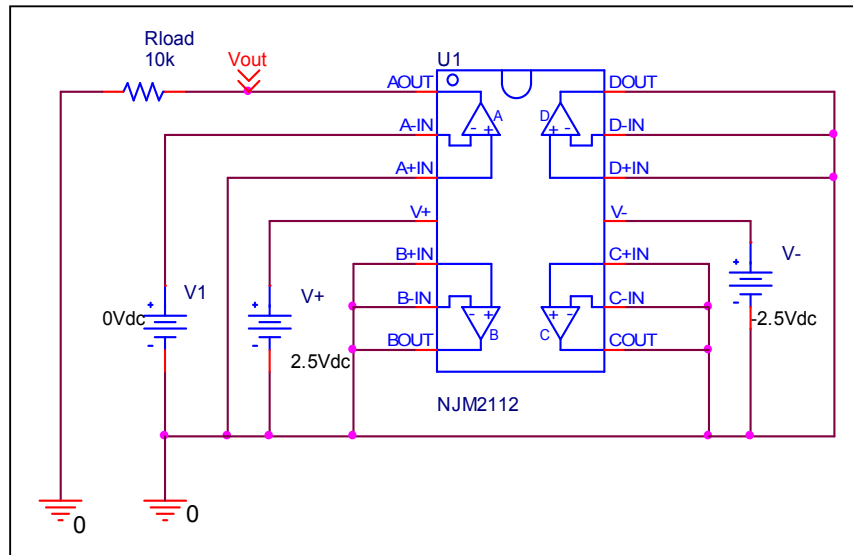
$$\text{CMRR} = 20 \cdot \text{LOG}(8834.867/2.0248) = 72.796 \text{ dB}$$

## Comparison table

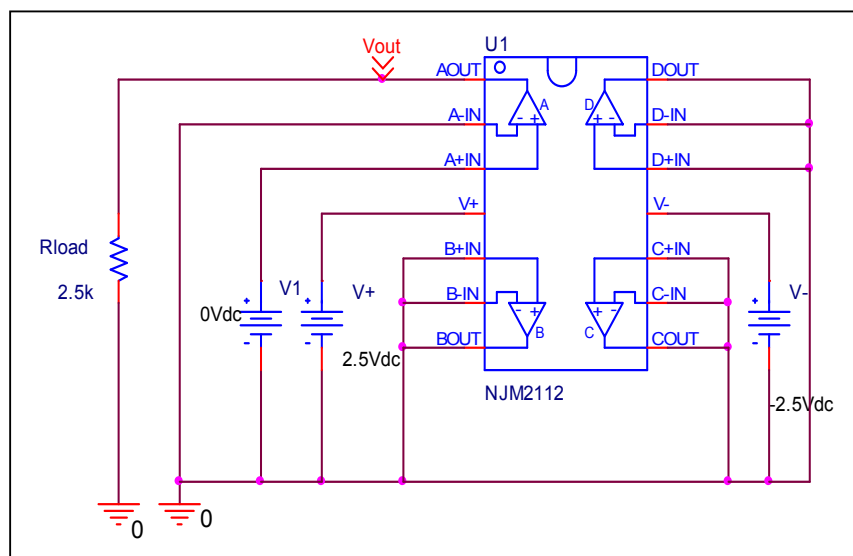
	Measurement	Simulation	%Error
CMRR(dB)	74	72.796	-1.627

## Remark Output Voltage Swing

Before

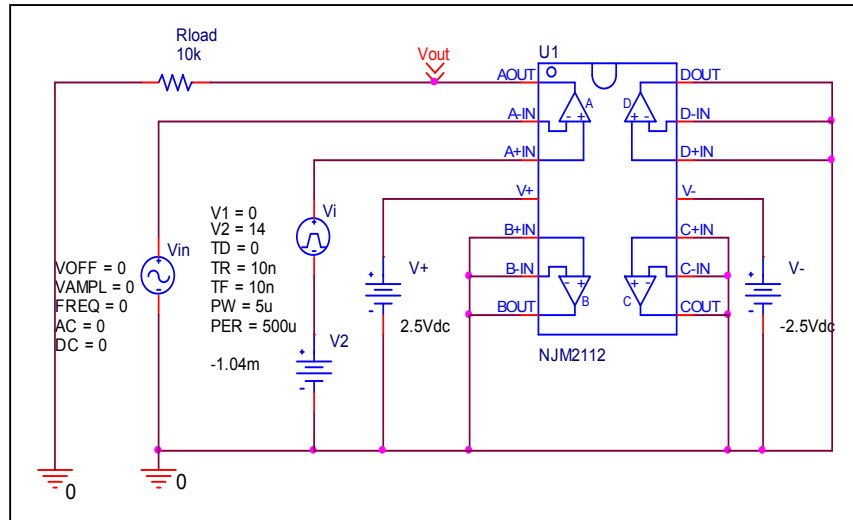


After

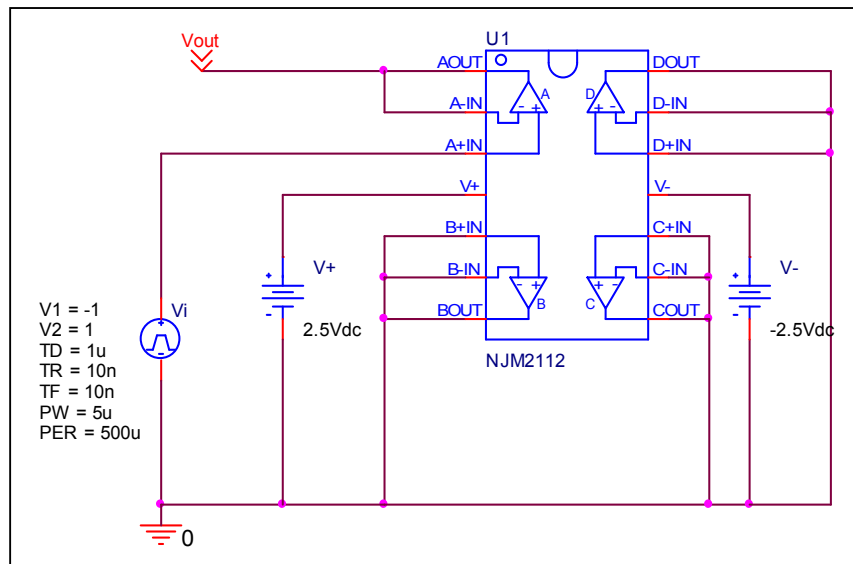


## Remark Slew Rate

Before

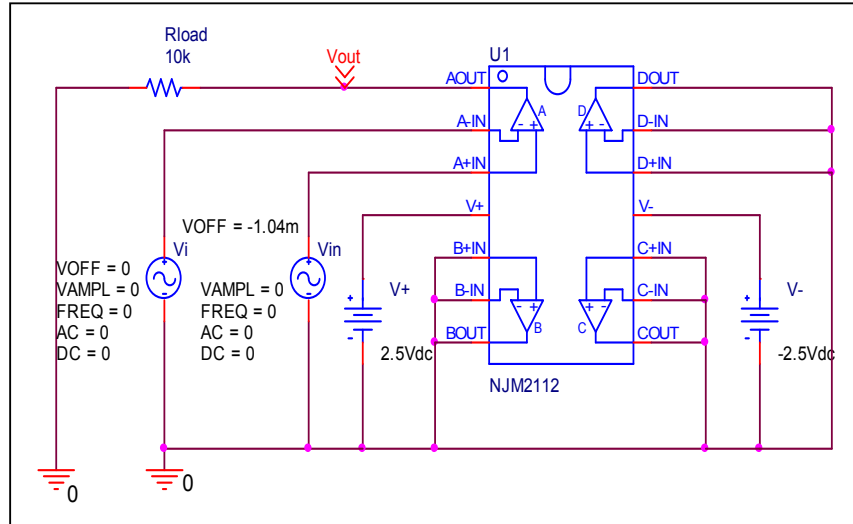


After

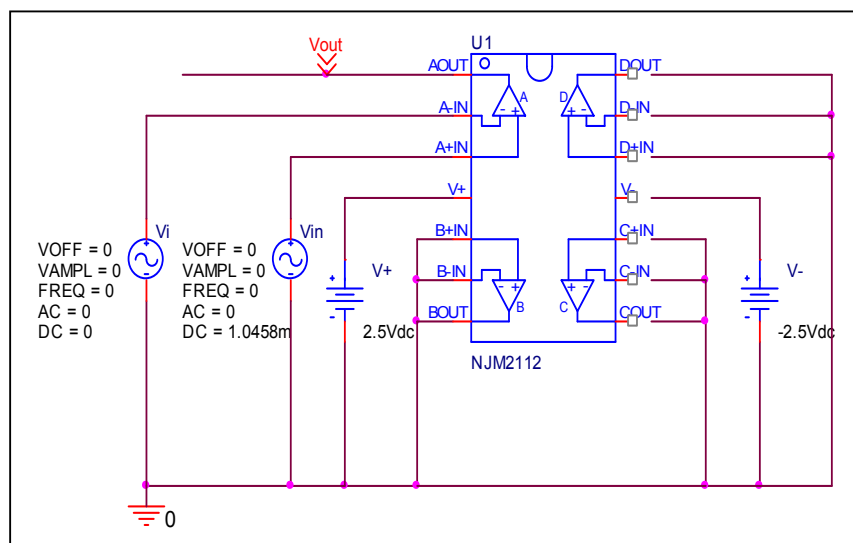


## Remark Input current

Before

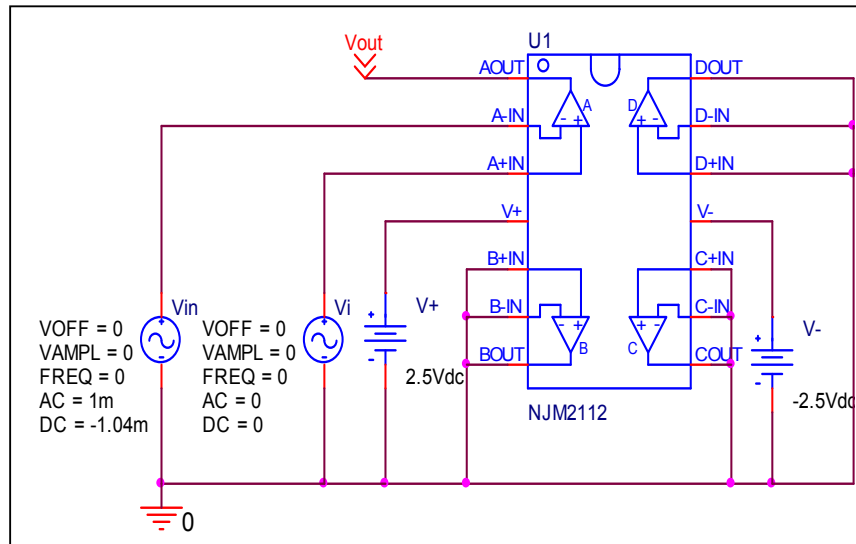


After

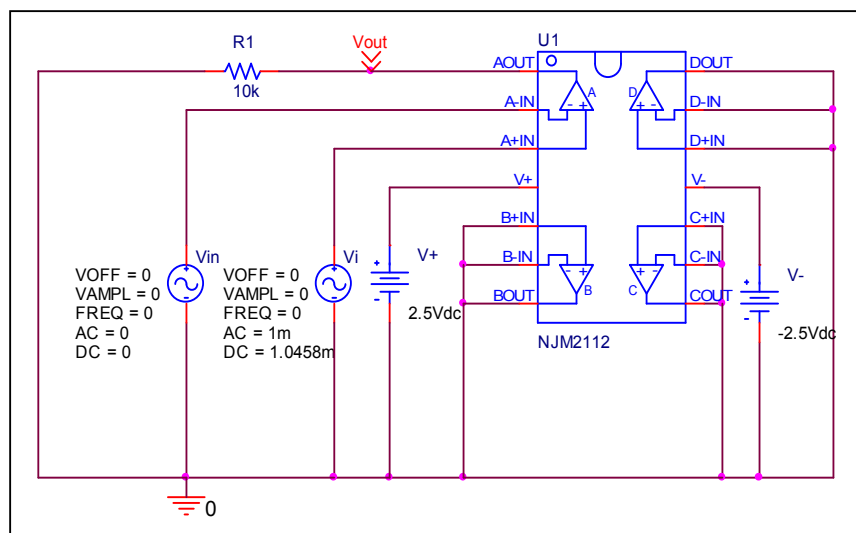


## Remark Open Loop Voltage Gain vs. Frequency

Before

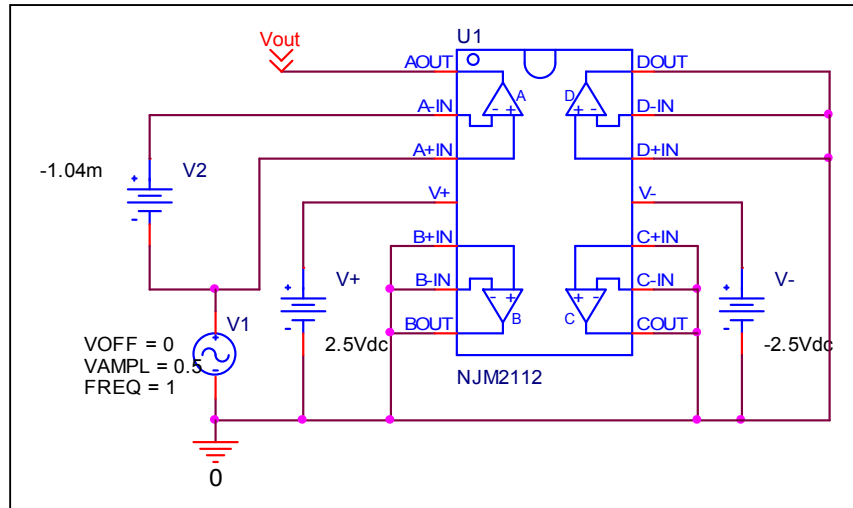


After



## Remark Common-Mode Rejection Voltage gain

Before



After

