AN11145

CLRC663, MFRC630, MFRC631, SLRC610 PC-Serial RS232 and low power card detection Quick Start Guide

Rev. 1.1 — 17 July 2012
223711

Application note
COMPANY PUBLIC

Document information

Info	Content
Keywords	CLRC663, MFRC630, MFRC631 and SLRC610, RedBoard quick start guide
Abstract	The document provides information on powering the evaluation board and executing scripts with the CLRC663, MFRC630, MFRC631 and SLRC610 test program.

Revision history

Rev	Date	Description
1.1	20120717	CLRC663 Derivates added
1.0	20111212	Initial version

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1. Introduction

The “CLRC663 Serial Test Program” is provided as an executable application with a graphical user interface. In principal it is build on very low level – just offering read and write register operations. It can also be operated with MFRC630, MFRC631 and SLRC610. To improve readability, in the subsequent text the whole product family is referenced as “CLRC663 family”.

The software can be used to communicate with CLRC663 family on register level. By the use of script files, single register operations are executed to configure the IC for a certain operating mode. The script files have the extension ***.jcf***.

Note that the CLRC663 family Serial Test Program is intended to show the chip functionality only on a very basic level.

In the following steps the PC serial and the LPCD is described by using the CLRC663 red board.

For MFRC630, MFRC631 and SLRC610 the protocol settings have to be set with load protocol, because the registers are locked.

Obviously not all scripts are useful on every derivate, e.g. the ISO 15693 inventory script will not find any tags in case the ISO 14443-only derivate chip MFRC631 is used.

Important: Read the LPCD section to correctly operate the low power card detection mode.

The following script files are provided:

- **RC663_ISO14443A_4byteUID.jcf** - returns the UID of an ISO14443-3A card. Only 4byte UIDs are retrieved for this script.

  →CLRC663, MFRC631 and MFRC630
- **RC663_ISO14443B_ReqB.jcf** - returns the UID of an ISO14443-3B card

  →CLRC663 and MFRC631
- **RC663_ISO15693_Inventory.jcf** - performs an ISO15693 Inventory command
- →CLRC663 and SLRC610
- **RC663_Felica_ReqC.jcf** - act as passive PICC Target

  →CLRC663
- **LPCD_ModeConfig_Part1.jcf** - configures the board to LPCD
- **LPCD_DetectPICC_Part2.jcf** – runs LPCD mode with prior defined settings

1.1 Getting Started

Please connect the CLRC663 RedBoard to the RS232 interface and power it up using the enclosed switched power supply.

The input voltage must be 7.5 Volts (or higher).

The polarity of the connector plug of power supply is not relevant.

The Baudrate must be set to 115200.

1. Start the *CLRC663 Serial RS232 Test Progra*m by clicking on the executable file. It is a standalone program, no further installation is required. An empty window opens as outlined in Fig 1:

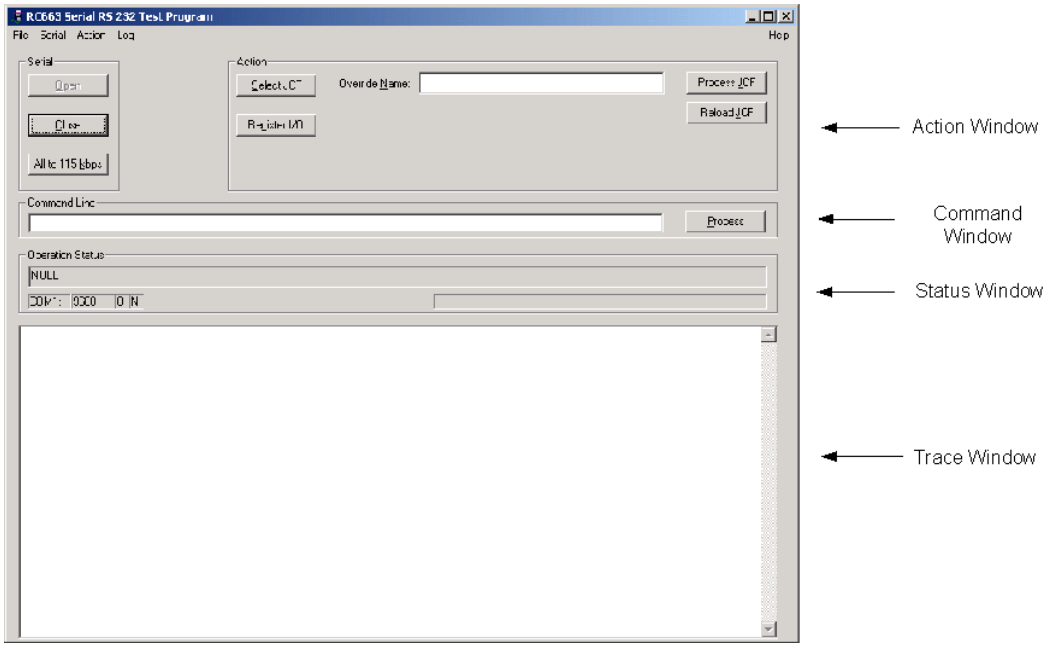

Fig 1. Main window of RC663 Serial

The *CLRC663 Serial RS232 Test Program* is a simple User Interface (UI) utility for register-based access to the RC663 hardware using the serial interface.

2. The RS232 COM port has to be configured: **Port/Settings…**

Choose the appropriate RS232 COM port for your serial communication, **Verify** (checks if the port is used or not) your selection and press **Apply**.

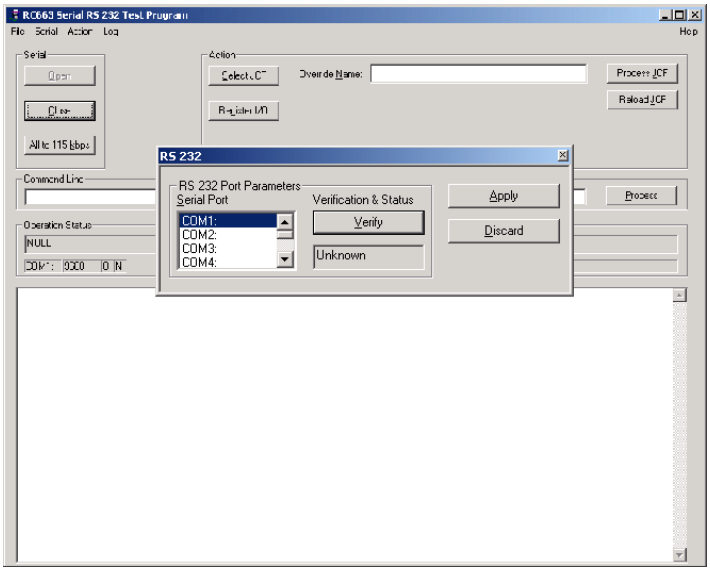

Fig 2. Com Port Selection

3. Use the **Open** button to establish the communication channel. An indicator of correct settings is the changing of all buttons but Open from inactive to active state.
4. By pressing **Select JCF** a window with all delivered scripts is opened. For this first try, please choose the file "**RC663_ISO14443A_4byteUID**".

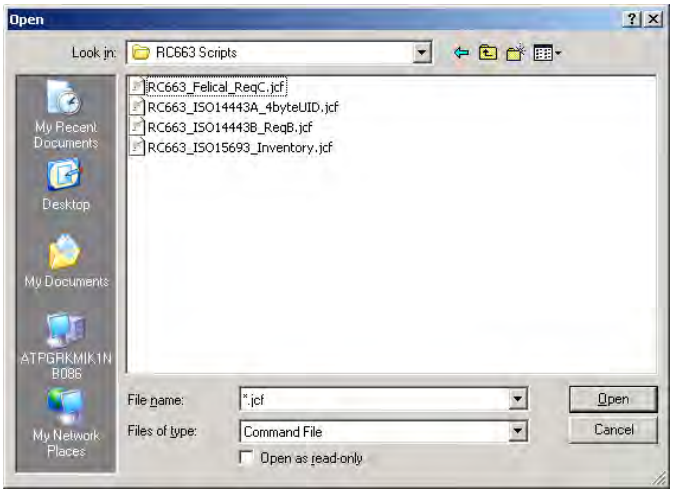

Fig 3. Select JCF file

It might be useful while investigating the different modes to open the files in a text editor, too, due to inline documentation which will not be displayed in the trace window.

5. Put a MIFARE Classic 1k on the Demo-Board and start the communication by using the **Process JCF** button.

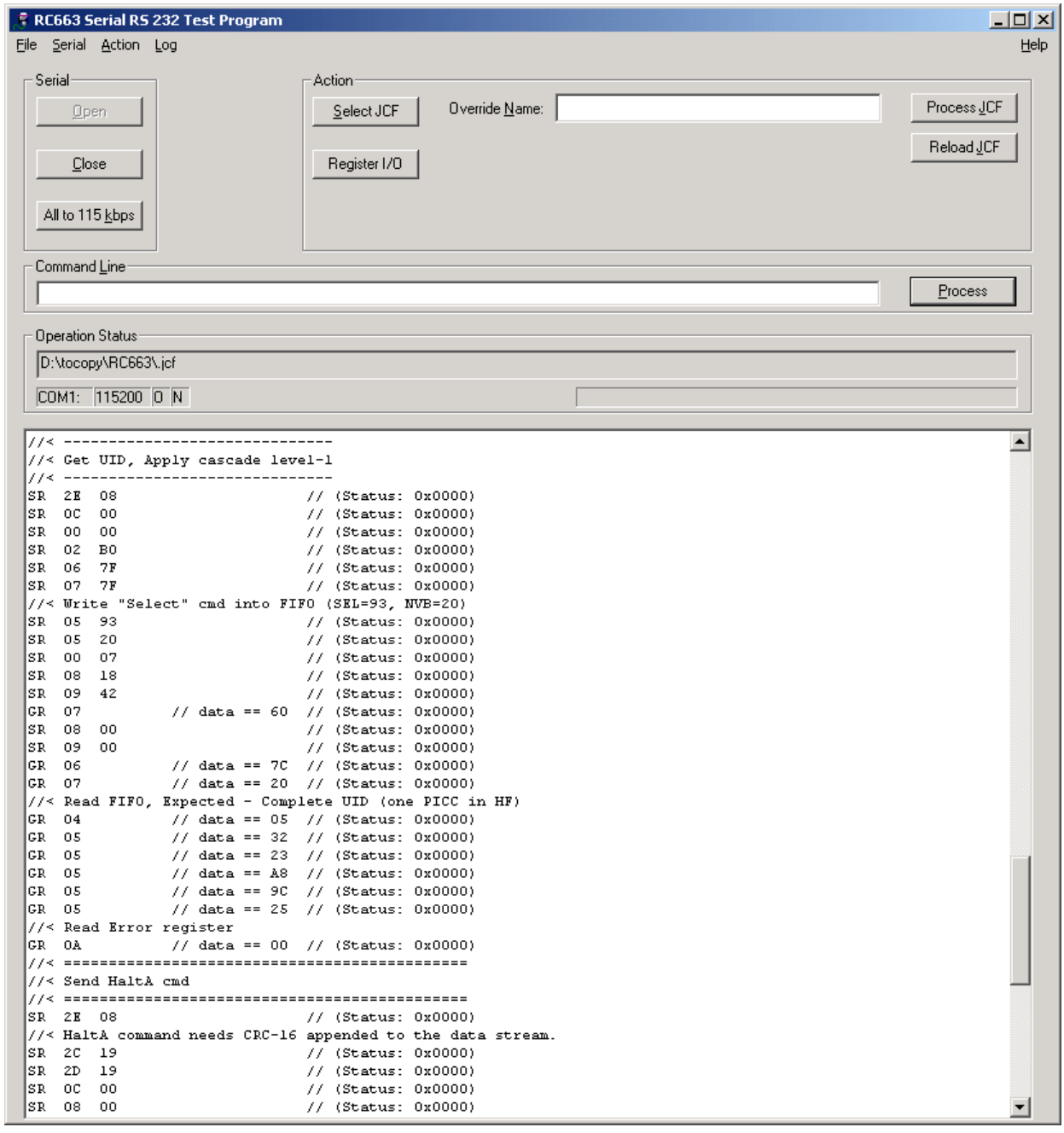

Fig 4. Reading 4 byte UID

All the possible commands (e.g. SR, RE…) used in the scripts are explained when selecting **Help/Commands**.

As mentioned above more details on the scripts can be viewed by opening the *.jcf file with a text editor.

The first comments of the script chosen: RC663_ISO14443A_4byteUID.jcf to compare it to the output of the trace window:

```
1    CLL
2    CHB 115200
3
4    //> ============================================
5    //> RC663 Script for (Iso14443-3A protocol):
6    //>   * ReqA
7    //>   * Get UID (Select: Casade level 1)
8    //>   * HaltA
9    //>
10   //> Note: Only one PICC shall be in HF
11   //> ============================================
12
13   //> ============================================
14   //> RC663 ApplyProtocolSettings:  ISO14443A=01
15   //> ============================================
16   //
17   //> Configure Timers
18   //
19   // Set Timer-0, T0Control_Reg:
20   // Starts at the end of Tx. Stops after Rx of first data. Auto-reloaded. 13.56
     MHz input clock.
21      SR 0F 98
22
23   // Set Timer-1, T1Control_Reg:
24   // Starts at the end of Tx. Stops after Rx of first data. Input clock - cascaded
     with Timer-0.
25      SR 14 92
26
27   // Set Timer-2, T2Control_Reg:  Timer used for LFO trimming
28      SR 19 20
29
30   // Set Timer-2 reload value (T2ReloadHi_Reg and T2ReloadLo_Reg)
31      SR 1A 03
32      SR 1B FF
33
34   // Set Timer-3, T3Control_Reg:
35   // Not started automatically. Not reloaded. Input clock 13.56 MHz
36      SR 1E 00
37
38   //> Configure FIFO Size=255 and Water-level
```

```
39  // Set FifoControl_Reg, Fifo size=255 bytes. Flush FIFO
40     SR 02 90
41
42  // Set WaterLevel =(FIFO length -1)
43     SR 03 FE
44
45  // RxBitCtrl_Reg(0x0c)     Received bit after collision are replaced with 1.
46     SR 0C 80
47
48  // DrvMod reg(0x28), Tx2Inv=1
49     GR 28
50     SR 28 80
51
52  // TxAmp_Reg(0x29)
53     SR 29 00
54
55  // DrvCon_Reg(0x2A)
56     SR 2A 01
57
58  // TxI_Reg(0x05),(0x05)
59     SR 2B 05
60
61  // RxSOFD_Reg(0x34),(0x00),
62        SR 34 00
63
64  // Rcv_Reg(0x38),(0x12)
65        SR 38 12
66  //
67  //> ============================================
68  //> 2. LoadProtocol( bTxProtocol=0, bRxProtocol=0)
69  //> ============================================
70
71  //> Terminate any running command. Flush_FiFo
72     SR 00 00
73     SR 02 b0
74
75  // Clear all IRQ 0,1 flags
76     SR 06 7f
77     SR 07 7f
78
79  //> Write in Fifo: Tx and Rx protocol numbers(0,0)
80     GR 04
81     SR 05 00    // Rx protocol=0
82     SR 05 00    // Tx prot=0
83
84  // Enable IRQ0 interrupt sources
85  //
86  // Idle interrupt(Command terminated), RC663_BIT_IDLEIRQ=0x10
87     GR 08
88     SR 08 10
89
```

```
90    // Enable Global IRQ propagation.
91       GR 09
92       SR 09 40
93
94    //> Start RC663 command "Load Protocol"=0x0d
95       SR 00 0D
96    …
97    …
98    …
```

1.2 Command Line

Besides the script files, single commands can be handled, too. This can be done by typing e.g. **GR 0A** (Gets the status of register 0A (error register)) in the Command Line and execute it with **Process**. In principle all lines of the scripts provided could be fed into the command line sequentially, each followed with a **Process**.

1.3 Register I/O

The button Register I/O can be used to read from and write to certain registers.

2. LPCD mode

2.1 How LPCD works

The low power card detection mode is an energy saving mode intended for use cases where CLRC663 family is supplied by battery and not connected to mains.

The LPCD feature is INDEPENDENT from the actual smartcard/tag communication protocol used.

The LPCD works in two phases:

The standby phase, controlled with the wake up timer 4 which defines the duration of the standby of the CLRC663 family.

Second phase is the detection-phase. The values of the I and Q channel are detected and stored in the register map. (LPCD_I_Result_Reg, LPCD_Q_Result_Reg).This time period can be handled with Timer3. The value is compared with the min/max values in the registers (LPCD_IMin_Reg, LPCD_IMax_Reg; LPCD_QMin_Reg, PCD_QMax_Reg). If it exceeds a certain limit the LPCDIrq will be raised.

2.2 Getting LPCD mode configured on CLRC663 family

- Connect the CLRC663 Reader and execute the LPCD_ModeConfig_Part1.jcf without card in the field.
- Note the I and Q values. See Fig 5 for more details.

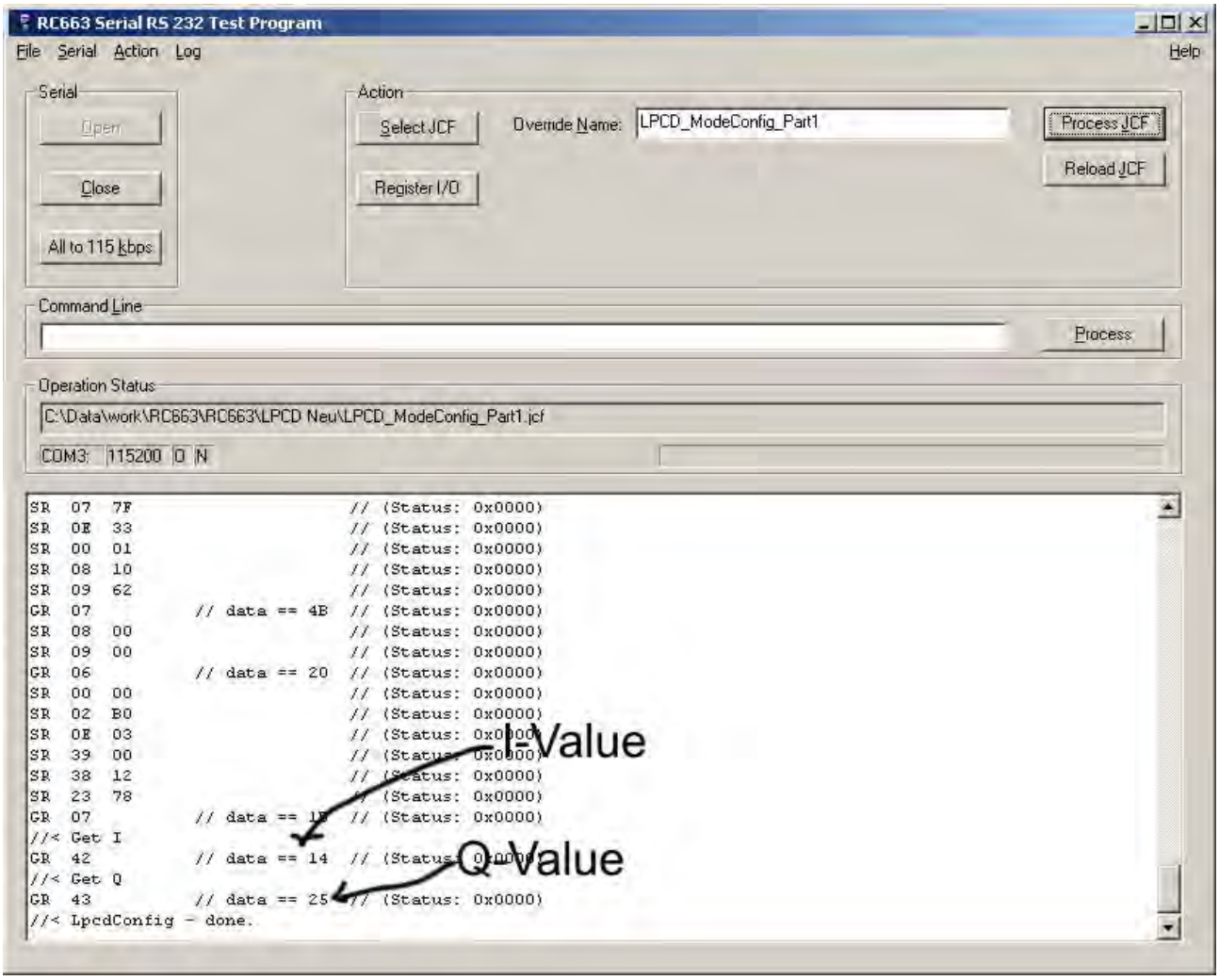

Fig 5. I and Q value

- Open the LPCD.xls Excel sheet and insert these values. The threshold values will be calculated accordingly for register 3F, 40 and 41. See Fig 6 for more details.

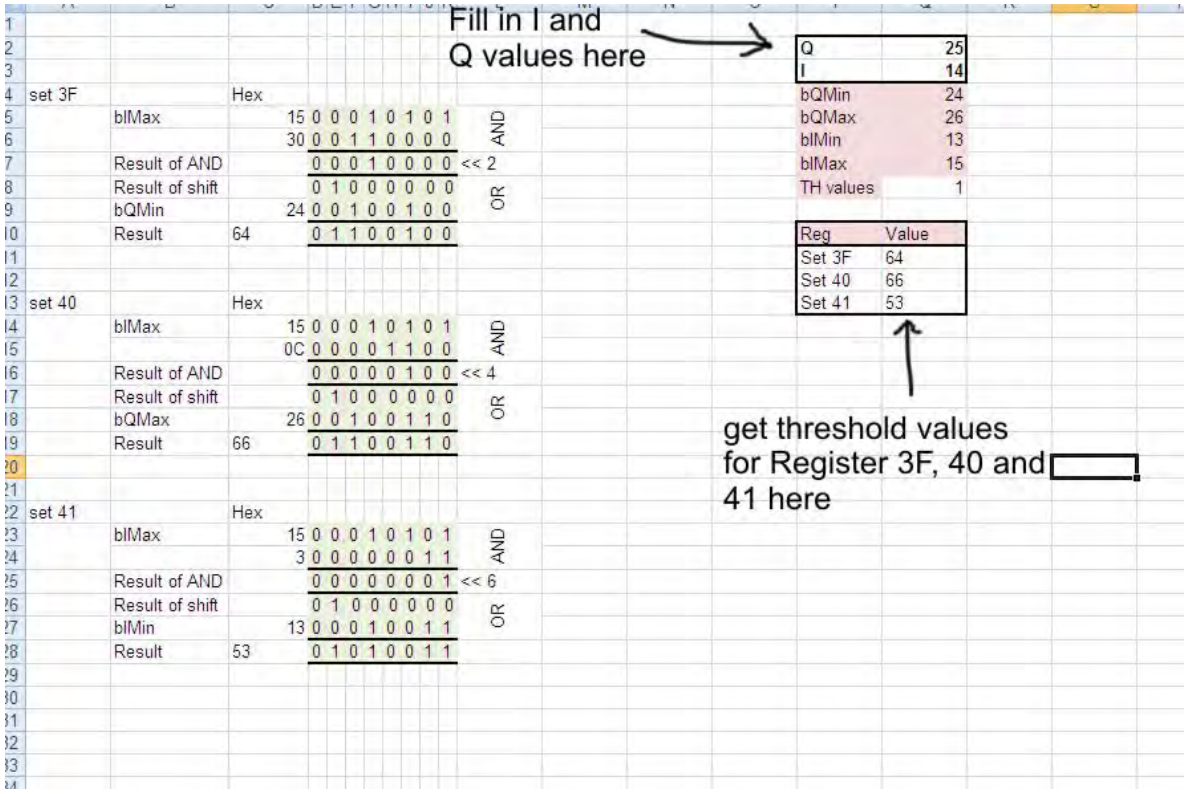

Fig 6. Fill in I and Q value, the threshold values are calculated automatically

- Open the **PCD_DetectPICC_Part2.jcf** file with an editor and fill in the calculated threshold values for 3F, 40 and 41.

```
1    //>
2    //> Insert 2 ISO14443-3A Cards in HF.
3    //> ============================================
4
5    //
6    // Example, Asumming Q=0x13, I=0x0C
7    //
8    //    bQMin = Q-1;   // 0x12
9    //    bQMax = Q+1;   // 0x14
10   //    bIMin = I-1;   // 0x0b
11   //    bIMax = I+1;   // 0x0d
12
13   //> 1. Set QMin register = bQMin | ((bIMax & 0x30) << 2));
14   SR  3F 64
15
16   //> 2. Set QMax register = bQMax | ((bIMax & 0x0C) << 4));
17   SR  40 66
18
19   //> 3. Set IMin register = bIMin | ((bIMax & 0x03) << 6));
```

```
20    SR  41 53
21
22    //> Prepare LPCD command, power down time 10[ms]. Cmd time 150[µsec].
```

- Save the **PCD_DetectPICC_Part2.jcf** file with the new values and execute with the “RC663 Serial” program. The executed script should stay in a loop until a card is detected in the field.
- A correct detection is indicated when bit5 (LPCD_Irq) in register 07 is set. See Fig 7 for more details.

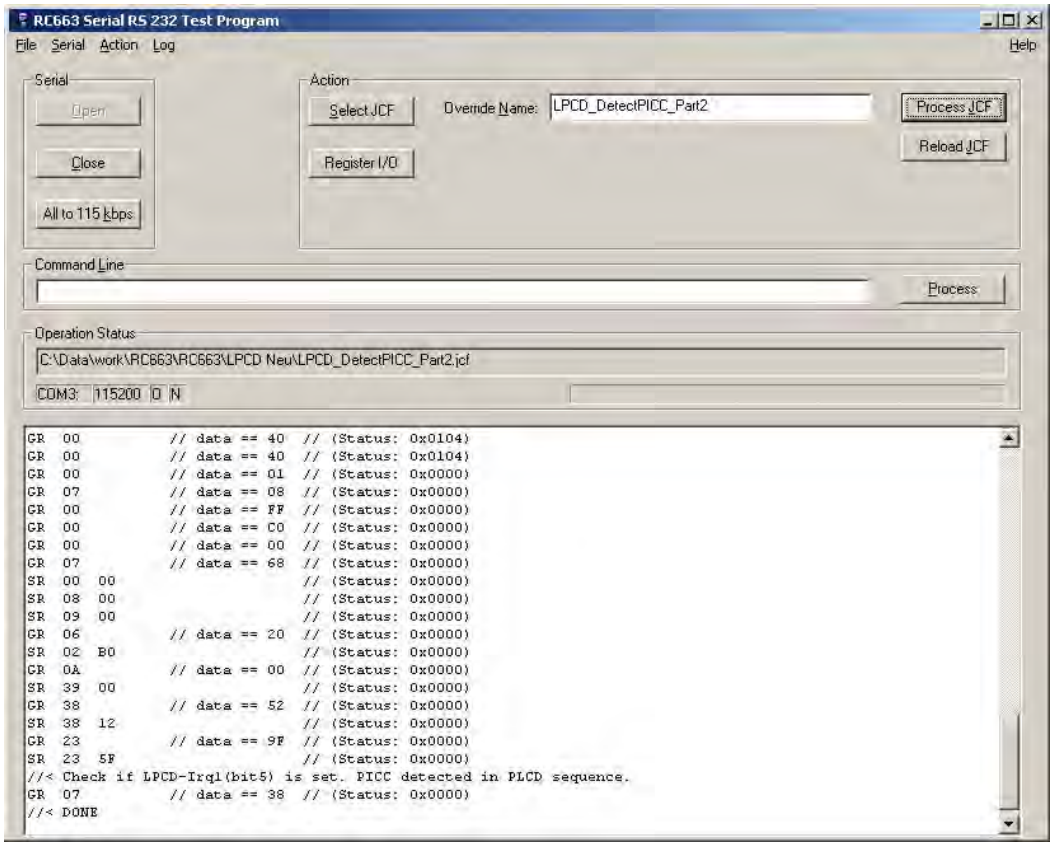

Fig 7. LPCD_Irq set

Important note: If the program terminates unexpectedly without a card in the field, then a higher “TH value” in the calculation is required. Therefore, iteratively increase cell “Q8” in the LPCD.xls by one and try with the new threshold values.

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Date of release: 17 July 2012
223711
Document identifier: AN11145