TL7230MD

FULL LAYER-III ISO/IEC 11172-3 AUDIO DECODER

- Single-chip ISO/IEC 11172-3 Layer III Audio Decoder
- Supports All MPEG Bit Rates Including Free Format
- Supports 32/44.1/48KHz Sampling Frequencies for MPEG Bit Stream
- Supports Single Channel, Dual Channel, Stereo, and Joint Stereo
- Any Combination of Intensity Stereo and MS Stereo is supported.
- Serial Bit Stream Input
- 8-bit Host Interface Port
- Digital Volume Control
- Digital Bass/Treble Control
- 6 Band Equalizer Function
- Voice Record/Playback Capability
- Supports Off-chip DAC Interface
- On-chip ADC with 12-bit Resolution
- Power Management to Reduce Power Consumption
- PLL for Internal Clocks and for Output PCM Clock Generation
- Single 16.9344MHz External Clock Input
- 3.0 V Operation
- Small Footprint 100-pin Thin Quad Flat Package

DESCRIPTION

TL7230MD is a single-chip ISO/IEC 11172-3 Layer III audio decoder, capable of decoding compressed elementary bit streams as specified in ISO/IEC standard. It is designed to be well suited for portable audio appliances.

TL7230MD receives the input data bit stream through a serial data interface. The decoded signal is 16-bit serial PCM format that can be sent directly to DAC. The generated PCM data can be sent to off-chip DAC. The off-chip DAC interface is programmable to adapt the PCM output of TL7230MD to the most common DACs used on the market.

An 8-bit host interface port is provided to receive control information from and send status information to host. 8-bit microcontrollers such as those of Intel or Motorola can be connected easily.

TL7230MD has the capability of compressing voice signals. It can receive voice signals through on-chip ADC. The compressed voice signals are transmitted to or received from host through serial data interface. It can also reproduce the voice signals from the compressed voice signals.

FUNCTIONAL BLOCK DIAGRAM

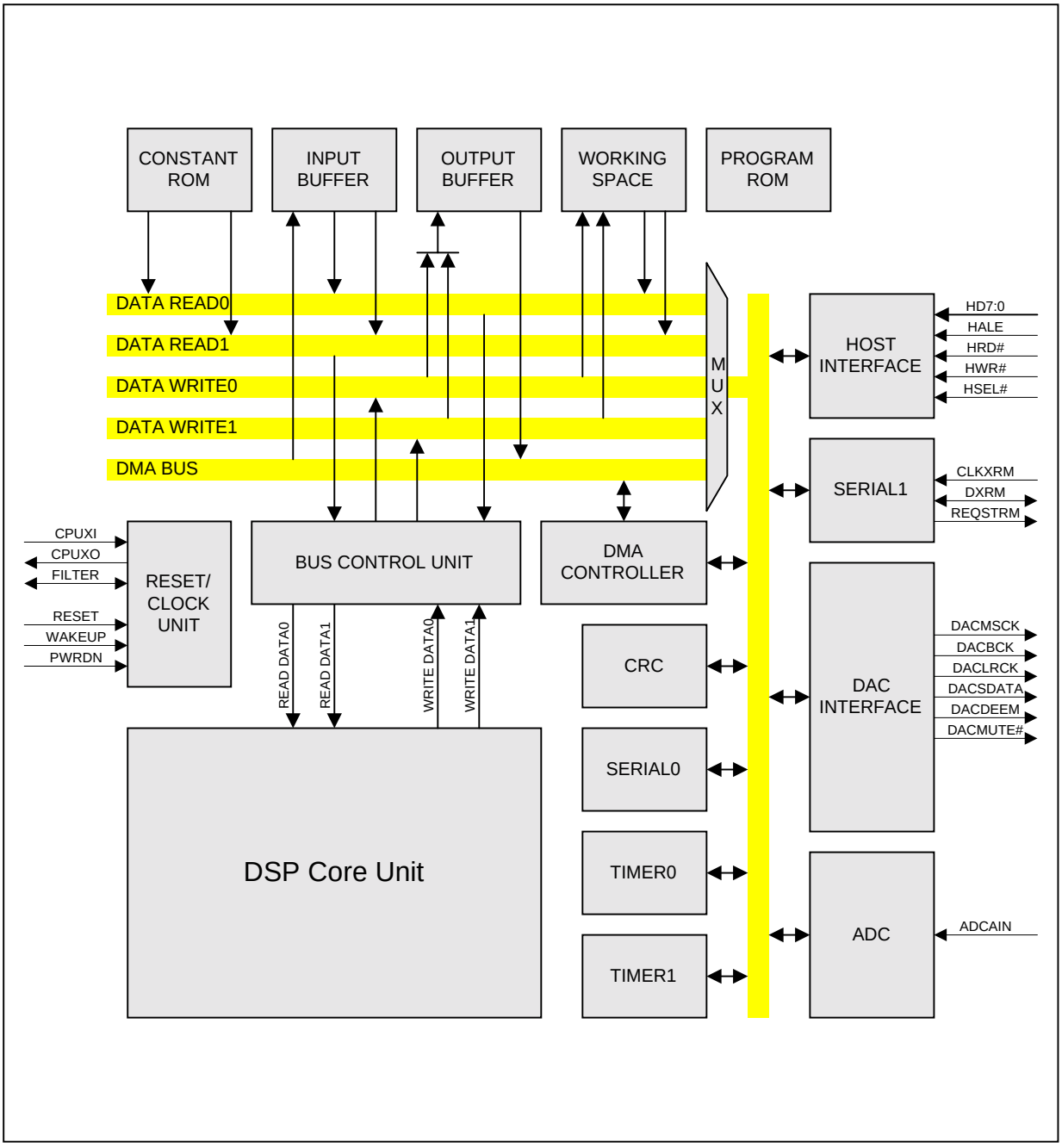


Figure 1. Functional Block Diagram of TL7230MD

PIN DESCRIPTION

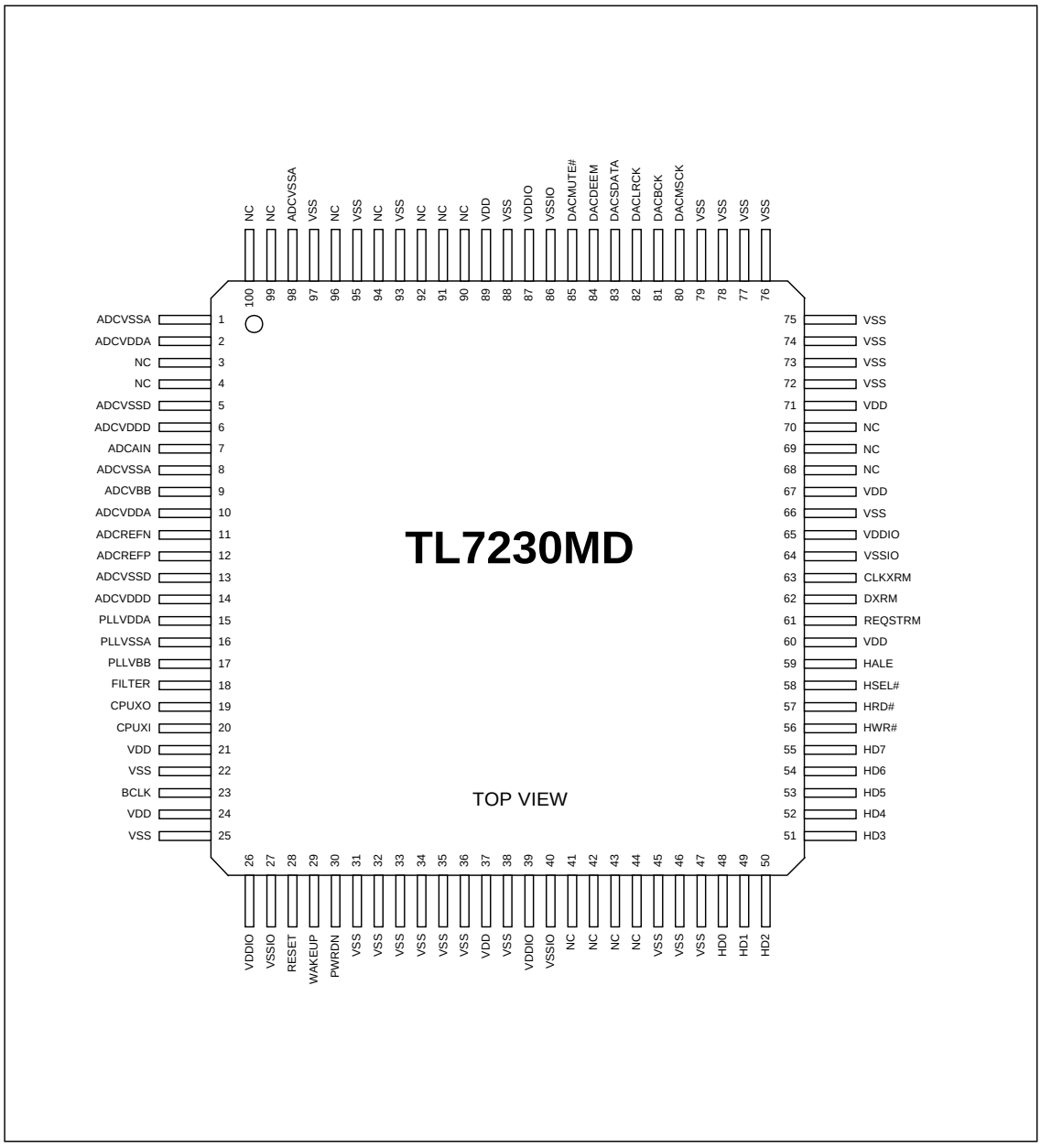


Figure 2. 100-pin Thin Quad Flat Package (TQFP)

Table 1. Pin Locations with Pin Names

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	ADCVSSA	26	VDDIO	51	HD3	76	VSS
2	ADCVDDA	27	VSSIO	52	HD4	77	VSS
3	NC	28	RESET	53	HD5	78	VSS
4	NC	29	WAKEUP	54	HD6	79	VSS
5	ADCVSSD	30	PWRDN	55	HD7	80	DACMSCK
6	ADCVDDD	31	VSS	56	HWR#	81	DACBCK
7	ADCAIN	32	VSS	57	HRD#	82	DACLRCK
8	ADCVSSA	33	VSS	58	HSEL#	83	DACSDATA
9	ADCVBB	34	VSS	59	HALE	84	DACDEEM
10	ADCVDDA	35	VSS	60	VDD	85	DACMUTE#
11	ADCREFN	36	VSS	61	REQSTRM	86	VSSIO
12	ADCREFP	37	VDD	62	DXRM	87	VDDIO
13	ADCVSSD	38	VSS	63	CLKXRM	88	VSS
14	ADCVDDD	39	VDDIO	64	VSSIO	89	VDD
15	PLLVDDA	40	VSSIO	65	VDDIO	90	NC
16	PLLVSSA	41	NC	66	VSS	91	NC
17	PLLVBB	42	NC	67	VDD	92	NC
18	FILTER	43	NC	68	NC	93	VSS
19	CPUXO	44	NC	69	NC	94	NC
20	CPUXI	45	VSS	70	NC	95	VSS
21	VDD	46	VSS	71	VDD	96	NC
22	VSS	47	VSS	72	VSS	97	VSS
23	BCLK	48	HD0	73	VSS	98	ADCVSSA
24	VDD	49	HD1	74	VSS	99	NC
25	VSS	50	HD2	75	VSS	100	NC

Table 2. Pin Functions with Location

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
ADCAIN	7	HD0	48	NC	96	VSS	34
ADCREFN	11	HD1	49	NC	99	VSS	35
ADCREFP	12	HD2	50	NC	100	VSS	36
ADCVBB	9	HD3	51	PLLVBB	17	VSS	38
ADCVDDA	10	HD4	52	PLLVDDA	15	VSS	45
ADCVDDA	2	HD5	53	PLLVSSA	16	VSS	46
ADCVDDD	6	HD6	54	PWRDN	30	VSS	47
ADCVDDD	14	HD7	55	REQSTRM	61	VSS	66
ADCVSSA	1	HALE	59	RESET	28	VSS	72
ADCVSSA	8	HRD#	57	VDD	21	VSS	73
ADCVSSA	98	HSEL#	58	VDD	24	VSS	74
ADCVSSD	5	HWR#	56	VDD	37	VSS	75
ADCVSSD	13	NC	3	VDD	60	VSS	76
BCLK	23	NC	4	VDD	67	VSS	77
CLKXRM	63	NC	41	VDD	71	VSS	78
CPUXI	20	NC	42	VDD	89	VSS	79
CPUXO	19	NC	43	VDDIO	26	VSS	88
DACBCK	81	NC	44	VDDIO	39	VSS	93
DACDEEM	84	NC	68	VDDIO	65	VSS	95
DACLRCK	82	NC	69	VDDIO	87	VSS	97
DACMSCK	80	NC	70	VSS	22	VSSIO	27
DACMUTE#	85	NC	90	VSS	25	VSSIO	40
DACSDATA	83	NC	91	VSS	31	VSSIO	64
DXRM	62	NC	92	VSS	32	VSSIO	86
FILTER	18	NC	94	VSS	33	WAKEUP	29

Table 3. Pin Descriptions

Signal Name	Type	Description
Internal PLL Interface		
CPUXI	I	**CPU Clock In.** 16.9344MHz crystal clock input.
CPUXO	O	**CPU Clock Out.** 16.9344MHz crystal clock output.
FILTER	O	**Charge Pump Out.** External capacitor should be connected between this pin and analog ground.
Clock Signal		
BCLK	O	**Processor Clock Output.**
Reset & Power Down Control		
RESET	I	**Chip Reset.** Reset input to the chip. Internal pull down.
WAKEUP	I	**Wake Up.** When high, chip is waked up from SLEEP state. This pin should be remained active at least 1 clock cycle and inactive before the host issues next SLEEP command. Internal pull down.
PWRDN	I	**Power Down.** This pin controls PWRDOWN state. When high, chip goes to very low power consumption state. After deactivation, WAKEUP pin should be remained low at least 150μs. Internal pull down. (Restriction: This pin should be active ONLY in SLEEP state. Otherwise, Chip reset should be activated.)
MCU Serial Interface		
CLKXRM	I	**Serial Clock.** MCU serial interface clock**.**
DXRM	I/O	**Serial Data.** When MCU transmits data, this data pin is sampled at negative edge of CLKXRM. When MCU receives data, Data is valid from negative edge of CLKXRM to next negative edge of CLKXRM. DXRM should be sampled at positive edge of CLKXRM. After reset, TL7230MD is set to transmit the most significant bit first.
REQSTRM	O	**Request Bit Stream Data.** MCU must check this pin to determine to continue receiving or transmitting. MCU should transmit or receive data during this signal active.
MCU HIP(Host Interface Port) Interface		
HSEL#	I	**HIP Enable.** When Low, HIP is selected.
HALE	I	**HIP Address Latch Enable.** When High, HD7:0 should have HIP address, which is sampled at negative edge of this signal.
HRD#	I	**HIP Read Enable.** When low, data is loaded to HD7:0, which should be sampled at positive edge of this signal.
HWR#	I	**HIP Write Enable.** Data at HD7:0 is sampled at positive edge of this signal.
HD7:0	I/O	**HIP Address/Data Bus.** Multiplexed address lines and data lines.
Internal ADC Interface		
ADCAIN	I	**ADC Analog Input.** Analog input spans between ADCREFP and ADCREFN.
ADCREFP	I	**ADC Internal Reference Top Bias**. Connect this pin to voltage between ADCVDDA and 2.0V.
ADCREFN	I	**ADC Internal Reference Bottom Bias.** Connect this pin to ground.

ADCVDDA	PWR	**ADC Supply Voltage for Analog Circuit.** Connect this pin to the +3.0V supply voltage.
ADCVSSA	GND	**ADC Ground for Analog Circuit.** Connect this pin to ground.
ADCVDDD	PWR	**ADC Supply Voltage for Digital Circuit.** Connect this pin to the +3.0V supply voltage.
ADCVSSD	GND	**ADC Ground for Digital Circuit.** Connect this pin to ground.
ADCVBB	GND	**ADC Analog/Digital Bulk Bias.** Connect this pin to ground.
External DAC Interface		
DACMSCK	O	**DAC Master Clock.** 384×Fs clock.
DACBCK	O	**DAC Bit Clock.** 32×Fs clock**.**
DACLRCK	O	**DAC Sample Rate Clock.** Fs clock.
DACSDATA	O	**DAC Serial Data.** Serial data**.**
DACDEEM	O	**DAC Deemphasis.** When deemphasis is on, this signal is high. It can be set/clear through HIP commands.
DACMUTE#	O	**DAC Mute.** Analog output mute. When external DAC is set to mute on, this signal is low. It can be set/clear through HIP commands.
Power/Ground Pins		
VDD	PWR	**Supply Voltage.** Connect this pin to the +3.0V supply voltage.
VSS	GND	**Circuit Ground.** Connect this pin to ground.
VDDIO	PWR	**Supply Voltage for I/O Buffers.** Connect this pin to the +3.0V supply voltage.
VSSIO	GND	**Circuit Ground for I/O Buffers.** Connect this pin to ground.

FUNCTIONAL DESCRIPTION

RESET/CLOCK UNIT

TL7230MD is driven by a single clock at the frequency of 16.9344MHz. The clock is derived from an external source or from an industry standard crystal oscillator, generating input frequency of 16.9344MHz. The clock generation unit has a PLL, and all the internal clock signals including internal DAC/ADC clocks are generated with the input clock.

When TL7230MD is in power-on-reset, RESET signal should be active at least 150μs till the internal PLL is stabilized. To reset TL7230MD during normal operation, RESET signal should be active at least 16 cycles.

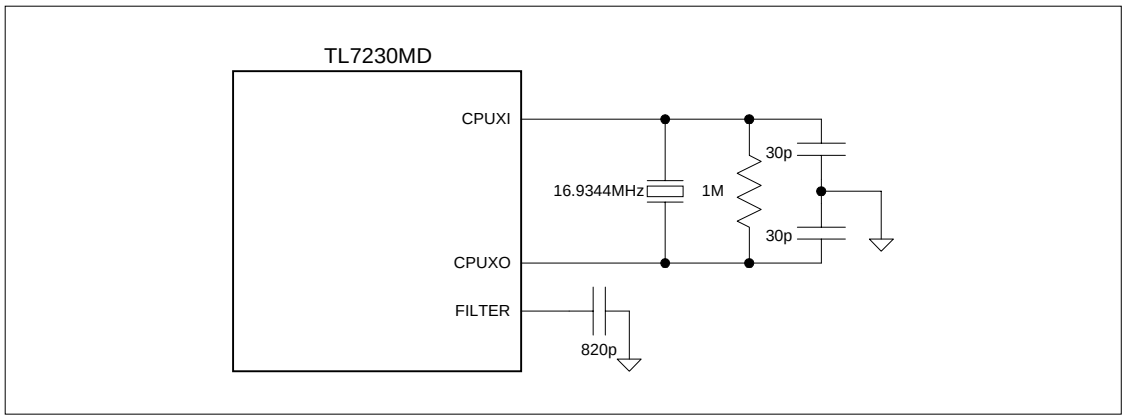


Figure 3. Clock Circuit

DSP CORE LOGIC

The core logic of TL7230MD is a 32-bit floating-point DSP processor. The independent multiplier and accumulator of TL7230MD can achieve high performance. Internal registers are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. Since all the data input/output transactions are managed by DMA, there is no computational overhead due to data transactions.

SERIAL INTERFACE

The serial interface of TL7230MD is used to receive MPEG bit stream data or transmit/receive voice data. It is configured to transfer 8 bits of data per word. It can be configured to be LSB-first or MSB first transfer mode. LSB-first means that the data bits are transmitted and received least-significant bit (LSB) first. MSB-first means that the data bits are transmitted and received most-significant bit (MSB) first. The clock for the serial interface should be generated externally.

The related signals are CLKXRM, DXRM, and REQSTRM. REQSTRM is used for synchronization between microcontroller and TL7230MD, and data is transferred during

REQSTRM active.

When microcontroller tries to send data to TL7230MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to transmit mode and send serial clock and serial data. After transmitting each byte, microcontroller should check REQSTRM to decide whether next byte is to be transmitted or not.

When microcontroller tries to receive data from TL7230MD, it should check whether REQSTRM is active or not. If the signal is active, microcontroller sets its serial interface to receive mode and send serial clock and receive serial data from TL7230MD. After receiving each byte, microcontroller should check REQSTRM to decide whether TL7230MD will transmit next byte or not.

HOST INTERFACE PORT (HIP)

Host interface port is used to send commands to and receive status information from TL7230MD. HIP of TL7230MD is a parallel I/O port that makes a connection to a host processor easily. Through the HIP, TL7230MD can be used as a memory-mapped peripheral to a host processor. The HIP can be thought of as an area of dual-port memory that allows communication between the computational core of the TL7230MD and host. The HIP is completely asynchronous. The host processor can write data into the HIP while the TL7230MD is operating at full speed. HIP transfers are managed using interrupt scheme.

HIP contains 21 registers. Four of them are data-in registers (HDI0/HDI1/HDI2/HDI3) and one of them is a status register (HSR4). The remaining 16 registers are data-out registers (HDO0/…/HDO15). Data written into HDIs by host are read by TL7230MD. Through these registers host can give necessary commands to TL7230MD. A command is written into a HDI0, and the required parameters of the command are written into the HDI1/HDI2/HDI3. The status register (HSR4) keeps the information whether data written into the data registers are read by TL7230MD. The status register is managed automatically by TL7230MD and can be read by host. TL7230MD starts HIP command processing when HDI0 register is written. So if any command requires parameters, user should write parameters first, and then write command.

Serial ID number can be used to check whether given command has been accepted or not. TL7230MD can receive the serial ID value into HDO0 when TL7230MD has accepted the given command. Thus when commands are given to TL7230MD with different serial ID numbers, it can be examined which command is being processed. Serial ID Number itself hasn't any special meaning. If this feature is not needed, it is not required to send ID values with commands. Then the value of HDO0 is undetermined. There is an exception for the ID number convention. If you use HIP command 0Dh(Revision Code), TL7230MD returns the revision number, not the ID number.

HDOs are written by TL7230MD and can be read by host. All HIP registers should be memory-mapped into the memory space of the host processor. The address space of those registers is shown in Table 4. The usable commands are listed in Table 5. The contents reported by HDOs are shown from Figure 4 to Figure 15.

Table 4. Address of Host Interface Port Registers

ADDRESS	REGISTERS	DESCRIPTION
00h	HDI0	Command
01h	HDI1	Serial ID Number
02h ~ 03h	HDI2/HDI3	Parameters if needed
04h	HSR4	Status Register (Fig. 4)
10h	HDO0	Command Serial ID Number (Fig. 5)
11h	HDO1	Decoder State (Fig. 6)
12h	HDO2	IO Status (Fig. 7)
13h	HDO3	IO Status (Fig. 8)
14h	HDO4	Volume (Fig. 9)
15h	HDO5	Serial Interface Mode (Fig. 10)
16h ~ 1Fh	HDO6 ~ HDO15	The reporting contents depend on the mode setting of TL7230MD. (Refer to Table 5)

The reporting contents of HDO6 to HDO15 depend on the mode setting of TL7230MD. The mode can be set by using HIP command 19h(Report Format). For this command, refer to Table 6.

Table 5. The contents of HDO6 ~ HDO15 according to mode setting

ADDRESS	REGISTERS	DESCRIPTION
16h	HDO6	Mode0: 00h Mode1: Tone Control Status. When tone control is enabled, 1 is reported. Otherwise, 0 is reported. Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: Equalizer Control Status. When equalizer control is enabled, 1 is reported. Otherwise, 0 is reported.
17h	HDO7	Mode0: 00h Mode1: Tone Control - Prescaling Information Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control – Prescaling Information
18h	HDO8	Mode0: 00h Mode1: Tone Control – Bass Cutoff Frequency Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control – Band1 Gain
19h	HDO9	Mode0: 00h Mode1: Tone Control – Bass Gain Mode2: MP3 Frame Count (Fig. 11) Mode3: Voice Data Code Count (Fig. 11) Mode4: EQ Control –Band2 Gain

1Ah	HDO10	Mode0: 00h Mode1: Tone Control – Treble Cutoff Frequency Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 12) Mode3: 00h Mode4: EQ Control – Band3 Gain
1Bh	HDO11	Mode0: 00h Mode1: Tone Control – Treble Gain Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 13) Mode3: 00h Mode4: EQ Control – Band4 Gain
1Ch	HDO12	Mode0: 00h Mode1: 00h Mode2: The most recently synchronized frame header of MP3 bit stream. (Fig. 14) Mode3: 00h Mode4: EQ Control – Band5 Gain
1Dh	HDO13	Mode0: 00h Mode1: 00h Mode2: Bass Boost Information (Fig. 15) Mode3: 00h Mode4: EQ Control – Band6 Gain
1Eh	HDO14	Mode0: 00h Mode1: 00h Mode2: 00h Mode3: 00h Mode4: 00h
1Fh	HDO15	Mode0: 00h Mode1: 00h Mode2: CRC Error Count Mode3: 00h Mode4: 00h

Table 6. Host Interface Port Commands

<table>
<tr><th>COMMAND</th><th>PARAMETER</th><th>MEANING</th><th>DESCRIPTION</th></tr>
<tr><td>00h</td><td>None</td><td>Stop</td><td>Stop execution and go into WAIT state.</td></tr>
<tr><td>01h</td><td>None</td><td>MP3 Decoding</td><td>Execute MP3 decoding.</td></tr>
<tr><td>04h</td><td>None</td><td>Voice Encoding</td><td>Execute voice encoding (16Kbps).</td></tr>
<tr><td>05h</td><td>None</td><td>Voice Decoding</td><td>Execute voice decoding (16Kbps).</td></tr>
<tr><td>06h</td><td>None</td><td>Voice Encoding</td><td>Execute voice encoding (24Kbps).</td></tr>
<tr><td>07h</td><td>None</td><td>Voice Decoding</td><td>Execute voice decoding (24Kbps).</td></tr>
<tr><td>08h</td><td>None</td><td>Voice Encoding</td><td>Execute voice encoding (32Kbps).</td></tr>
<tr><td>09h</td><td>None</td><td>Voice Decoding</td><td>Execute voice decoding (32Kbps).</td></tr>
<tr><td>0Dh</td><td>None</td><td>Revision Code</td><td>Report the TL7230MD revision number in HDO0.</td></tr>
<tr><td>0Fh</td><td>None</td><td>Sleep</td><td>Go into SLEEP state. This command should be used in WAIT state. If this command is used during algorithm execution, TL7230MD becomes unstable.</td></tr>
<tr><td>10h</td><td>None</td><td>Mute ON</td><td>DACMUTE# becomes active. After reset, TL7230MD is set to be mute on.</td></tr>
<tr><td>11h</td><td>None</td><td>Mute OFF</td><td>Mute is disabled.</td></tr>
<tr><td>15h</td><td>None</td><td>External DAC</td><td>Use external DAC. After reset, external DAC interface is disabled. So, system user should use this command to enable external DAC interface. The waveform of I/O pin related to external DAC is controlled according to External DAC Format or External DAC Format 2.</td></tr>
<tr><td>16h</td><td>1byte</td><td>External DAC Format</td><td>Set the waveform of I/O pin related to external DAC. The parameter value of External DAC Format command should be as follows: {0, 0, 0, 0, 0, I^2S, PL, PB}. For the meaning of I^2S, PL, and PB, refer to Figure 8.</td></tr>
<tr><td>17h</td><td>None</td><td>MSB First</td><td>Serial Interface MSB-first mode. This is the default mode after reset.</td></tr>
<tr><td>18h</td><td>None</td><td>LSB First</td><td>Serial Interface LSB-first mode</td></tr>
<tr><td>19h</td><td>1byte</td><td>Report Format</td><td>The reported contents of HDO6 to HDO15 are changed according to parameter of this command.
<table>
<tr><th>Parameter</th><th>Reporting Contents</th></tr>
<tr><td>0</td><td>all 00h</td></tr>
<tr><td>1</td><td>Tone Control Information</td></tr>
<tr><td>2</td><td>MP3 Decoding Information</td></tr>
<tr><td>3</td><td>Voice Encoding/Decoding Information</td></tr>
<tr><td>4</td><td>Equalizer Control Information</td></tr>
</table>
</td></tr>
</table>

20h	1byte	Bass Boost Control (MP3 Only)	Control Bass boost. The upper nibble of the parameter controls the cutoff frequency of bass boost, and the lower nibble controls the level of bass boost. The value of upper nibble should be in the range of 0 to 6. The cutoff frequency is 25 × upper nibble + 50 (Hz). If the values of the lower nibble is in the range of 0 to 12, the low frequency band below the cutoff frequency is boosted by 0dB ~ 18dB (1.5dB step). The other values mean no boost. For example, if the parameter value is 42h, then the cutoff frequency will be 25×4+50=150Hz, and the frequency band below 150Hz will be boosted by 3dB compared to the upper frequency band. In case of using bass boost, volume is reduced by 1.5 × *n* dB where *n* means the parameter value. The reset value is FFh(disabled).
21h	1byte	Volume Control	Control volume. The parameter should have the value of range from 0 to 255. If the value is *n*, the volume is attenuated by *n*/2 dB compared to maximum volume. The reset value is 0.
22h	1byte	Prescale Control	Control the prescaling. The parameter is a signed value and can be -128 to 127. The prescaling is done by 0.5 × *n* dB according to parameter value *n*. That is, 0h ~ 7Fh means 0dB ~ 63.5dB scaling, 80h ~ FFh means –64dB ~ -0.5dB scaling. The reset value is 0dB.
23h	1byte	Tone Control – Bass Gain (MP3 Only)	Control the Bass Gain. The parameter is a signed value and can be -128 to 127. The gain can be 0.5 × *n* dB according to parameter value *n*. The reset value is 0.
24h	1byte	Tone Control – Treble Gain (MP3 Only)	Control the Treble Gain. The parameter is a signed value and can be -128 to 127. The gain can be 0.5 × *n* dB according to parameter value *n*. The reset value is 0.
25h	1byte	Tone Control – Bass Cutoff (MP3 Only)	Control the Bass Cutoff Frequency. The parameter can have the value of 0 to 255. The cutoff frequency can be 20 + 5 × *n* Hz according to parameter value *n*. The reset value is 0.
26h	1byte	Tone Control – Treble Cutoff (MP3 Only)	Control the Treble Cutoff Frequency. The parameter can have the value of 0 to 255. The cutoff frequency can be 5000 + 20 × *n* Hz according to parameter value *n*. The reset value is 0.
27h	none	Tone Control – Enable (MP3 Only)	Enable the Tone Control Function. Tone Control Function is disabled when reset.
28h	none	Tone Control – Disable (MP3 Only)	Disable the Tone Control Function. Tone Control Function is disabled when reset.
30h	none	MP3 CRC Bypass (MP3 Only)	During MP3 decoding, even if the input bit stream contains the CRC field, TL7230MD doesn't check the CRC error. After reset, TL7230MD is set to check CRC error.

31h	none	MP3 CRC Check	During MP3 decoding, if the input bit stream contains the CRC field, check the CRC error. If an error occurs, TL7230MD outputs 0 during the period of corresponding MP3 frame. The reset value is MP3 CRC check.
40h	1byte	EQ Control – Band1 Gain (MP3 Only)	Control the gain of Band1(<30Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
41h	1byte	EQ Control – Band2 Gain (MP3 Only)	Control the gain of Band2(30Hz~125Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
42h	1byte	EQ Control – Band3 Gain (MP3 Only)	Control the gain of Band3(125Hz~500Hz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
43h	1byte	EQ Control – Band4 Gain (MP3 Only)	Control the gain of Band4(500Hz~2KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
44h	1byte	EQ Control – Band5 Gain (MP3 Only)	Control the gain of Band5(2KHz~8KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
45h	1byte	EQ Control – Band6 Gain (MP3 Only)	Control the gain of Band6(>8KHz) of 6-band equalizer. The parameter is a signed value and can be -128 to 127. The gain can be $0.5 \times n$ dB according to parameter value *n*. The reset value is 0dB.
46h	none	EQ Control – Enable (MP3 Only)	Enable the Equalizer Function. The equalizer function is disabled after reset.
47h	none	EQ Control – Disable (MP3 Only)	Disable the Equalizer Function. The equalizer function is disabled after reset.
8xh	None	External DAC Format2	Same as External DAC Format command. Parameter values are located at lower nibble of the command. The command should be the form of {1, 0, 0, 0, 0, I^2S, PL, PB}.

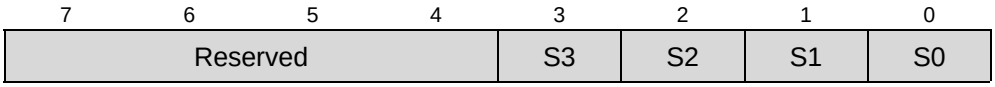
Bass boost control command(20h) is another form of tone control command(23h ~28h). It is implemented by using the same filter as tone control command. Thus, if bass boost control command is received with valid parameter value, gains and cutoffs are changed as follows;

- Bass gain and cutoff frequency of tone control are changed according to the parameter value.
- Treble gain is changed to 0.
- Prescaling is set to –12dB to remove clipping noise.
- Tone control is enabled.

If bass boost command is received with invalid parameter value, the gains and cutoff frequencies are not changed, and tone control is disabled. If a command related to tone control is received, only the related gain or cutoff frequency is changed, and the command has no effect on the tone control enable/disable and prescaling, and the information of bass boost which is reported through HDO13 is not changed. For the tone control enable command(27h), it just enables the tone control function, and has no effect on the gains and cutoff frequencies. Tone control disable command(28h) disable tone control function, and change the bass boost status which is reported through HDO13 to FFh(disable).

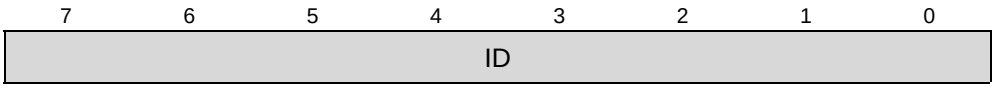
Prescaling has effect when tone control or equalizer is enabled or bass boost command is received.

Equalizer consists of 6 bands, and band1 and band6 are shelving type, band2 to band5 are peaking type. Since each band has relatively small Q value, correction matrix is automatically used to complement this small Q value whenever attenuation value is set by using EQ gain control commands(40h ~ 45h). It is not recommended that gain difference of neighbor bands exceeds 10dB.



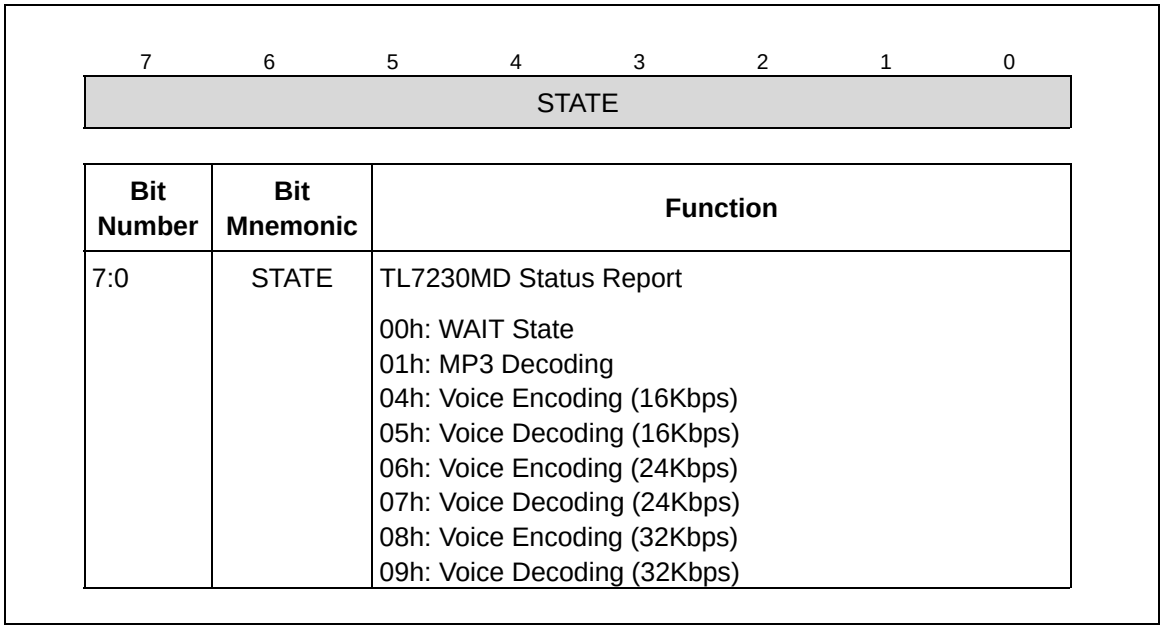
Bit Number	Bit Mnemonic	Function
3	S3	When set, it means that host wrote parameter to HDI3 register, but it isn't read by TL7230MD.
2	S2	When set, it means that host wrote parameter to HDI2 register, but it isn't read by TL7230MD.
1	S1	When set, it means that host wrote command ID to HDI1 register, but it isn't read by TL7230MD.
0	S0	When set, it means that host wrote command to HDI0 register, but it isn't read by TL7230MD.

Figure 4. HDI Status Reported through HSR4



Bit Number	Bit Mnemonic	Function
7:0	ID	Serial ID Number

Figure 5. Command ID reported through HDO0



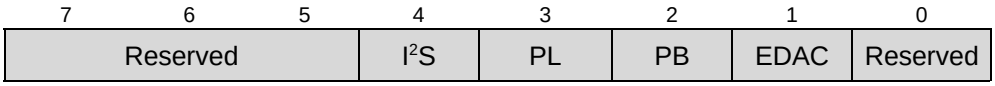
Bit Number	Bit Mnemonic	Function
7:0	STATE	TL7230MD Status Report 00h: WAIT State 01h: MP3 Decoding 04h: Voice Encoding (16Kbps) 05h: Voice Decoding (16Kbps) 06h: Voice Encoding (24Kbps) 07h: Voice Decoding (24Kbps) 08h: Voice Encoding (32Kbps) 09h: Voice Decoding (32Kbps)

Figure 6. TL7230MD Status reported through HDO1

7	6	5	4	3	2	1	0
Reserved				DE	MU#	SF	

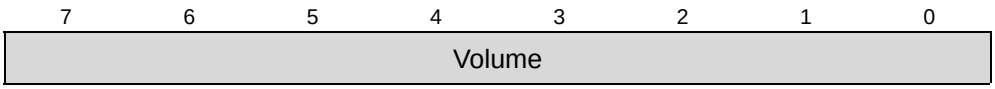
Bit Number	Bit Mnemonic	Function
3	DE	Deemphasis Enable: When set, deemphasis is enabled. Reset value is 0.
2	MU#	Mute Enable: When cleared, mute is on. Reset value is 0.
1:0	FS	Sampling Frequency: During MP3/voice decoding, it shows the sampling frequency of bit stream. DACLRCK is set as follows: 00: 44.1KHz 01: 48KHz 10: 32KHz 11: not used During voice encoding, it shows the sampling frequency of bit stream. ADCADEN# is set as follows: 00: not used 01: not used 10: not used 11: 8KHz Reset value is 00.

Figure 7. I/O Status reported through HDO2



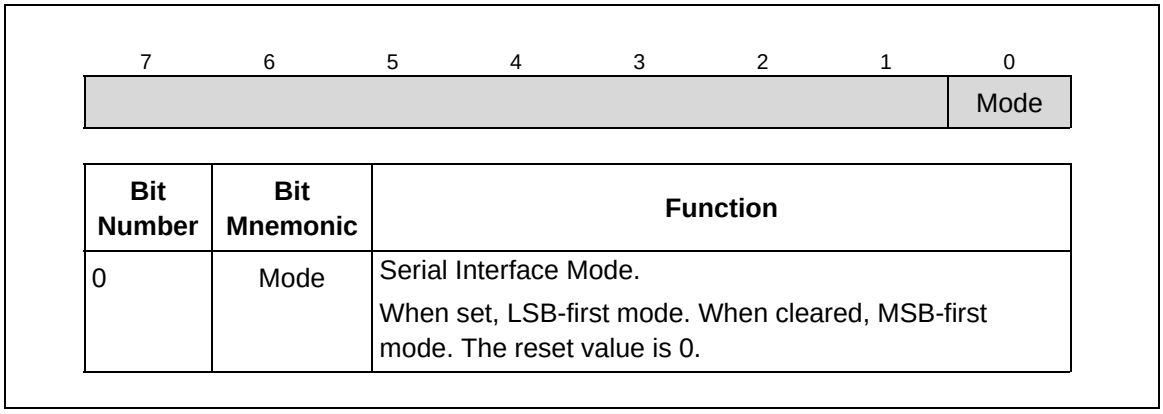
Bit Number	Bit Mnemonic	Function
4	I^2S	I^2S Format Enable: When set, I^2S format (1 bit delay), When cleared normal PCM format. Reset value is 0.
3	PL	Polarity of DACLRCK: When cleared, left channel data is sent through DACSDATA during LRCK=0. When set, right channel data is sent through DACSDATA during LRCK=0. Reset value is 0. (Refer Figure17.)
4	PB	Polarity of DACBCK: When cleared, DACSDATA has valid data between falling edges of DACBCK. When set, DACSDATA has valid data between rising edges of DACBCK. (Refer Figure17.) Reset value is 0.
1	EDAC	External DAC Enable: When set, external DAC is used. Reset value is 0.

Figure 8. I/O Status reported through HDO3



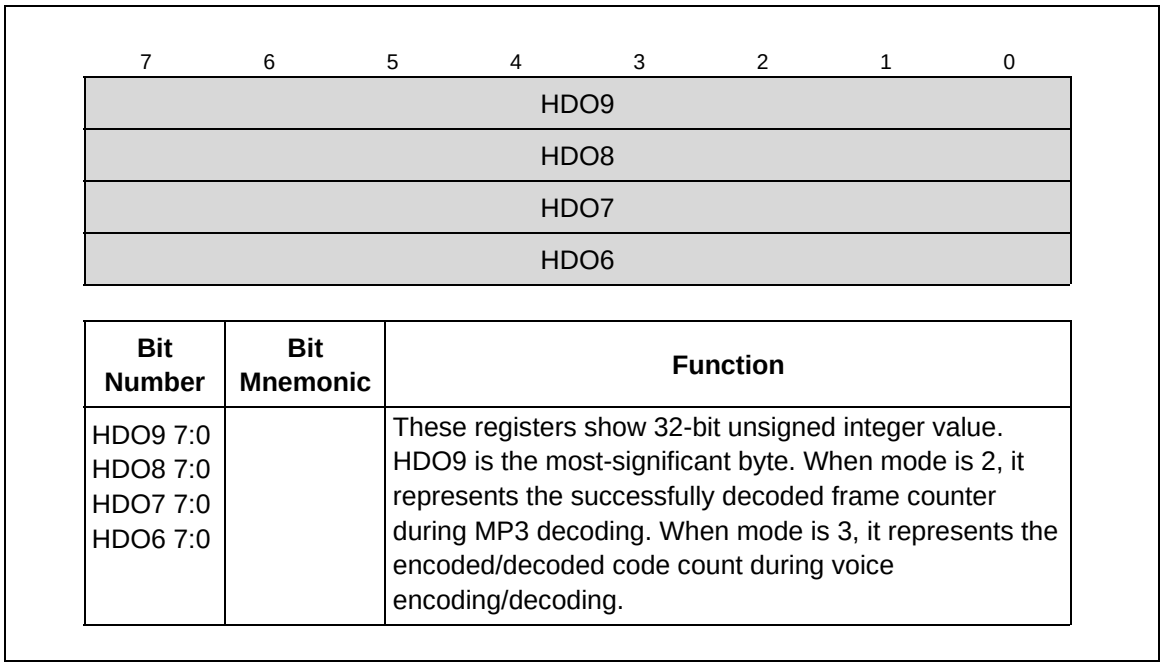
Bit Number	Bit Mnemonic	Function
7:0	Volume	The value can be 0 to 200.

Figure 9. Command ID reported through HDO4



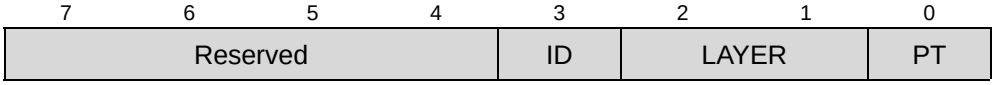
Bit Number	Bit Mnemonic	Function
0	Mode	Serial Interface Mode. When set, LSB-first mode. When cleared, MSB-first mode. The reset value is 0.

Figure 10. Serial Interface Mode reported through HDO5



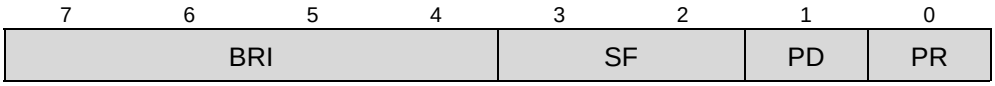
Bit Number	Bit Mnemonic	Function
HDO9 7:0 HDO8 7:0 HDO7 7:0 HDO6 7:0		These registers show 32-bit unsigned integer value. HDO9 is the most-significant byte. When mode is 2, it represents the successfully decoded frame counter during MP3 decoding. When mode is 3, it represents the encoded/decoded code count during voice encoding/decoding.

Figure 11. Count Value reported through HDO6 ~ HDO9



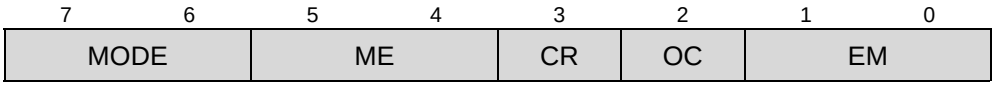
Bit Number	Bit Mnemonic	Function
3	ID	0: Reserved 1: ISO/IEC standard 11172-3 audio (MP3)
2:1	LAYER	00: Reserved 01: Layer3 10: Layer2 11: Layer1 TL7230MD decodes only layer3 bit stream.
0	PT	Protection Bit: 0: CRC Protection 1: No CRC Protection

Figure 12. Frame Header reported through HDO10 when mode is 2.



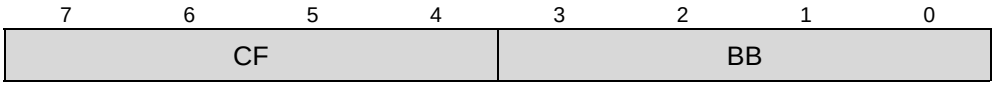
Bit Number	Bit Mnemonic	Function
7:4	BRI	Bit Rate Index: 0000: Free 0001: 32Kbps 0010: 40Kbps 0011: 48Kbps 0100: 56Kbps 0101: 64Kbps 0110: 80Kbps 0111: 96Kbps 1000: 112Kbps 1001: 128Kbps 1010: 160Kbps 1011: 192Kbps 1100: 224Kbps 1101: 256Kbps 1110: 320Kbps 1111: Forbidden
3:2	SF	Sampling Frequency: 00: 44.1KHz 01: 48KHz 10: 32KHz 11: Reserved
1	PD	Padding Bit 0: No Padding Bit 1: One Padding Bit
0	PR	Private Bit Bit for private use.

Figure 13. Frame Header reported through HDO11 when mode is 2.



Bit Number	Bit Mnemonic	Function
7:6	MODE	Audio Channel Mode: 00: Stereo 01: Joint Stereo (Intensity Stereo and/or MS Stereo) 10: Dual Channel 11: Single Channel
5:4	ME	Joint Stereo Coding Method: 00: Neither Intensity Stereo nor MS Stereo 01: Only Intensity Stereo 10: Only MS Stereo 11: Both Intensity Stereo and MS Stereo
3	CR	Copyright: 0: No Copyright 1: Copyright Protected
2	OC	Original/Copy: 0: Copy 1: Original
1:0	EM	Type of Deemphasis: 00: None 01: 50/15 microseconds 10: Reserved 11: CCITT J.17 DACDEEM of TL7230MD becomes active if deemphasis is needed without relation to deemphasis type.

Figure 14. Frame Header reported through HDO12 when mode is 2



Bit Number	Bit Mnemonic	Function
7:4	CF	Cutoff Frequency: The value can be in the range of 0 to 6.
3:0	BB	Base Boost Value

Figure 15. Bass Boost Status reported through HDO13 when mode is 2.

DAC

TL7230MD supports the external DAC interface. To use the external DAC, system user should use HIP command(15h). The interface format of DAC can be configured through HIP commands(16h or 8xh) shown in Table 5.

External DAC Interfaces

TL7230MD supports eight external interface formats. Three of them, for example, are shown in Figure 16. The interface can be configured through HIP commands. The frequency of DACBCLK is 32 times of that of DACLRCK. When voice decoding, only 32KHz of DACLRCK of is used.

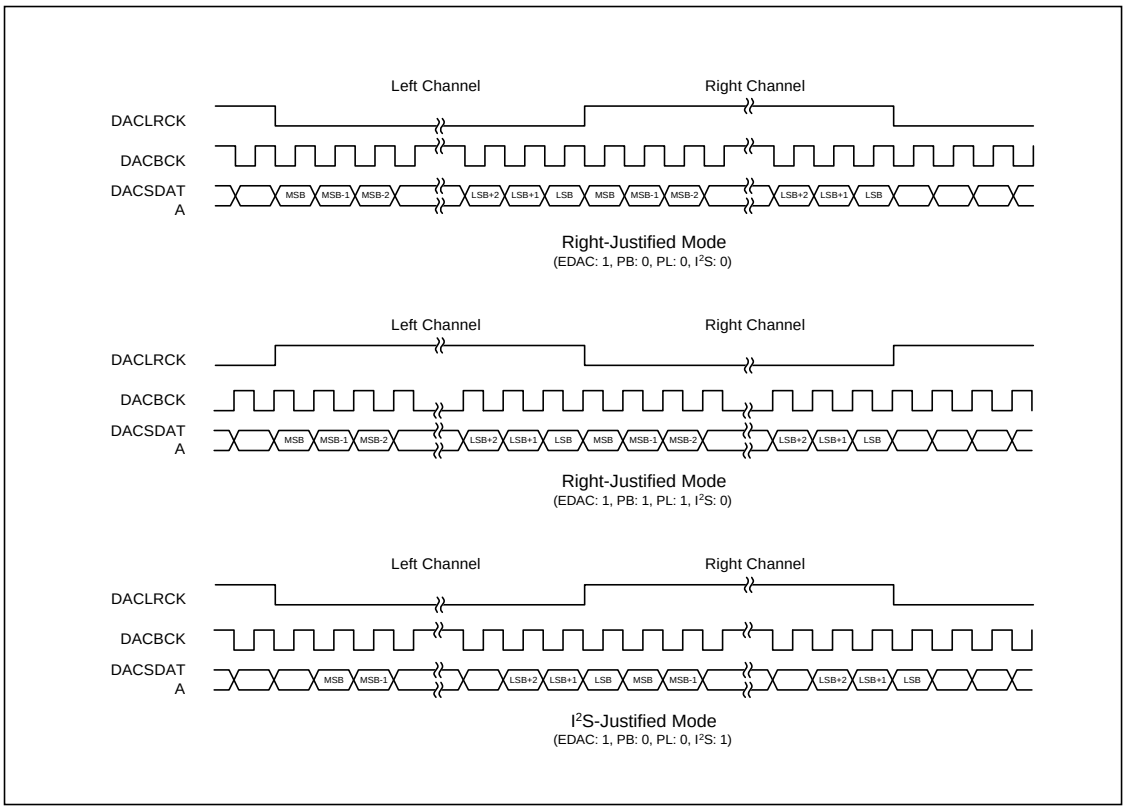


Figure 16. Examples of External DAC Interfaces

ADC

The internal ADC of TL7230MD is 12-bit resolution ADC. It is recycling type ADC with sample-and-hold function. The analog input ADCAIN should be single-ended type with the range from ADCREFP to ADCREFN. This ADCAIN voltage follows reference voltage range fundamentally. So, if user wants to alter the input range, the voltage value of ADCREFP should be changed. But ADCREFP should be greater than 2.0V. The characteristic of Internal ADC is shown Table 7. When using internal ADC, the circuit in Figure 17 is recommended.

Table 7. Characteristics of Internal ADC

PARAMETER	MIN	TYP	MAX	UNITS
THD		74.3		dB
SNR		64.9		dB
SNDR		64.4		dB

(ADCVDDD/ADCVDDA=3.0V, ADCAIN=8KHz)

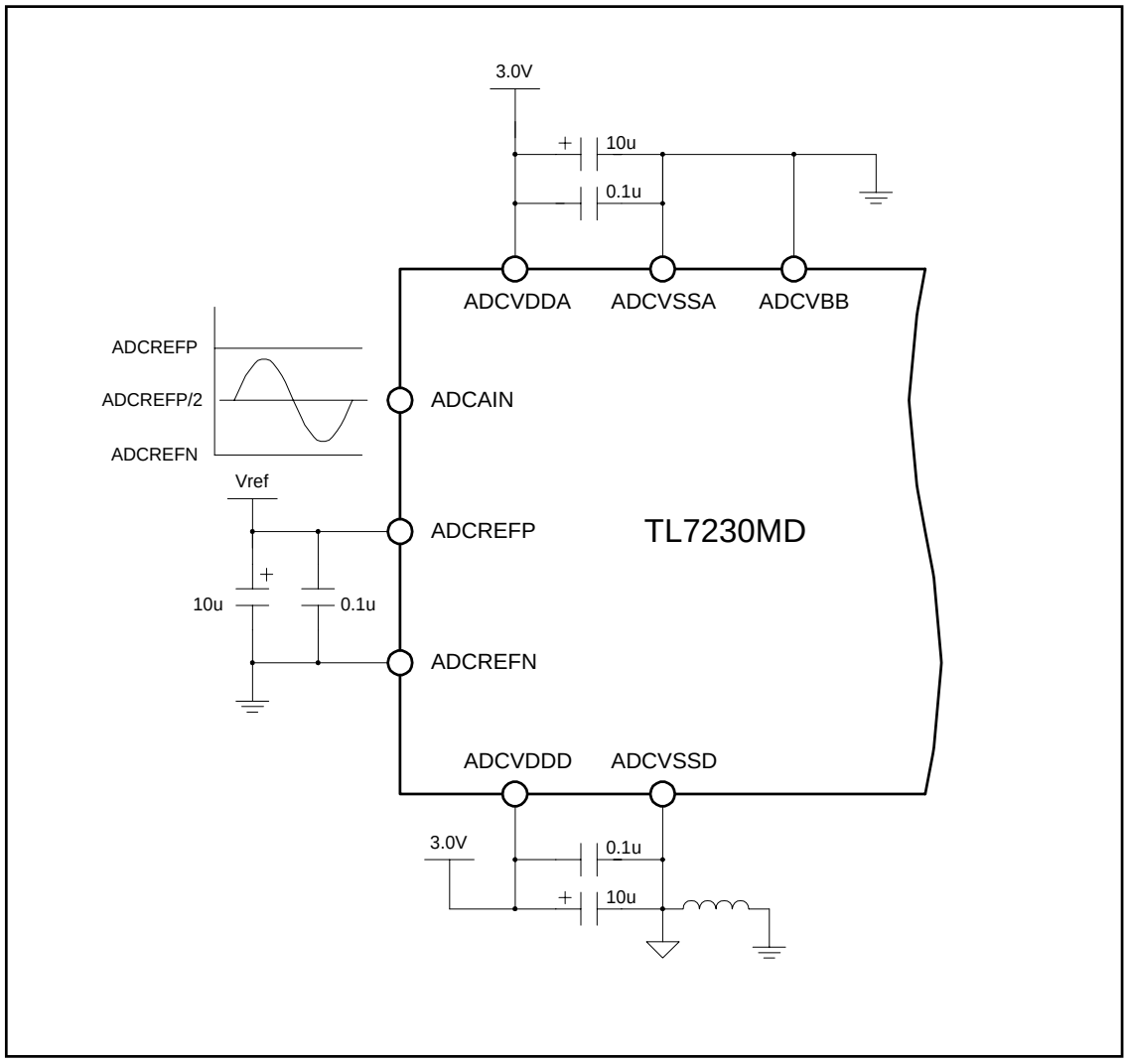


Figure 17. Reference Circuit when using internal ADC

Voice Record/Playback Function

TL7230MD records voice data from ADC in 8kHz sampling rate. There are three compression modes according to bit rates of compressed data: high quality (32Kbps), medium quality (24Kbps) and low quality (16Kbps). In high quality mode, relatively large bits are allocated for compressed data to achieve high quality of the sound. In low quality mode, smaller bits are allocated to record much more samples in the same size of storage media. Medium quality mode gives tradeoff between high and low quality modes. Compressed codes are byte-aligned and transmitted to host MCU through the serial port.

In playback the codes are uncompressed to PCM samples, with the compression mode in recording, and then oversampled to 32 kHz and output to DAC. Compressed codes are transmitted from host MCU through the serial interface.

Table 8 is the summary of the relation between compression modes and code size.

Table 8. Summary of Three Voice Compression Modes

COMPRESSION MODES	CODE LENGTH (BIT)	RECORDING TIME FOR 32MB STORAGE MEDIA
High Quality (32Kbps)	4	140 min.
Medium Quality (24Kbps)	3	186 min.
Low Quality (16Kbps)	2	280 min.

Lower Power Operation

TL7230MD has low-power feature that makes the processor get into very low-power dormant states through hardware or software control. The power saving scheme is explained with the state diagram of TL7230MD shown in Figure 18.

RUN

In this state, TL7230MD decodes MP3 or compressed voice bit stream, or encodes voice signal. Also in this state it can process other HIP commands such as 20h and 21h. HIP command 01h, 04h through 09h, and 0Fh should not be used in this state. TL7230MD consumes normal power at this state, it processes all internal functions and drives external pads. It can transit to WAIT state with HIP command 00h. When there is no job left or it waits available data, power consumption is reduced as that of WAIT state.

WAIT

When RESET signal becomes active, TL7230MD goes into WAIT state. There it can transit to RUN, or SLEEP state. When TL7230MD is in this state, it is ready to receive any HIP commands from host. It can go into RUN state when it receives HIP commands such as 01h, 04h though 09h. Also it can process other HIP commands such as volume control (21h) etc. in this state. TL7230MD goes into this state through HIP command 00h from RUN state. When TL7230MD is in this state, only peripheral interface block consumes power. That is, internally generated peripheral clock is active but clock for the DSP core logic is not. When it receives HIP command 0Fh, it goes into SLEEP state in which more power is saved.

SLEEP

In SLEEP state, only internal analog blocks such as PLL, ADC and DAC of TL7230MD consume power. In this state, internal ADC is disabled. But PLL consumes normal operation power. In this state, TL7230MD can transit to PWRDOWN state when external PWRDN pin becomes active. Active WAKEUP signal changes its state from SLEEP to WAIT.

PWRDOWN

When TL7230MD is in SLEEP state and PWRDN signal becomes active, it transits to PWRDOWN. To make TL7230MD stay in this state, the external PWRDN signal keep its active state. When the PWRDN signal becomes inactive, TL7230MD exits from this PWRDOWN state, and then goes into SLEEP state. When it changes its state from PWRDOWN to SLEEP, this state should not be changed during minimum 150μs until internal PLL is stabilized. TL7230MD consumes the minimum power at this state because all internal logic blocks and analog blocks are power-downed.

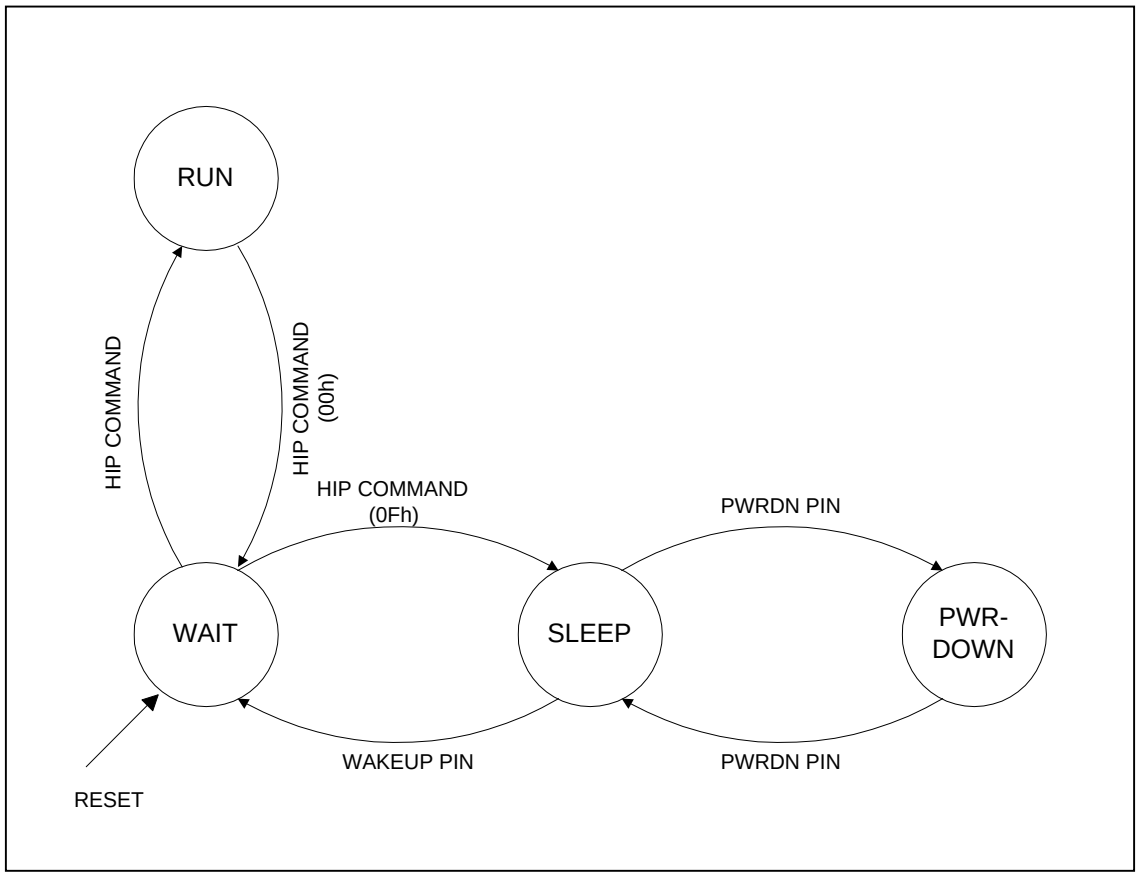


Figure 18. Decoder States and Power Management

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (See Notes)†

Symbol	Parameter	Rating	Unit
V_{DD}	DC Supply Voltage	-0.3 to 3.6	V
V_{IN}	DC Input Voltage	-0.3 to 5.5	V
I_{IN}	DC Input Current	±10	mA
T_{STG}	Storage Temperature	-40 to 125	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “DC ELECTRICAL CHARACTERISTICS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.
NOTE 2: This value was obtained under specially produced worst-case test conditions for the TL7230MD, which are not sustained during normal device operation.

DC ELECTRICAL CHARACTERISTICS (Note3)†

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	2.7	3.0	3.3	V
V_{SS}	Supply voltage		0		V
V_{IH}	High level input voltage	1.8		V_{DD}+0.3	V
V_{IL}	Low level input voltage	-0.3		0.6	V
V_{OH}	High level output voltage	2			V
V_{OL}	Low level output voltage			0.4	V
I_{IH}	High level input leakage current without internal pull-up	-10		+10	µA
I_{IL}	Low level input leakage current without internal pull-up	-10		+10	µA
I_{RN}	Supply current in RUN state	56			mA
I_{WT}	Supply current in WAIT state	21			mA
I_{SL}	Supply current in SLEEP	12			mA
I_{PD}	Supply current in PWRDOWN state	250			µA
C_{IN}	Input capacitance			4	pF
C_{OUT}	Output capacitance			4	pF
T_A	Air temperature	-40		85	°C
V_{CPUXI}	High level input voltage for CPUXI				V

† For TL7230MD, all typical values are at V_{DD} = 3.0V, T_A (air temperature) = 25°C.

NOTE 3: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by CMOS clock.

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice.

AC ELECTRICAL CHARACTERISTICS

AC Test Condition

Parameter	Value
Temperature	85°C
Supply Voltage	3.0V
Input Rise and Fall Times	2ns
Output Load	10pF

Serial port

The following table defines the timing parameters for the serial port pins. The numbers shown in Figure 19 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
1	T_{CC}	Cycle time of CLKXRM	144.7		ns
2	T_D	Delay time, CLKXRM to DXRM valid	42.2	78.4	ns
3	T_{SU}	Setup time, DXRM before CLKXRM low	1.9		ns
4	T_H	Hold time, DXRM from CLKXRM low	1.2		ns
5	T_{REQ}	Request check time, falling edge of CLKXRM to falling edge of REQSTRM	295.2	331.3	ns

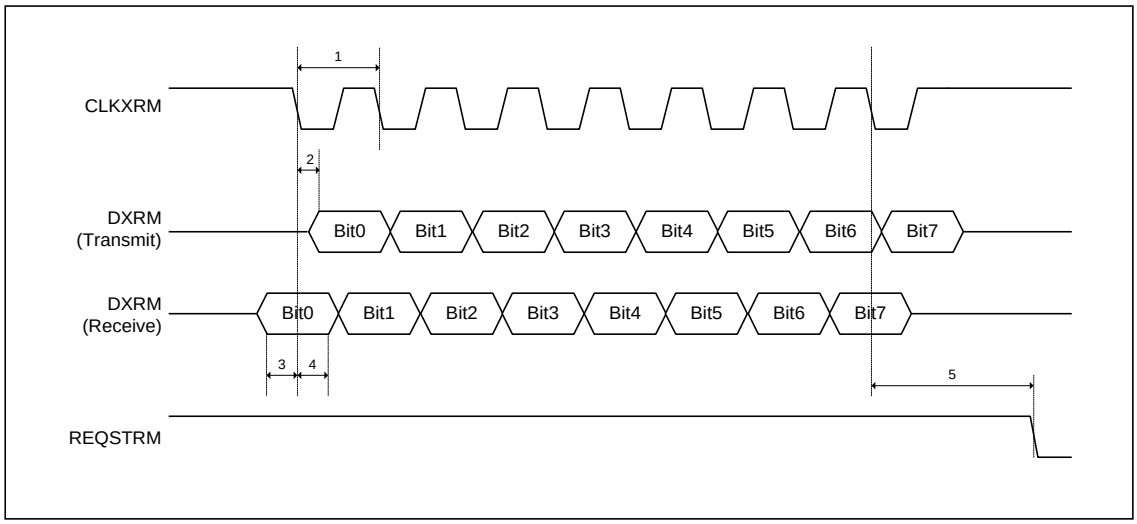


Figure 19. Timing for Serial Port in case of LSB-First Mode

Host interface Port

The following table defines the timing parameters for the Host Interface Port I/O pins. The numbers shown in Figure 20 correspond to each number in the first column of the table.

NO.	Symbol	Description	MIN	MAX	Unit
6	T_{HAW}	HALE pulse width	2.0		ns
7	T_{HDSU}	Setup time, HD address setup before HALE low	2.0		ns
8	T_{HDH}	Hold time, HD address hold after HALE low	0.8		ns
9	T_{HAS}	Start of write or read after HALE low	0.0		ns
10	T_{HDSU}	Setup time, HD data setup before end of write	0.7		ns
11	T_{HDH}	Hold time, HD data hold after end of write	2.2		ns
12	T_{HRW}	Read or write pulse width	36.2		ns
13	T_{HDE}	HD data enabled after start of read	7.8		ns
14	T_{HDD}	HD data valid after start of read	7.9		ns
15	T_{HRDH}	HD data hold after end of read	3.7	7.8	ns
16	T_{HRDD}	HD data disabled after end of read	4.2	7.9	ns

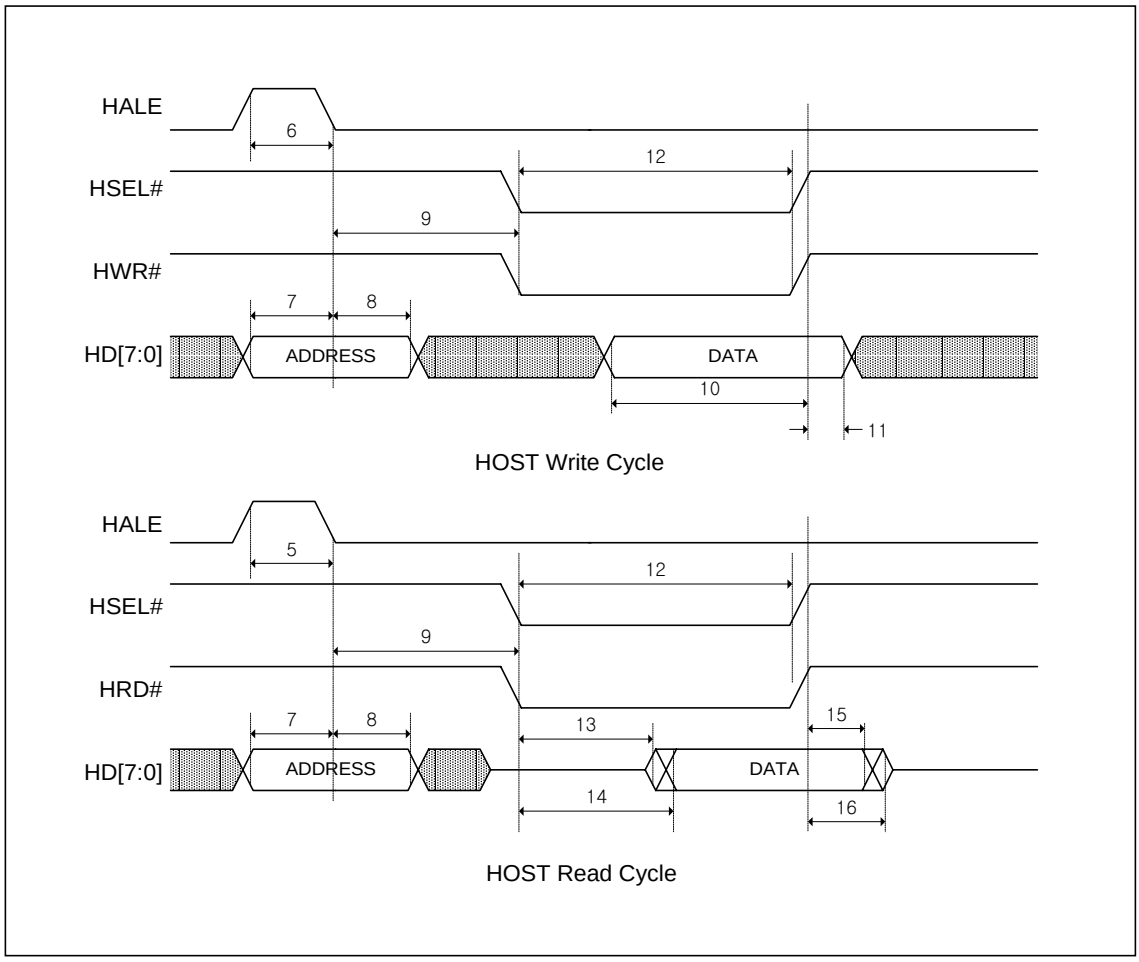


Figure 20. Timing for Host Interface Port pins

PACKAGE DIMENSION