SheevaPlug Development Kit
Reference Design

Rev 1.1

Introduction

The SheevaPlug DevKit Reference Design demonstrates the capabilities of the Marvell© high-performance MV88F6281 general purpose integrated SOC controller with CPU. Network connectivity in the SheevaPlug Development Kit is provided through Gigabit Ethernet and peripheral connectivity is provided through USB2.0

The SheevaPlug Development Kit includes the following components:

- Marvell® high-performance MV88F6281 general purpose controller with integrated CPU running at 1200 MHz
- Double Data Rate II (DDR2) SDRAM memory on board:

  Up to 4 one Gigabit x8 device -16 bit width, for a total of 512 MB running at a clock frequency of 400 MHz, data rate at 800 MHz
- Gigabit Ethernet port:

  On-board Gigabit Ethernet port on RJ-45 connector (J1) Connected to 88E1116R Marvell PHY using RGMII interface.
- USB 2.0 Interface:

  Host to Device USB adapter (J6)
- NAND Flash - 512 MB, U-boot, included Kernel, and File System
- RS-232 COM port connector by UART FDT2322D adapter via a mini USB connector.
- ARM-compliant JTAG connector , also via a mini USB connector

Shipping Contents

The SheevaPlug Development Kit package is shipped with the following components:

- One SheevaPlug including the SheevaPlug board and Debug adapter
- USB Cable
- Ethernet Cable
- CD containing software and documentation
- North American Power Cord (7A/125V)

The power cord can be used instead of the A/C plug on the SheevaPlug.

To remove the A/C plug, the suggested method is to hold the SheevaPlug with both hands, with the A/C plug facing you and away from you. Use both your thumbs to press the plastic just below the prongs and push down and away.

Related Documentation

. *88F6281, 88F6192, and 88F6180 Functional Specifications*
(Document Number MV-S104860-00)

. *88F6192 Hardware Specifications* (Document Number MV-S104987-00)

. *SheevaPlug Schematic and PCB layout*

. *88F6180, 88F6192, and 88F6281 Functional Errata, Interface Guidelines, and Restrictions*
(Document Number MV-S501081-00)

Technical Support

Marvell may have updated the collateral that was shipped with this product. Contact your local sales representative or FAE for updates. This collateral information includes the following: Assembly, BOM, and schematic and monitor source code.

Section 1 Overview

1.1 SheevaPlug description.

The main board components are detailed in Figure 1. 1

Figure 1.1: SheevaPlug board Components and JTAG adapter card

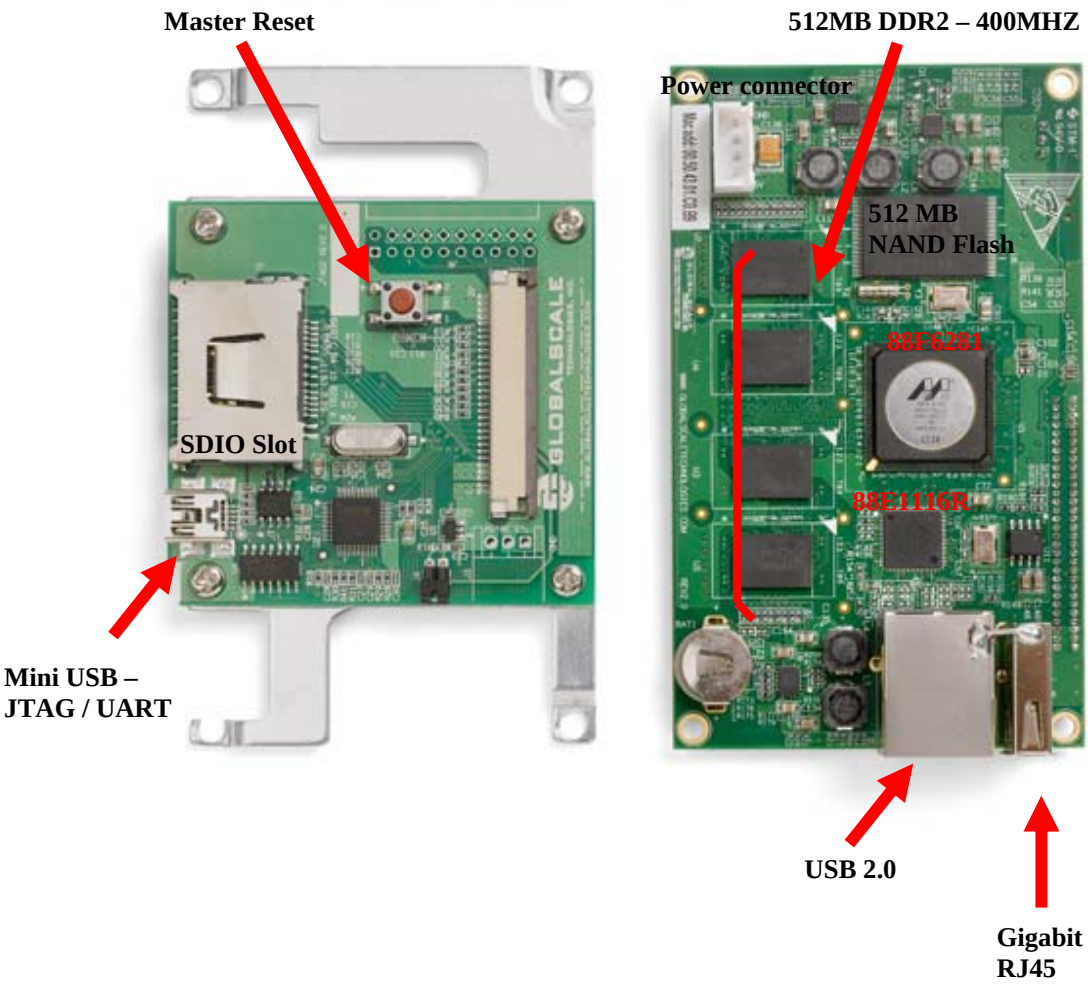


Figure 1.2: SheevaPlug and JTAG inside the box

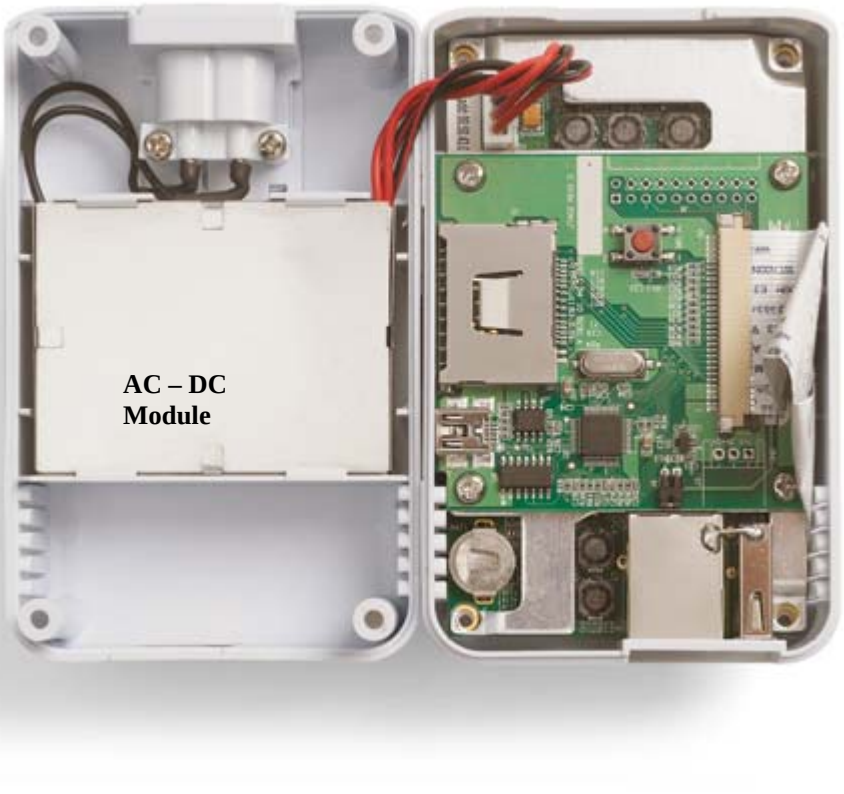


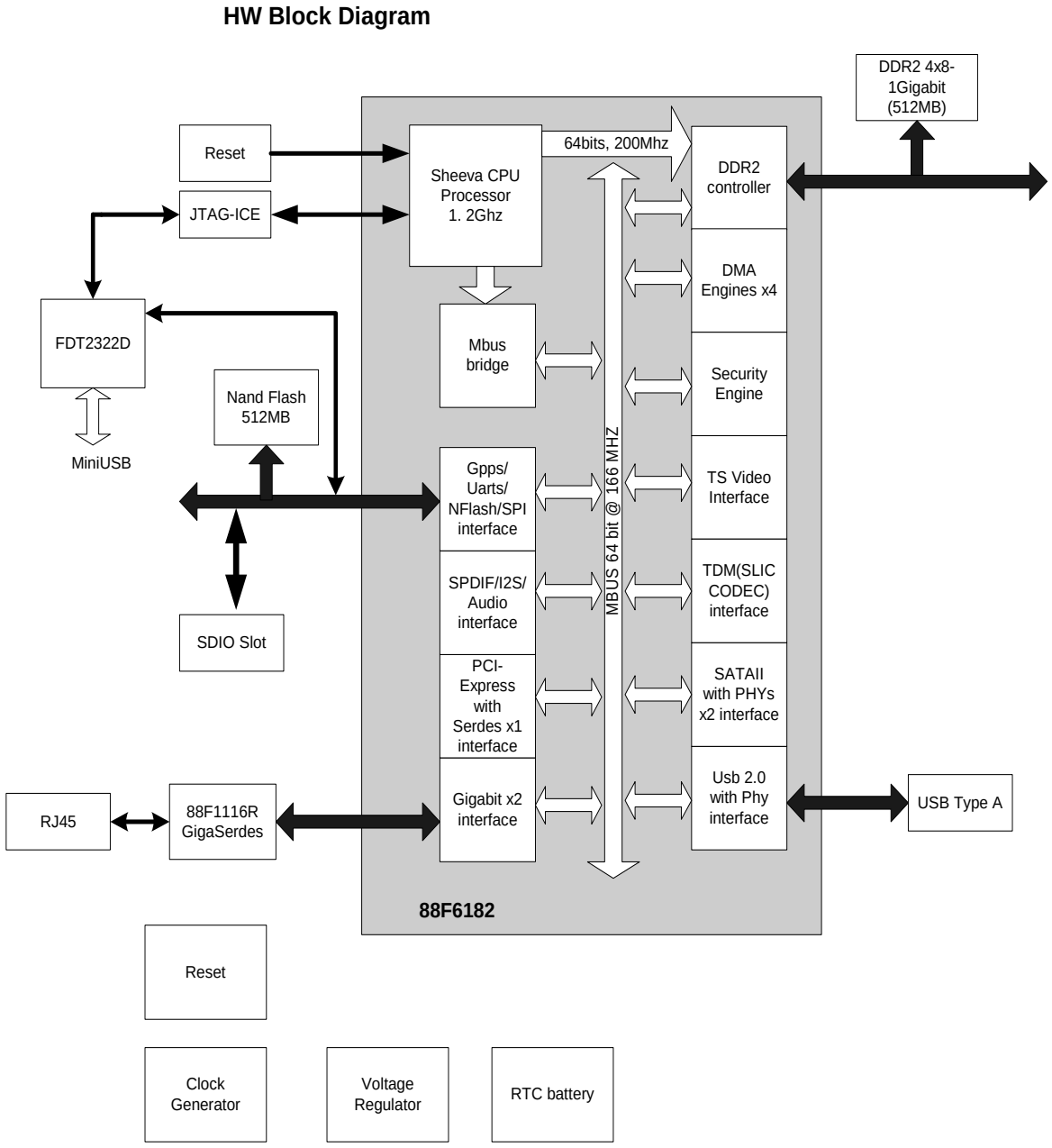
Figure 1.3: Front Panel

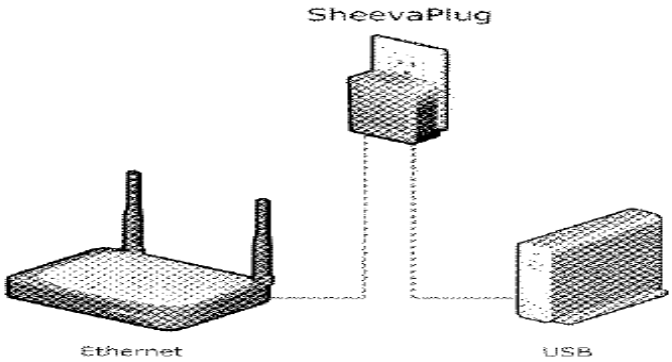
Figure 1.4: side Panel

Figure 1.5: Bottom Panel

Figure 1.6: Side Panel

Figure 1.7: Block Diagram





Section 2 Setting up the SheevaPlug Development Kit Board

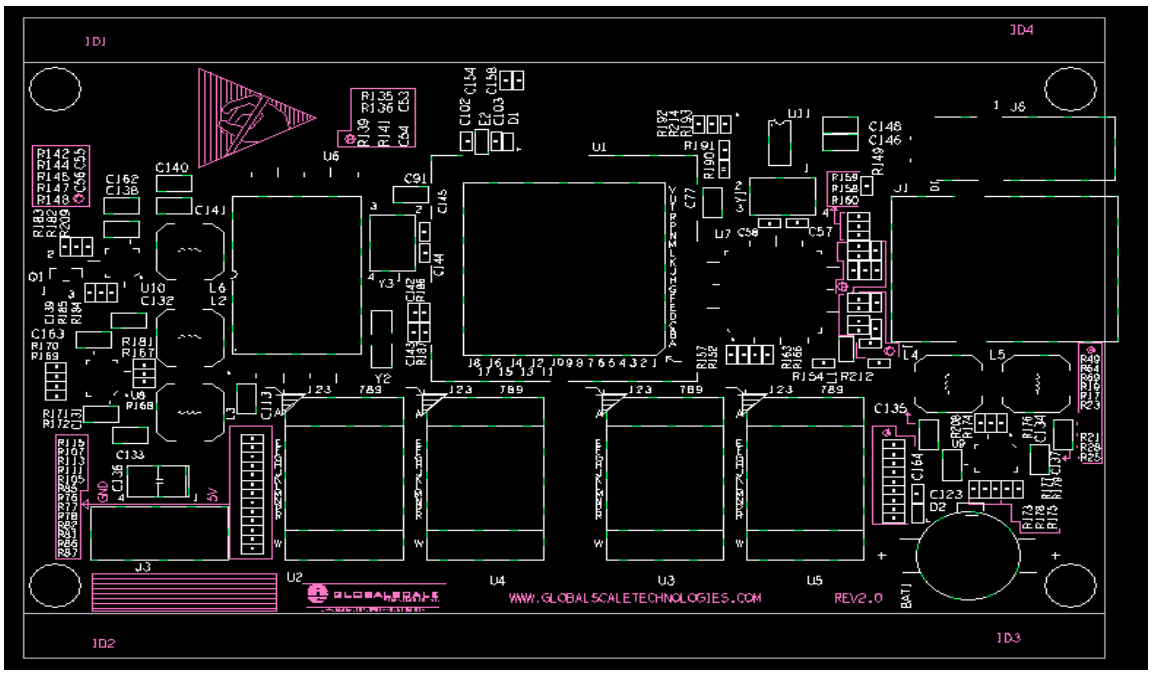
2.1 Requirements

Requirements in order to set up the plug board are:

- The SheevaPlug itself
- AC power plug or AC cord
- USB cable type A to min B (UART and Open OCD connection)
- Ethernet connection

2.2 Layout

Figure 2-1 shows the layout of the SheevaPlug board



2.3 Jumper Settings

There is no jumper setting for this board. The processor clock is running at 1.2 GHz, DDR2 clock frequency is 400 MHz, and TCLK is 200MHz internally.

2.4 AC Power Consumption

TBA

2.5 DC Power Consumption

The processor consumed ~ 2 Watt MAX

2.6 Dimensions (L x W x D)

The case dimension is 4” x 2.5 “x 2”

2.7 Power requirement

AC power requirement is 110V/220V input current: 50mA MAX

2.8 Drive Connection

USB 1.1 or USB 2.0 are supported

2.9 Network Connection

Ethernet connections supported 10/100/1000 Mb/sec

Section 3 Circuitry Description

3.1 Top Level

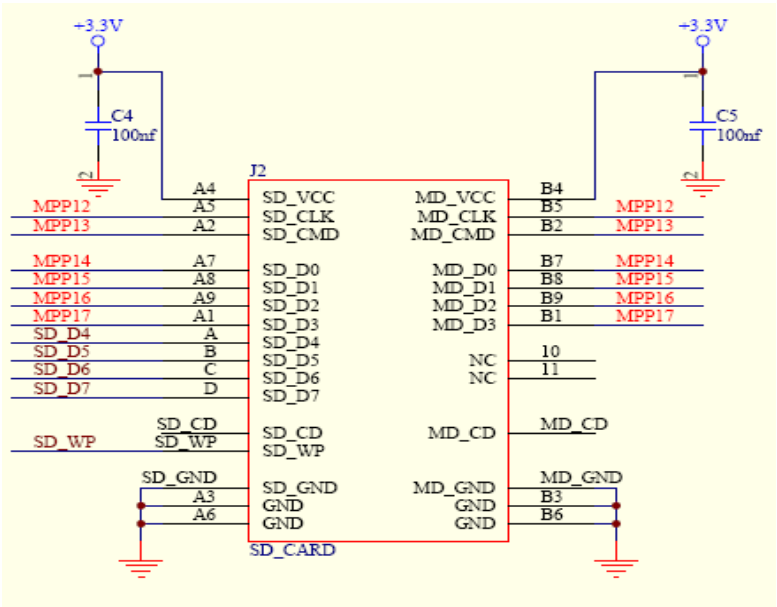
The top level schematic is in Appendix A - Schematics. It depicted the blocks in details and how they are connected.

3.2 Processor

The 88F6281 is a high performance processor, low power consumption, and embedded full useful features. The processor is packaged in a HSBGA 288 pin footprint; descriptive part numbering is 88F6281-0A-BIA2C120

3.3 IO expansion

The I/O expansion connector is a SDIO type. It’s available to user in the SDIO format or as a general purpose I/O lines. Both VDD and GND pins are connected to slot as provided in a pre-defined SDIO form factor and can be leveraged by other designs to provide additional functionalities such as WIFI or SD MEMORY CARD. See figure 1.2 for details SDIO slot location. Circuit below illustrated the SDIO pins assignment and MPP pins assignment.



MPP12: SD_CLK
MPP13: SD_CMD

MPP [14..17] : SD_D0..D3

Note: MPP [12..17] can be used for general purposes IO if SDIO is not needed.

3.4 External bus Interface

3.4.1 NAND Flash memory

88F6281 uses a single NAND 4Gigabit density (X8) Flash device to provide 512 MBYTES FLASH memory. The NAND flash device is accessible through a glueless NAND interface controller built in the 88F6281 processor. The interface controller can support boot strap sequence accesses on page 0 from the device. See Application Note AN-265 Booting from NAND Flash for detail information.

3.4.2 DDR2 Memory

The 88F6281processor can supported up to 4 banks of memory, each bank can support up to a maximum of 512MB address space; SheevaPlug board used only 2 banks of 256MB to provide a total of 512 MB. The board DDR2 banks are accessible through a DDR2 interface and using CS0# and CS1# chip select decoder feature of the 88F6281 DDR2 interface.

88F6282 processor can support any of DDR2 type devices as follows: 256Mb (32Mx8 or 16Mx8), 512Mb (64Mx8 or 32Mx16), 1-Gb (128Mx8 or 64Mx16) and2-Gb (256Mx8 or 128M x16)

DDR2 memory interface is running at 400 MHZ clock frequency and double data rate at 800 MHZ.

3.4.3 USB 2.0

88F6281 contains a Universal Serial Bus 2.0 port includes an embedded USB 2.0 PHY. The USB interface can support either Host or Device mode. The SheevaPlug design supports HOST mode only. There is no strapping provided by the SheevaPlug board to switch between HOST or DEVICE USB mode.

USB 2.0 port feature 480 Mbps, 12Mbpsm and 1.5Mbps data rate; bit stuff error detection, NRZ bit stuffing, and built in FS/HS termination signaling.

3.4.4 Ethernet

The 88F6281 has two built in two GbE controller that can supports up to four different modes; RGMII, MII, and MMII and GMII. Each port is fully IEEE 802.3 compliant 10/100/1000 Mb MAC. The SheevaPlug board used only one port RGMII MAC feature of 88F6281 processor and 88F1116R GbE PHY (Marvell Gigabit Ethernet transceiver) to provide a complete Layer-4 to Layer-0 solution for GbE connection. For details information, see Marvell Doc # MV-S104860-00 Rev.B

3.5 Power and Crystal Clocks

The board featured three crystal clocks; a 32.768 KHZ connected to the RTC low power oscillator of the 88F6281 processor and 25 MHZ connected to the 88F6281 processor master clock. The third crystal clock is also 25 MHZ connected to the 88F1116R GbE PHY device.

The 88F6281 master clock derived from 25 MHZ crystal clock depending on the strapping pins at power on sequencing. The on-chip PLL based frequency multiplier and the prescaler results in a programmable CPU clock between 800 MHZ and 1200 MHz. It's also resulted other master clocks for CPU L2 cache clock, DDR2 clock, TCK clock, SDIO clock, SPI, SMI, TWSI and Gigabit Ethernet Clock, SATA, USB, PCI-Express and PTP clocks. See 88F6281 Hardware Specification, Doc. No. MV-S104859-00

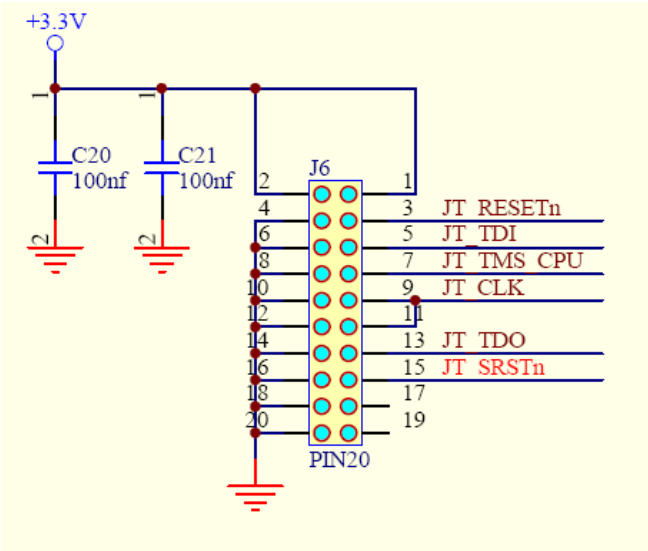
3.6 JTAG interface and reset

The board featured two alternative options to connect to JTAG; a standard 20-pin box header (J6) located in the JTAG V2 board, or via a mini USB connection feature by a FDT2322D device.

The 20 pin header enables direct connection of an ICE to the JTAG inputs to the 88F6281 processor; this is done commonly interfaced through a Lauterbach probe.

The second option is via a mini USB connection, it is a very cost effective interface for the 88F6281 JTAG via a mini USB cable, it utilizes an Open On-chip Debug codes (Open OCD), in which it's been widely used by the open source codes Linux community to develop debug capability and flash capability. You can find more details by perform a web search under the "Open OCD" or "FDT2322D" key subject.

Circuit below illustrated the JTAG direct connection from 88F6281 to J6 header.



For details JTAG connection from mini USB to 88F6281 device, see Appendix A – Schematics.

Note: In addition, SheevaPlug's processor can be reset via a pin hole on the side.

3.7 Serial Interface – Open ocd interface

The 88F6281 processor supports two UART interface. It can support FIFO or non FIFO mode. In the FIFO mode, the TX can hold 16 Bytes data from device until it is ready to transmit or vice versa for the RX direction.

The board used only one UART for serial connection featured by the 88F6281 processor. This connection is provided via a mini USB connection cable. There is no direct connection to the 88F6281 UART from USB, the TX and RX is filtered via FDT2322D device. The SheevaPlug board does not include RS232 transceiver; it's now done from the FDT2322D device conveniently.

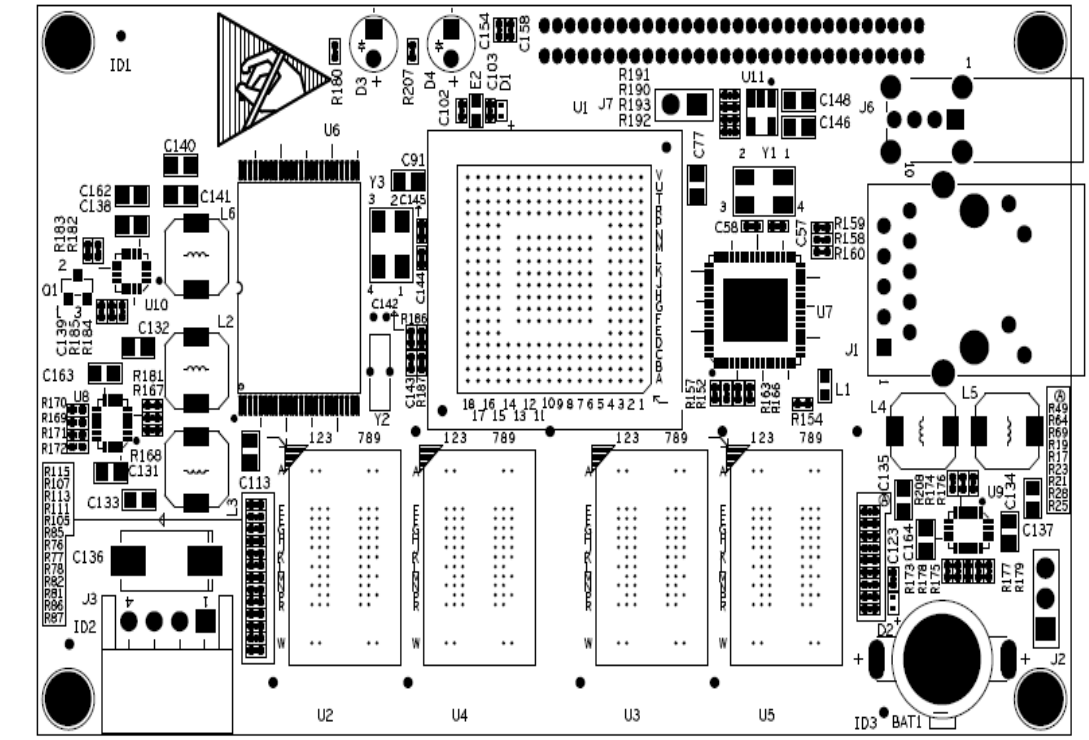
The following steps below are required in order to connect to the serial port via the FDT2322D device for Windows users.

A. Download CDM 2.04.14 driver from the SheevaPlug Marvell website or from the CD.
B. After down load it to your computer, unzip it to a folder in drive C. Once it's done, you can proceed to plug mini USB cable to the SheevaPlug box; located on the side panel – see figure 1.6 illustrations. A message will pop up and ask for the CDM driver, click "yes" in the first time when it asks for it, and point it to the folder name where the driver folder is located. You will be asked to do it second time since there are two channels; A and B on the FDT2322D device.
C. When you have successfully installed FDT2322D driver in the host computer, open up a Tera Term application or HyperTerminal application. Select the highest com port assigned by the system; for example, COM4 was assigned for channel B and COM3 for channel A. Select COM4 in the Tera Term.

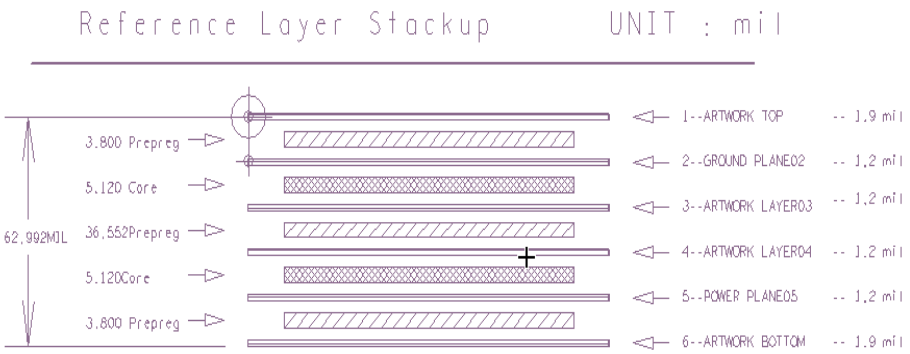
D. Display console properties are settings as follows: 115200 baud rate, 8 data bits, no parity, 1 stop bits and no flow control.
E. You might need to close and re-open the Tera Term again if the banner did not display the first time since the driver may yet have completed connections to the FDT2322 driver. If needed, you can push reset button on the side of the SheevaPlug box to get it displays message again.

3.8 Layout Drawing

The layout diagram schematic show an approximate floodplain for the board. The board is provided with four mounting holes, heat shielding, thermal filler and JATG V2 board.



3.9 SheevaPlug PCB stack up



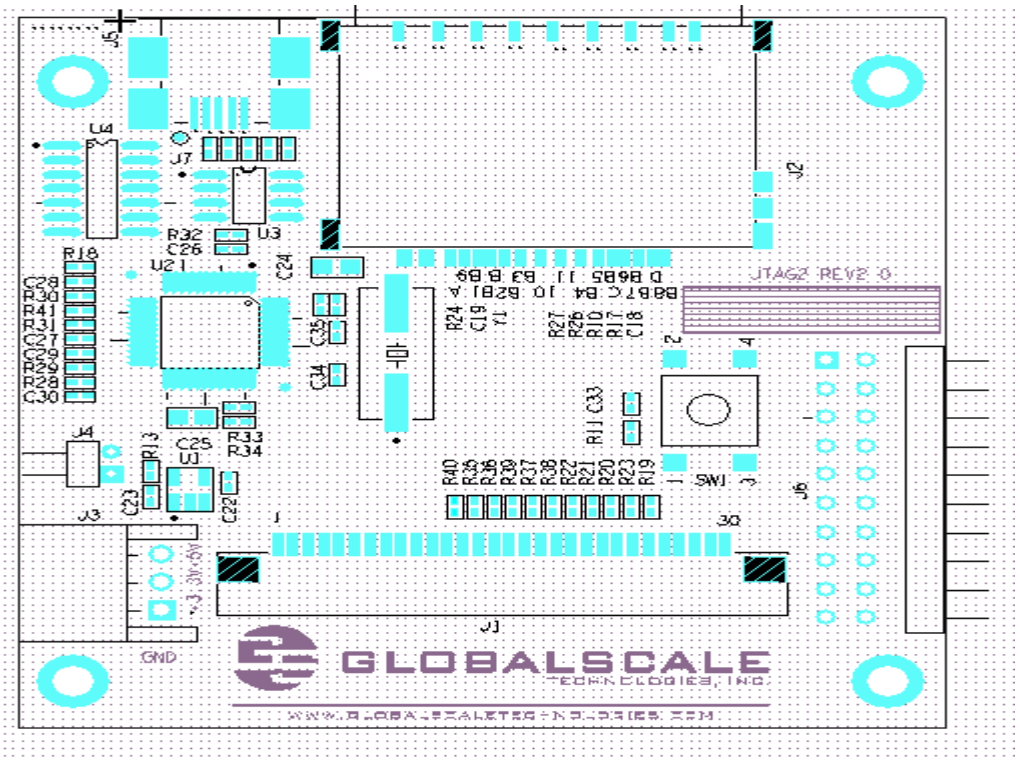
SINGLE TRACE IMPEDANCE CONTROL

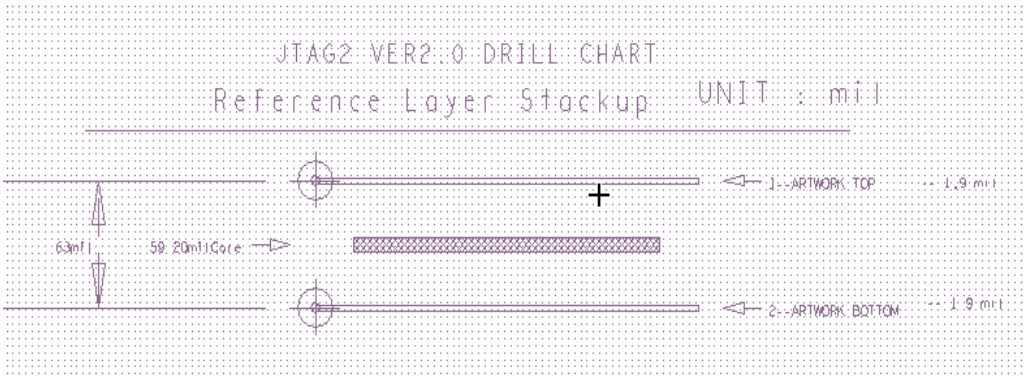
LAYER	WIDTH (mil)	IMPEDANCE (ohm)	PRECISION	FREQUENCY (MHZ)	REMARK
1 6	5	50	+/-10%	DEFAULT	
3 4	5	50	+/-10%	DEFAULT	

DIFFERENTIAL PAIR IMPEDANCE CONTROL

LAYER	WIDTH/SPACE (mil)	IMPEDANCE (ohm)	PRECISION	FREQUENCY (MHZ)	REMARK
1 6	5 1/7.8	100	+/-10%	DEFAULT	
3 4	5 1/7.8	100	+/-10%	DEFAULT	
1 6	4.5/7.8	100	+/-10%	DEFAULT	
3 4	4.5/7.8	100	+/-10%	DEFAULT	

3.10 JTAG V2 PCB drawing and PCB Stack up





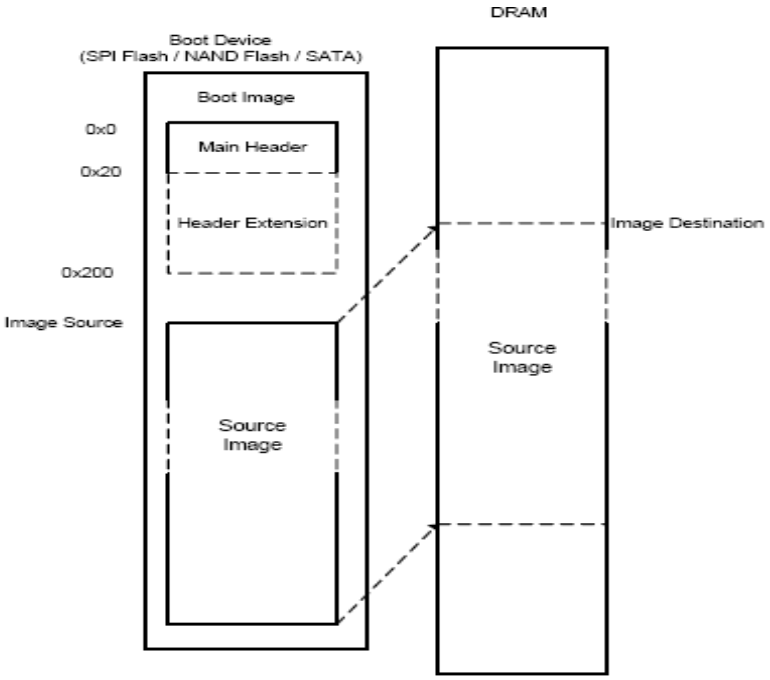
Section 4 On-board Software

4.1 Flash Memory

4.1.1 Flash Memory Organization

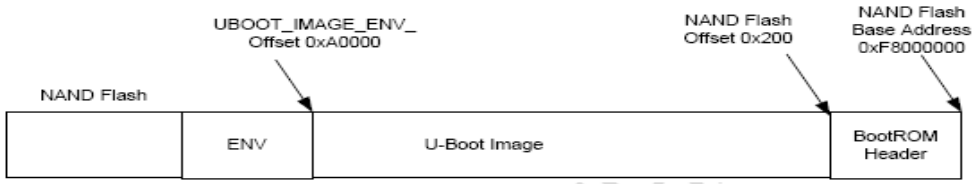
The NAND Flash memory used for 88F6281 processor is a Samsung K9F4G08U0A – 4G-bit device, organized as 262,144 pages by 2112 x 8 columns and the Spare is organized as 64x8 columns. The write and read operation are executed on a page basis, while the erase operation is executed on a block basis. Bit erase operation on the NAND Flash device is not supported. Erasable Size is 256KB blocks.

The 88F6281 processor internal boot ROM initializes the DDR2 memory according to the parameter located in the image extended header running at 0xFFFF0000. It copies the U-boot image from the NAND flash into the DRAM at location 0xF0000000 accordingly to the imager header, which is located on the first page of the NAND flash at offset 0.



4.2 Flash Write Access

The flash mapping for the image layout as follows:



Boot Software

The boot software a.k.a. U-Boot starts at the reset after it asserted low for 20 ms, and then the POR circuit is triggered. The SysRSTn stays asserted for additional 300us after the power and clocks are stable. The NAND flash performs a boot sequence during the additional 300us time to prepare page 0 ready to be read, upon completing the above sequence, the internal CPU reset is de-asserted, and CPU starts to execute boot code form the NAND device. When the reset button is pressed, the POR circuit is triggered and the whole process is started all over again.

Since the SheevaPlug board is booting from NAND Flash device, there are no optional strapping pin to support booting from other devices.

The boot sequence upon power on reset is as follows:

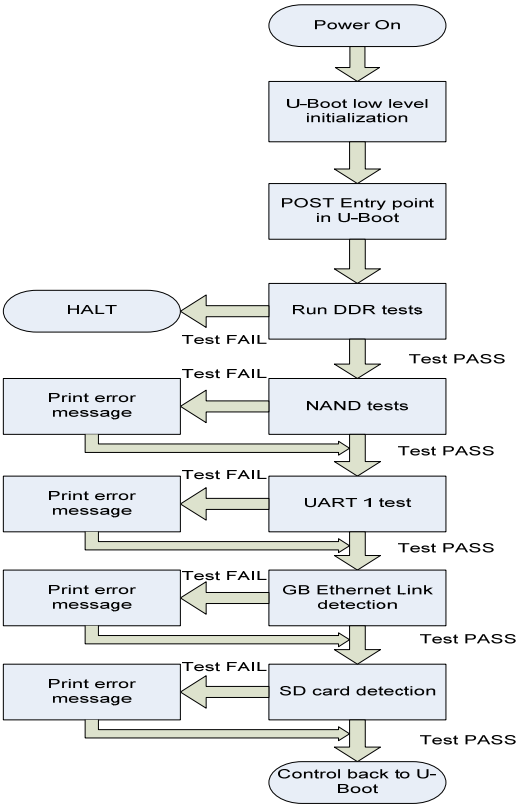
- U-Boot image is resided in the NAND FLASH – page 0
- CPU jumps to reset vector at 0xFFFF0000
- CPU executed vector code at 0xFFF9000
- CPU internal boot loader initializes register 0xF100000
- CPU internal boot loader initializes register DDRAM 0xF0000000
- CPU internal boot loader copied Flash image from 0xF0000000 to DRAM location 0xFFF90000
- CPU running codes from 0XFFF90000 location
- CPU performed system POST and display U-Boot prompt

4.3 Functional Test Software

Functional Test SW is part of the boot software that allows testing of the 88F6281 processor device. From U-Boot Monitor mode, commands are extended with extra functionality which can be useful for running diagnostic and

benchmarks. There are two types of Functional Test Software; POST and manufacturing diagnostic test.

POST testing is expected to be an application on top of Boot loader performing sanity checks to ensure that peripherals critical to SheevaPlug are checked every time platform is powered on. Manufacturing Diagnostics is expected to be application on top of Boot loader performing functional checks to ensure that peripherals on SheevaPlug are usable postproduction; such diagnostics will help contract manufacturer to perform quality control on SheevaPlug at the time of production from functional standpoints using software. Prior to loading Boot loader, contract manufacturer shall perform power supply checks as well as JTAG tests to the extent possible. In addition, contract manufacturer will have to populate SheevaPlug as per HW assembly guidelines and connect peripheral connectors essential for Manufacturing Diagnostics tests. POST flow chart test is illustrated below.



POST test will perform following checks:

- MBUS-L to MBUS Address Decoding Tests
- Cache Detection
- DDR2 Tests
- NAND Tests
- UART Tests
- GbE Tests
- SATA Detection
- PCI-Express Detection
- RTC
- USB controller initialization (No USB stack)
- SDIO detection

4.4 OS Kernel and File System

When SheevaPlug is ready to install UImage, U-Boot passes its tags list data structure to the kernel. The data structure consists of tag_mv_uboot and tag_mem. The table below illustrated the Tag list

Structure	Field	Purpose
tag_mv_uboot	Sys Clock	System Clock recognized by U-Boot
	T - Clock	T-Clock recognized by U-Boot
	Board ID	Board ID of the Board on which U-Boot is running
	U-Boot version	Current version of U-Boot
	OverEthAddr	Whether to override the MAC address in the SoC registers
	macAddr	Ethernet MAC address
	usb0Mode	Load first USB controller as a Host or as a Device
tag_mem	Memory structure	DRAM bank number and size
NOTE: For the complete list, check the include/asm-arm/setup.h. Linux must get an indication of the DRAM size either by tag_mem or through the bootcmd mem parameter.		

The steps listed here are helpful to understand how to boot a Linux Kernel from the Flash.

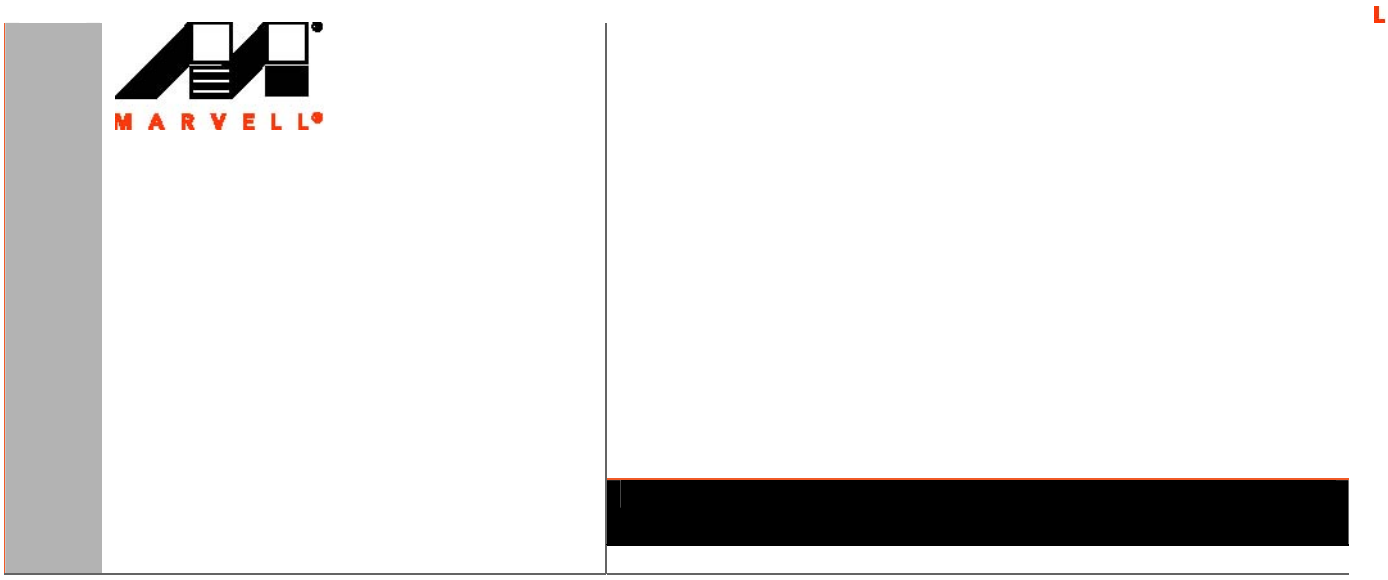
- Get on U-Boot prompt
- Under U-Boot prompt, set the following environment parameters:
  - Ipaddr = new ip address
  - Serverip = ip address of your host PC
  - Define Image namein the flash "setenv image_name /boot/uImage"
  - Set the u-Boot to booter mode "enaMonExt = no"
  - Copy the Linux image from the flash to run it "setenv bootcmd $(standalone)"
- Save these environment parameters
- Reset command or power cycle the unit

See U-boot user Manual for MV88F6281 for details Kernel and File System installation on the NAND Flash.

Section 5 Appendix A- Schematics

5.1 The following schematics are appended:

Figure 5.13 SHEEVAPLUG BOM



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