Micro-Technology

Technology

&

Applications

Outline

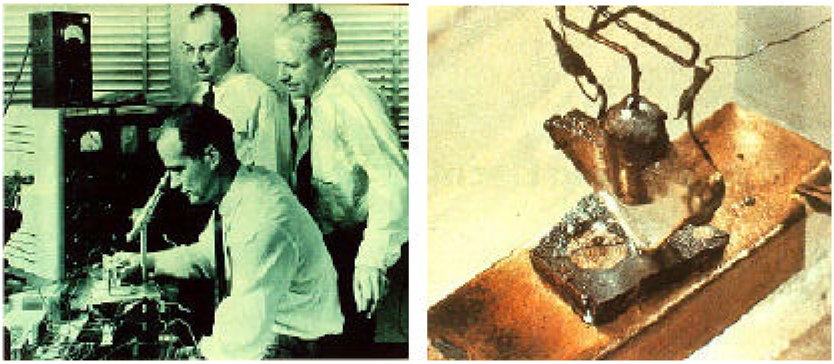
- Applications - motivation
- Micro-Technology
  - Silicon Starting Material
  - Microlithography
  - Pattern Transfer
  - Material Deposition
  - Material Modification

Applications of Micro-Technology

- Electronics
  - IC’s: CMOS, Bipolar
  - Discrete devices
  - Power Devices
- Optoelectronics
  - Imaging: CCD, CMOS
  - Lasers & LED’s
  - Photodetectors
  - Solar Cells
  - Silica Wave-guides on Si

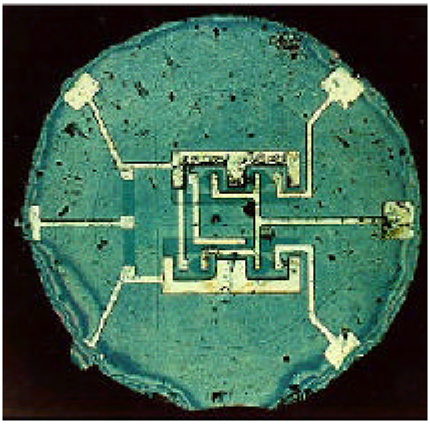
- Sensors & Actuators
  - Pressure sensors
  - Accelerometers
  - Gyroscopes
  - Micro-probes (AFM)
- Bio/chemical µ–systems
  - µTAS
  - Cell-sorting
  - DNA-chips
  - PCR-reactors
  - Katalytic reactors

The start of the Silicon Age

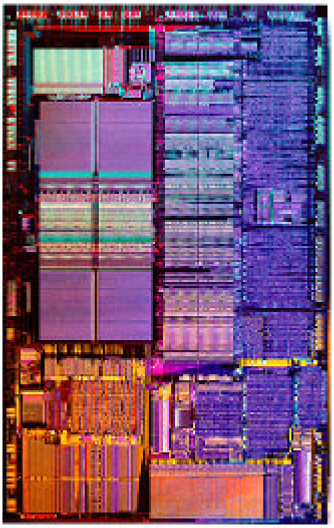


December 1947: Invention of the Bipolar Transistor
Bardeen, Brattain & Shockley

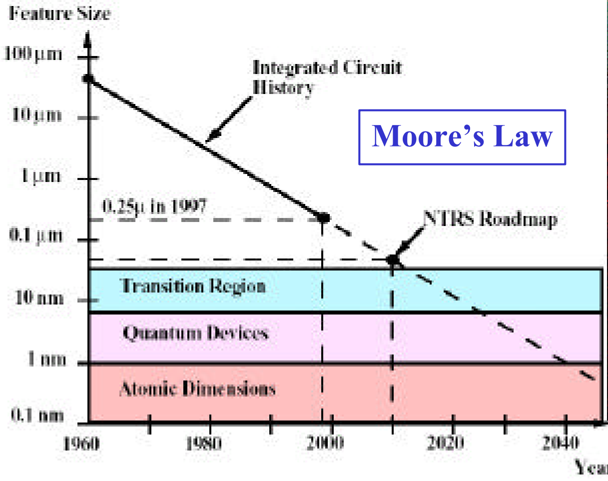
IC’s from 1960 to 2002



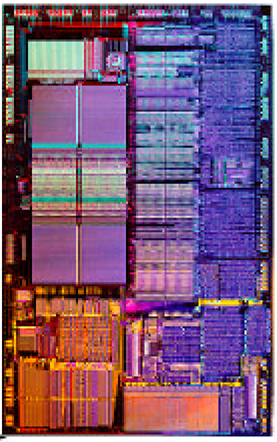
Fairchild, Gordon Moore, 1960
First planar IC.



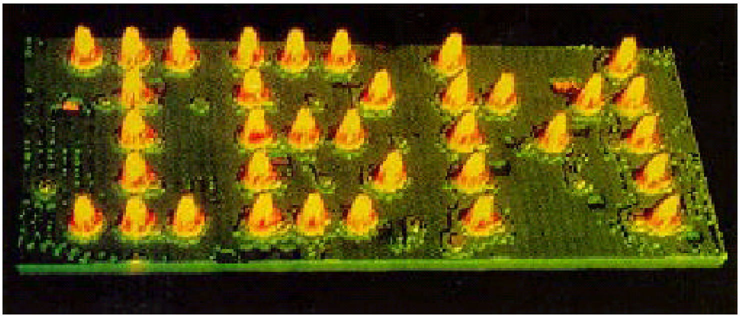
IC Technology History



Moore’s Law

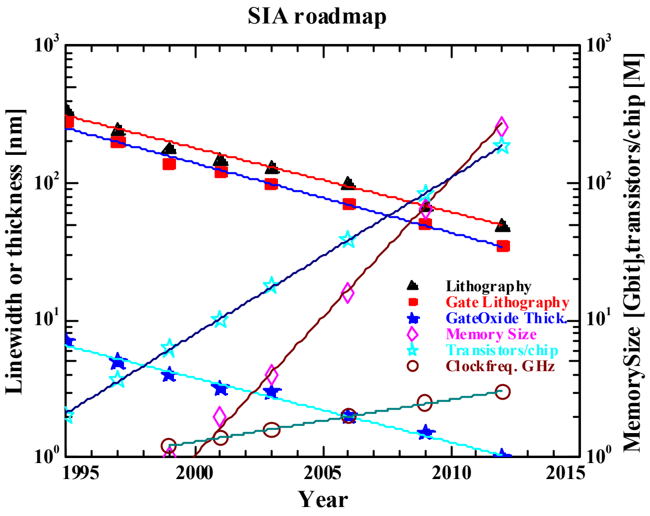


Where is the Limit?

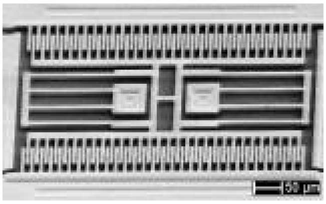


IBM 1990: STM image
STM modified surface, Xe on Silicon

Expected future Si technology

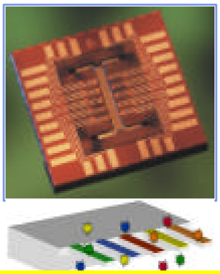


MEMS
Non-electronic Applications

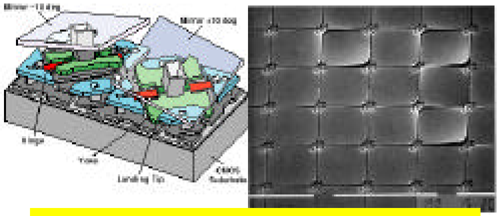


Comb drive resonator

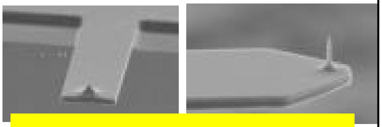
Fold-up mirror



Microcantilevers in flowchannel
Selective coating
Piezoresistive strain gauge



Mirror-array for image projection



AFM-probes-
Sharp tips on microcantilevers

Why Silicon?

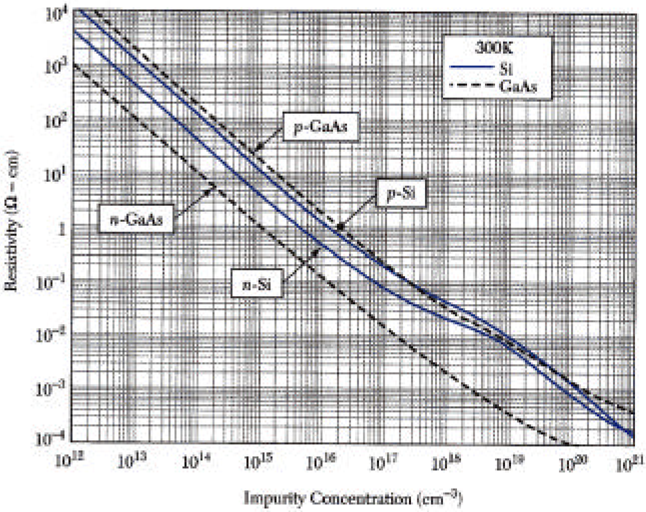
Technological properties

- Abundant element ~28%
- Simple purification
- Good crystal quality
- Strong & hard material, 7GPa
- Controllable doping
- **Good oxide SiO_2**
  - Diffusion mask
  - Dense pin-hole free dielectric
  - Good adhesion
  - Surface passivation

Physical properties

- Appropriate bandgap ~1.1eV
  - High breakdown voltage
  - No deep traps
  - Indirect-high carrier lifetime
- Reasonable mobility
  - Electrons 1400cm^2/Vs
  - Holes 500cm^2/Vs

Resistivity vs. doping density
An ”Extrinsic” material



Dopants:

Donors: **P, As, Sb**

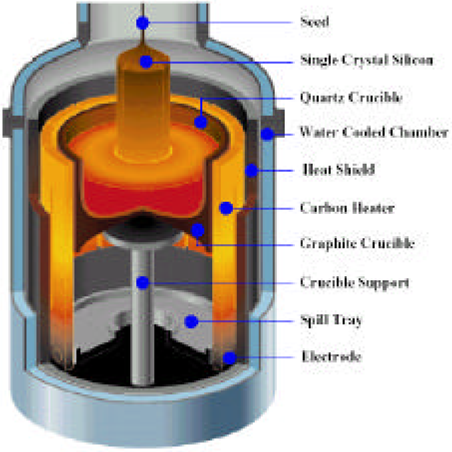
Acceptors: **B, Al, Ga**

$$r = \frac{1}{qm_n n + qm_p p}$$

$$r_n \approx \frac{1}{qm_n N_D}$$

$$r_p \approx \frac{1}{qm_p N_A}$$

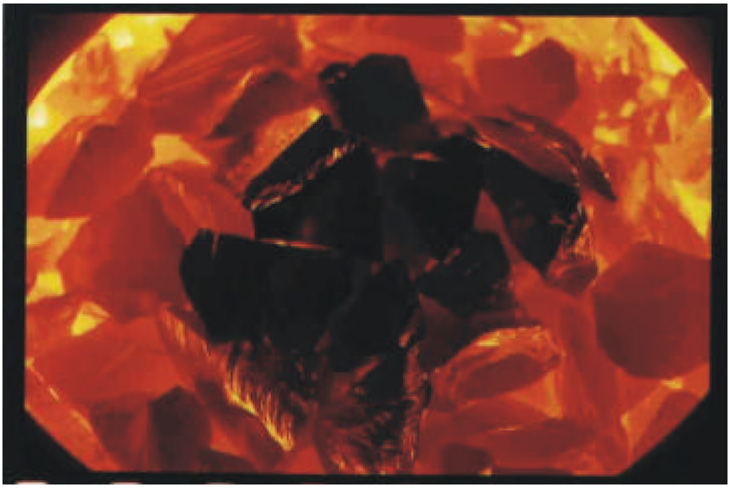
Czochralsky Crystal Growth



- Low cost
- Large diameter crystals ~300mm
- Low defect density
- Low dislocation density <100/cm^2

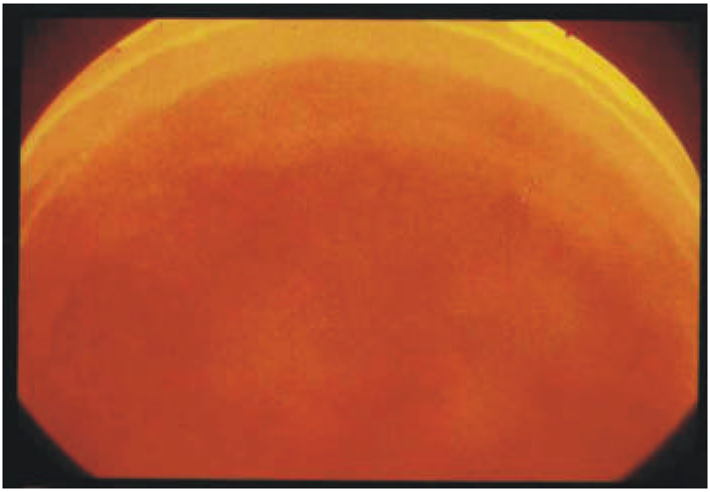
- High contamination from crucible
  - O~25ppm, C~5ppm
- Heavy metal ~ 1ppb
- Moderate resistivity <50Ωcm
- Moderate carrier lifetime 0.3ms

Heat Poly-Silicon Lumps – Melt it



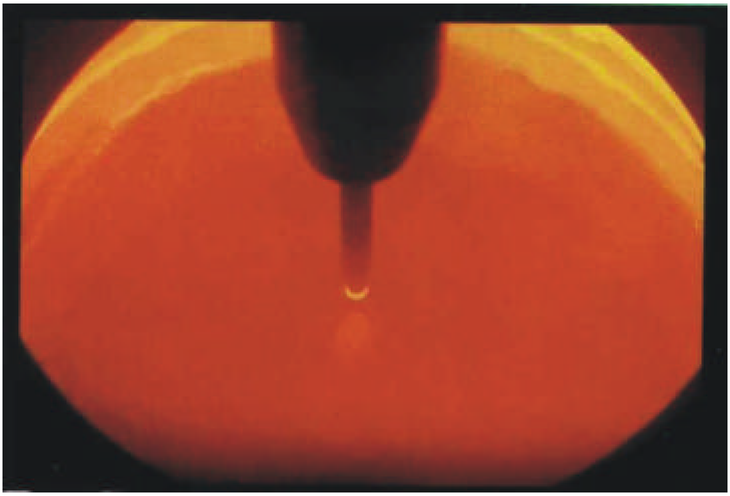
19 August 2002.
Ole Hansen MIC
Topics in Microelectronics

Molten Silicon

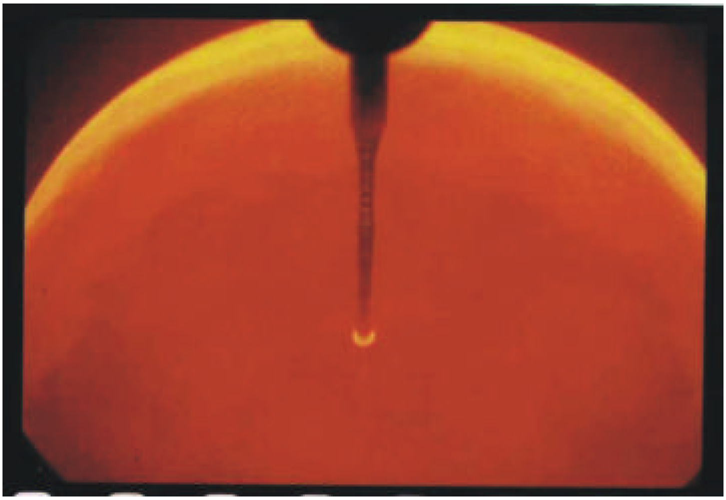


19 August 2002.
Ole Hansen MIC
Topics in Microelectronics

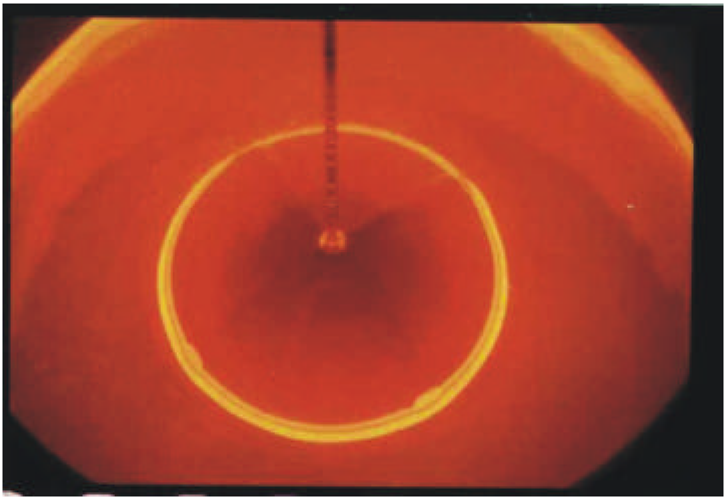
Dip Seed Crystal in the Melt



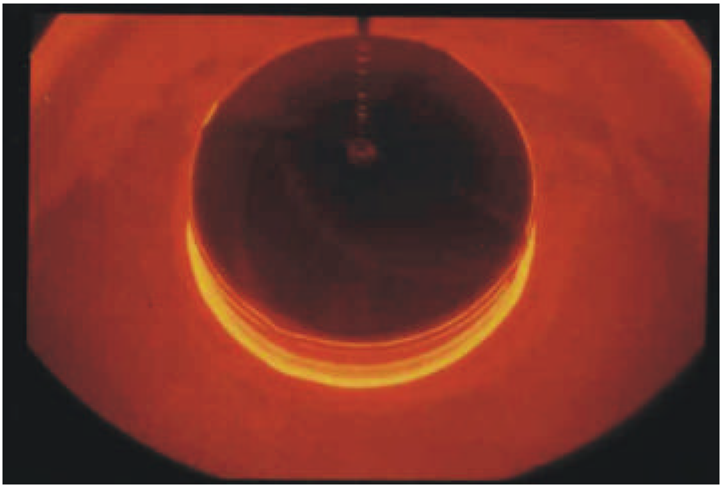
Pull Seed Rapidly
Necking – Eliminates Defects



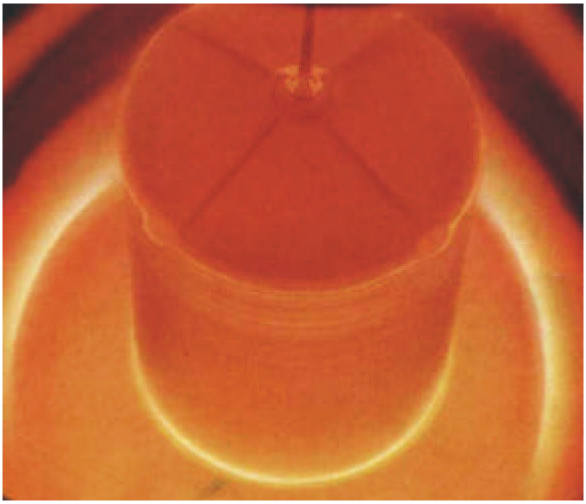
Slow Pull to Final Diametre



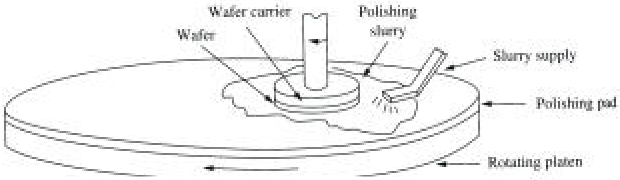
Control Pull Speed Keep Constant Diametre



Almost Finished Crystal Hanging in the Seed Crystal

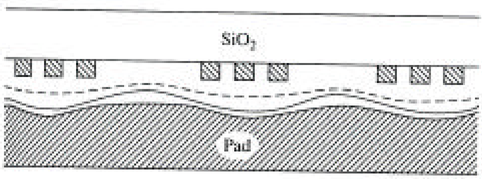


Chemical Mechanical Polishing CMP



Slurry: KOH/H_2O with 10nm Silica Particles

($KFe(CN)/H_2O$ with Alumina Particles)

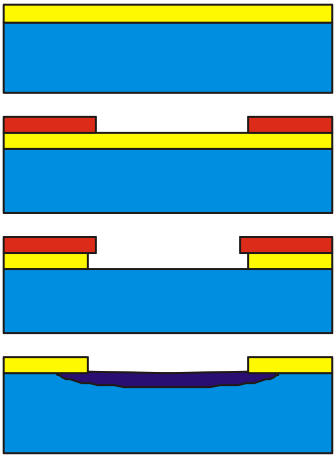


Semirigid Polishing pad: Global Planarization

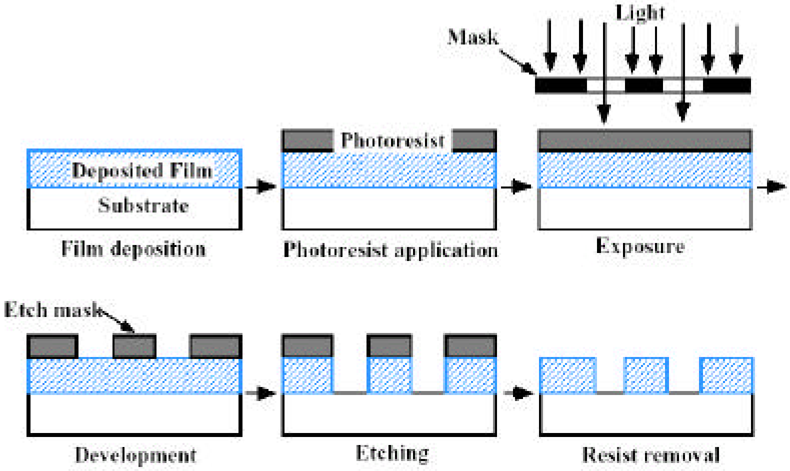
Etchrate: $R=K*p*v$

Basic Micro-Technology

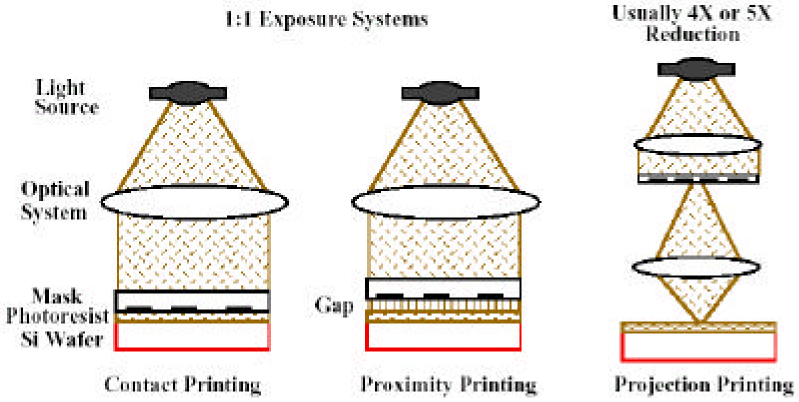
- Material Deposition
- Photolithography
- Pattern Transfer
- Material Modification
  - Doping & anneal



Photolithography & Pattern Transfer
The Key Technology



Basic Optical Aligners
Photoresist Exposure Systems

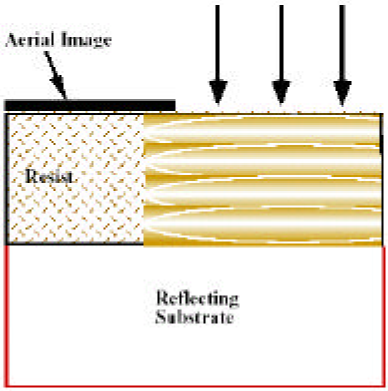


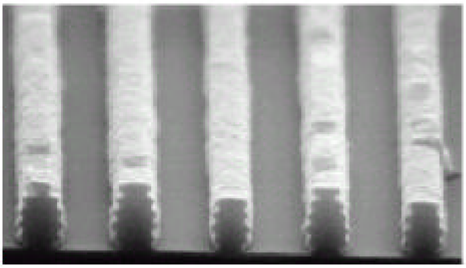
Resolution : $W \approx \sqrt{\lambda \bullet G}$

$$W \approx 0.6\frac{\lambda}{NA}$$

$$\textbf{DOF} \approx \frac{\lambda}{2(NA)^2}$$

Standing Wave Interference
Monochromatic Illumination





Photoresists & Photosensitive Materials

Photoresists

removed after pattern transfer

- Positive
- Negative
- Electrodeposited resists

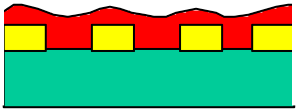
Spin-on deposition

- Simple process
- Good thickness control
- Planarising process

Photosensitive structure materials

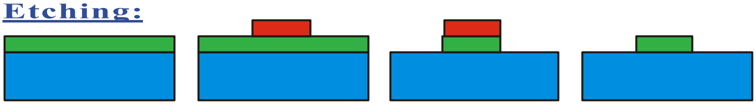
interlayer dielectrics & mechanical structures

- Polyimides
- SU-8 Epoxy
- BCB Cyclotene

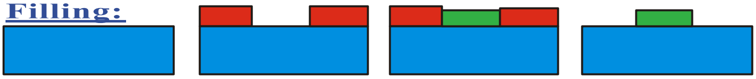


Pattern Transfer

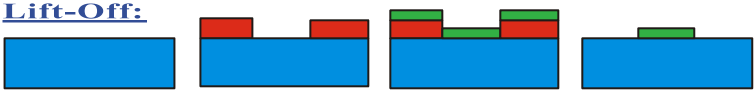
Etching:



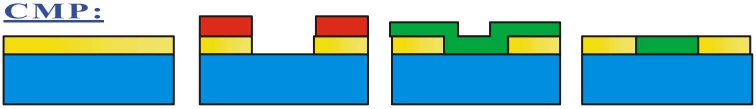
MOULD Filling:



Lift-Off:



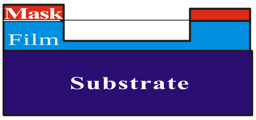
CMP:



Pattern Transfer - Etching
Important Parameters

Anisotropy

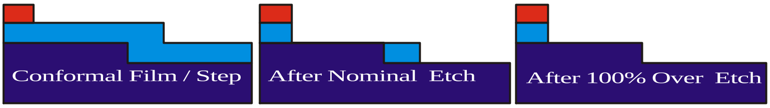
Selectivity



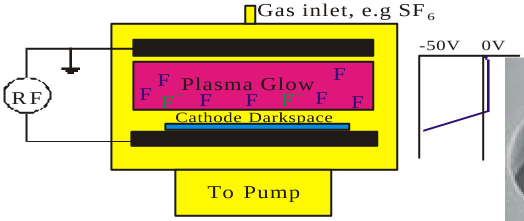
$S_{mask} = R_{film}/R_{mask}$

$S_{substrate} = R_{film}/R_{substrate}$

Selectivity & Anisotropy interaction



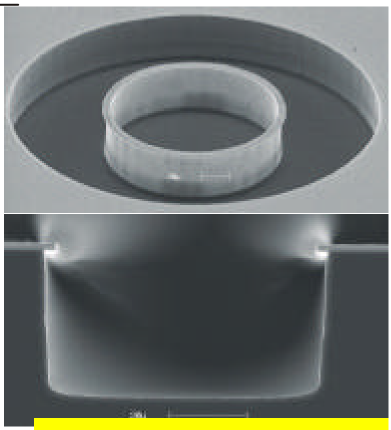
Dry Etching
Reactive Ion Etching- RIE



Pressure: 0.01-1Torr
Etchant :e.g. Atomic Flourine
Enhanced by ion bombardment
Anisotropy : Sidewall passivation
Selectivity: good to poor

Gas additives:

O_2: Increase F and Silicon etch rate
Sidewall passivation - Anisotropy
H_2: Decrease F and Silicon etch rate
Selective oxide etch



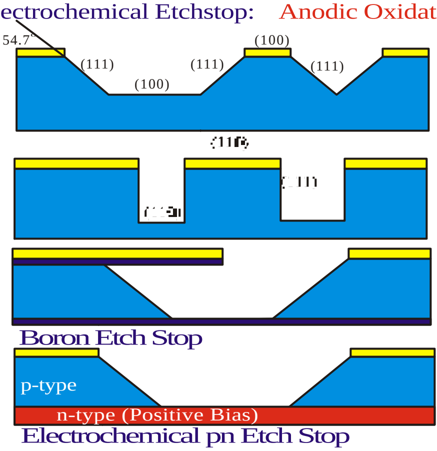
SF_6+O_2 Silicon etch
Oxide mask

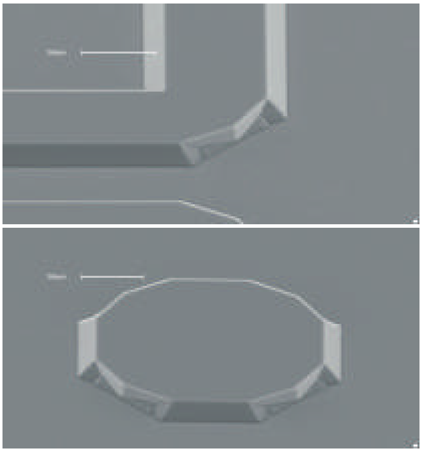
Wet Silicon Etching in Alcaline Solutions

Crystallographic Anisotropy $R_{111} << R_{100}, R_{110}$

Boron Etchstop ($N > 5*10^{19}/cm^3$): $R \sim N^{-4}$

Electrochemical Etchstop: Anodic Oxidation





Outer corners are attacked by the etch

Thin Film Deposition Methods

Native Films

- Thermal Oxidation / Nitridation

Chemical Vapour Deposition - CVD

- Vapour phase epitaxy - VPE
- Atmospheric pressure – APCVD
- Low pressure CVD – LPCVD
- Plasma enhanced CVD – PECVD
- Semiconductors
- Dielectrics
- Metals

Liquid Phase Epitaxy – LPE

- Semiconductors III-V

Physical Vapour deposition - PVD

- Vacuum Evaporation
- Molecular Beam Epitaxy – MBE
- Sputtering – Reactive sputtering
- Metals & Semiconductors III-V

Electrochemical deposition

- Electroplating, Electroless plating
- Metals

Spin-on deposition

- Dielectrics (Doped glasses)
- Polymers (Photoresist)

Wafer Bonding

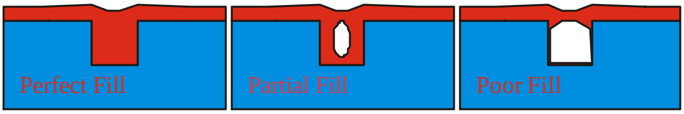
- Anodic bonding (Silicon/PYREX)
- Fusion bonding (Silicon/Silicon)

Thin Film Deposition
Important Issues

Step Coverage

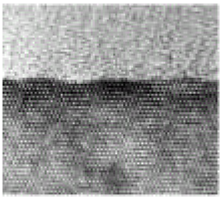
(LPCVD PECVD PVD-evaporation)

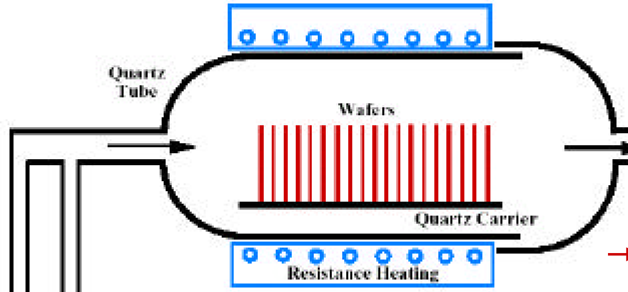
Trench Filling



Additionally: Growth temperature. Uniformity < 5%. Adhesion. Morphology, stoichiometry & density. Pinhole density < 1/cm^2. Stress – built-in and thermal mismatch.

Oxidation Furnaces

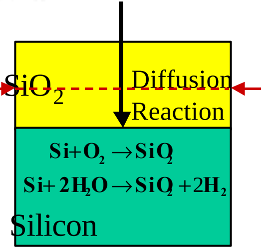




800-1200°C

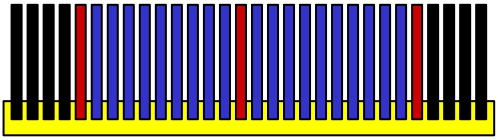
N_2, O_2, H_2, H_2O, HCl

O_2 or H_2O



$Si + O_2 \rightarrow SiO_2$

$Si + 2H_2O \rightarrow SiO_2 + 2H_2$



Typical boat-load

2x4 Dummy-wafers

3 Test-wafers

15-190 Production-wafers

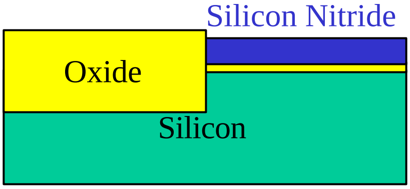
LOCOS: Local Oxidation

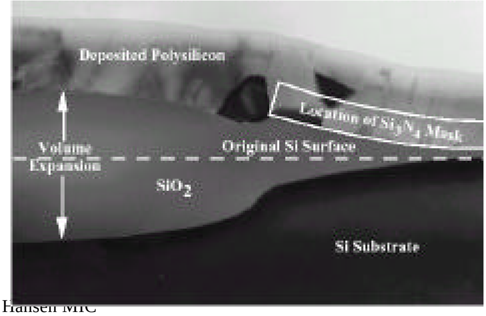
- Silicon nitride mask
- Low diffusivity of O_2, H_2O in Si_3N_4
- Slow oxidation of Si_3N_4

LOCal Oxidation of Silicon

LOCOS

- Reduced surface topography
- Self aligned diffusions
- Used in most modern processes
- Needs a stress relieve oxide - Pad oxide
  - Eliminates slip lines in Si

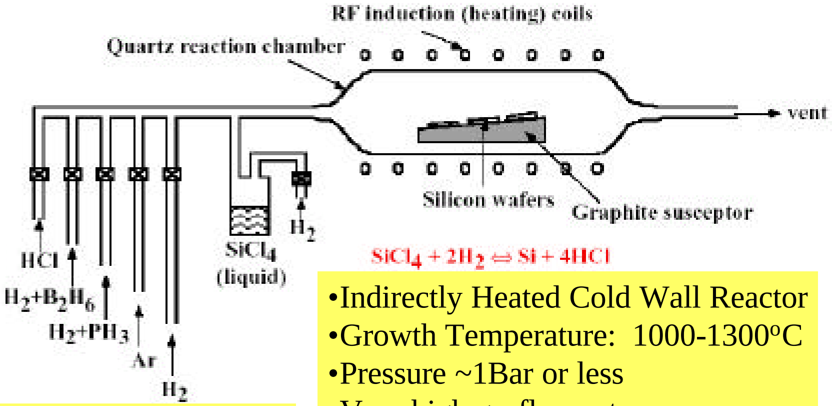




Epitaxy

- Single Crystal Films on Single Crystal Substrates
- Homo Epitaxy: Substrate & Film Identical
  - Si/Si, GaAs/GaAs etc.
- Hetero Epitaxy: Substrate & Film Different
  - GaAlAs/GaAs, SiGe/Si

Vapour Phase Epitaxy – VPE
The Horizontal Reactor



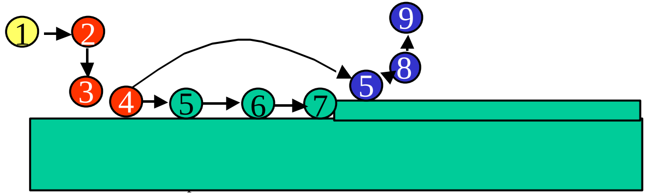
$SiCl_4 + 2H_2 \Leftrightarrow Si + 4HCl$

- Indirectly Heated Cold Wall Reactor
- Growth Temperature: 1000-1300°C
- Pressure ~1Bar or less
- Very high gasflow rates
- Low Si-compound Molar Fraction
- Quite Low Wafer Throughput
- HCl used for pre-epi etch/clean

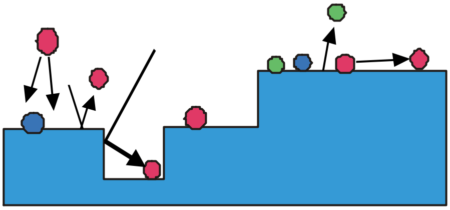
Other Si-Sources:
Silane: SiH_4
Chlorosilane: SiH_xCl_y

Elemental Steps in VPE/CVD

1. Convective Gas Phase Transport
2. Gas Phase Reactions: $SiCl_4+H_2 \leftrightarrow SiCl_2+2HCl$
3. Mass Transport to Surface (Diffusion)
4. Adsorption to surface (Desorption from Surface)
5. Chemical reaction on Surface
6. Diffusion on Surface
7. Lattice Incorporation
8. Product Desorption
9. Mass Transport from surface



Step Coverage &Trench Filling Important Parametres



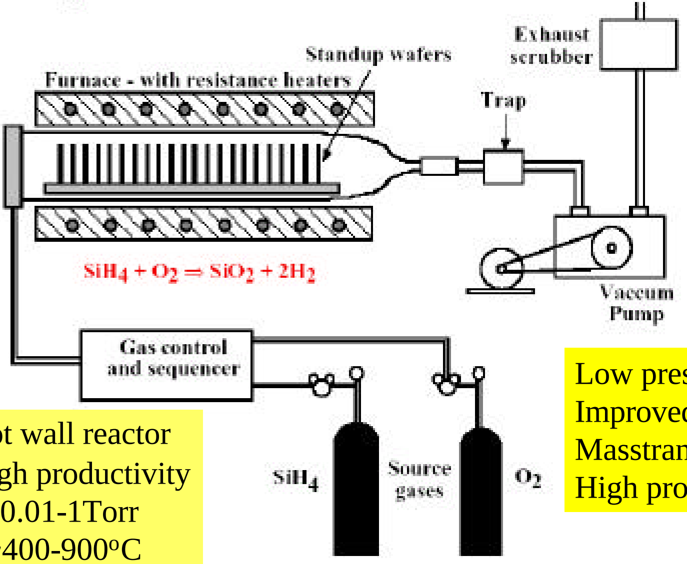
Source Material:
- Flux intensity
- Angular Distribution

Source/sample:
- Sticking coefficient
- Surface Diffusivity
- Surface Reaction Rate
- Product Desorbtion

Sample:
- Angle of view

Improved Coverage/Filling:
High surface diffusivity
Low sticking coefficient
Wide angular distribution (SC)
Low flux intensity
Low reaction rate
High angle of view

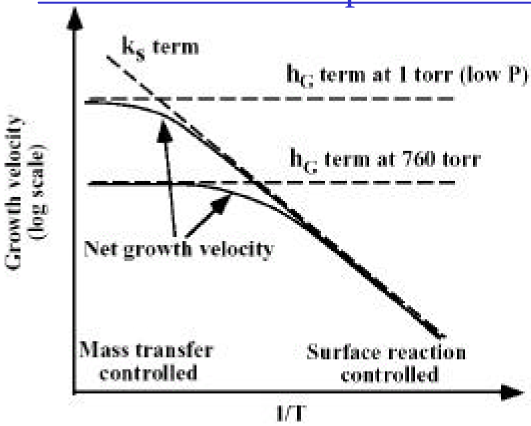
Low Pressure CVD - LPCVD



Hot wall reactor
High productivity
P~0.01-1Torr
T~400-900^{o}C

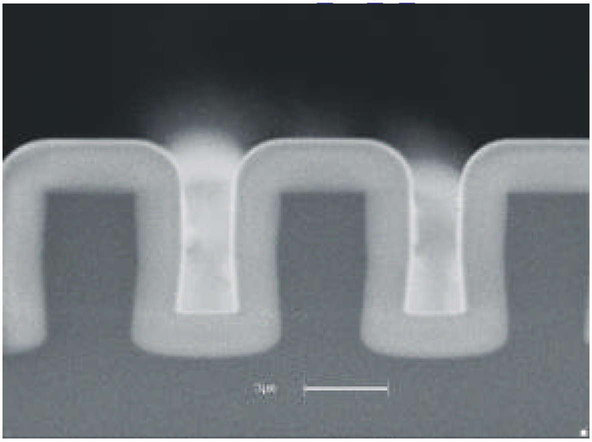
Low pressure =>
Improved
Masstransport=>
High productivity

APCVD – LPCVD
Growth Rate Temperature Dependence



APCVD/LPCVD Growth Rates Compared.
Source gas concentration assumed constant.
Surface reaction control maintained at higher rates & temperatures.

LPCVD TEOS Oxide
$Si(OC_2H_5)_4$



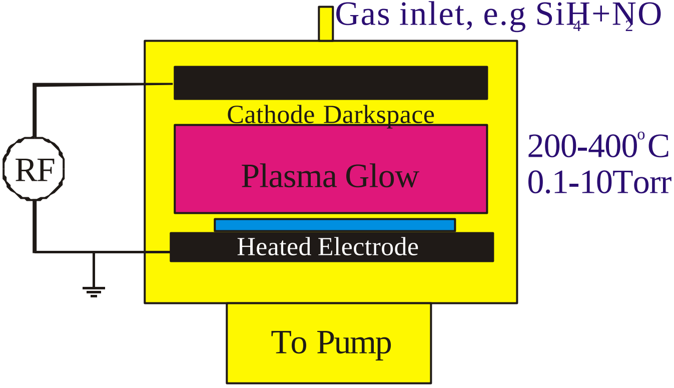
Good Step Coverage & Trench Filling – Almost Conformal
Due to high mobility of TEOS on the surface

Problems in APCVD - LPCVD

Low temperature deposition impractical:

- Very low rates at low temperature
  - – ~exp($-E_a/kT$)
- Low film quality
  - – Porous due to low surface diffusivity
  - – Poor step coverage/ trench filling
    - High sticking coefficient
    - Low surface diffusivity
- Solution: PECVD – Plasma Enhanced CVD

Plasma Enhanced CVD
PECVD



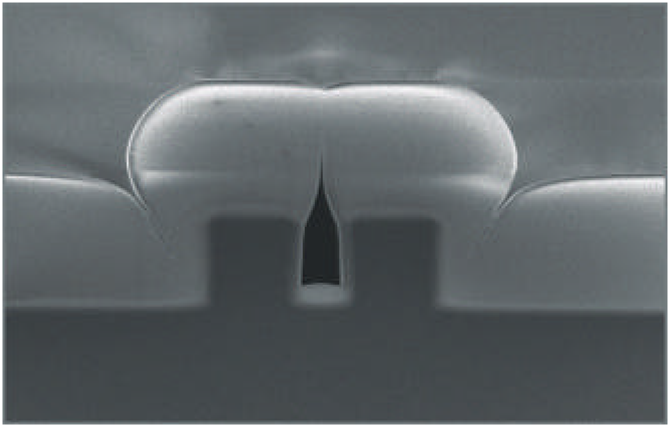
The gas discharge creates:

Reactive, Energetic Molecular Fragments – Increases k_s

Energetic Ions – Ion bombardment densify the film

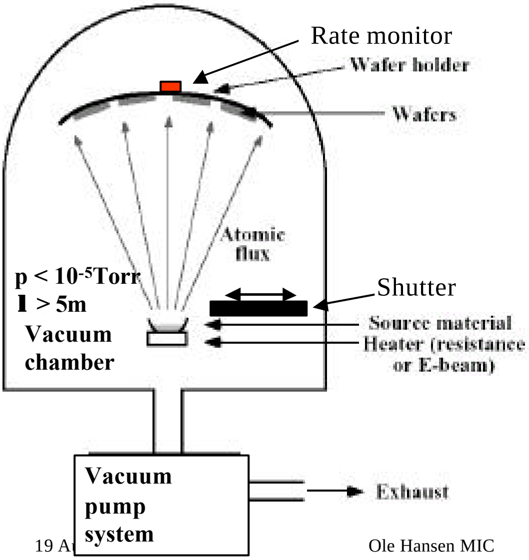
Result: High deposition rates & dense films at low temperatures.

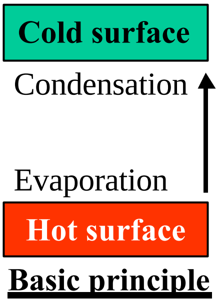
PECVD Oxide Film
SiH_4+N_2O at 300°C



Poor trench filling, voids & cracks due to low surface mobility
Step coverage and trench filling is a general PECVD problem.

PVD - Evaporation

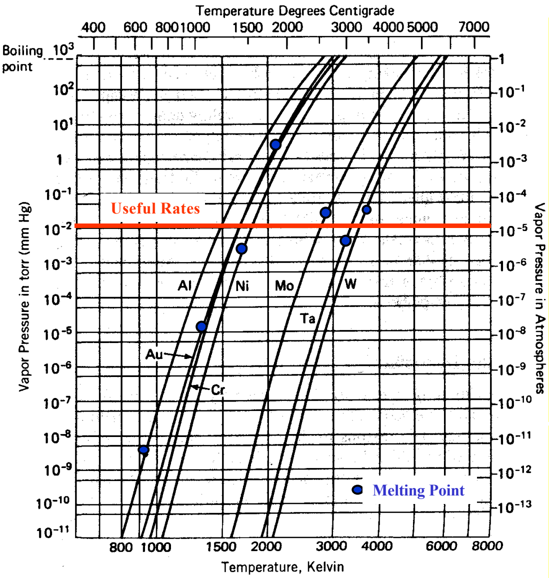




Basic principle

- **Very flexible tool**
- **Wide range of pure materials**
- **"No" gas-phase collisions**
- **Line-of-sight deposition**
- **High purity possible**
  - **UHV, $p < 10^{-9}$ Torr**
  - **Pure source & e-beam**

Vapour Pressure



Clausius-Clapeyron (Carnot engine):

$$\frac{dp}{dT} = \frac{\Delta H}{T\left(v_g - v_l\right)}$$

Ideal gas: $pv_g = RT$

$$\frac{dp}{dT} = \frac{\Delta H}{T\left(\frac{RT}{p} - v_l\right)} \approx \frac{p\Delta H}{RT^2}$$

$$p = C\exp\left(-\frac{\Delta H}{RT}\right), \textbf{ or } \ln p = -\frac{\Delta H}{RT} + A$$

Real materials: $\Delta H = f(T)$

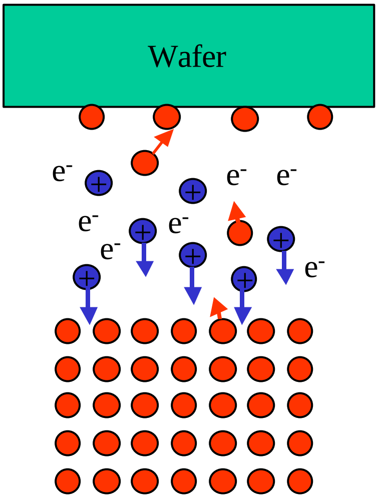
$$\ln p = -\frac{\Delta H}{RT} + A + B\ln T + DT + +$$

Parameters, see CRC handbook.

Evaporation: Melt→Gas
Sublimation: Solid→Gas

Useful rates: p >10mTorr

PVD – Sputtering: Basic Principle

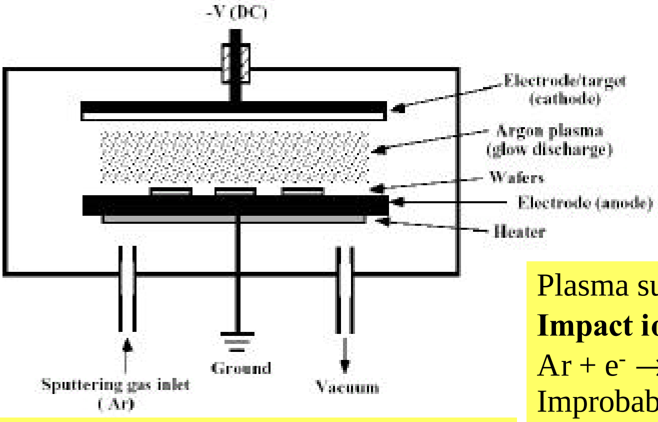


Target: source material

Energetic ions, usually Ar^+, knock out source atoms.
These atoms travel and deposit on the substrate.
Gas phase collisions occur before deposition, p~10-100mTorr, λ<5mm.
Result: Deposited atoms arrive from a wide space angle.
Improved step coverage.

Sputter yields (atoms/ion) rather insensitive to material:
Alloy deposition possible

DC - Sputtering

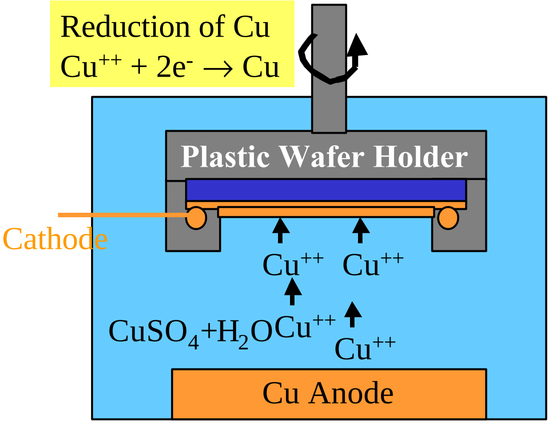


Plasma sustaining reaction:
Impact ionisation
$Ar + e^- \rightarrow Ar^+ + 2e^-$
Improbable at low pressure, since $\lambda \geq L$,
Improbable at high pressure, since $E \sim \lambda V/L < E_{ionization}$

Basic two-electrode DC sputter system
$p \sim 10\text{-}100\text{mTorr}$, $V_{DC} \sim 0.5\text{-}5\text{kV}$.

Electroplating

Reduction of Cu
$Cu^{++} + 2e^- \rightarrow Cu$



Oxidation & dissolution of Cu
$Cu \rightarrow Cu^{++} + 2e^-$

Low cost technology
Easily scaled to industrial scale

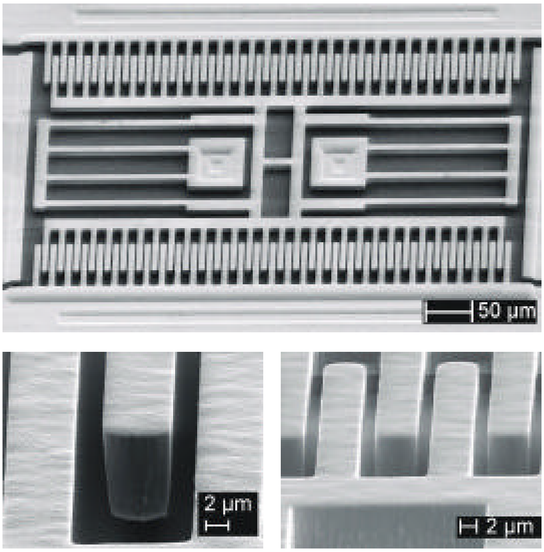
Current density ~1-5A/dm^2
Temperature 20-70^{o}C

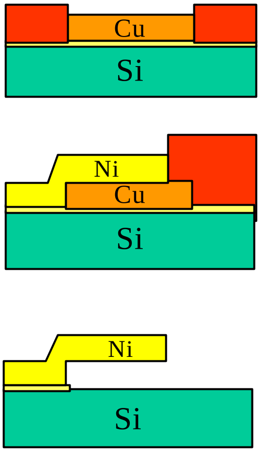
Stress & morphology affected by
- Current density
- Temperature
- Bath composition
- Bath additives

Materials:
Cu, Ni, Au, NiFe, CoNiFe, Sn

Problems: Purity, uniformity, composition & stress control

Electroplated Ni Structures



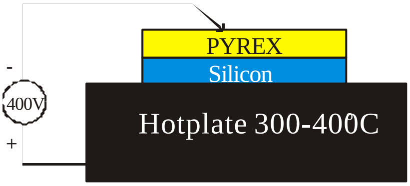


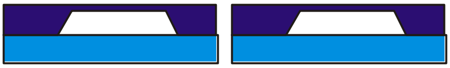
Cu sacrificial layer

Wafer Bonding
Anodic & Fusion Bonding

Anodic Bonding

Fusion Bonding





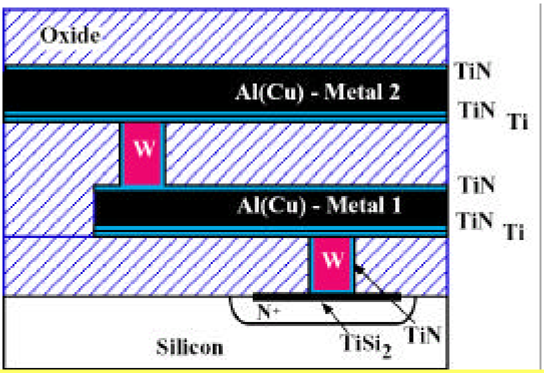
Room Temperature Pre-Bonding

High Temperature Anneal

Needs:Thermal Matched Pyrex
Medium Ionic (Na^+) Conductivity
Low Particle Density

Needs: Particle Free Surfaces
Atomically Smooth Surfaces

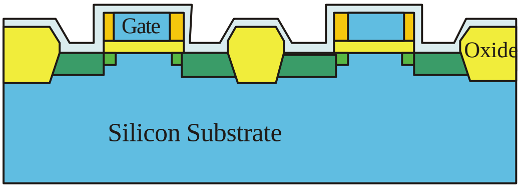
Modern Metallizations
A Paradigm Shift



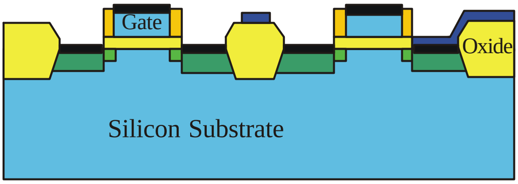
Cu conductors: lower resistivity & electromigration
TiSi2/Si contacts: improved stability & lower contact resistance
TiN barrier: protects Si against ”unfriendly” Cu
Fabrication using CMP – Chemical mechanical polishing

Selfaligned TiSi$_2$/Si Contacts
TiN Local Interconnects

Sputterdeposit Titanium



Form TiSi$_2$ & TiN (N_2 @ 600C, 1 min.)
Selective masked TiN etch

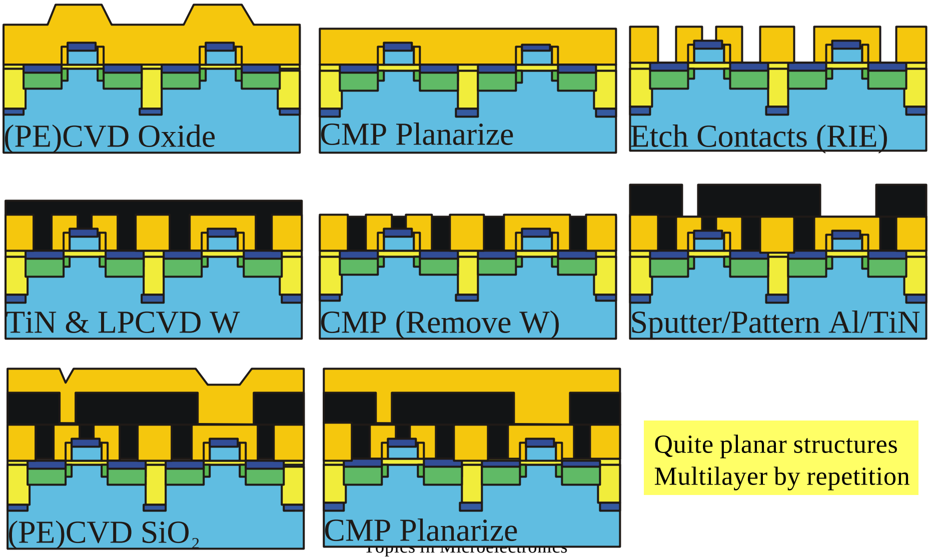


Silicide formation:

1. Diffusion of Si in Silicide
2. Reaction Ti+Si $\rightarrow$ TiSi$_2$
3. Selective, only in contacts
4. Simultaneous thermal nitridation possible
5. Oxygen free atmosphere

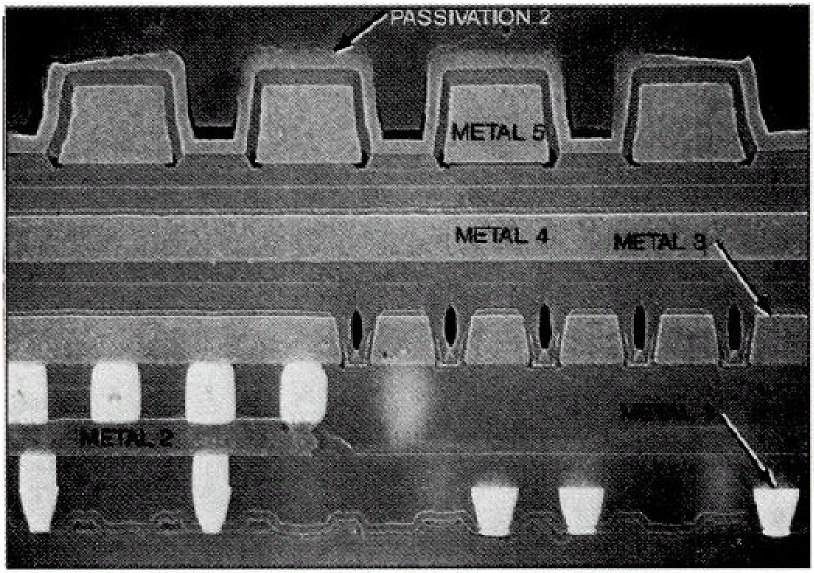
Stable contacts TiSi$_2$/Si
Local TiN interconnects (10Ω)
Integrated TiN diffusionbarrier
Local interconnect ”price”
1 mask-etch step

Single Damascene Metallisation

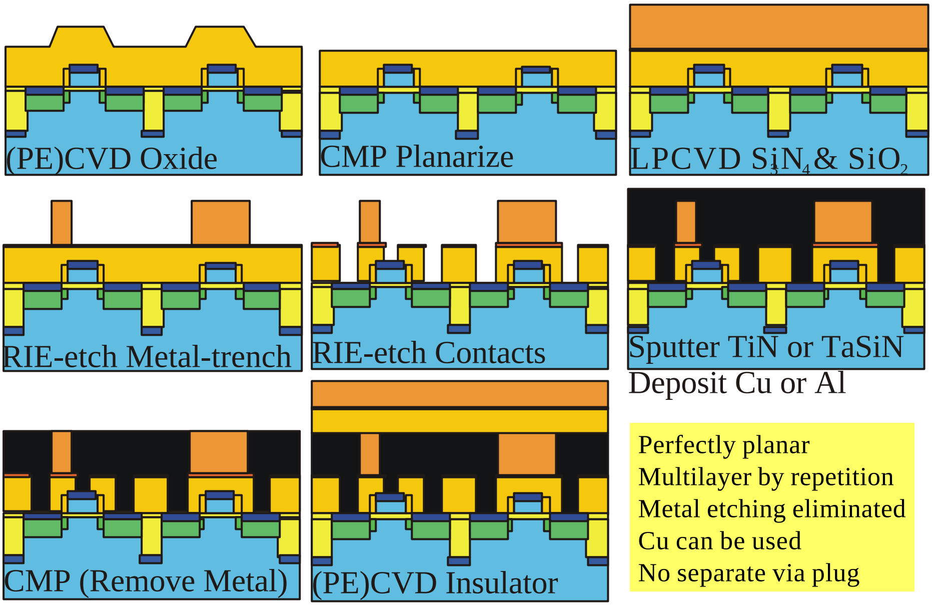


Quite planar structures
Multilayer by repetition

Conventional & Damascene Metal



Double Damascene


(PE)CVD Oxide

CMP Planarize

LPCVD Si_3N_4 & SiO_2

RIE-etch Metal-trench

RIE-etch Contacts

Sputter TiN or TaSiN

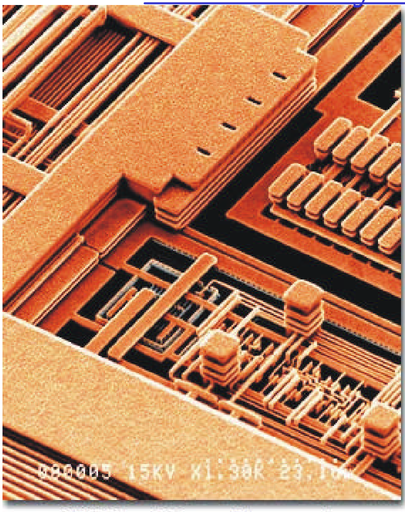
Deposit Cu or Al

CMP (Remove Metal)

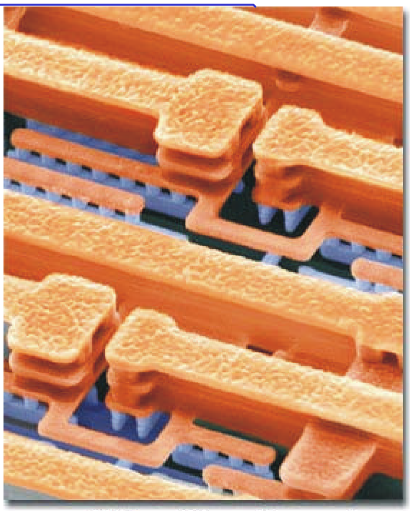
(PE)CVD Insulator

- Perfectly planar
- Multilayer by repetition
- Metal etching eliminated
- Cu can be used
- No separate via plug

Double Damascene
Cu Multilayer Metallization

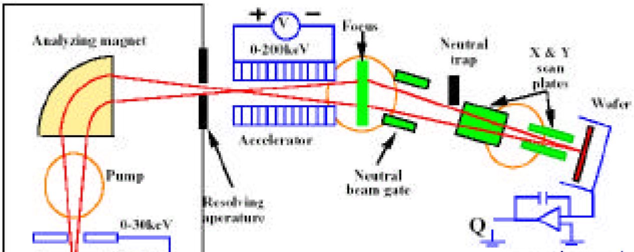


SEM view of Copper Interconnect
(IBM Microelectronics)

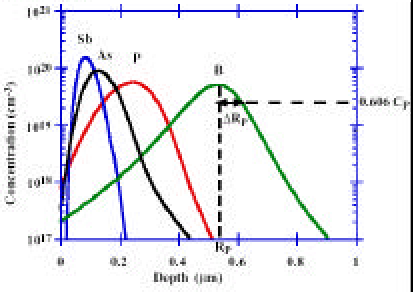


SEM view of Copper Interconnect
(IBM Microelectronics)

Material Modification
Ion-implant Doping



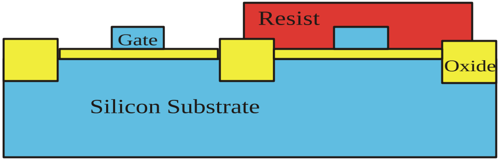
Disadvantages:
- Crystal damage
- Anomalous TED
  - transient diffusion
- Insulator charging

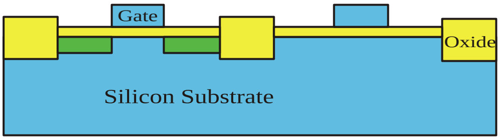


Preferred doping method:
- Accurate dose control
- High purity
- Buried profiles
- Easy masking

Composite Masking &
Self-Registration

Implant B^+ or As^+





Final Structure:

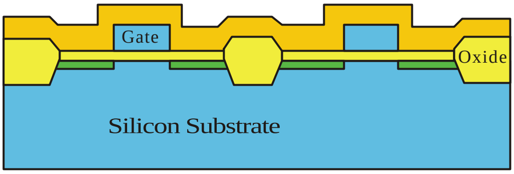
FieldMask GateMask ImplantMask

Perfect registration :

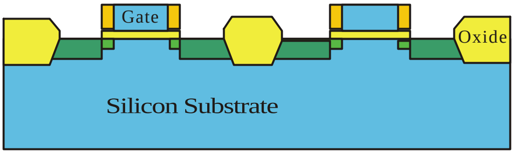
SourceDrain Diffusion-Gate,
SourceDrain Diffusion-FieldOxide

Sub-Lithographic Features - Sidewall Oxide

Deposit Conformal CVD Oxide



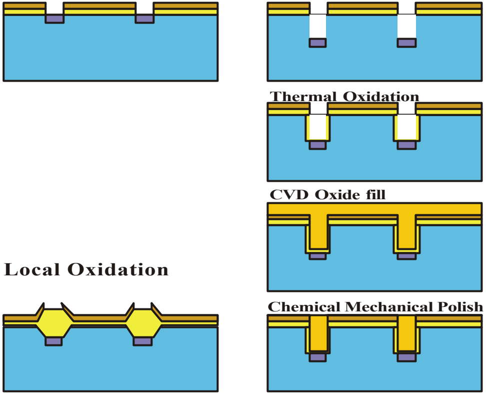
Anisotropic RIE Oxide Etch & Implant



Lightly Doped Drain with offset
Heavily Doped Drain-Contact

Device Isolation LOCOS or Trench/CMP

Form $Si_3N_4/SiO_2/Si$ Field Pattern
Implant Channel Stop



LOCOS Isolation

CMP Isolation
Planar & Compact