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# HM629127H Series

131072-word × 9-bit High Speed CMOS Static RAM

# HITACHI

Rev. 0.0  
Dec. 1, 1995

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## Description

The HM629127H is an asynchronous high speed static RAM organized as 131,072-word × 9-bit. It realizes high speed access time (20/25 ns) with employing 0.8 μm CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM629127H is packaged in 400-mil 32/36-pin SOJ for high density surface mounting.

## Features

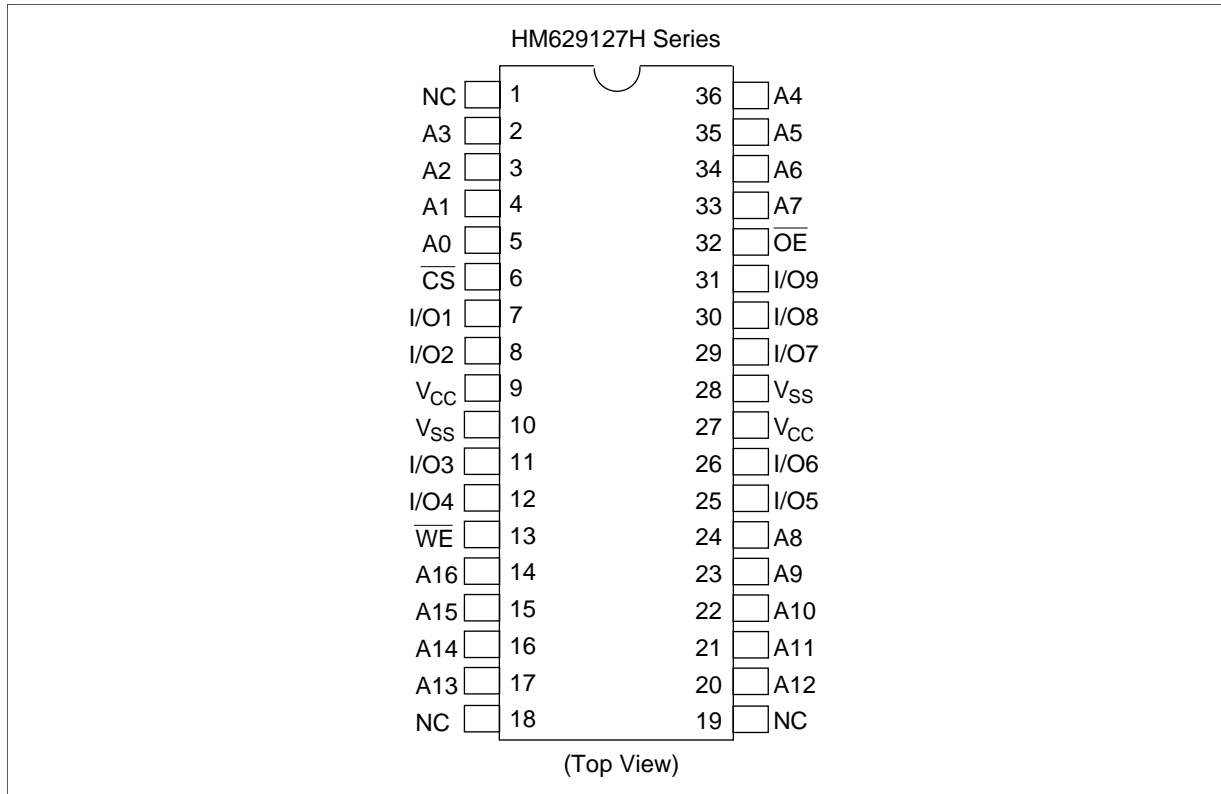
- Single 5 V supply: 5 V ± 10%
- Access time 20/25 ns (max)
- Completely static memory  
No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible  
All inputs and outputs
- 400-mil 36-pin SOJ package
- Center V<sub>CC</sub> and V<sub>SS</sub> type pinout

## Ordering Information

Type No.	Access Time	Package
HM629127HJP-20	20 ns	400-mil 36-pin Plastic SOJ (CP-36D)
HM629127HJP-25	25 ns	
HM629127HLJP-20	20 ns	
HM629127HLJP-25	25 ns	

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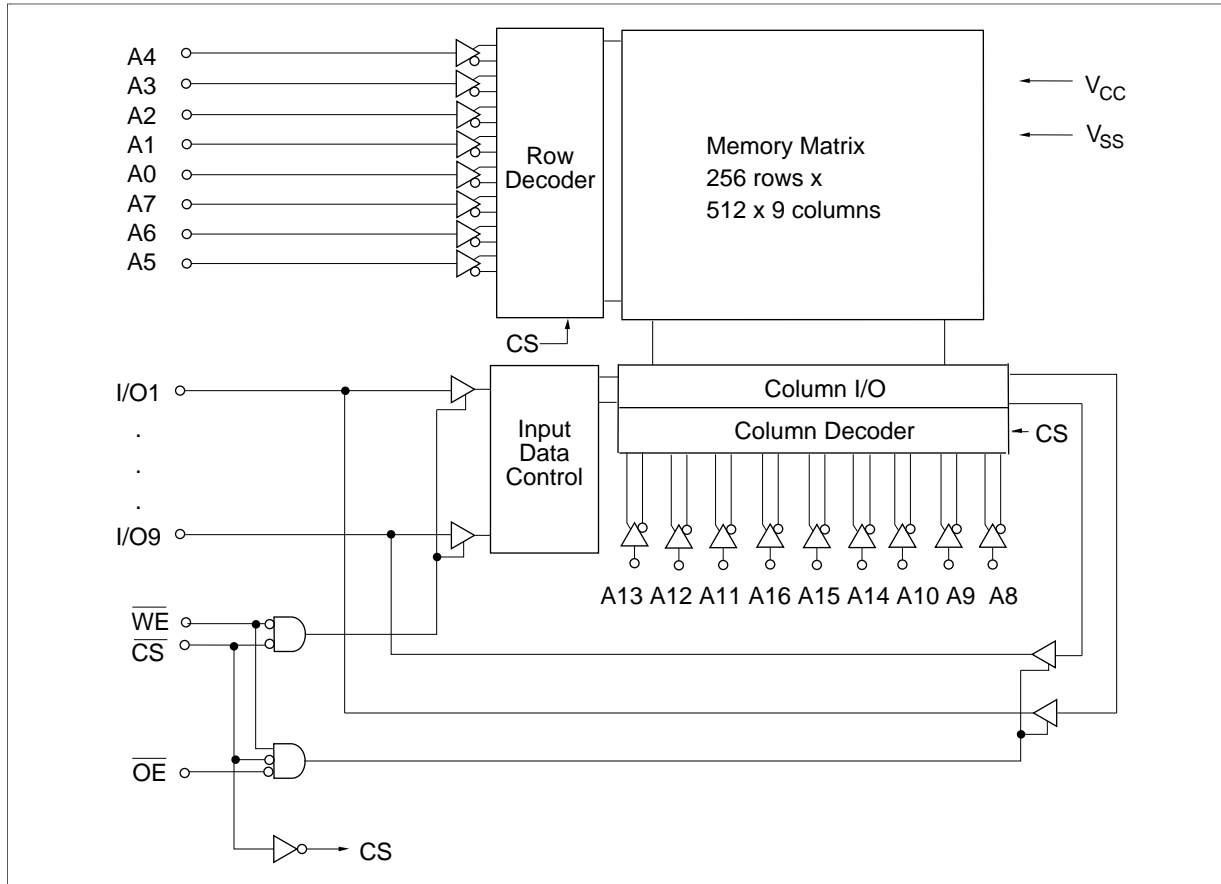
## HM629127H Series



### Pin Description

Pin name	Function
A0 – A16	Address
I/O1 – I/O9	Data input/output
CS	Chip select
WE	Write enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>1</sup> to $V_{CC} + 0.5$	V
Power dissipation	$P_T$	1.0 <sup>2</sup> / 1.5 <sup>3</sup>	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

- Notes: 1. -2.5 V for pulse width (under shoot)  $\leq 10$  ns  
 2. at still air condition  
 3. at air flow  $\geq 1.0$  m/s

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### Function Table

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$V_{\text{CC}}$ Current	I/O	Ref. Cycle
H	X	X	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	H	$I_{\text{CC}}$	High-Z	—
L	L	H	$I_{\text{CC}}$	Output	Read cycle
L	X	L	$I_{\text{CC}}$	Input	Write cycle

Note: X: H or L

### Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage <sup>2</sup>	$V_{\text{CC}}$	4.5	5.0	5.5	V
	$V_{\text{SS}}$	0	0	0	V
Input voltage	$V_{\text{IH}}$	2.2	—	$V_{\text{CC}} + 0.5$	V
	$V_{\text{IL}}$	-0.5 <sup>1</sup>	—	0.8	V

- Notes: 1. -2.0 V for pulse width (under shoot)  $\leq 10$  ns  
2. The supply voltage with all  $V_{\text{CC}}$  pins must be on the same level.  
The supply voltage with all  $V_{\text{SS}}$  pins must be on the same level.

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### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ <sup>1</sup>	Max	Unit	Test Conditions	Note
Input leakage current	I <sub>LI</sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	2	μA	V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating power supply current	I <sub>CC</sub>	—	130	180	mA	20 ns cycle	$\overline{CS} = V_{IL}$ , I <sub>out</sub> = 0 mA Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
			—	100		160	25 ns cycle
Standby power supply current	I <sub>SB</sub>	—	50	90	mA	20 ns cycle	$\overline{CS} = V_{IH}$ , Other inputs = V <sub>IH</sub> /V <sub>IL</sub>
			—	40		85	25 ns cycle
Standby power supply current (1)	I <sub>SB1</sub>	—	—	2	mA	V <sub>CC</sub> ≥ $\overline{CS}$ ≥ V <sub>CC</sub> - 0.2 V, 0 V ≤ V <sub>in</sub> ≤ 0.2 V or V <sub>CC</sub> ≥ V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V	
				—		—	0.2
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA	
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4 mA	

Note: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

### Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	—	8	pF	V <sub>I/O</sub> = 0 V

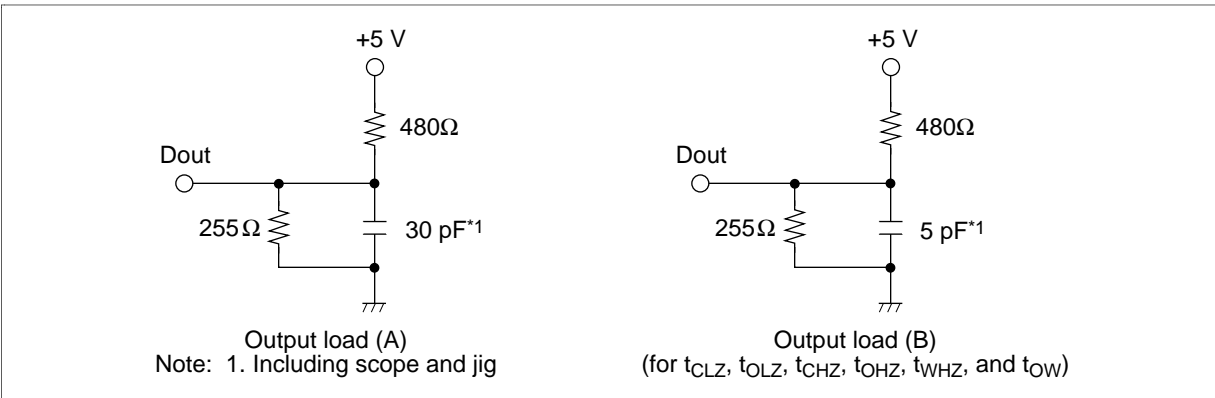
Note: 1. This parameter is sampled and not 100% tested.

## HM629127H Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

### Test Conditions

- Input pulse levels:  $V_{SS}$  to 3.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures

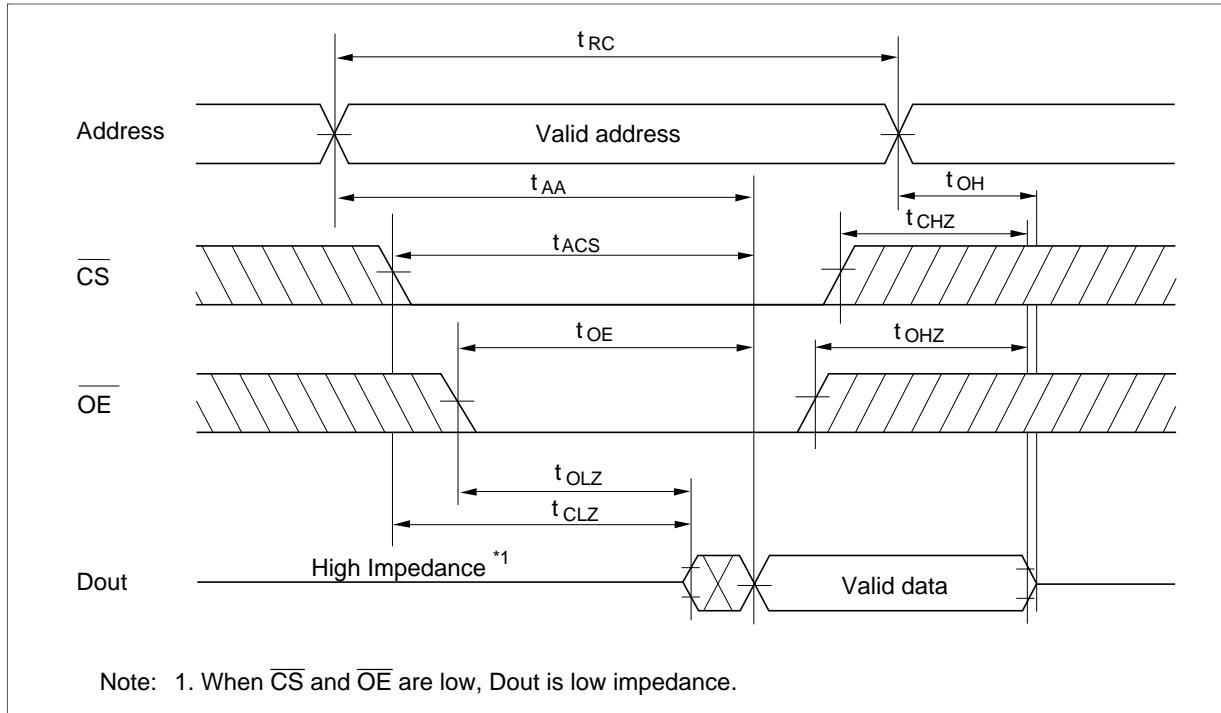


### Read Cycle

HM629127H						
		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Unit Note
Read cycle time	$t_{RC}$	20	—	25	—	ns
Address access time	$t_{AA}$	—	20	—	25	ns
Chip select access time	$t_{ACS}$	—	20	—	25	ns
Output enable to output valid	$t_{OE}$	—	10	—	12	ns
Output hold from address change	$t_{OH}$	5	—	5	—	ns
Chip select to output in low-Z	$t_{CLZ}$	3	—	3	—	ns 1
Output enable to output in low-Z	$t_{OLZ}$	1	—	1	—	ns 1
Chip deselect to output in high-Z	$t_{CHZ}$	—	7	—	7	ns 1
Output disable to output in high-Z	$t_{OHZ}$	—	7	—	7	ns 1

Note: 1. Transition is measured  $\pm 200$  mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform<sup>\*3</sup>



## HM629127H Series

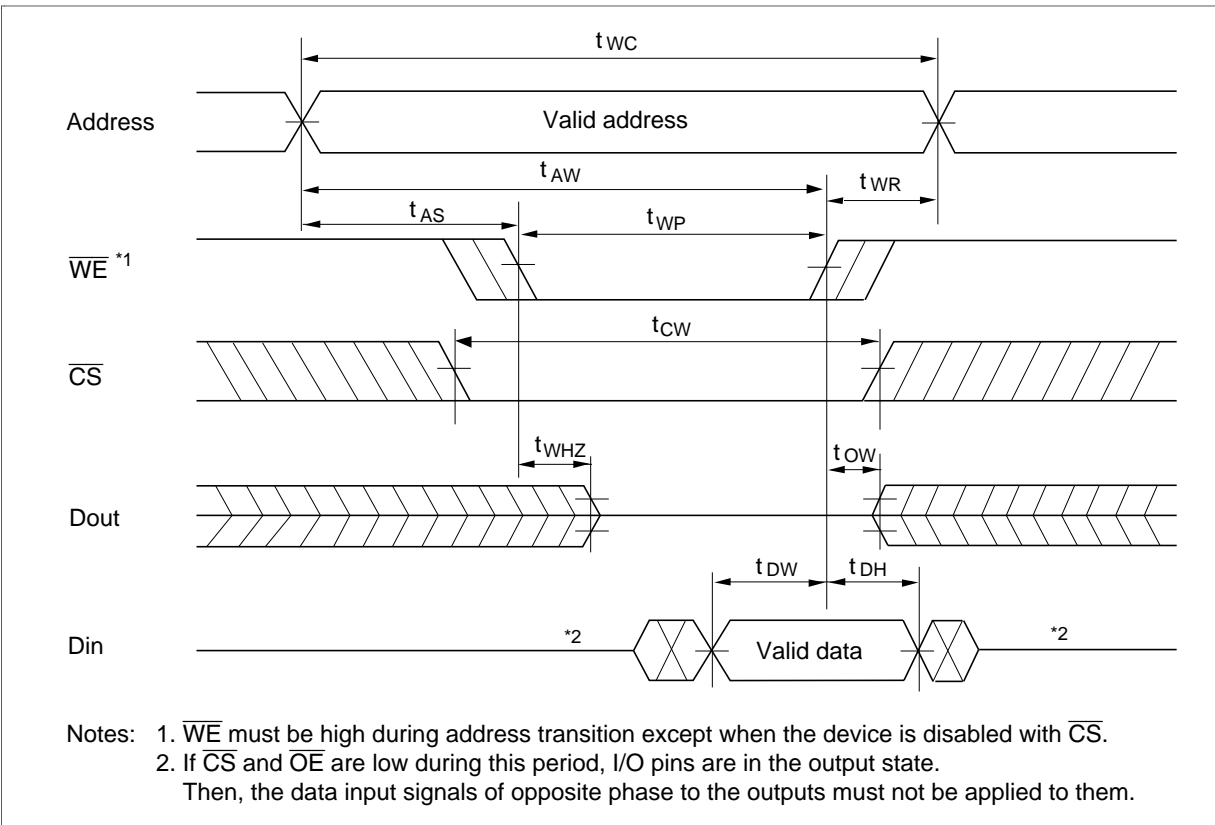
### Write Cycle<sup>\*1</sup>

HM629127H							
		-20		-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	$t_{WC}$	20	—	25	—	ns	
Address valid to end of write	$t_{AW}$	15	—	20	—	ns	
Chip select to end of write	$t_{CW}$	12	—	12	—	ns	
Write pulse width	$t_{WP}$	12	—	12	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	ns	2
Write recovery time	$t_{WR}$	0	—	0	—	ns	3
Data to write time overlap	$t_{DW}$	10	—	10	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	3	—	ns	4
Write enable to output in high-Z	$t_{WHZ}$	—	7	—	7	ns	4

- Notes: 1. A write occurs during the overlap of low  $\overline{CS}$ , low  $\overline{WE}$ .  
 2.  $t_{AS}$  is measured from the latest address transition to the later of  $\overline{CS}$  or  $\overline{WE}$  going low.  
 3.  $t_{WR}$  is measured from the earliest of  $\overline{CS}$  or  $\overline{WE}$  going high to the first address transition.  
 4. Transition is measured  $\pm 200$  mV from high impedance state's voltage with Load (B). This parameter is sampled and not 100% tested.

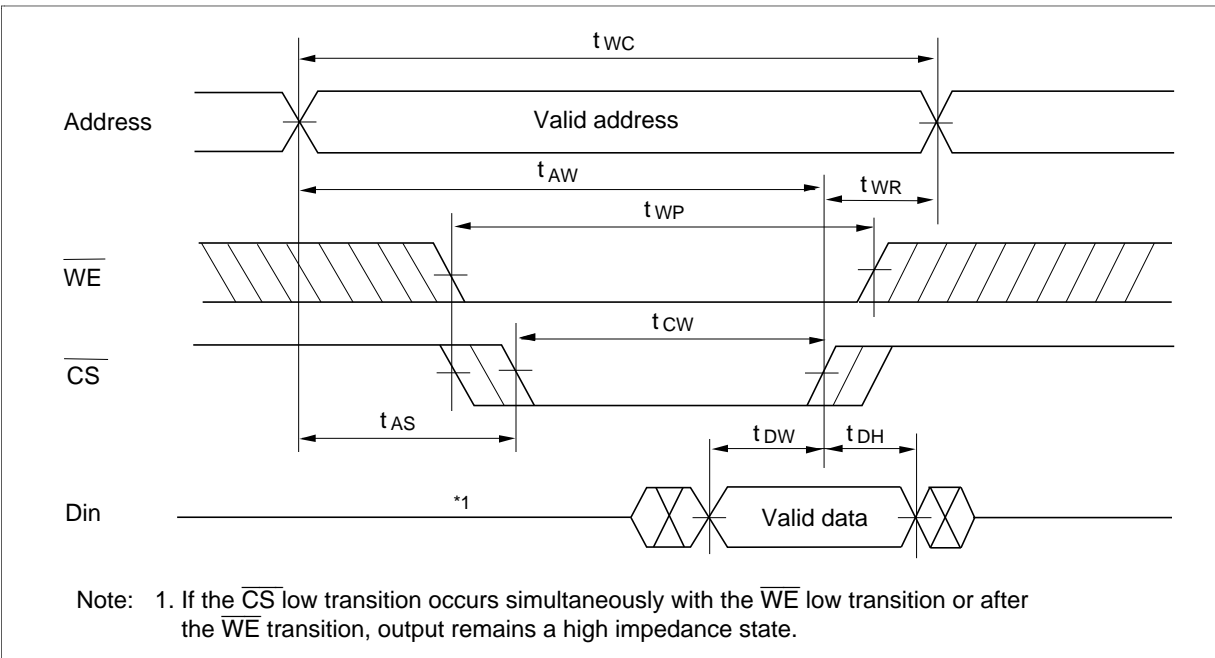


Write Timing Waveform (1) ( $\overline{WE}$  Controlled)



## HM629127H Series

### Write Timing Waveform (2) ( $\overline{CS}$ Controlled)



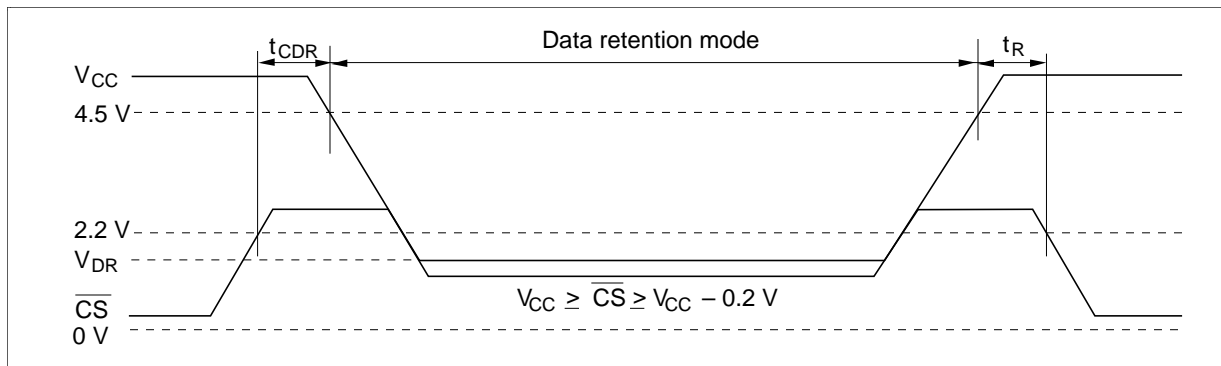
**Low  $V_{CC}$  Data Retention Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	2	$80^{*1}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1.  $V_{CC} = 3.0 \text{ V}$

**Low  $V_{CC}$  Data Retention Timing Waveform**



# HM629127H Series

## Package Dimensions

HM629127H Series (CP-36D)

Unit: mm

