K9K2G08X0A

INFORMATION IN THIS DOCUMENT IS PROVIDED IN RELATION TO SAMSUNG PRODUCTS, AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

NOTHING IN THIS DOCUMENT SHALL BE CONSTRUED AS GRANTING ANY LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE,

TO ANY INTELLECTUAL PROPERTY RIGHTS IN SAMSUNG PRODUCTS OR TECHNOLOGY. ALL INFORMATION IN THIS DOCUMENT IS PROVIDED

ON AS "AS IS" BASIS WITHOUT GUARANTEE OR WARRANTY OF ANY KIND.

1. For updates or additional information about Samsung products, contact your nearest Samsung office.

2. Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where Product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

* Samsung Electronics reserves the right to change products or specification without notice.

SAMSUNG

ELECTRONICS

1

Document Title

256M x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	May. 31. 2004	Advance
0.1	1. Technical note is changed 2. Notes of AC timing characteristics are added 3. The description of Copy-back program is changed 4. TSOP package is deleted	Oct. 25. 2004	Preliminary
0.2	1. $\overline{CE}$ access time : 23ns->35ns (p.9)	Feb. 14. 2005	
0.3	1. The value of tREA is changed. (18ns->20ns) 2. EDO mode is added.	May 4 2005	
0.4	1. The flow chart to creat the initial invalid block table is changed.	May 6 2005	
1.0	1. 1.8V FBGA spec is merged 2. 3.3V FBGA package is added 3. FBGA package size is changed to 9.5 x 12 4. Leaded part is deleted	Feb. 1 2006	

256M x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9K2G08U0A-F	2.7 ~ 3.6V	X8	WSOP1
K9K2G08R0A-J	1.65 ~ 1.95V	X8	FBGA

FEATURES

- Voltage Supply
  - 2.7 V ~3.6 V
  - 1.65V ~ 1.95V
- Organization
  - Memory Cell Array
    - (256M + 8,192K)bit x 8bit
  - Data Register
    - (2K + 64)bit x8bit
- Automatic Program and Erase
  - Page Program
    - (2K + 64)Byte
  - Block Erase
    - (128K + 4K)Byte
- Page Read Operation
  - Page Size
    - 2K-Byte
  - Random Read : 25μs(Max.)
  - Serial Access : 50ns(Min.)

- Fast Write Cycle Time
  - Program time : 300μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
  - K9K2G08U0A-FIB0
    48 - Pin WSOP I (12x17x0.7mm)- Pb-free Package
  - K9K2G08R0A-JCB0/JIB0
    63- Ball FBGA (9.5x12) - Pb-free Package

GENERAL DESCRIPTION

Offered in 256Mx8bit the K9K2G08X0A is 2G bit with spare 64M bit capacity. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 300μs on the 2112byte page and an erase operation can be performed in typical 2ms on a 128K-byte block. Data in the data page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9K2G08X0A's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9K2G08X0A is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.
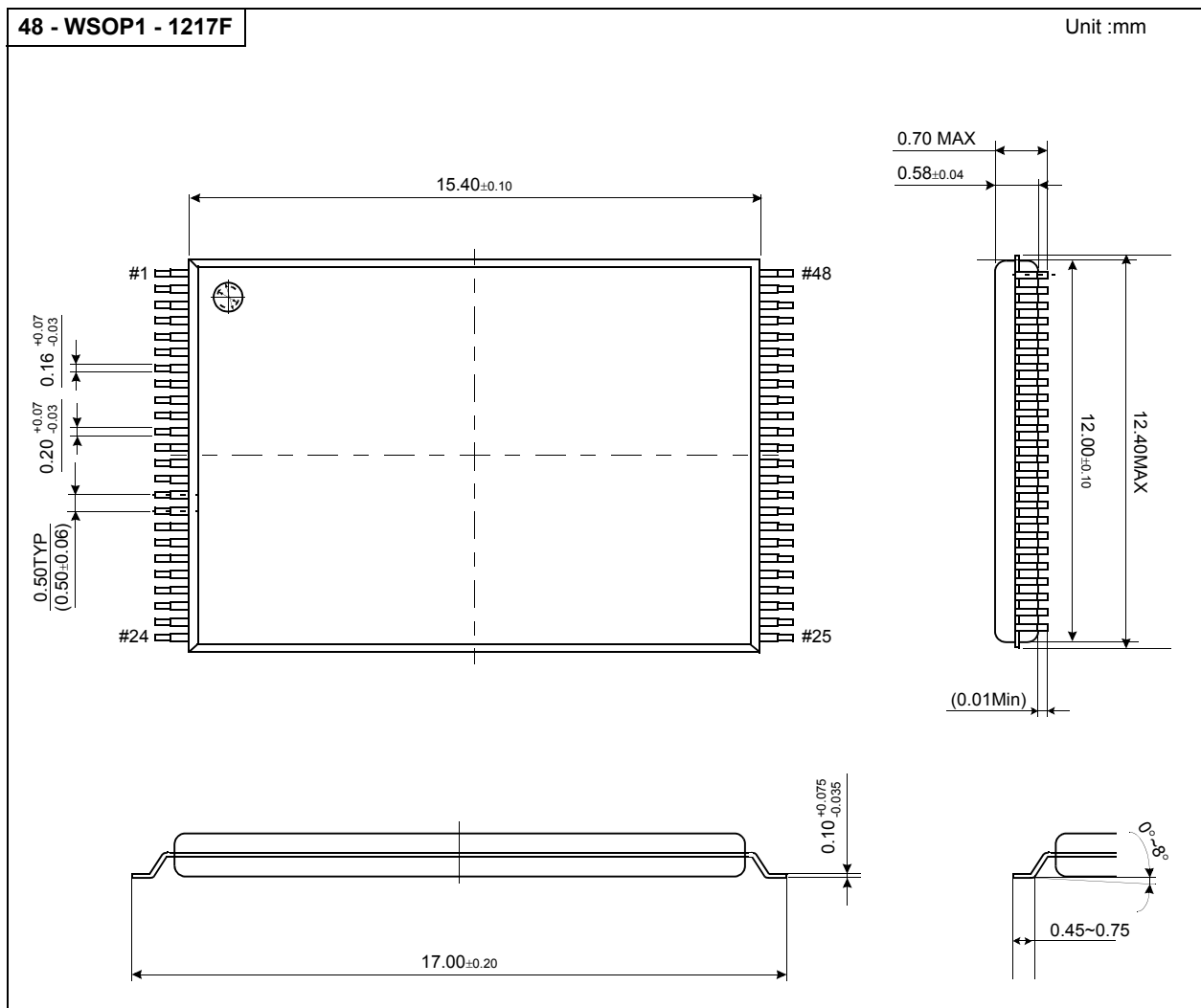
SAMSUNG
ELECTRONICS

PIN CONFIGURATION (WSOP1)

K9K2G08U0A-FIB0

N.C	1		48	N.C
N.C	2		47	N.C
DNU	3		46	DNU
N.C	4		45	N.C
N.C	5		44	I/O7
N.C	6		43	I/O6
R/B	7		42	I/O5
RE	8		41	I/O4
CE	9		40	N.C
DNU	10		39	DNU
N.C	11		38	N.C
Vcc	12		37	Vcc
Vss	13		36	Vss
N.C	14		35	N.C
DNU	15		34	DNU
CLE	16		33	N.C
ALE	17		32	I/O3
WE	18		31	I/O2
WP	19		30	I/O1
N.C	20		29	I/O0
N.C	21		28	N.C
DNU	22		27	DNU
N.C	23		26	N.C
N.C	24		25	N.C

PACKAGE DIMENSIONS

48-PIN LEAD PLASTIC VERY VERY THIN SMALL OUT-LINE PACKAGE TYPE (I)

48 - WSOP1 - 1217F

Unit :mm

0.70 MAX

$0.58_{\pm0.04}$

$15.40_{\pm0.10}$

#1

#48

$0.16\,{}^{+0.07}_{-0.03}$

$0.20\,{}^{+0.07}_{-0.03}$

0.50TYP
$(0.50_{\pm0.06})$

#24

#25

$12.00_{\pm0.10}$

12.40MAX

(0.01Min)

$0.10\,{}^{+0.075}_{-0.035}$

$17.00_{\pm0.20}$

$0°\sim8°$

0.45~0.75

SAMSUNG
ELECTRONICS

PIN CONFIGURATION (FBGA)

K9F1G08R0A-JCB0/JIB0

	1	2	3	4	5	6
	N.C	N.C			N.C	N.C
	N.C				N.C	N.C
A	/WP	ALE	Vss	/CE	/WE	R/B
B	NC	/RE	CLE	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	NC	NC	NC	NC	NC	NC
F	NC	NC	NC	NC	NC	NC
G	NC	I/O0	NC	NC	NC	Vcc
H	NC	I/O1	NC	Vcc	I/O5	I/O7
	Vss	I/O2	I/O3	I/O4	I/O6	Vss
	N.C	N.C			N.C	N.C
	N.C	N.C			N.C	N.C

Top View

SAMSUNG
ELECTRONICS

PACKAGE DEMENSIONS(FBGA)

Top View

Bottom View

#A1 INDEX MARK(OPTIONAL)

9.50±0.10

0.80 x 9= 7.20

0.80 x 5= 4.00

0.80

9.50±0.10

6   5   4   3   2   1

#A1

(Datum A)

0.80

12.00±0.10

A

B

0.80 x 7= 5.60

(Datum B)   C

D

12.00±0.10

0.80 x 11= 8.80

E

2.80   F

G

H

63-⌀0.45±0.05

⊕ ⌀ 0.20 Ⓜ A B

2.00

Side View

0.25(Min.)

1.20(Max)

12.00±0.10

⌀ 0.10MAX

0.45±0.05

SAMSUNG
ELECTRONICS

PIN DESCRIPTION

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$	**CHIP ENABLE** The $\overline{CE}$ input is the device selection control. When the device is in the Busy state, $\overline{CE}$ high is ignored, and the device does not return to standby mode in program or erase opertion. Regarding $\overline{CE}$ control during read operation, refer to 'Page read' section of Device operation .
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$	**READY/BUSY OUTPUT** The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	**POWER** VCC is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE:
1. Connect all VCC and VSS pins of each device to common power supply outputs.
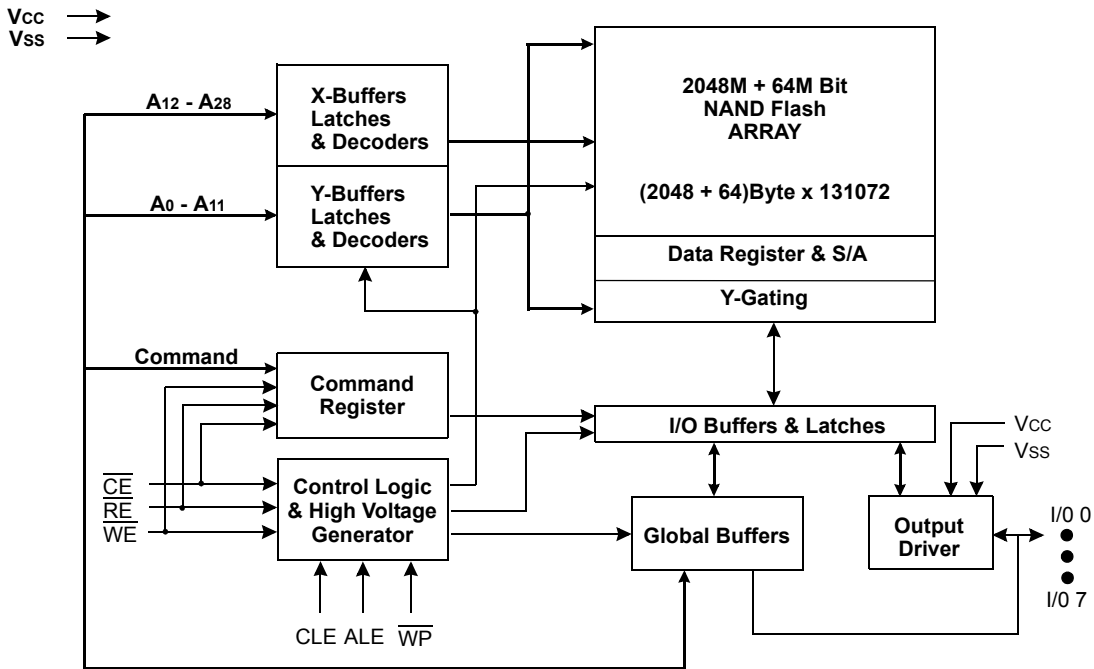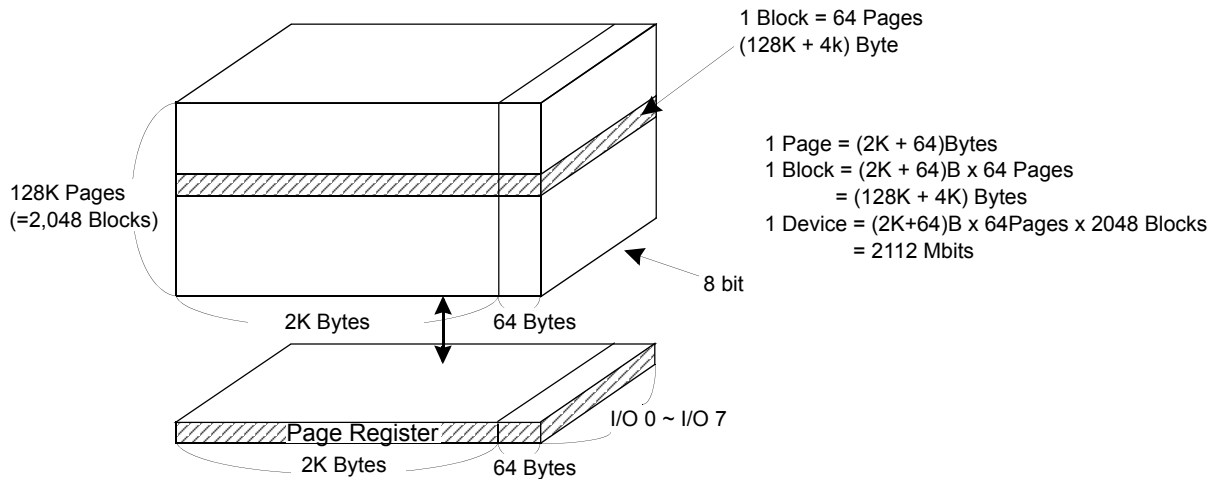2. Do not leave VCC or VSS disconnected.

Figure 1. Functional Block Diagram

Figure 2 Array Organization

1 Block = 64 Pages
(128K + 4k) Byte

1 Page = (2K + 64)Bytes
1 Block = (2K + 64)B x 64 Pages
        = (128K + 4K) Bytes
1 Device = (2K+64)B x 64Pages x 2048 Blocks
        = 2112 Mbits

128K Pages
(=2,048 Blocks)

2K Bytes   64 Bytes   8 bit

Page Register   I/O 0 ~ I/O 7

2K Bytes   64 Bytes

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	**Column Address**
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	**Row Address**
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	**Row Address**
5th Cycle	A_{28}	*L	*L	*L	*L	*L	*L	*L	**Row Address**

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than required.

SAMSUNG
ELECTRONICS

Product Introduction

The K9K2G08X0A is a 2112Mbit(2,214,592,512 bit) memory organized as 131,072 rows(pages) by 2112x8 columns. Spare 64 columns are located from column address of 2048~2111. A 2112-byte data register is connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structures. A NAND structure consists of 32 cells. Total 135,168 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 2048 separately erasable 128K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9K2G08X0A.

The K9K2G08X0A has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command and etc require just one cycle bus. Some other commands, like Page Read, Block Erase and Page Program, require two cycles: one cycle for setup and the other cycle for execution. The 264M byte physical space requires 29 addresses, thereby requiring five cycles for addressing: 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9K2G08X0A.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input[1]	85h	-	
Random Data Output[1]	05h	E0h	
Read Status	70h		O

NOTE : 1. Random Data Input/Output can be executed in a page.

      2. Cache program and Copy-Back program are supported only with 3.3V device.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating		Unit
			1.8V DEVICE	3.3V DEVICE	
Voltage on any pin relative to Vss		$V_{IN/OUT}$	-0.6 to + 2.45	-0.6 to + 4.6	V
		V_{CC}	-0.6 to + 2.45	-0.6 to + 4.6	
Temperature Under Bias	K9K2G08X0A-XCB0	T_{BIAS}	-10 to +125		°C
	K9K2G08X0A-XIB0		-40 to +125		
Storage Temperature	K9K2G08X0A-XCB0	T_{STG}	-65 to +150		°C
	K9K2G08X0A-XJIB0				
Short Circuit Current		Ios	5		mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS
(Voltage reference to GND, :T_A=0 to 70°C, K9K2G08X0A-XIB0:T_A=-40 to 85°C)

Parameter	Symbol	K9K2G08R0A(1.8V)			K9K2G08U0A(3.3V)			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Supply Voltage	V_{CC}	1.65	1.8	1.95	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	K9K2G08R0A(1.8V)			K9K2G08U0A(3.3V)			Unit
				Min	Typ	Max	Min	Typ	Max	
Operating Current	Page Read with Serial Access	Icc1	tRC=50ns, (30ns with 3.3V device) $\overline{CE}$=V_{IL} I_{OUT}=0mA	-	10	20	-	10	30	mA
	Program	Icc2	-	-	10	20	-	10	30	
	Erase	Icc3	-	-	10	20	-	10	30	
Stand-by Current(TTL)		Isb1	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	-	-	1	μA
Stand-by Current(CMOS)		Isb2	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	20	100	-	20	100	
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±20	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±20	-	-	±10	
Input High Voltage		V_{IH}	-	0.8xVcc	-	Vcc+0.3	0.8xVcc	-	Vcc+0.3	V
Input Low Voltage, All inputs		V_{IL}	-	-0.3	-	0.2xVcc	-0.3	-	0.2xVcc	
Output High Voltage Level		V_{OH}	K9K2G08R0A: I_{OH}=-100μA K9K2G08U0A: I_{OH}=-400μA	Vcc-0.1	-	-	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9K2G08R0A: I_{OL}=100mA K9K2G08U0A: I_{OL}=2.1mA	-	-	0.1	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	K9K2G08R0A: V_{OL}=0.1V K9K2G08U0A: V_{OL}=0.4V	3	4	-	8	10	-	mA

![SAMSUNG ELECTRONICS logo]

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	2008	-	2048	Blocks

NOTE :
1. The K9K2G08X0A may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block and does not require Error Correction up to 1K Program/ Earase cycles..

AC TEST CONDITION
(K9K2G08X0A-XCB0 :TA=0 to 70°C, K9K2G08X0A-XIB0:TA=-40 to 85°C
 K9K2G08R0A : Vcc=1.65V~1.95V, K9K2G08U0A : Vcc=2.7V~3.6Vunless otherwise noted)

Parameter	K9K2G08R0A	K9K2G08U0A
Input Pulse Levels	0V to Vcc	0V to Vcc
Input Rise and Fall Times	5ns	5ns
Input and Output Timing Levels	Vcc/2	Vcc/2
Output Load	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF

CAPACITANCE(TA=25C, VCC=1.8V/3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⌐_⌐	H	X	Read Mode	Command Input
L	H	L	⌐_⌐	H	X		Address Input(5clock)
H	L	L	⌐_⌐	H	H	Write Mode	Command Input
L	H	L	⌐_⌐	H	H		Address Input(5clock)
L	L	L	⌐_⌐	H	H	Data Input	
L	L	L	H	‾⌐_	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
   2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}*1	-	200	700	μs
Dummy Busy Time for Cache Program		t_{CBSY}*2		3	700	μs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	4	cycles
	Spare Array		-	-	4	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

NOTE : 1.Typical program time is defined as the time within which more than 50% of whole pages are programmed at Vcc of 3.3V and 25°C

   2. Max. time of t_{CBSY} depends on timing between internal program completion and data in

SAMSUNG
ELECTRONICS

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9K2G08R0A	K9K2G08U0A	K9K2G08R0A	K9K2G08U0A	
CLE setup Time	t_{CLS}[1]	25	15	-	-	ns
CLE Hold Time	t_{CLH}	10	5	-	-	ns
$\overline{CE}$ setup Time	t_{CS}[1]	35	20	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	5	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	15	-	-	ns
ALE setup Time	t_{ALS}[1]	25	15	-	-	ns
ALE Hold Time	t_{ALH}	10	5	-	-	ns
Data setup Time	t_{DS}[1]	20	15	-	-	ns
Data Hold Time	t_{DH}	10	5	-	-	ns
Write Cycle Time	t_{WC}	45	30	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	10	-	-	ns
Address to Data Loading Time	t_{ADL}[2]	100[2]	100[2]	-	-	ns

NOTE : 1. The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low.
    2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
    3. **For cache program operation, the whole AC Charcateristics must be same as that of K9K2G08R0A.**

AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9K2G08R0A	K9K2G08U0A	K9K2G08R0A	K9K2G08U0A	
Data Transfer from Cell to Register	t_R	-	-	25	25	μs
ALE to $\overline{RE}$ Delay	t_{AR}	10	10	-	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	10	-	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	20	-	-	ns
RE Pulse Width	t_{RP}	25	15	-	-	ns
WE High to Busy	t_{WB}	-	-	100	100	ns
Read Cycle Time	t_{RC}	50	30	-	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	-	30	20	ns
$\overline{CE}$ Access Time	t_{CEA}	-	-	45	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	-	30	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	-	20	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	15	-	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	10	-	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	0	-	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	60	-	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	-	5/10/500[1]	5/10/500[1]	μs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
    2. **For cache program operation, the whole AC Charcateristics must be same as that of K9K2G08R0A.**

SAMSUNG
ELECTRONICS

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, does not require Error Correction up to 1K Program/Erase cycles.

Identifying Initial Invalid Block(s)

All device locations are erased except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.
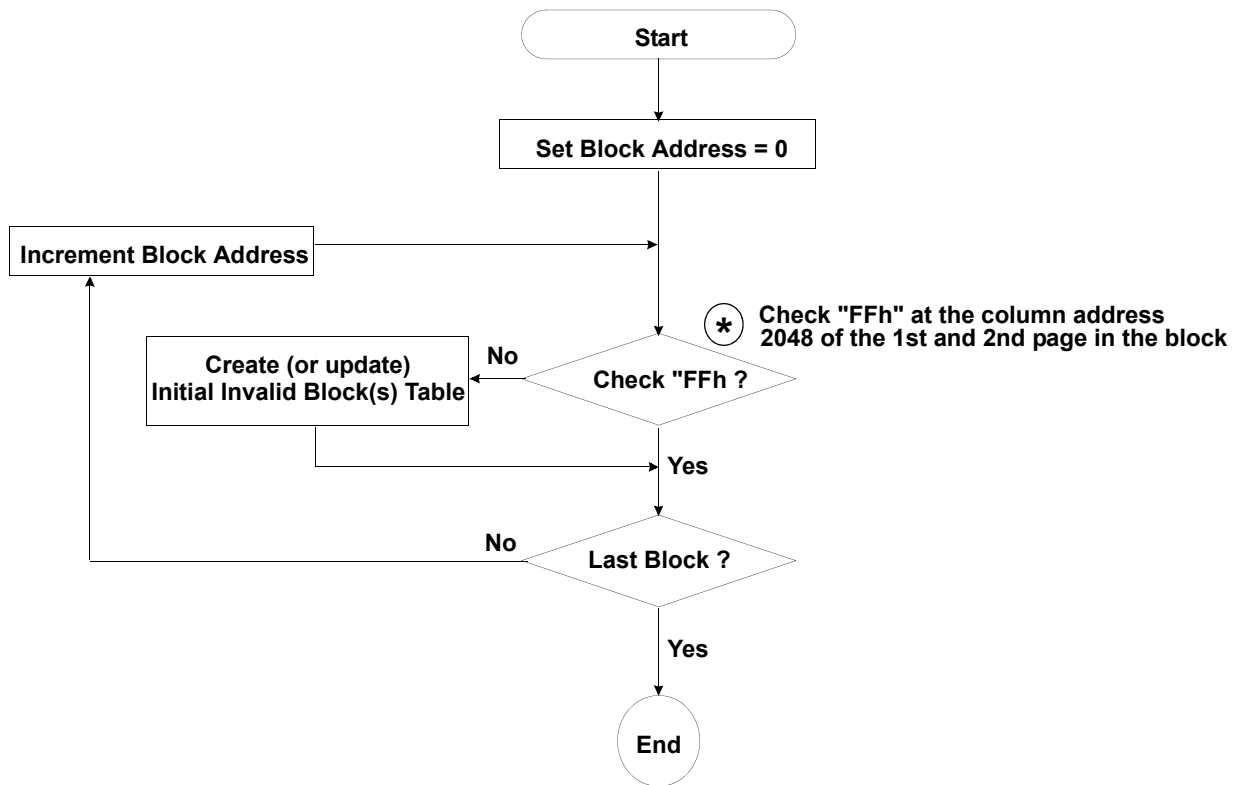
Figure 3. Flow chart to create initial invalid block table.

NAND Flash Technical Notes *(Continued)*

Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

<u>**ECC**</u>   : Error Correcting Code --> Hamming Code etc.
          Example) 1bit correction & 2bit detection

<u>Program Flow Chart</u>

```
                    ┌─────────────────┐
                    (     Start       )
                    └─────────────────┘
                             │
                    ┌─────────────────┐
                    │   Write 80h     │
                    └─────────────────┘
                             │
                    ┌─────────────────┐
                    │  Write Address  │
                    └─────────────────┘
                             │
                    ┌─────────────────┐
                    │   Write Data    │
                    └─────────────────┘
                             │
                    ┌─────────────────┐
                    │   Write 10h     │
                    └─────────────────┘
                             │
                    ┌──────────────────────┐
                    │ Read Status Register │◄───┐
                    └──────────────────────┘    │
                             │                   │
                          ╱─────────╲            │ No
                         ╱ I/O 6 = 1 ? ╲─────────┘
                         ╲ or R/B = 1 ? ╱
                          ╲─────────╱
                             │ Yes
       (*)              ╱─────────╲
  ( Program Error )◄───╱ I/O 0 = 0 ? ╲
                 No    ╲─────────╱
                             │ Yes
                    ┌──────────────────────┐
                    ( Program Completed    )
                    └──────────────────────┘
```
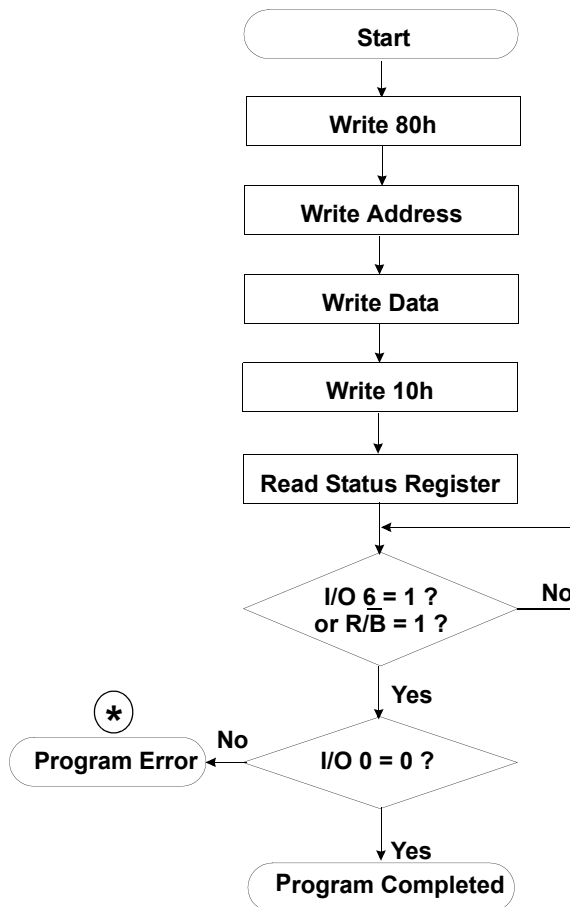
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

```
                Start
                  │
                  ▼
            Write 60h
                  │
                  ▼
        Write Block Address
                  │
                  ▼
            Write D0h
                  │
                  ▼
        Read Status Register  ◄──────┐
                  │                   │
                  ▼                   │ No
         ╱ I/O 6 = 1 ?  ╲ ───────────┘
         ╲ or R/B = 1 ? ╱
                  │
                 Yes
                  │
    ✱             ▼
           ╱ I/O 0 = 0 ? ╲  ── No ──►  Erase Error
           ╲             ╱
                  │
                 Yes
                  │
                  ▼
          Erase Completed
```

Read Flow Chart

```
                Start
                  │
                  ▼
            Write 00h
                  │
                  ▼
          Write  Address
                  │
                  ▼
            Write 30h
                  │
                  ▼
            Read Data
                  │
                  ▼
          ECC Generation
                  │
                  ▼
                         No
    Reclaim the Error ◄────── ╱ Verify ECC ╲
                             ╲             ╱
                                    │
                                   Yes
                                    │
                                    ▼
                         Page Read Completed
```
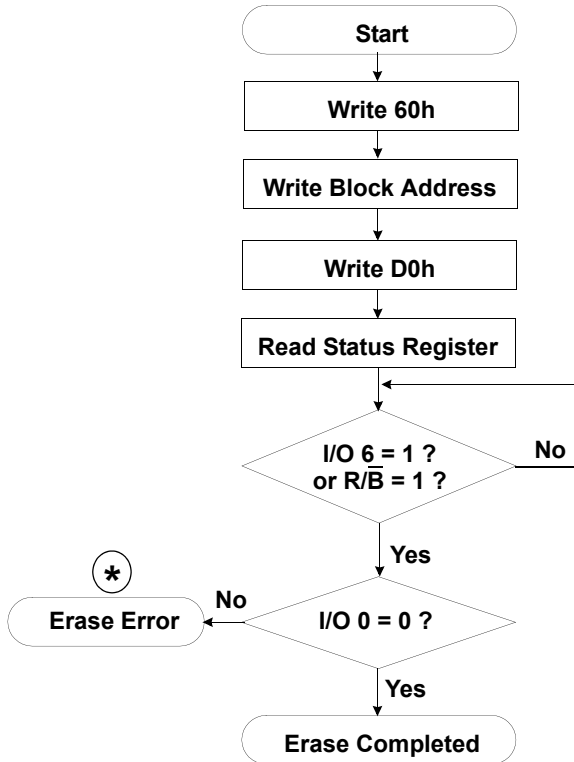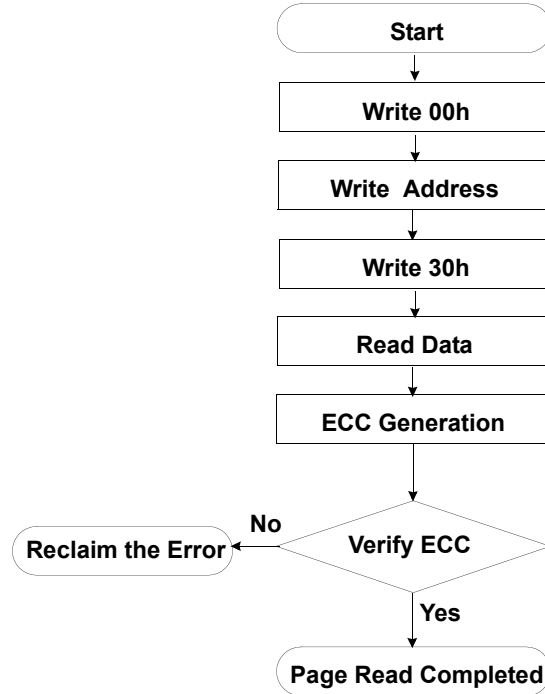
✱ : **If erase operation results in an error, map out the failing block and replace it with another block.**

Block Replacement

```
               Block A
1st  ⎧  ▨▨▨▨▨▨▨▨▨▨
~    ⎨  ▨▨▨▨▨▨▨▨▨▨          ①
(n-1)th⎩  ▨▨▨▨▨▨▨▨▨▨
nth ──►  an error occurs.         Buffer memory of the controller.
(page)                            ┌──────────────┐
                                  └──────────────┘
               Block B
1st  ⎧  ▨▨▨▨▨▨▨▨▨▨
~    ⎨  ▨▨▨▨▨▨▨▨▨▨          ②
(n-1)th⎩  ▨▨▨▨▨▨▨▨▨▨
nth ──►  
(page)
```
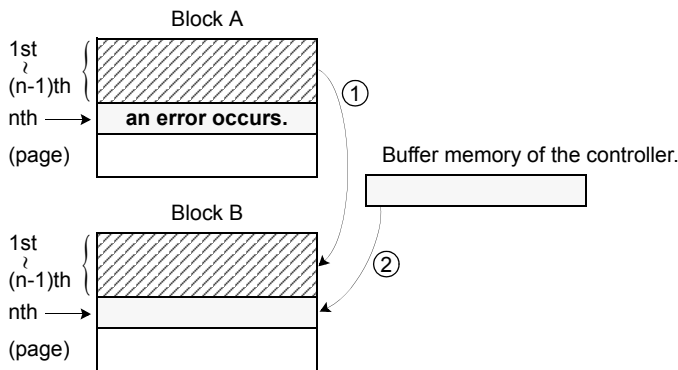
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes *(Continued)*

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited.

<table>
<tr><td>Page 63</td><td>(64)</td></tr>
<tr><td></td><td>:</td></tr>
<tr><td>Page 31</td><td>(32)</td></tr>
<tr><td></td><td>:</td></tr>
<tr><td>Page 2</td><td>(3)</td></tr>
<tr><td>Page 1</td><td>(2)</td></tr>
<tr><td>Page 0</td><td>(1)</td></tr>
</table>

Data register

<u>From the LSB page to MSB page</u>

DATA IN: Data (1) ⟶ Data (64)

<table>
<tr><td>Page 63</td><td>(64)</td></tr>
<tr><td></td><td>:</td></tr>
<tr><td>Page 31</td><td>(1)</td></tr>
<tr><td></td><td>:</td></tr>
<tr><td>Page 2</td><td>(3)</td></tr>
<tr><td>Page 1</td><td>(32)</td></tr>
<tr><td>Page 0</td><td>(2)</td></tr>
</table>

Data register

<u>Ex.) Random page program (Prohibition)</u>

DATA IN: Data (1) ⟶ Data (64)
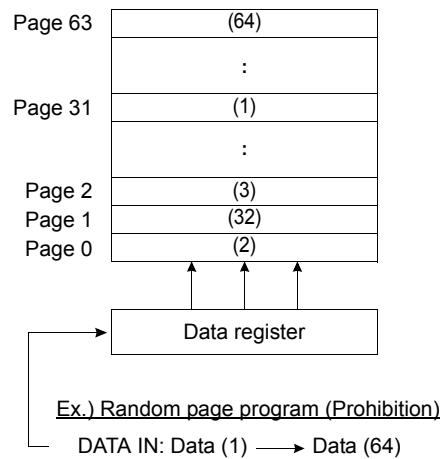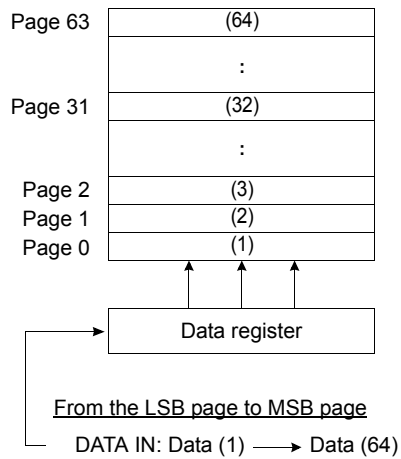
System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.
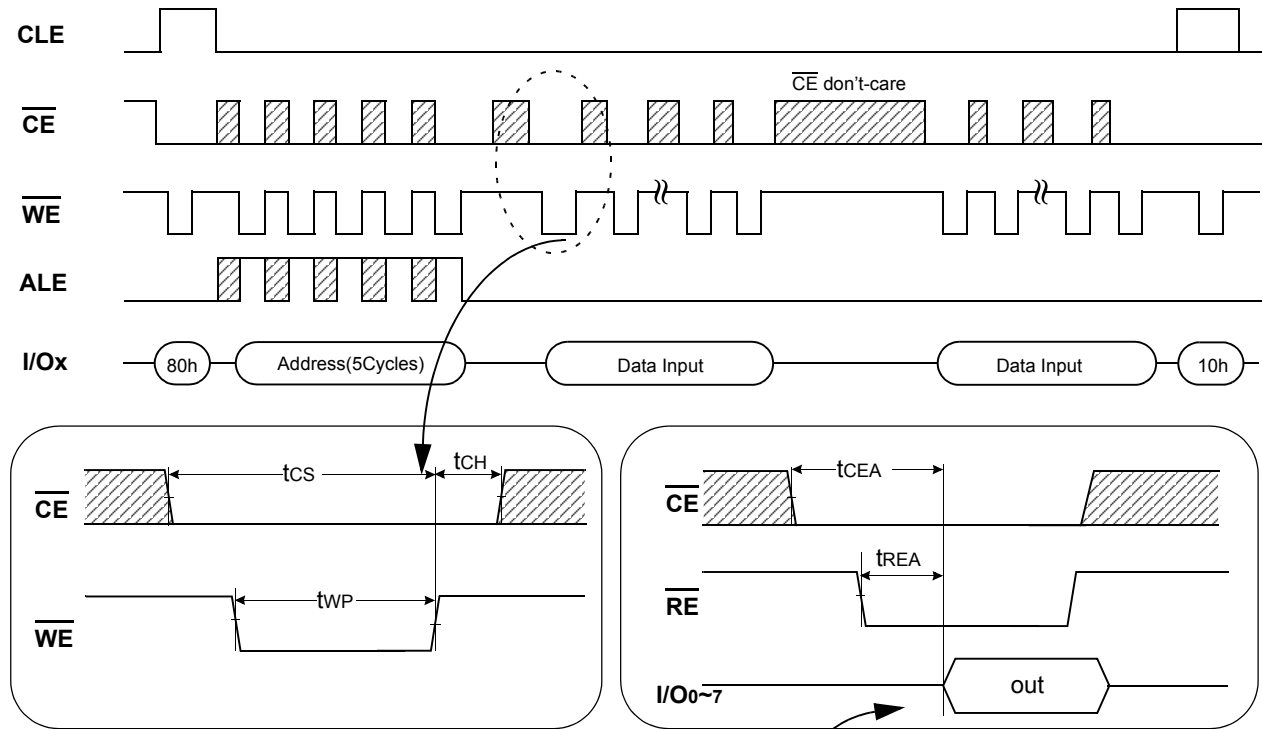
Figure 5. Read Operation with $\overline{CE}$ don't-care.
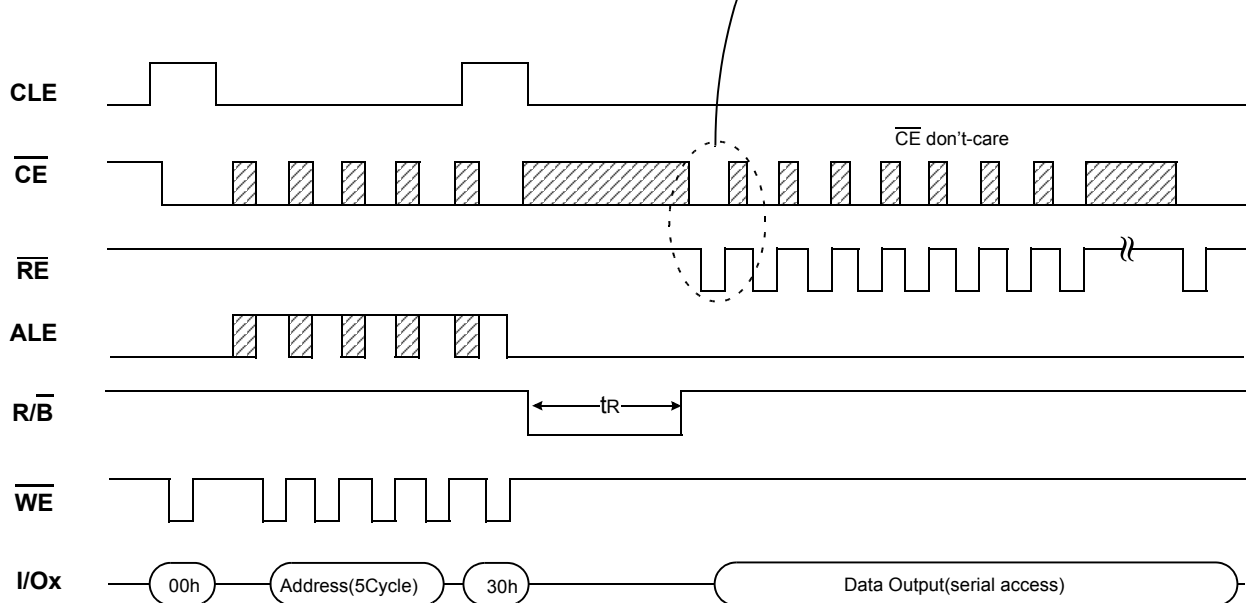
NOTE

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9K2G08X0A	I/O 0 ~ I/O 7	~2112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28

Command Latch Cycle
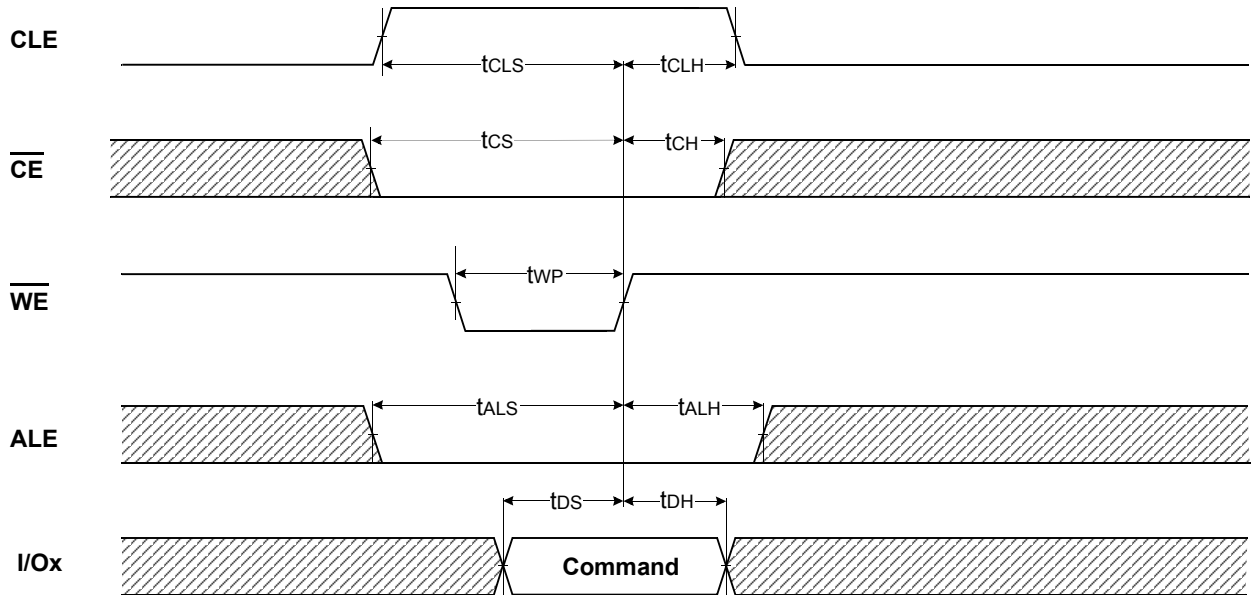
Address Latch Cycle
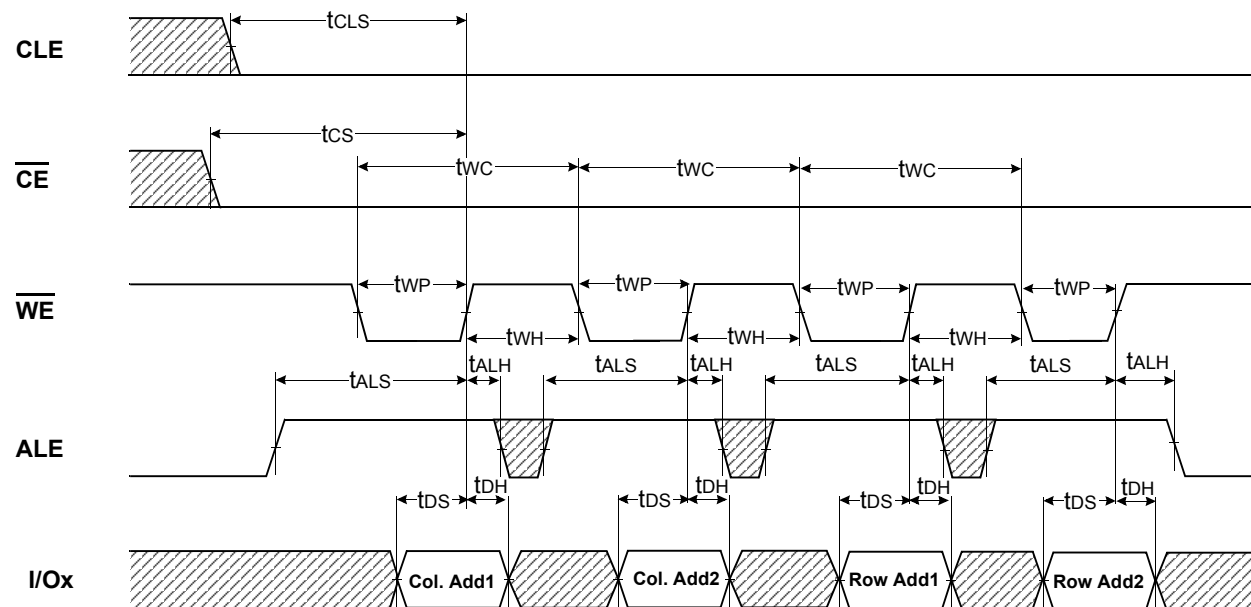
Input Data Latch Cycle
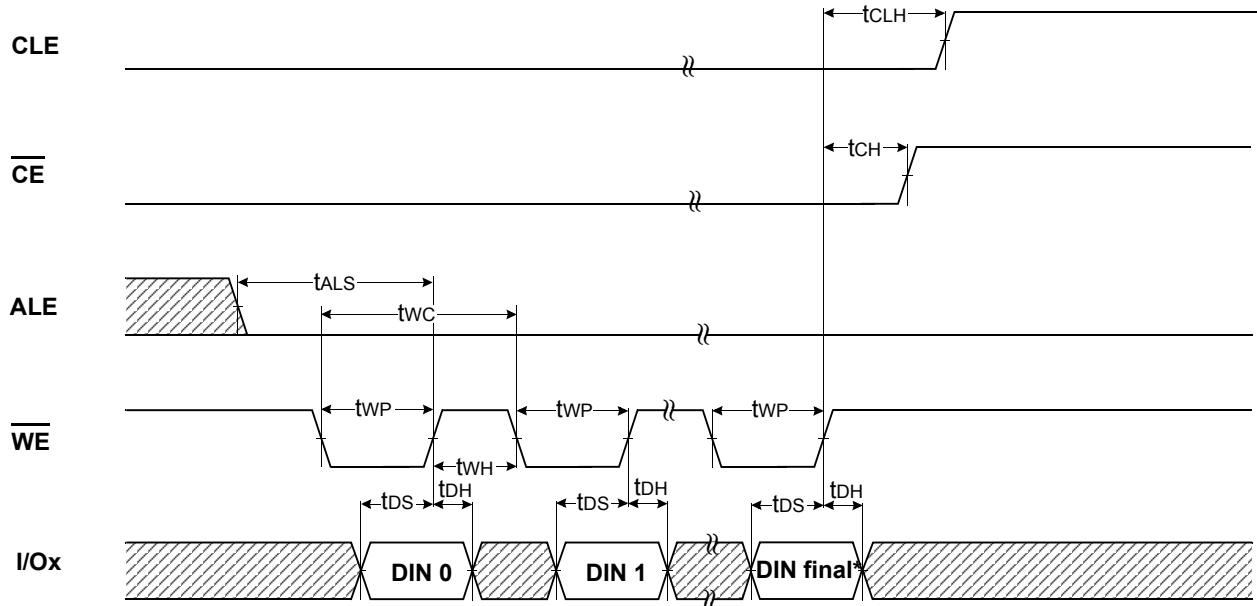
NOTES : DIN final means 2112

Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)
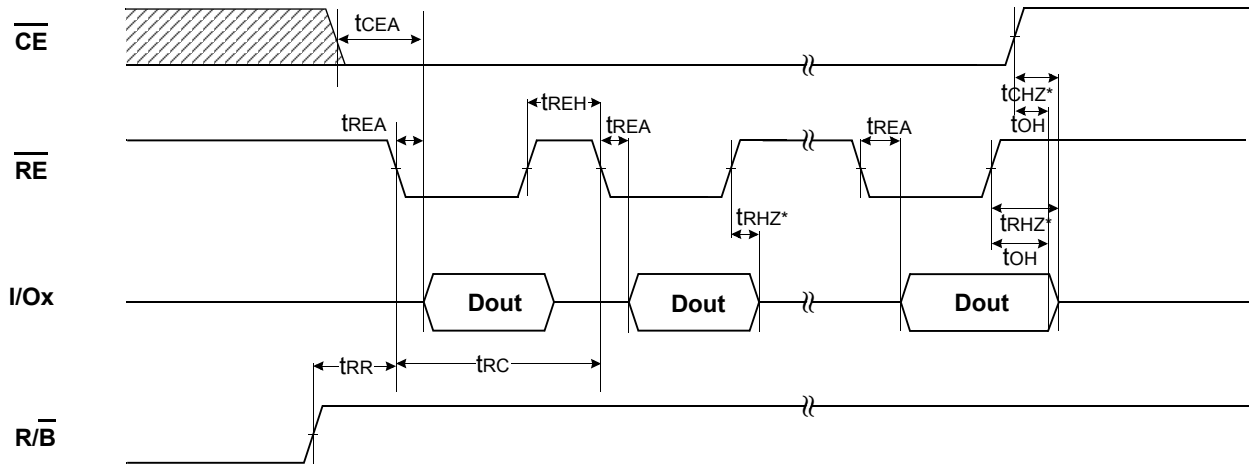
NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Status Read Cycle
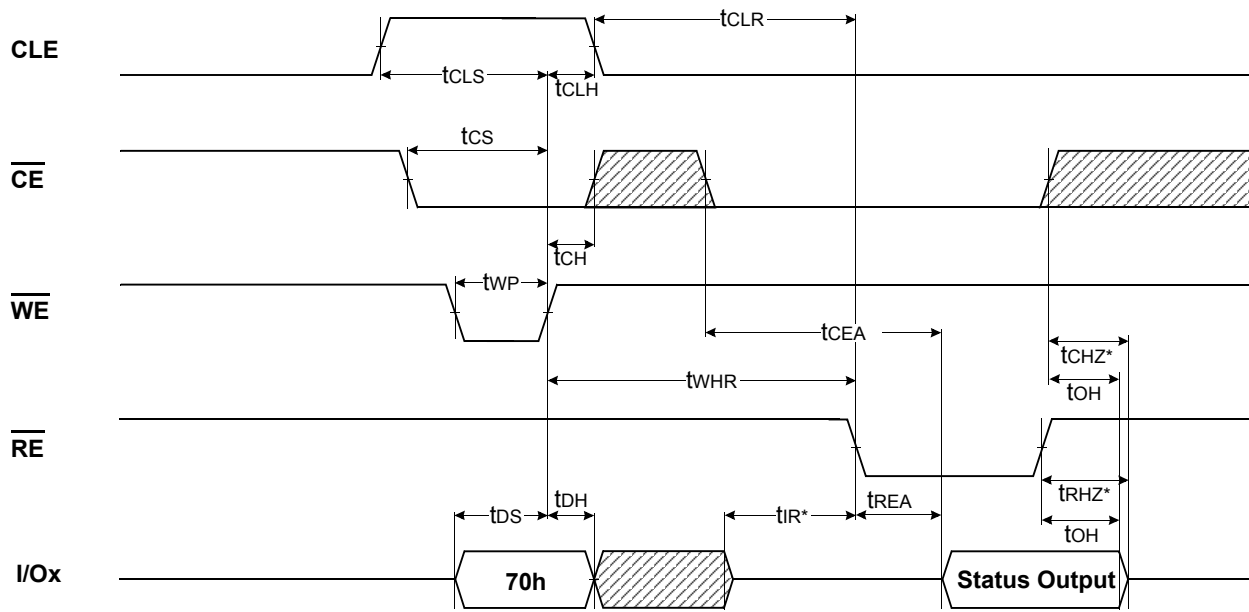
Read Operation
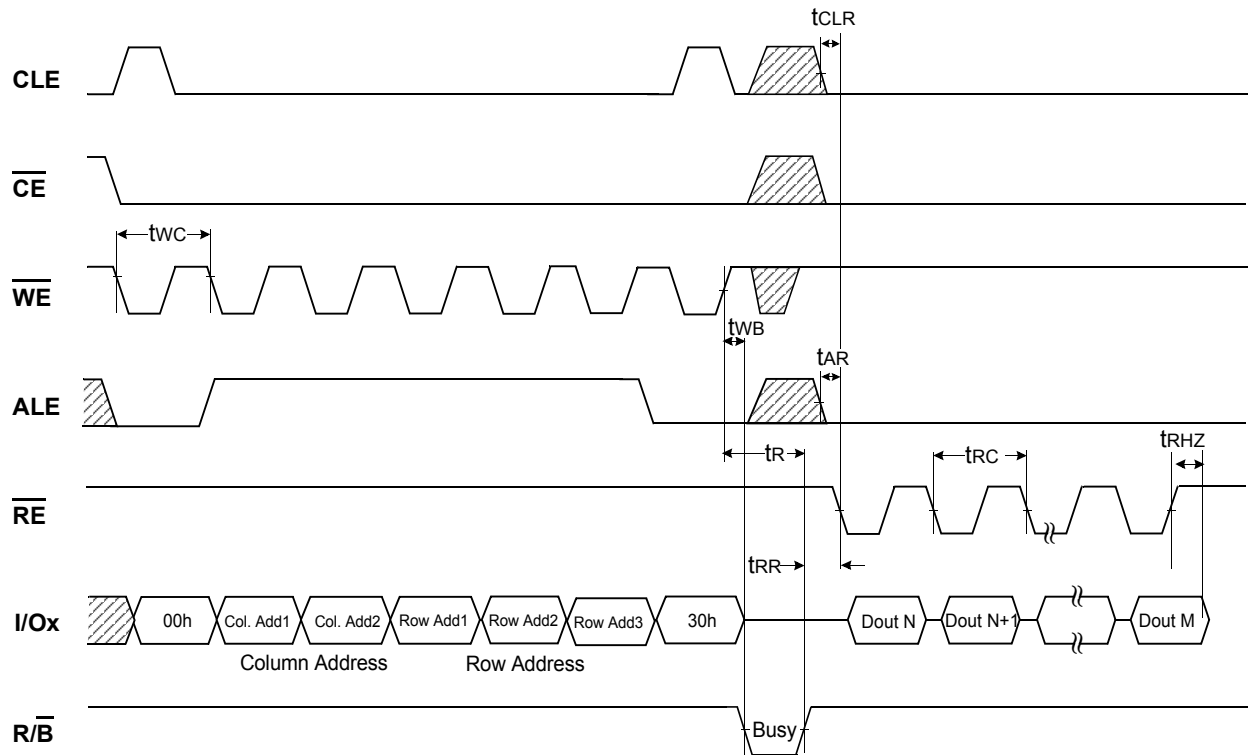
Read Operation(Intercepted by CE)
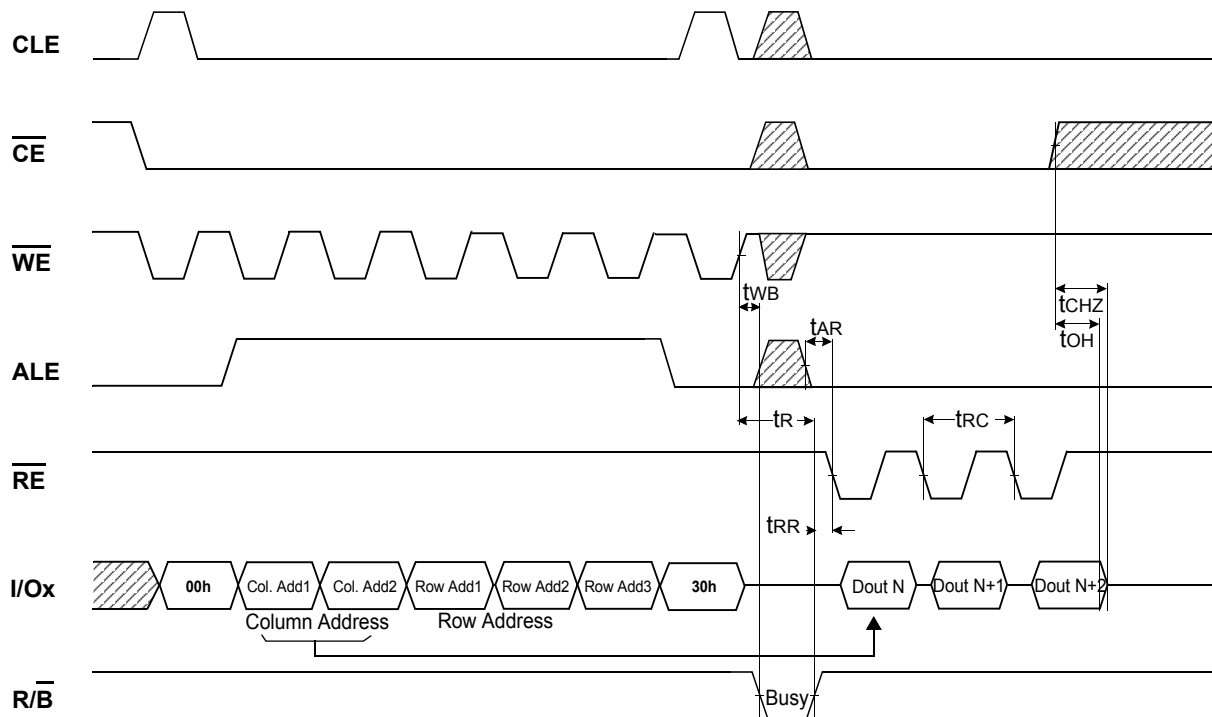
Random Data Output In a Page
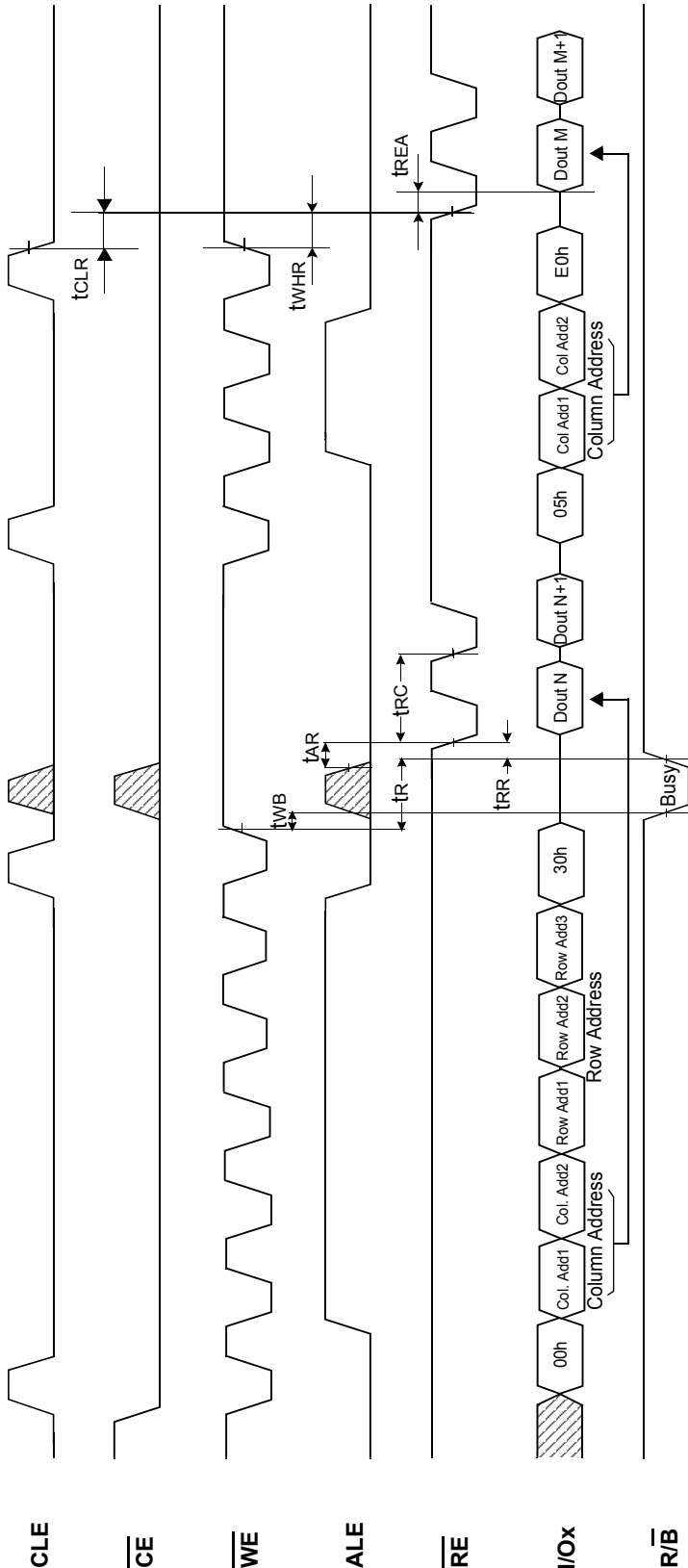
Page Program Operation
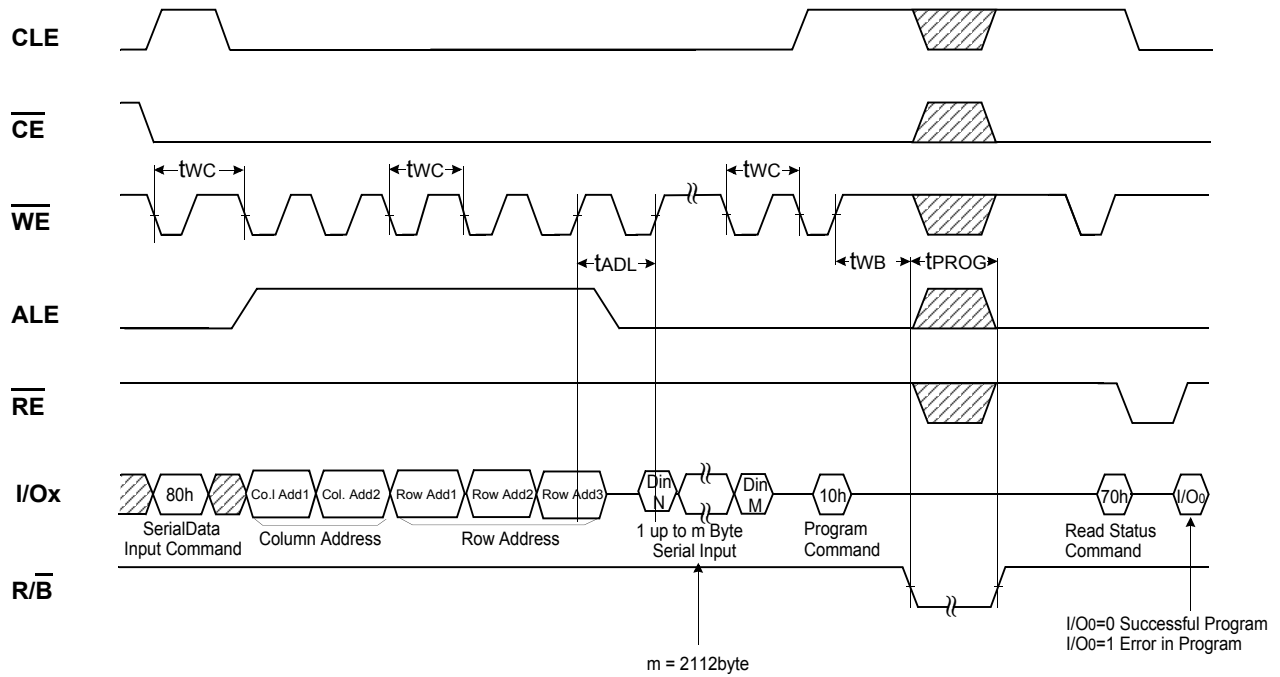
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Page Program Operation with Random Data Input
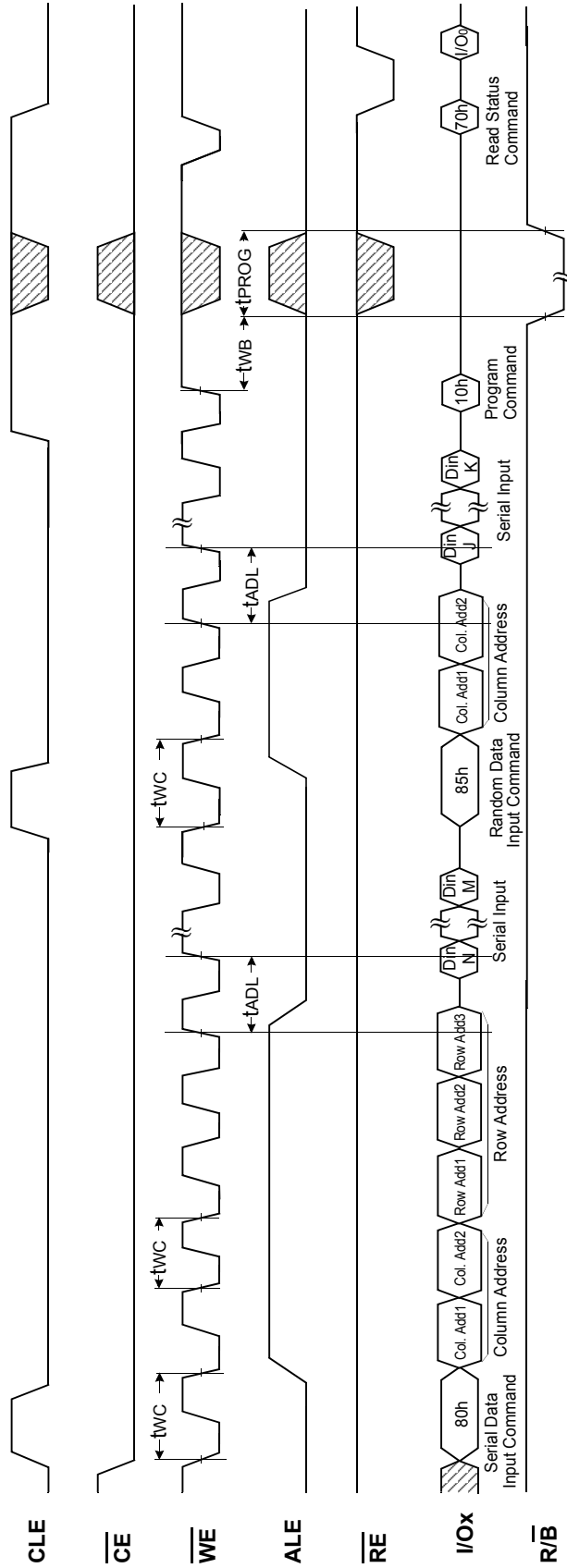
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Copy-Back Program Operation With Random Data Input
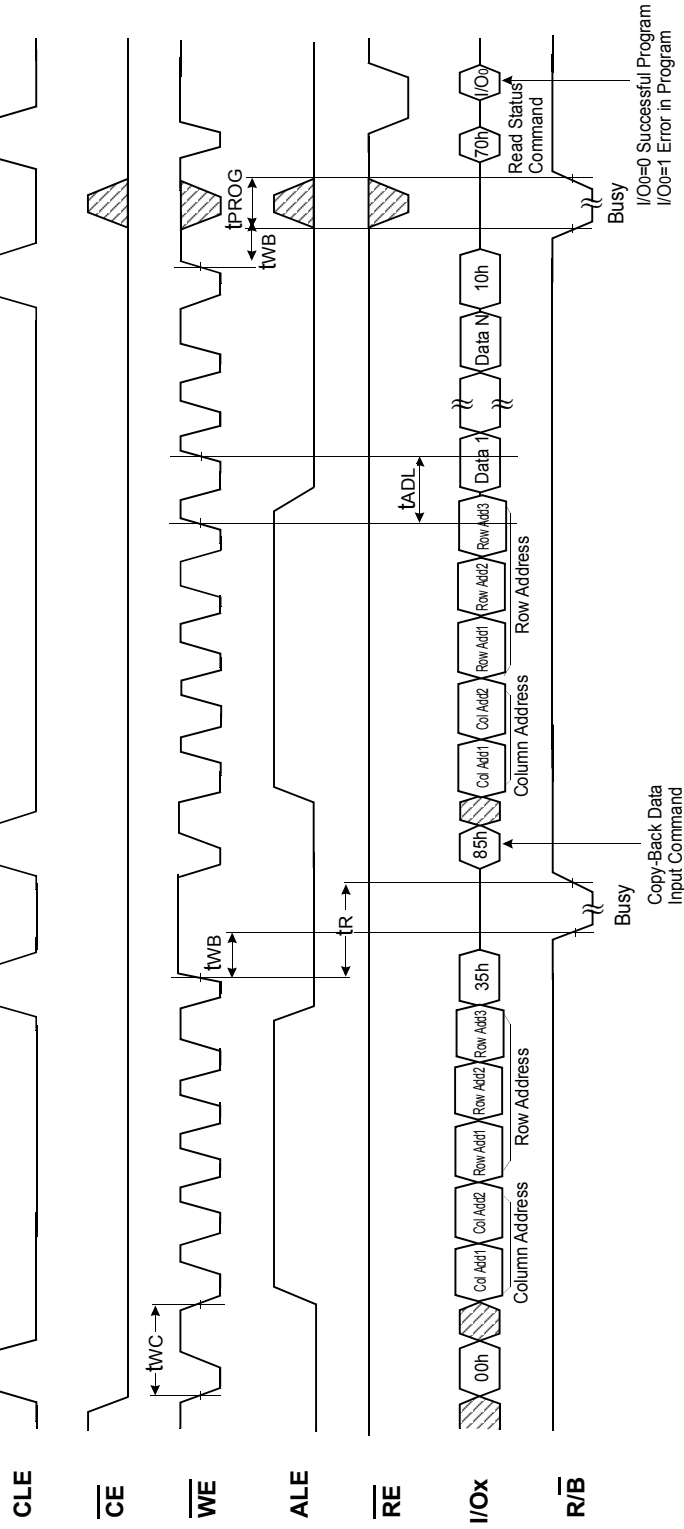
CLE

CE

WE

ALE

RE

I/Ox

R/B

twC

twB

tR

twB

tPROG

tWB

tADL

00h | Col Add1 | Col Add2 | Row Add1 | Row Add2 | Row Add3 | 35h

Column Address

Row Address

Busy

Copy-Back Data
Input Command

85h | Col Add1 | Col Add2 | Row Add1 | Row Add2 | Row Add3 | Data 1 | Data N | 10h

Column Address

Row Address

70h | I/O0

Read Status
Command

Busy

I/O0=0 Successful Program
I/O0=1 Error in Program

NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Cache Program Operation(available only within a block)

CLE

CE

WE

ALE

RE

I/Ox

R/B

tWC

Serial Data Column Address
Input Command

80h   Col Add1   Col Add2   Row Add1   Row Add2   Row Add3

Column Address   Row Address

Serial Data
Input Command

tADL

Din N   Din M   15h

Serial Input   Program Command (Dummy)

tWB   tCBSY

Max. 63 times repeatable

80h   Col Add1   Col Add2   Row Add1   Row Add2   Row Add3

tADL

Din N   Din M   10h   70h   I/O

Program Confirm Command (True)

tWB   tCPROG

Last Page Input & Program

tCBSY : max. 700us

NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Ex.) Cache Program

R/B

I/Ox

80h   Address & Data Input   15h   80h   Address & Data Input   15h   80h   Address & Data Input   15h   80h   Address & Data Input   10h   70h

Col Add1,2 & Row Add1,2
Data

tCBSY   tCBSY   tCBSY   tPROG

Block Erase Operation
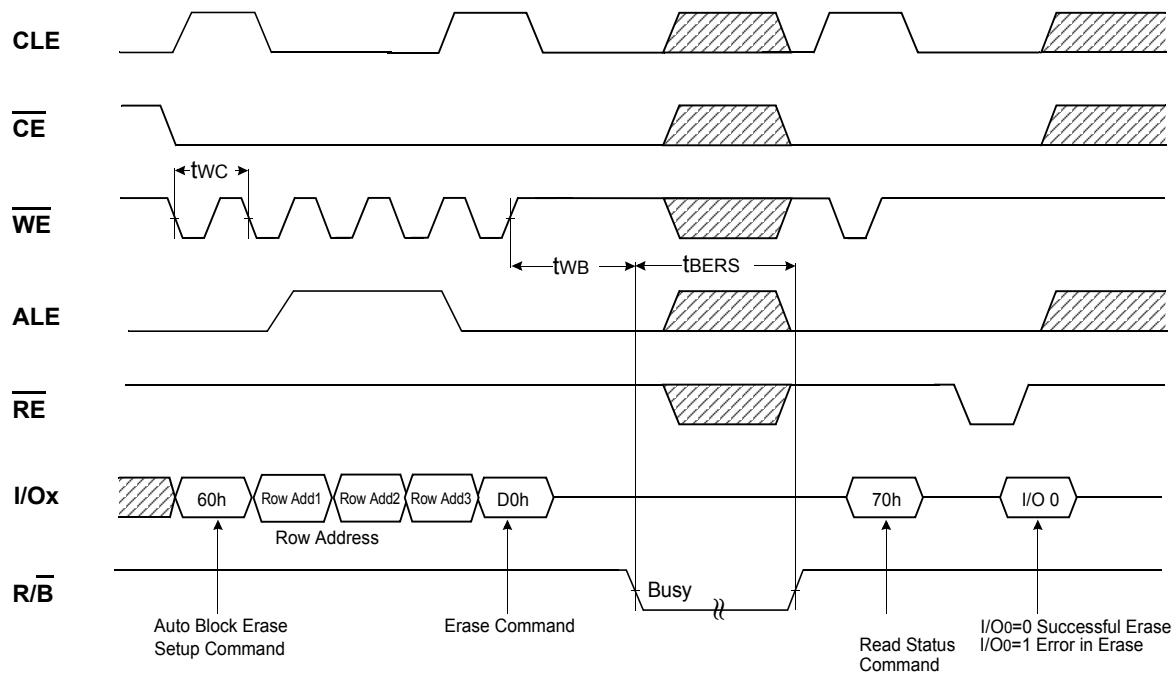
Read ID Operation
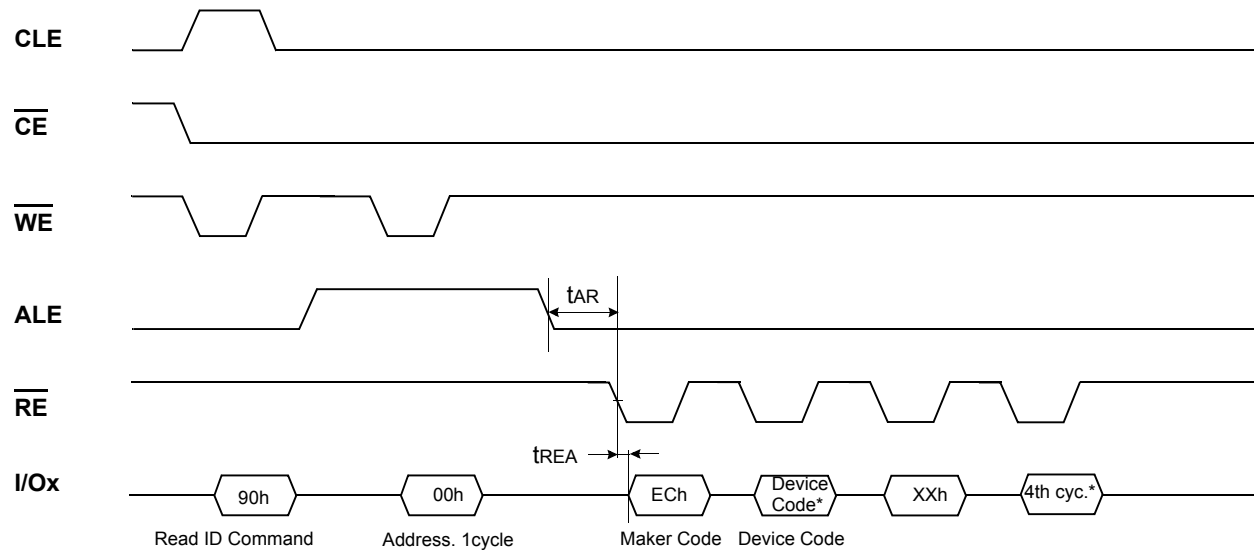
Device	Device Code*(2nd Cycle)	4th Cycle*
K9K2G08R0A	AAh	15h
K9K2G08U0A	DAh	15h

ID Defintition Table

90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Don't care
4th Byte	Page Size, Block Size, Spare Size, Organization

SAMSUNG
ELECTRONICS

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	Reserved							1	0
	Reserved							1	1
Blcok Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	Reserved			1	1				
Redundant Area Size (byte/512byte)	8						0		
	16						1		
Organization	x8		0						
	x16		1						
Serial AccessMinimum	50ns	0				0			
	Reserved	1				0			
	Reserved	0				1			
	Reserved	1				1			

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs(t$_R$). The system controller can detect the completion of this data transfer(t$_R$) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

Col Add1,2 & Row Add1,2,3

Data Field   Spare Field
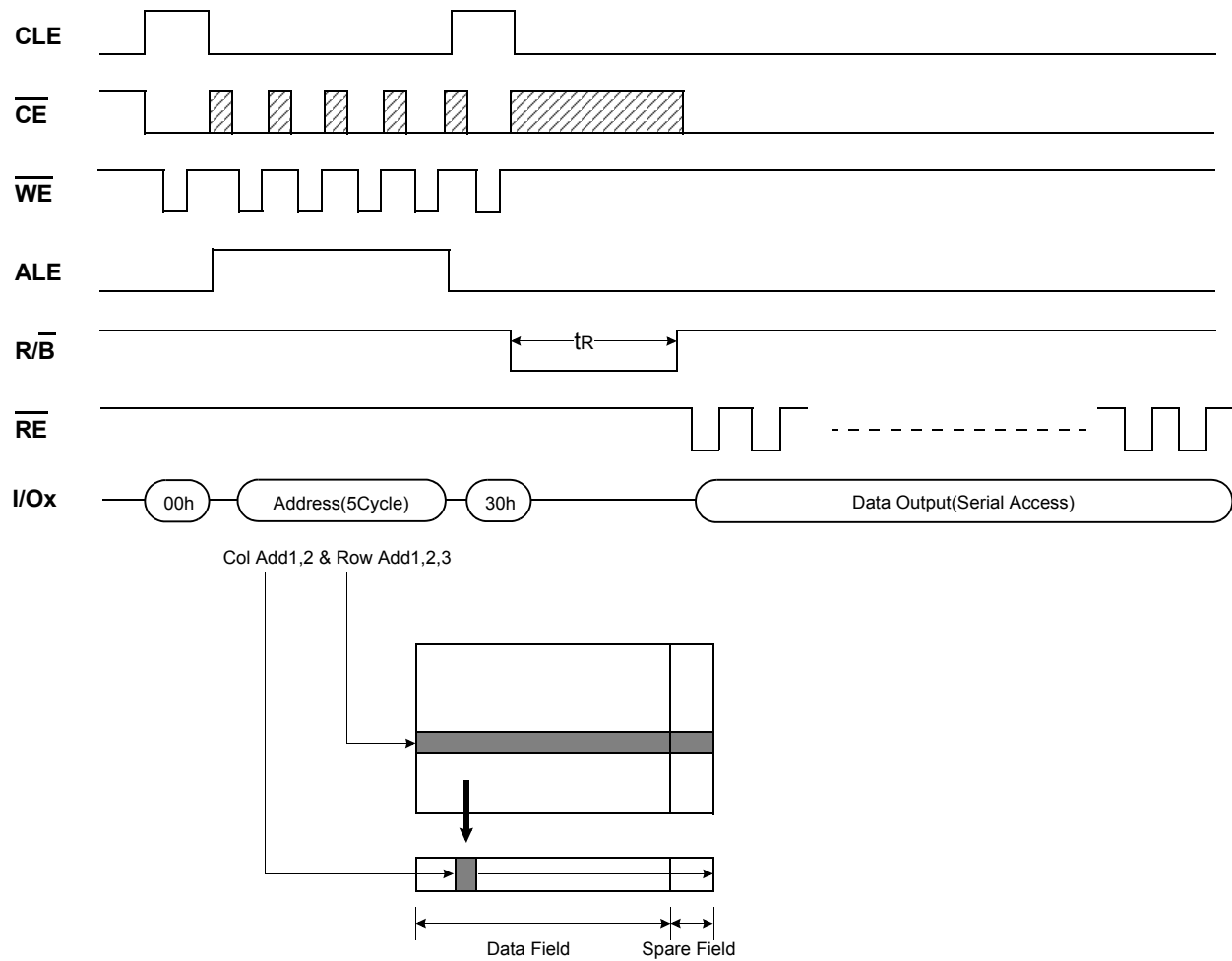
Figure 7. Random Data Output In a Page
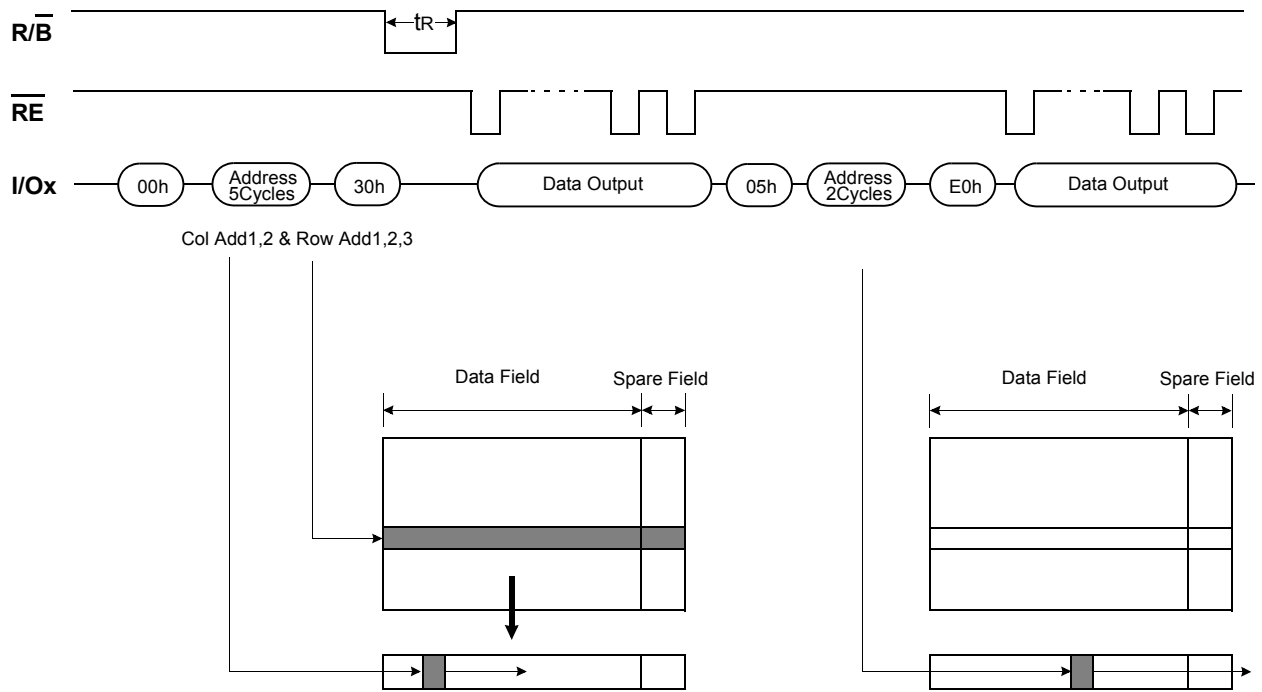
PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a word or consecutive bytes up to 2112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array(1time/512byte) and 4 times for spare array(1time/16byte). The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation
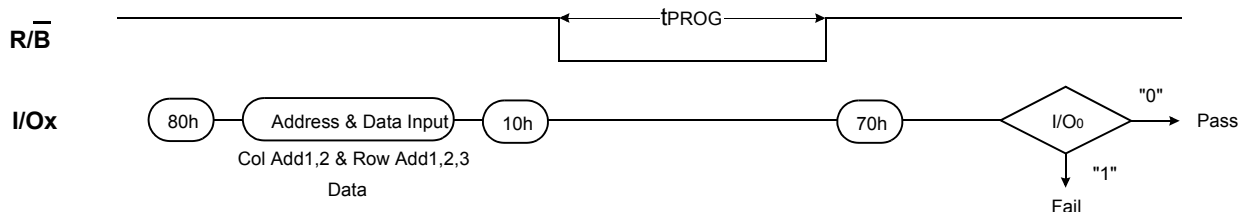
Figure 9. Random Data Input In a Page
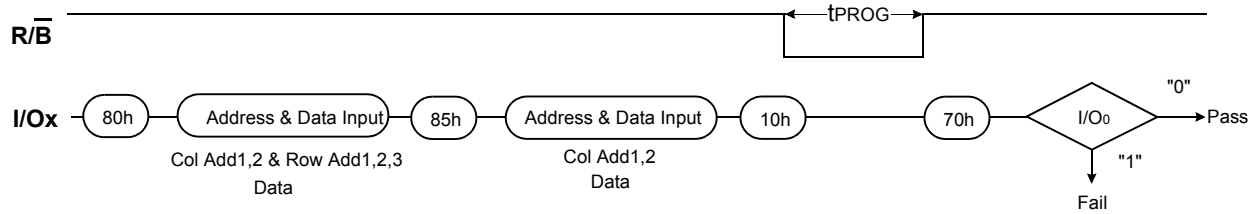
Cache Program

Cache Program is an extension of Page Program, which is executed with 2112byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2112byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previouse page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be progammed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked.

Figure 10. Cache Program(available only within a block)

SAMSUNG

ELECTRONICS
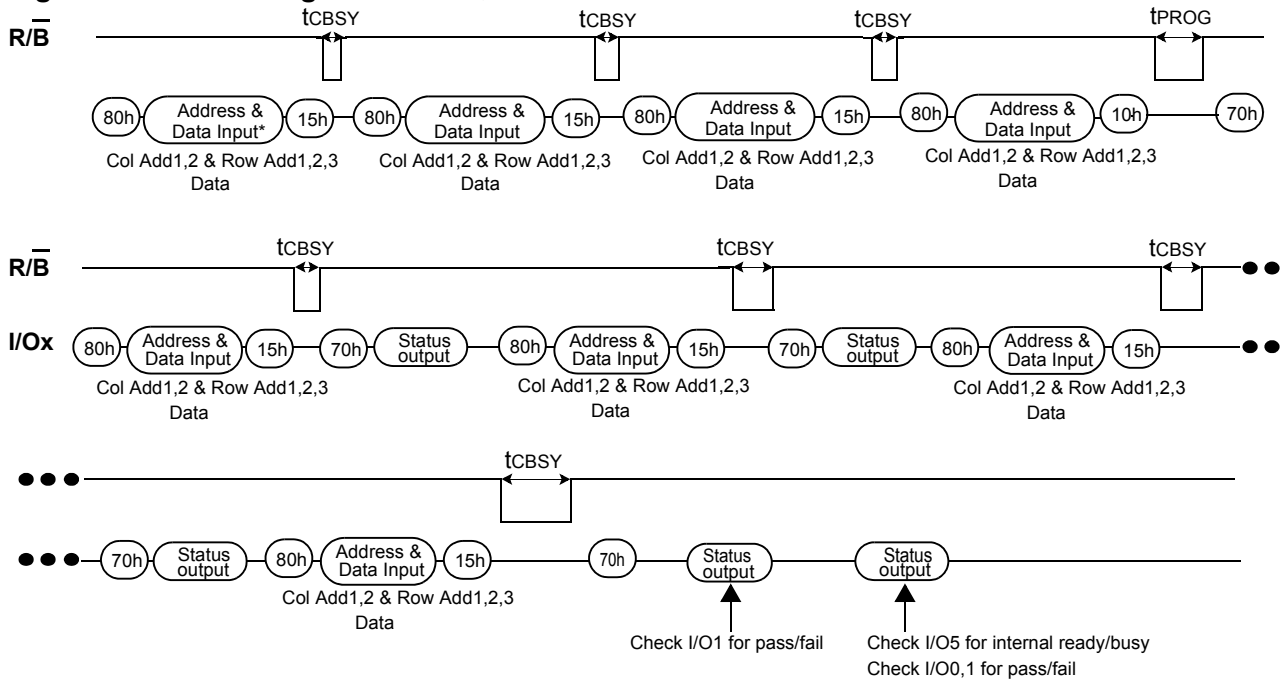
NOTE : Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG= Program time for the last page+ Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

Copy-Back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. A27 must be the same between source and target page. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 11. **"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But if the soure page has an error bit by charge loss, accumulated copy-back operations could also accumulate bit errors. In this case, verifying the source page for a bit error is recommended before Copy-back program"**

Figure 11. Page Copy-Back program Operation
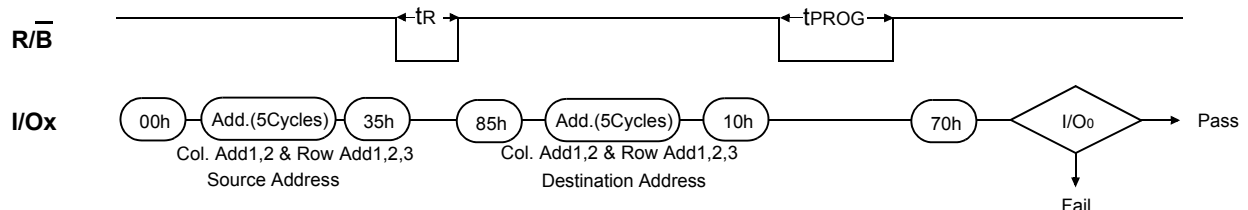
NOTE: It's prohibited to operate Copy-Back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the Copy-Back program is permitted just between odd address pages or even address pages.

## Figure 12. Page Copy-Back program Operation with Random Data Input
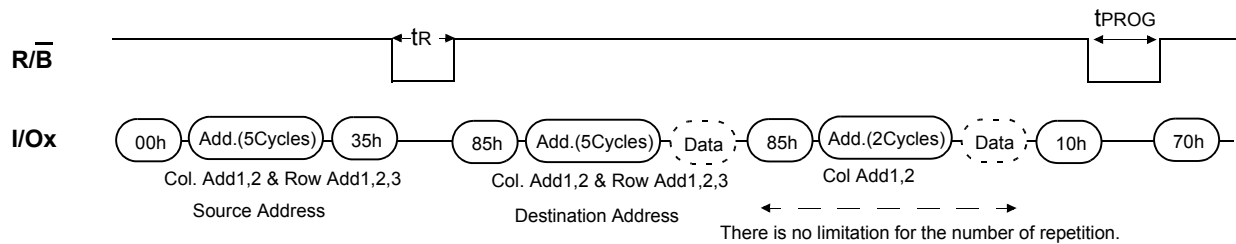
BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{28} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation
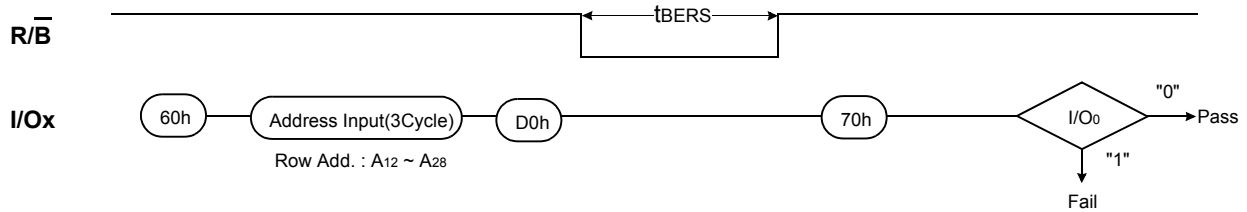
READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table2. Read Staus Register Definition

I/O No.	Page Program	Block Erase	Cache Prorgam	Read	Definition	
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not use	Pass : "0"	Fail : "1"
I/O 1	Not use	Not use	Pass/Fail(N-1)	Not use	Pass : "0"	Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Don't -cared	
I/O 3	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected

NOTE : 1. True Ready/Busy represents internal program operation status which is being executed in cache program mode.

2. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and XXh, 4th cycle ID, 15h respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 11 shows the operation sequence.

Figure 14. Read ID Operation
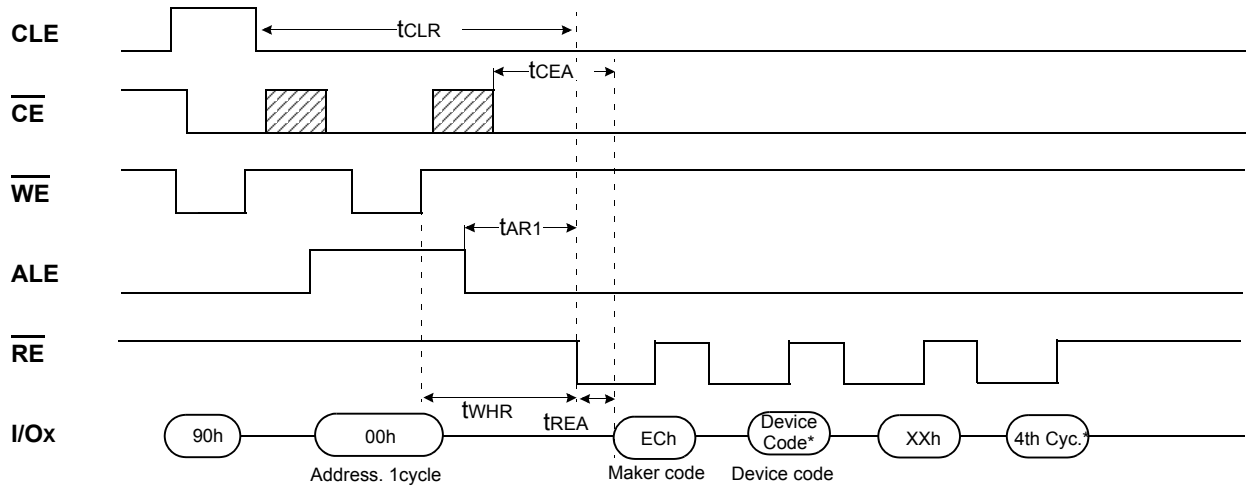
Device	Device Code*(2nd Cycle)	4th Cycle*
K9K2G08R0A	AAh	15h
K9K2G08U0A	DAh	15h

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Refer to Figure 12 below.

Figure 15. RESET Operation
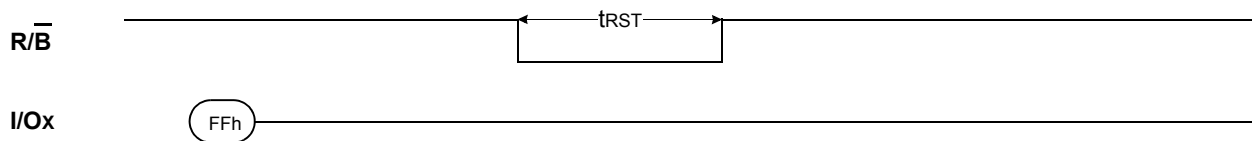
Table3. Device Status

	After Power-up	After Reset
Operation Mode	00h command is latched	Waiting for next command

READY/BUSY

The device has a R/B̄ output that provides a hardware method of indicating the completion of a page program, erase and random read. The R/B̄ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B̄ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B̄) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 13). Its value can be determined by the following guidance.
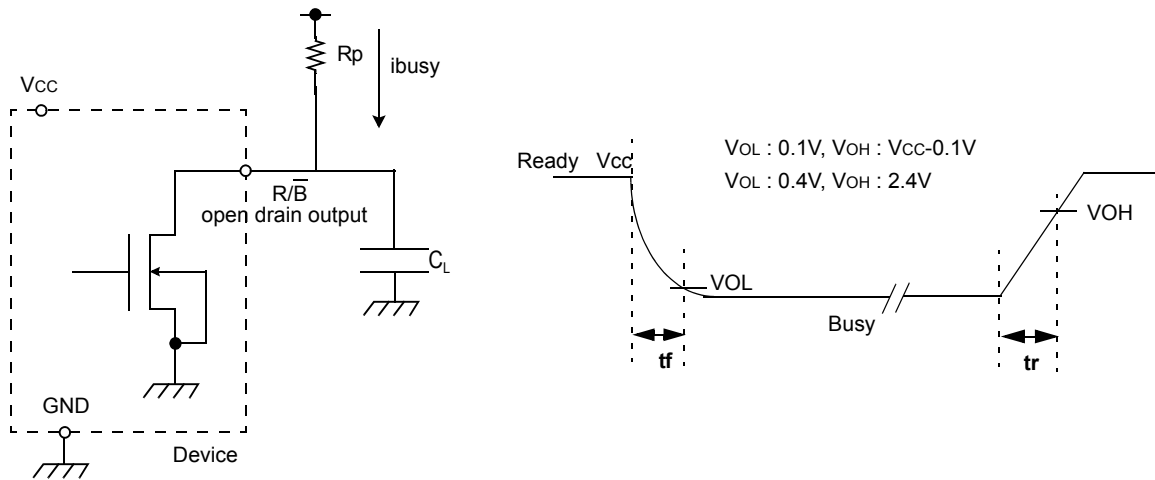
Figure 16. Rp vs tr ,tf &   Rp vs ibusy
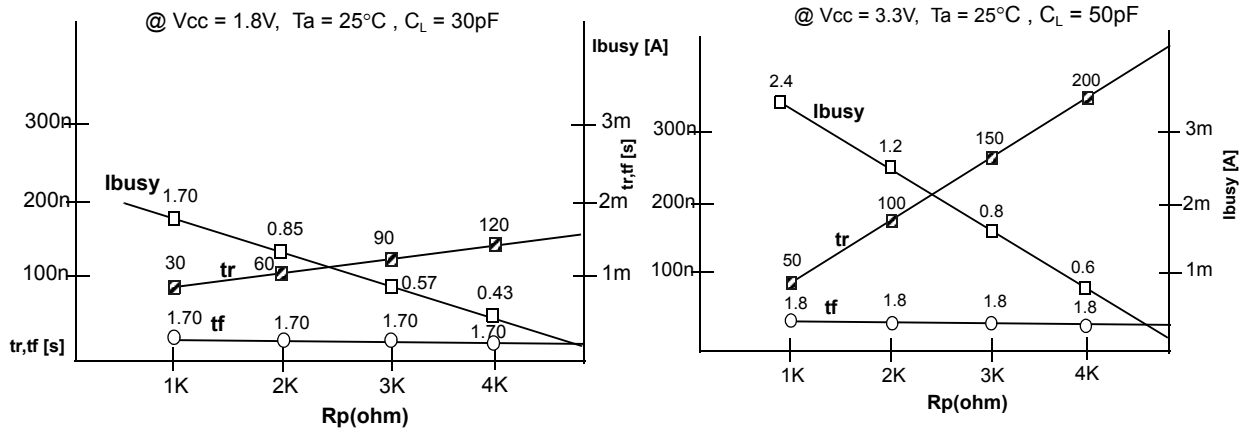
Rp value guidance

$$Rp(min, 1.8V \ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min, 3.3V \ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/B̄ pin.

Rp(max) is determined by maximum permissible limit of tr

SAMSUNG
ELECTRONICS

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power transitions. An internal voltage detector disables all functions whenever Vcc is below about 1.1V(1.8V device) and 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 14. The two step command sequence for program/erase provides additional software protection.

## Figure 17. AC Waveforms for Power Transition
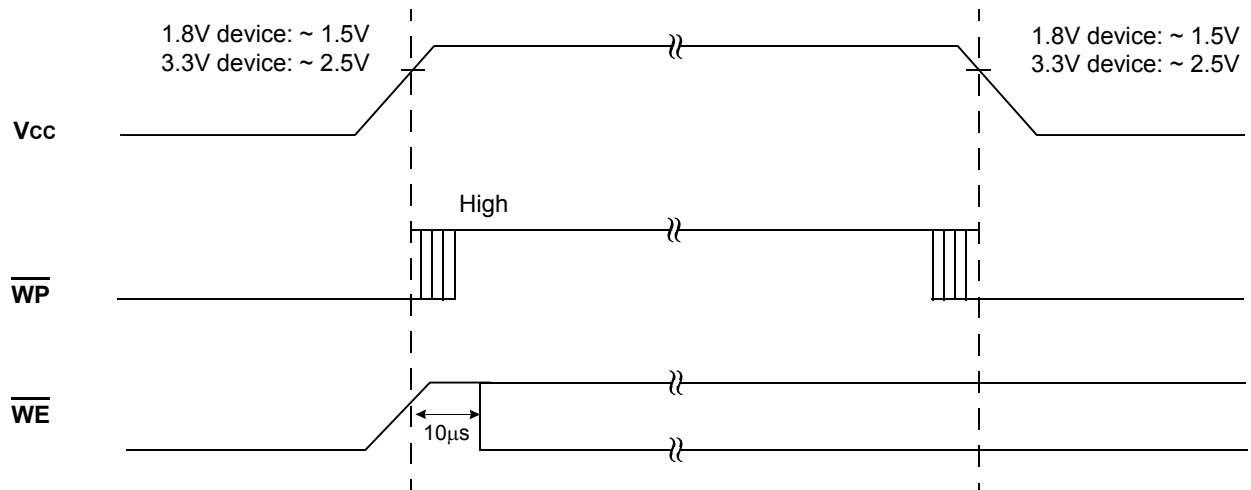
Extended Data Out Mode

For the EDO mode, the device should hold the data on the system memory bus until the beginning of the next cycle, so that controller could fetch the data at the falling edge. However NAND flash dosen't support the EDO mode exactly.
The device stops the data input into the I/O bus after $\overline{RE}$ rising edge. But since the previous data remains in the I/O bus, the flow of I/O data seems like Figure 18 and the system can access serially the data with EDO mode. tRLOH which is the parameter for fetching data at RE falling time is necessary. Its appropriate value can be obtained with the reference chart as shown in Figure 19. The tRHOH value depands on output load(C_L) and I/O bus Pull-up resistor (Rp).

Figure 18. Serial Access Cycle after Read(EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)
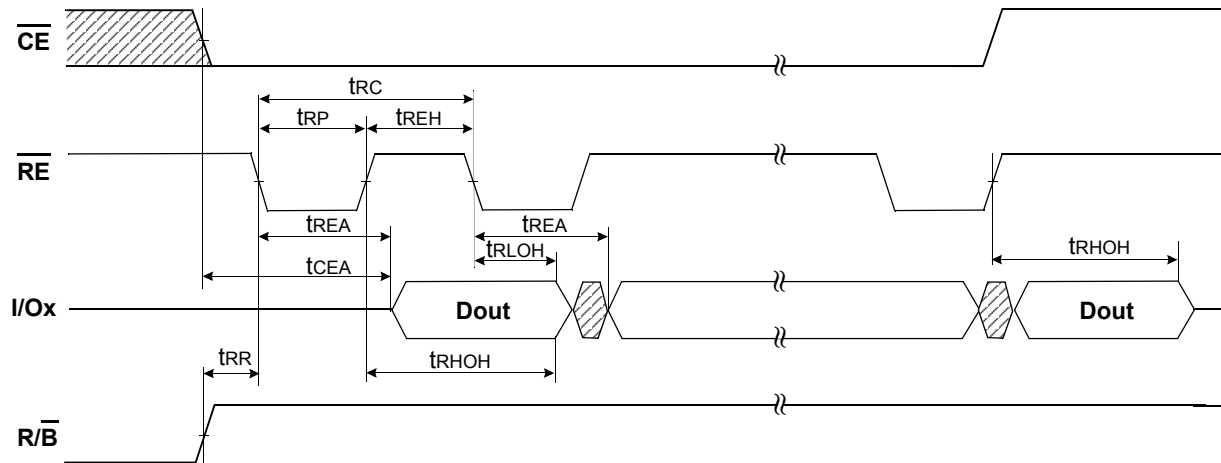
NOTES : Transition is measured at $\pm200mV$ from steady state voltage with load.
This parameter is sampled and not 100% tested.

Figure 19. Rp vs tRHOH vs C_L

@ Vcc = 3.3V, Ta = 25°C
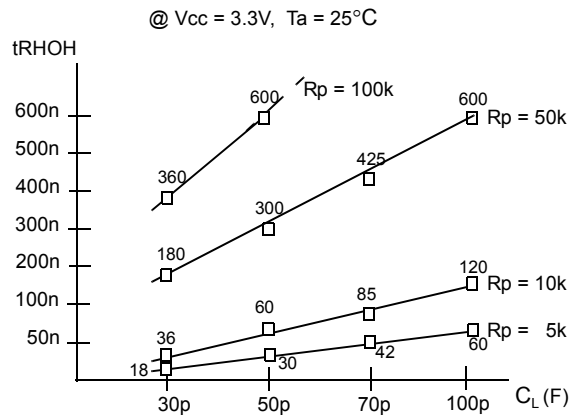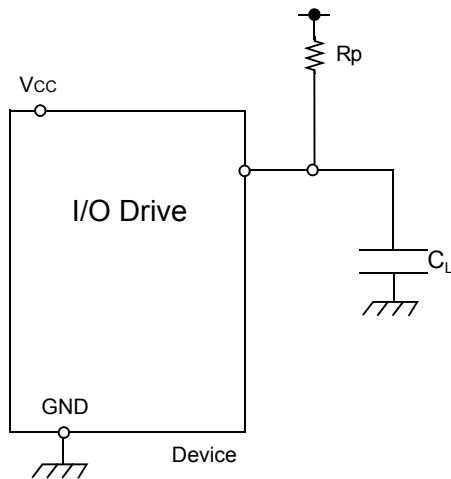
tRLOH / tRHOH value guidance

$$tRHOH = C_L * V_{OL} * Rp / Vcc$$
$$tRLOH(min, 3.3V \text{ part}) = tRHOH - tREH$$