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# HM5164805A Series

# HM5165805A Series

8388608-word × 8-bit Dynamic Random Access Memory

# HITACHI

ADE-203-458(B) (Z)  
Preliminary Rev. 0.2  
Jun. 12, 1996

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## Description

The Hitachi HM5164805A Series, HM5165805A Series are CMOS dynamic RAMs organized 8,388,608-word × 8-bit. They employ the most advanced CMOS technology for high performance and low power. The HM5164805A Series, HM5165805A Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have the package variation of standard 400-mil 32-pin plastic SOJ and standard 400-mil 32-pin plastic TSOPII.

## Features

- Single 3.3 V ( $\pm 0.3$  V)
- High speed
  - Access time: 50 ns/60 ns/70 ns (max)
- Low power dissipation
  - Active mode: TBD/540 mW/468 mW (max) (HM5164805A Series)  
: TBD/666 mW/594 mW (max) (HM5165805A Series)
  - Standby mode: 7.2 mW (max)  
: TBD (L-version)
- EDO page mode capability
- Refresh cycle
  - 8192  $\overline{\text{RAS}}$ -only refresh cycles: 64 ms (HM5164805A Series)  
4096 CBR/Hidden refresh cycles: 64ms  
: 128 ms (L-version)
  - 4096  $\overline{\text{RAS}}$ -only refresh cycles: 64 ms (HM5165805A Series)  
4096 CBR/Hidden refresh cycles: 64ms  
: 128 ms (L-version)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

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## HM5164805A Series, HM5165805A Series

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- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)
- Battery backup operation (L-version)

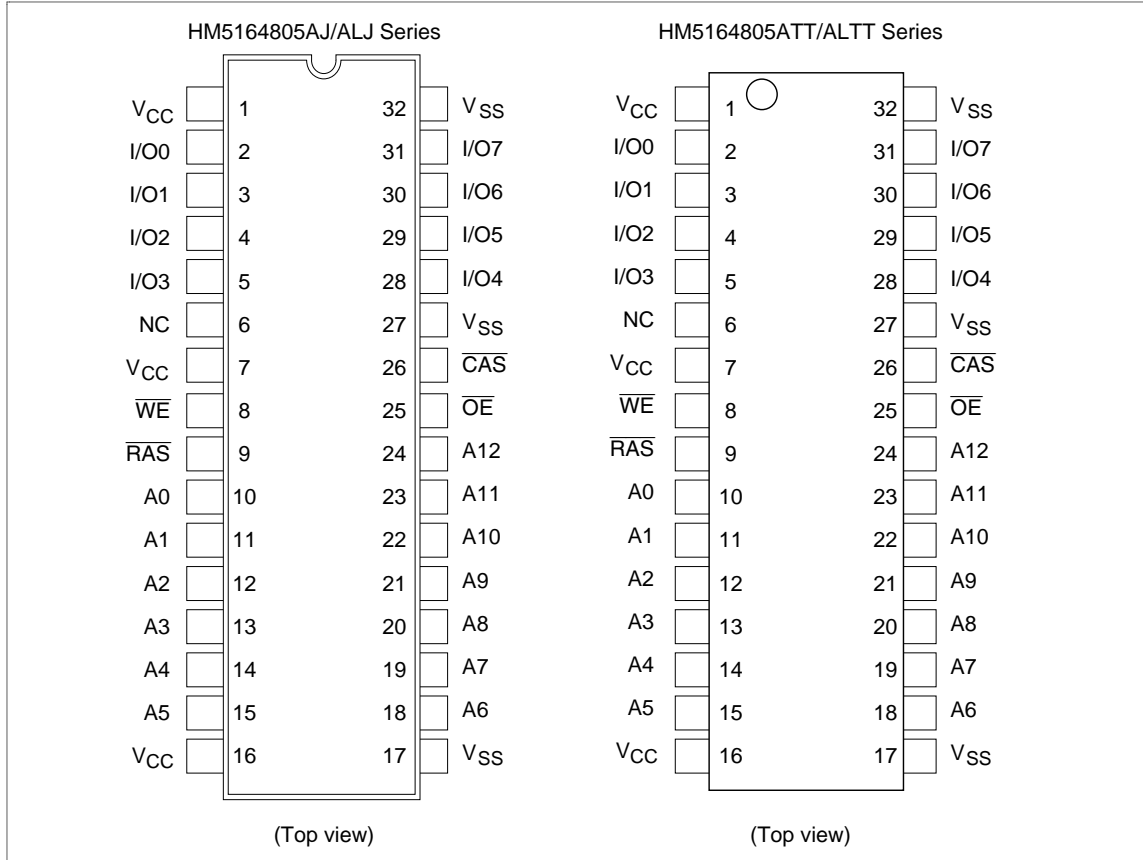
### Ordering Information

Type No.	Access time	Package
HM5164805AJ-5	50 ns	400-mil 32-pin plastic SOJ (CP-32DC)
HM5164805AJ-6	60 ns	
HM5164805AJ-7	70 ns	
HM5164805ALJ-5	50 ns	
HM5164805ALJ-6	60 ns	
HM5164805ALJ-7	70 ns	
HM5165805AJ-5	50 ns	
HM5165805AJ-6	60 ns	
HM5165805AJ-7	70 ns	
HM5165805ALJ-5	50 ns	
HM5165805ALJ-6	60 ns	
HM5165805ALJ-7	70 ns	
HM5164805ATT-5	50 ns	400-mil 32-pin plastic TSOP II (TTP-32DC)
HM5164805ATT-6	60 ns	
HM5164805ATT-7	70 ns	
HM5164805ALTT-5	50 ns	
HM5164805ALTT-6	60 ns	
HM5164805ALTT-7	70 ns	
HM5165805ATT-5	50 ns	
HM5165805ATT-6	60 ns	
HM5165805ATT-7	70 ns	
HM5165805ALTT-5	50 ns	
HM5165805ALTT-6	60 ns	
HM5165805ALTT-7	70 ns	

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## HM5164805A Series, HM5165805A Series

### Pin Arrangement

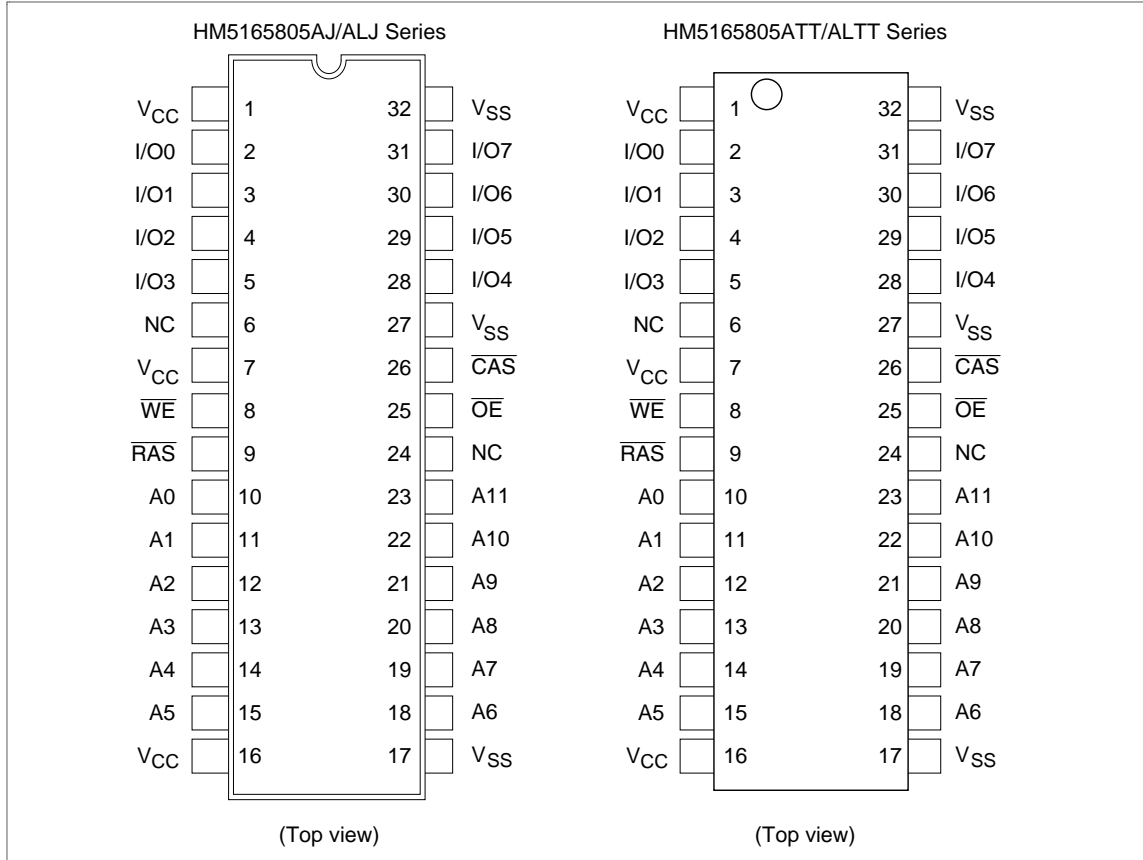


### Pin Description

Pin name	Function
A0 to A12	Address input — Row/Refresh address A0 to A12 — Column address A0 to A9
I/O0 to I/O7	Data input/Data output
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/Write enable
$\overline{\text{OE}}$	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

# HM5164805A Series, HM5165805A Series

## Pin Arrangement



## Pin Description

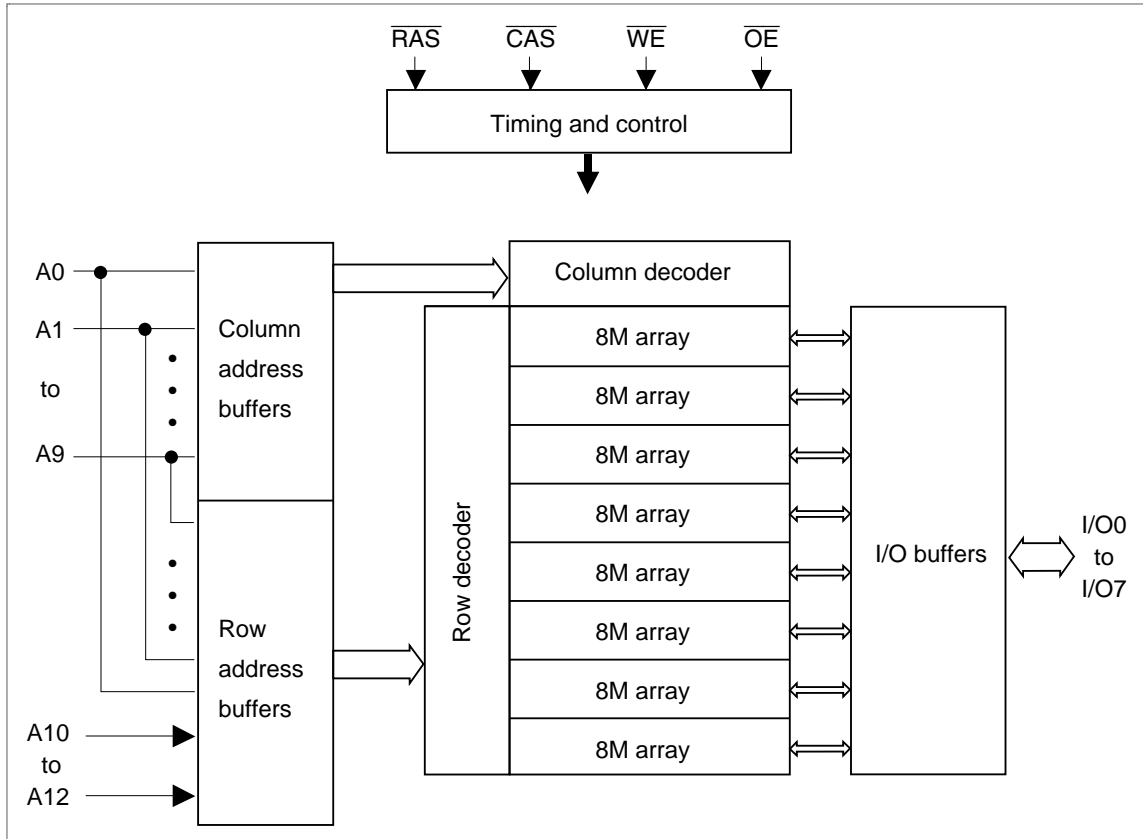
Pin name	Function
A0 to A11	Address input — Row/Refresh address A0 to A11 — Column address A0 to A10
I/O0 to I/O7	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

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## HM5164805A Series, HM5165805A Series

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### Block Diagram (HM5164805A Series)

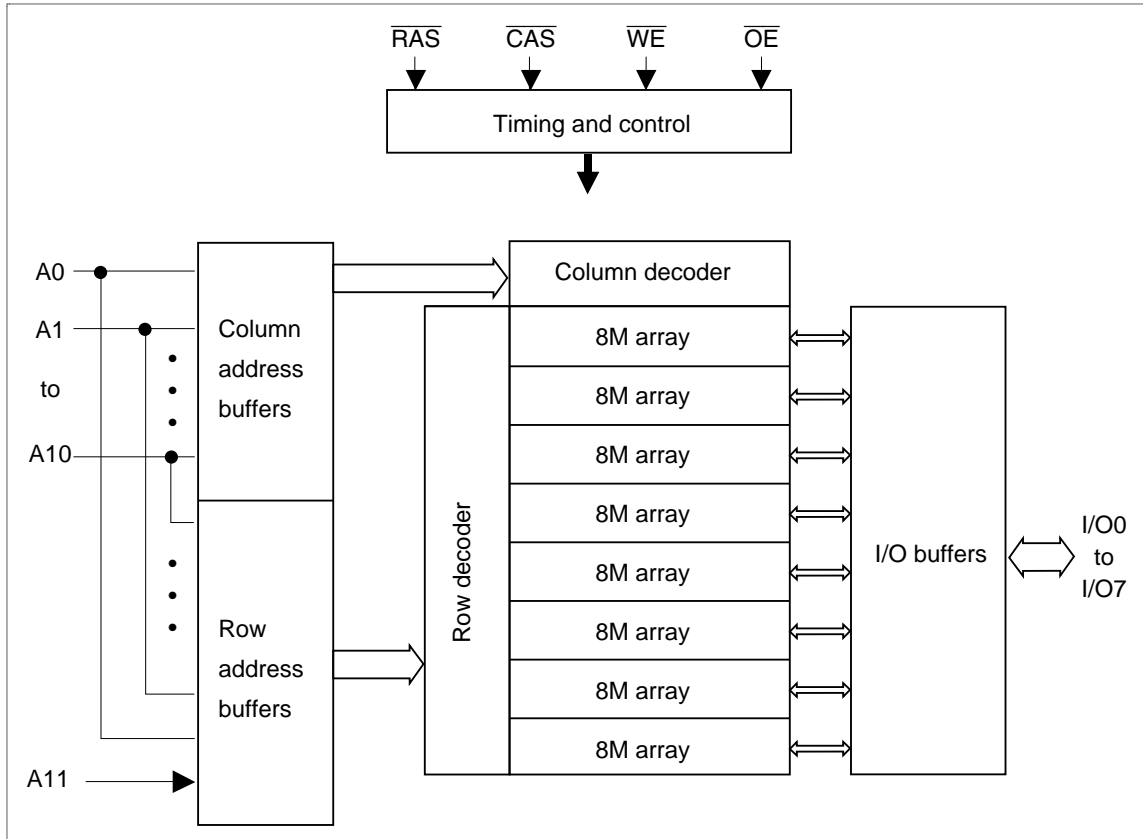


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## HM5164805A Series, HM5165805A Series

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### Block Diagram (HM5165805A Series)



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## HM5164805A Series, HM5165805A Series

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### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	$-0.5$ to $V_{CC} + 0.5$ ( $\leq 4.6$ V (max))	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	$-0.5$ to $+4.6$	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	$T_{stg}$	$-55$ to $+125$	$^{\circ}\text{C}$

### Recommended DC Operating Conditions ( $T_a = 0$ to $+70^{\circ}\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	$V_{CC}$	3.0	3.3	3.6	V	1, 2
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	$-0.3$	—	0.8	V	1

- Note: 1. All voltage referred to  $V_{SS}$ .  
2. The supply voltage with all  $V_{CC}$  pins must be on the same level. The supply voltage with all  $V_{SS}$  pins must be on the same level.

## HM5164805A Series, HM5165805A Series

### DC Characteristics

(Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V) (HM5164805A Series)

Parameter	Symbol	HM5164805A						Unit	Test conditions
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Operating current* <sup>1</sup> , * <sup>2</sup>	I <sub>CC1</sub>	—	TBD	—	135	—	115	mA	t <sub>RC</sub> = min
Standby current	I <sub>CC2</sub>	—	TBD	—	2	—	2	mA	TTL interface R <sub>AS</sub> , C <sub>AS</sub> = V <sub>IH</sub> Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
Standby current (L-version)	I <sub>CC2</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
R <sub>AS</sub> -only refresh current* <sup>2</sup>	I <sub>CC3</sub>	—	TBD	—	135	—	115	mA	t <sub>RC</sub> = min
Standby current* <sup>1</sup>	I <sub>CC5</sub>	—	TBD	—	5	—	5	mA	R <sub>AS</sub> = V <sub>IH</sub> , C <sub>AS</sub> = V <sub>IL</sub> Dout = enable
C <sub>AS</sub> -before-R <sub>AS</sub> refresh current	I <sub>CC6</sub>	—	TBD	—	150	—	130	mA	t <sub>RC</sub> = min
EDO page mode current* <sup>1</sup> , * <sup>3</sup>	I <sub>CC7</sub>	—	TBD	—	145	—	125	mA	t <sub>HPC</sub> = min
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface Dout = High-Z, CBR refresh: t <sub>RC</sub> = 31.3 μs t <sub>RAS</sub> ≤ 0.3 μs
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≤ 0.2 V Dout = High-Z
Input leakage current	I <sub>LI</sub>	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V <sub>CC</sub> + 0.3
Output leakage current	I <sub>LO</sub>	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V <sub>CC</sub> + 0.3 Dout = disable
Output high voltage	V <sub>OH</sub>	TBD	TBD	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA
Output low voltage	V <sub>OL</sub>	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while R<sub>AS</sub> = V<sub>IL</sub>.

3. Address can be changed once or less within one page mode cycle t<sub>HPC</sub>.

4. V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.2 V, 0 V ≤ V<sub>IL</sub> ≤ 0.2 V.



## HM5164805A Series, HM5165805A Series

### DC Characteristics

(Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, V<sub>SS</sub> = 0 V) (HM5165805A Series)

Parameter	Symbol	HM5165805A						Unit	Test conditions
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Operating current* <sup>1</sup> , * <sup>2</sup>	I <sub>CC1</sub>	—	TBD	—	185	—	165	mA	t <sub>RC</sub> = min
Standby current	I <sub>CC2</sub>	—	TBD	—	2	—	2	mA	TTL interface R <sub>AS</sub> , C <sub>AS</sub> = V <sub>IH</sub> Dout = High-Z
		—	TBD	—	1	—	1	mA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
Standby current (L-version)	I <sub>CC2</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z
R <sub>AS</sub> -only refresh current* <sup>2</sup>	I <sub>CC3</sub>	—	TBD	—	185	—	165	mA	t <sub>RC</sub> = min
Standby current* <sup>1</sup>	I <sub>CC5</sub>	—	TBD	—	5	—	5	mA	R <sub>AS</sub> = V <sub>IH</sub> , C <sub>AS</sub> = V <sub>IL</sub> Dout = enable
C <sub>AS</sub> -before-R <sub>AS</sub> refresh current	I <sub>CC6</sub>	—	TBD	—	150	—	130	mA	t <sub>RC</sub> = min
EDO page mode current* <sup>1</sup> , * <sup>3</sup>	I <sub>CC7</sub>	—	TBD	—	145	—	125	mA	t <sub>HPC</sub> = min
Battery backup current* <sup>4</sup> (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface Dout = High-Z, CBR refresh: t <sub>RC</sub> = 31.3 μs t <sub>RAS</sub> ≤ 0.3 μs
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	TBD	—	TBD	—	TBD	μA	CMOS interface R <sub>AS</sub> , C <sub>AS</sub> ≤ 0.2 V Dout = High-Z
Input leakage current	I <sub>LI</sub>	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V <sub>CC</sub> + 0.3 V
Output leakage current	I <sub>LO</sub>	TBD	TBD	-10	10	-10	10	μA	0 V ≤ Vin ≤ V <sub>CC</sub> + 0.3 V Dout = disable
Output high voltage	V <sub>OH</sub>	TBD	TBD	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA
Output low voltage	V <sub>OL</sub>	TBD	TBD	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes : 1. I<sub>CC</sub> depends on output load condition when the device is selected. I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while R<sub>AS</sub> = V<sub>IL</sub>.

3. Address can be changed once or less within one page mode cycle t<sub>HPC</sub>.

4. V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.2 V, 0 V ≤ V<sub>IL</sub> ≤ 0.2 V.

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## HM5164805A Series, HM5165805A Series

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**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	—	5	pF	1
Input capacitance (Clocks)	$C_{i2}$	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{i/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}} = V_{IH}$  to disable Dout.

## HM5164805A Series, HM5165805A Series

**AC Characteristics** ( $T_a = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ) \*<sup>1</sup>, \*<sup>2</sup>, \*<sup>3</sup>, \*<sup>18</sup>

### Test Conditions

- Input rise and fall time: 2 ns
- Input levels:  $V_{IL} = 0\text{ V}$ ,  $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM5164805A/HM5165805A						Unit	Notes
		-5		-6		-7			
Random read or write cycle time	$t_{RC}$	TBD	—	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	$t_{RP}$	TBD	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	$t_{CP}$	TBD	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ pulse width	$t_{RAS}$	TBD	TBD	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	TBD	TBD	10	10000	13	10000	ns	
Row address setup time	$t_{ASR}$	TBD	—	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	TBD	—	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	TBD	—	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	TBD	—	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	TBD	TBD	20	45	20	52	ns	3
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	TBD	TBD	15	30	15	35	ns	4
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	TBD	—	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	TBD	—	48	—	58	—	ns	21
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	TBD	—	5	—	5	—	ns	
$\overline{\text{OE}}$ to Din delay time	$t_{OED}$	TBD	—	15	—	18	—	ns	5
$\overline{\text{OE}}$ delay time from Din	$t_{DZO}$	TBD	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	$t_{DZC}$	TBD	—	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	TBD	TBD	2	50	2	50	ns	7

## HM5164805A Series, HM5165805A Series

### Read Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	TBD	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	TBD	—	15	—	18	ns	9, 10, 16
Access time from address	$t_{\text{AA}}$	—	TBD	—	30	—	35	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	TBD	—	15	—	18	ns	9
Read command setup time	$t_{\text{RCS}}$	TBD	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	TBD	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	TBD	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	TBD	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	TBD	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	TBD	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	TBD	—	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	TBD	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	TBD	—	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	TBD	—	15	—	15	ns	13, 20
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	TBD	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	TBD	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	TBD	—	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	TBD	—	15	—	15	ns	20
Output buffer turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	TBD	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WED}}$	TBD	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	TBD	—	15	—	18	—	ns	

### Write Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	$t_{\text{WCS}}$	TBD	—	0	—	0	—	ns	14
Write command hold time	$t_{\text{WCH}}$	TBD	—	10	—	13	—	ns	
Write command pulse width	$t_{\text{WP}}$	TBD	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	TBD	—	10	—	13	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	TBD	—	10	—	13	—	ns	
Data-in setup time	$t_{\text{DS}}$	TBD	—	0	—	0	—	ns	
Data-in hold time	$t_{\text{DH}}$	TBD	—	10	—	13	—	ns	

## HM5164805A Series, HM5165805A Series

### Read-Modify-Write Cycle

Parameter	Symbol	HM5164805A/HM5165805A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	$t_{RWC}$	TBD	—	149	—	175	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	TBD	—	78	—	91	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	TBD	—	33	—	39	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	TBD	—	48	—	56	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	$t_{OEh}$	TBD	—	15	—	18	—	ns	

### Refresh Cycle

Parameter	Symbol	HM5164805A/HM5165805A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	TBD	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	TBD	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	$t_{WRP}$	TBD	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	$t_{WRH}$	TBD	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	TBD	—	0	—	0	—	ns	

### EDO Page Mode Cycle

Parameter	Symbol	HM5164805A/HM5165805A						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	$t_{HPC}$	TBD	—	25	—	30	—	ns	19
EDO page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	TBD	—	100000	—	100000	ns	15
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	TBD	—	35	—	40	ns	9, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	TBD	—	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	$t_{DOH}$	TBD	—	3	—	3	—	ns	9, 16
$\overline{CAS}$ hold time referred $\overline{OE}$	$t_{COL}$	TBD	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	$t_{COP}$	TBD	—	10	—	10	—	ns	
Read command hold time from $\overline{CAS}$ precharge	$t_{RCHC}$	TBD	—	35	—	40	—	ns	
Write pulse width during $\overline{CAS}$ precharge	$t_{WPE}$	TBD	—	10	—	10	—	ns	
$\overline{OE}$ precharge time	$t_{OEP}$	TBD	—	10	—	10	—	ns	

## HM5164805A Series, HM5165805A Series

### EDO Page Mode Read-Modify-Write Cycle

		HM5164805A/HM5165805A							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	$t_{\text{HPRWC}}$	TBD	—	68	—	79	—	ns	
WE delay time from CAS precharge	$t_{\text{CPW}}$	TBD	—	54	—	62	—	ns	14

### Refresh (HM5164805A Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	$t_{\text{REF}}$	64	ms	8192 cycles
Refresh period (L-version)	$t_{\text{REF}}$	128	ms	4096 cycles

### Refresh (HM5165805A Series)

Parameter	Symbol	Max	Unit	Notes
Refresh period	$t_{\text{REF}}$	64	ms	4096 cycles
Refresh period (L-version)	$t_{\text{REF}}$	128	ms	4096 cycles

## HM5164805A Series, HM5165805A Series

### Self-Refresh Mode (L-version)

Parameter	Symbol	HM5164805AL/HM5165805AL						Unit	Notes
		-5		-6		-7			
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ pulse width (self refresh)	$t_{\text{RASS}}$	TBD	—	100	—	100	—	$\mu\text{s}$	
$\overline{\text{RAS}}$ precharge time (self refresh)	$t_{\text{RPS}}$	TBD	—	110	—	130	—	ns	
$\overline{\text{CAS}}$ hold time (self refresh)	$t_{\text{CHS}}$	TBD	—	-50	—	-50	—	ns	

- Notes:
- AC measurements assume  $t_t = 2$  ns.
  - An initial pause of 200  $\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh).
  - Operation with the  $t_{\text{RCD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RCD}}$  (max) is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
  - Operation with the  $t_{\text{RAD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RAD}}$  (max) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
  - Either  $t_{\text{OED}}$  or  $t_{\text{CDD}}$  must be satisfied.
  - Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
  - $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  - Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}$  (max) and  $t_{\text{RAD}} \leq t_{\text{RAD}}$  (max). If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
  - Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  - Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}}$  (max) and  $t_{\text{RCD}} + t_{\text{CAC}}$  (max)  $\geq t_{\text{RAD}} + t_{\text{AA}}$  (max).
  - Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}}$  (max) and  $t_{\text{RCD}} + t_{\text{CAC}}$  (max)  $\leq t_{\text{RAD}} + t_{\text{AA}}$  (max).
  - Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
  - $t_{\text{OFF}}$  (max),  $t_{\text{OEZ}}$  (max),  $t_{\text{WEZ}}$  (max) and  $t_{\text{OFR}}$  (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  - $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}$  (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}$  (min),  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (min), and  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (min), or  $t_{\text{CWD}} \geq t_{\text{CWD}}$  (min),  $t_{\text{AWD}} \geq t_{\text{AWD}}$  (min) and  $t_{\text{CPW}} \geq t_{\text{CPW}}$  (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  - $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in EDO page mode cycles.
  - Access time is determined by the longest among  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
  - All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
  - In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device.
  - $t_{\text{HPC}}$  (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of  $\overline{\text{CAS}}$  cycle ( $t_{\text{CAS}} + t_{\text{CP}} + 2 t_t$ ) becomes greater than the specified  $t_{\text{HPC}}$  (min) value. The value of  $\overline{\text{CAS}}$  cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
  - Output is disable after both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  go to high.
  - $t_{\text{CSH}}$  (min) can be achieved when  $t_{\text{RCD}} \leq t_{\text{CSH}}$  (min) -  $t_{\text{CAS}}$  (min).
  - Please do not use  $t_{\text{RASS}}$  timing,  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{\text{RASS}} > 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .

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## HM5164805A Series, HM5165805A Series

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23. CBR burst refresh or 4096 cycles of distributed CBR refresh with 15.6  $\mu$ s interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
24. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
25. XXX: H or L (H:  $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ , L:  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$ )

///: Invalid Dout

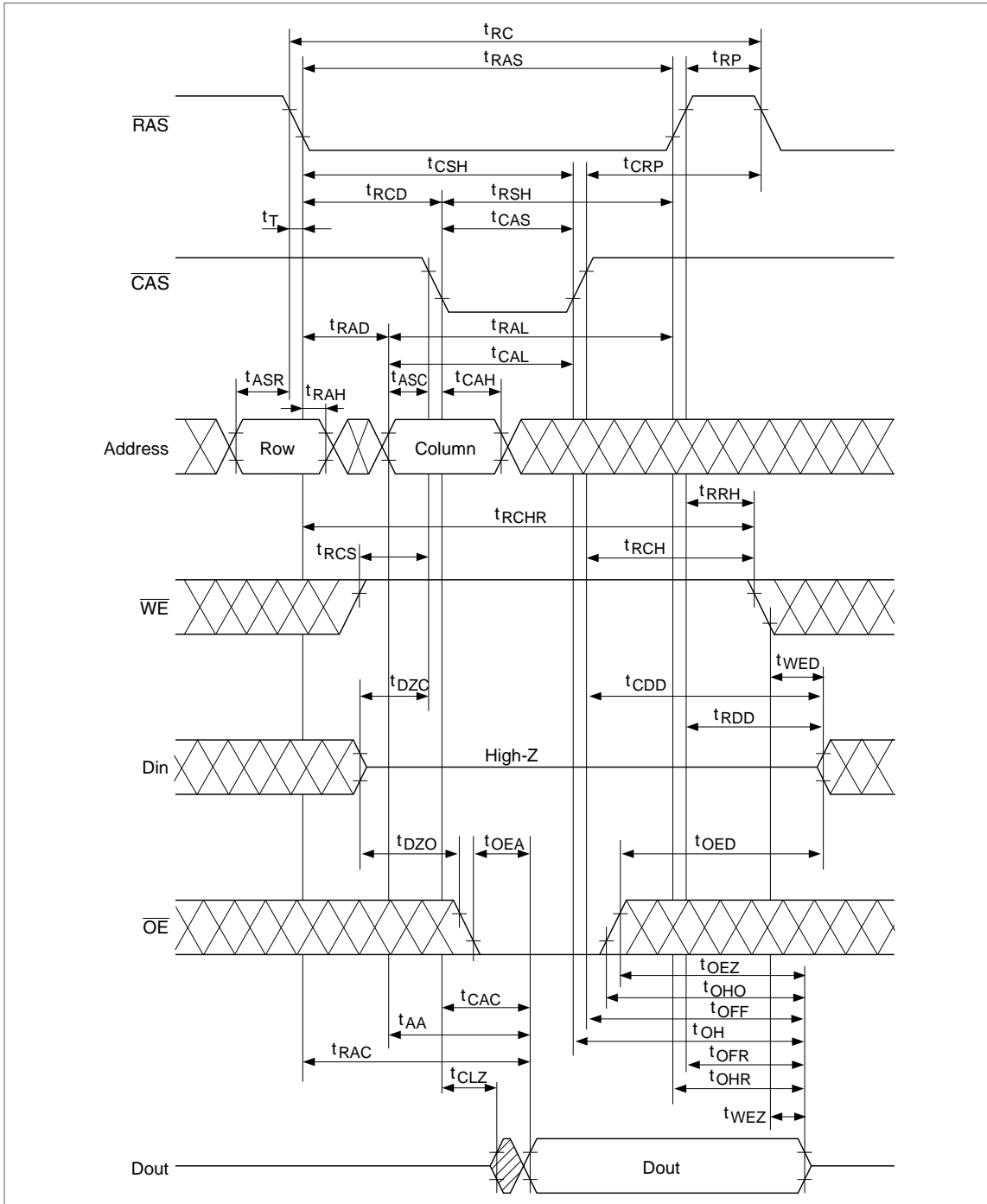
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{IH}$  or  $V_{IL}$ .



# HM5164805A Series, HM5165805A Series

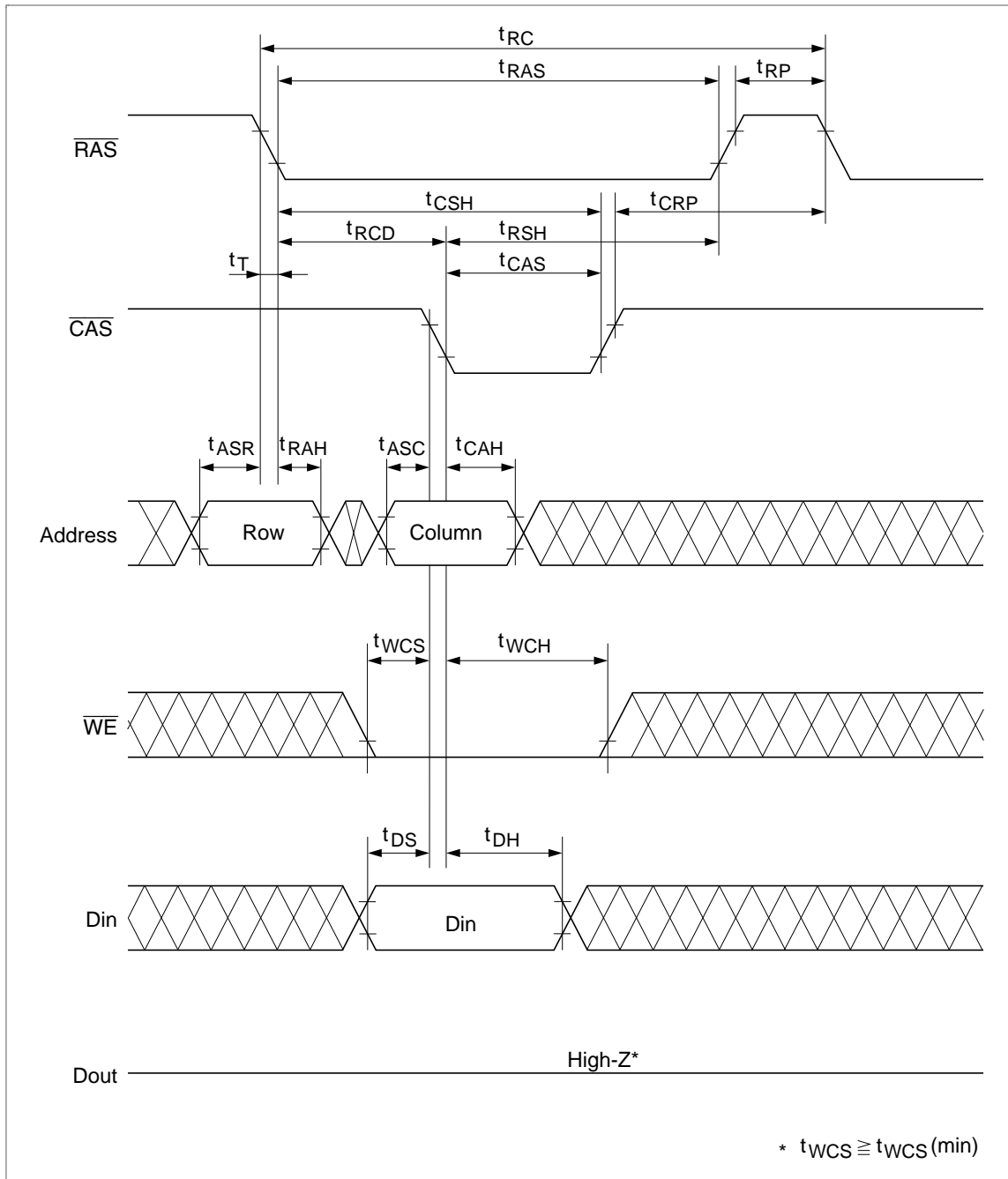
## Timing Waveforms\*<sup>25</sup>

### Read Cycle



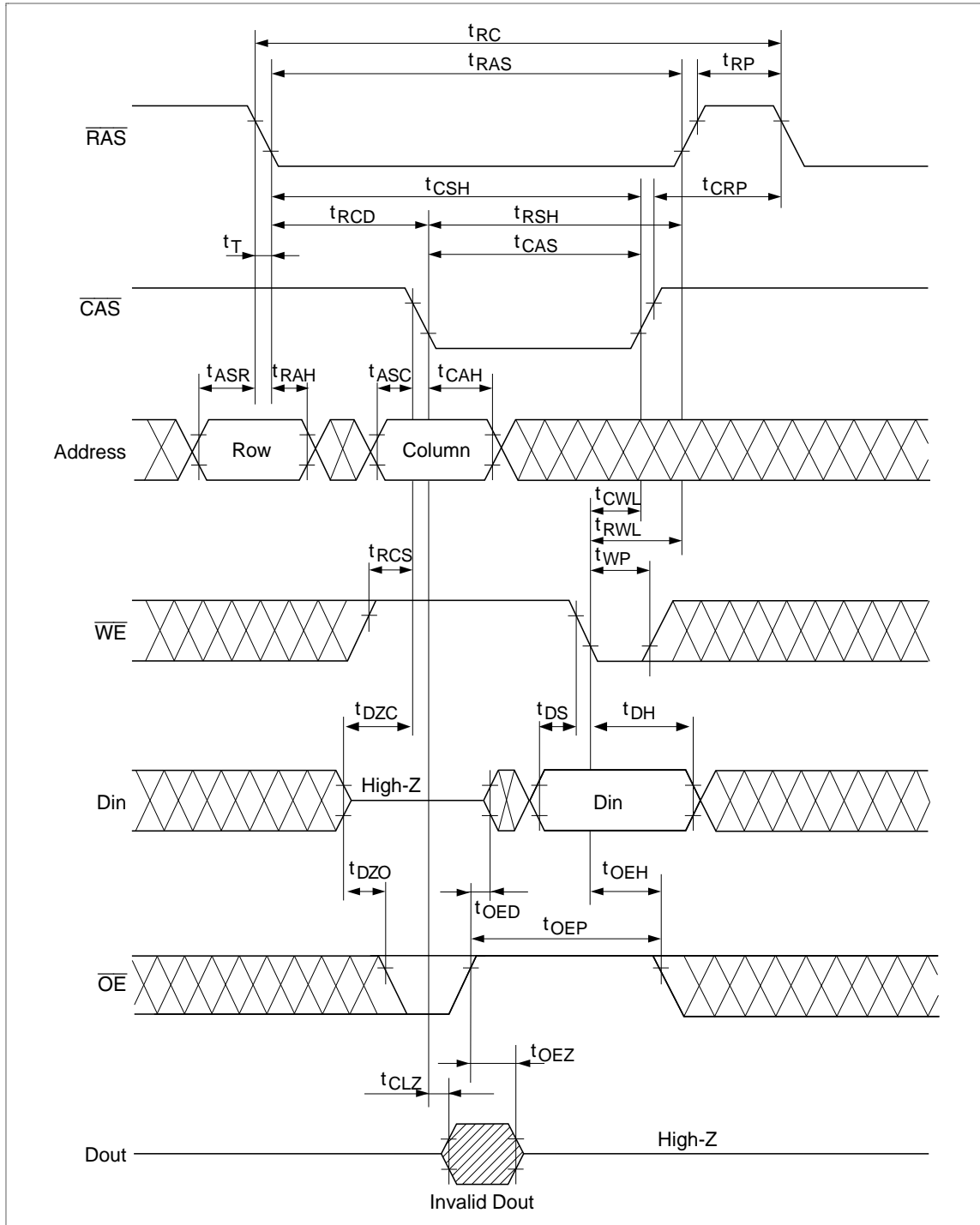
### Early Write Cycle

# HM5164805A Series, HM5165805A Series



## HM5164805A Series, HM5165805A Series

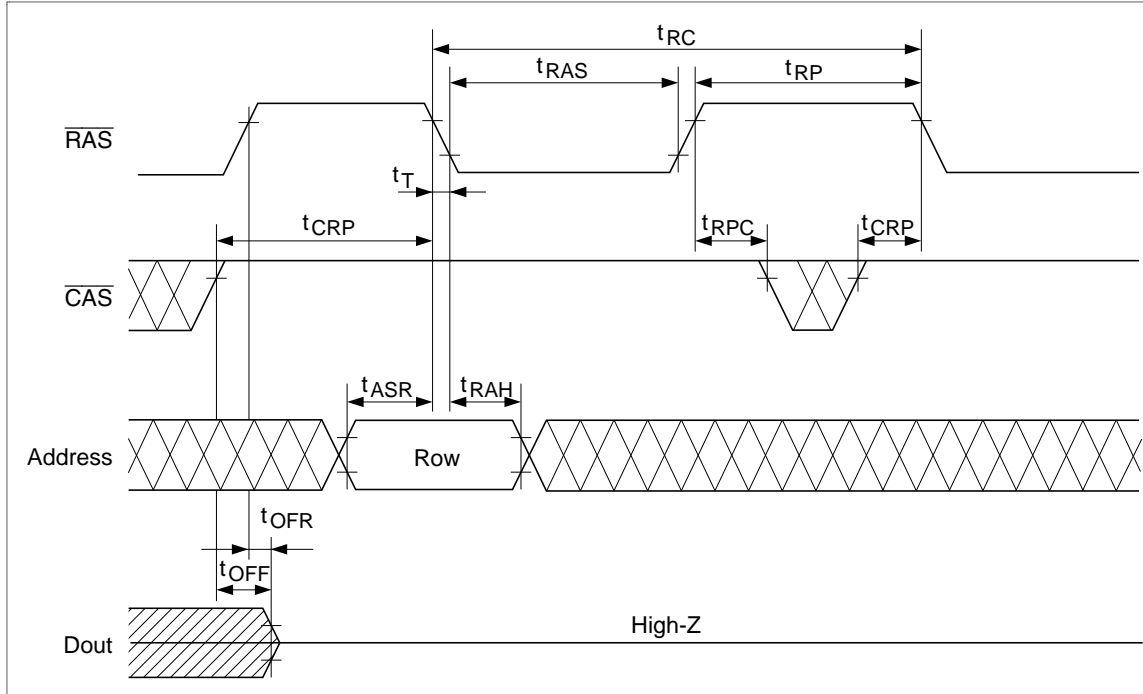
### Delayed Write Cycle\*<sup>18</sup>





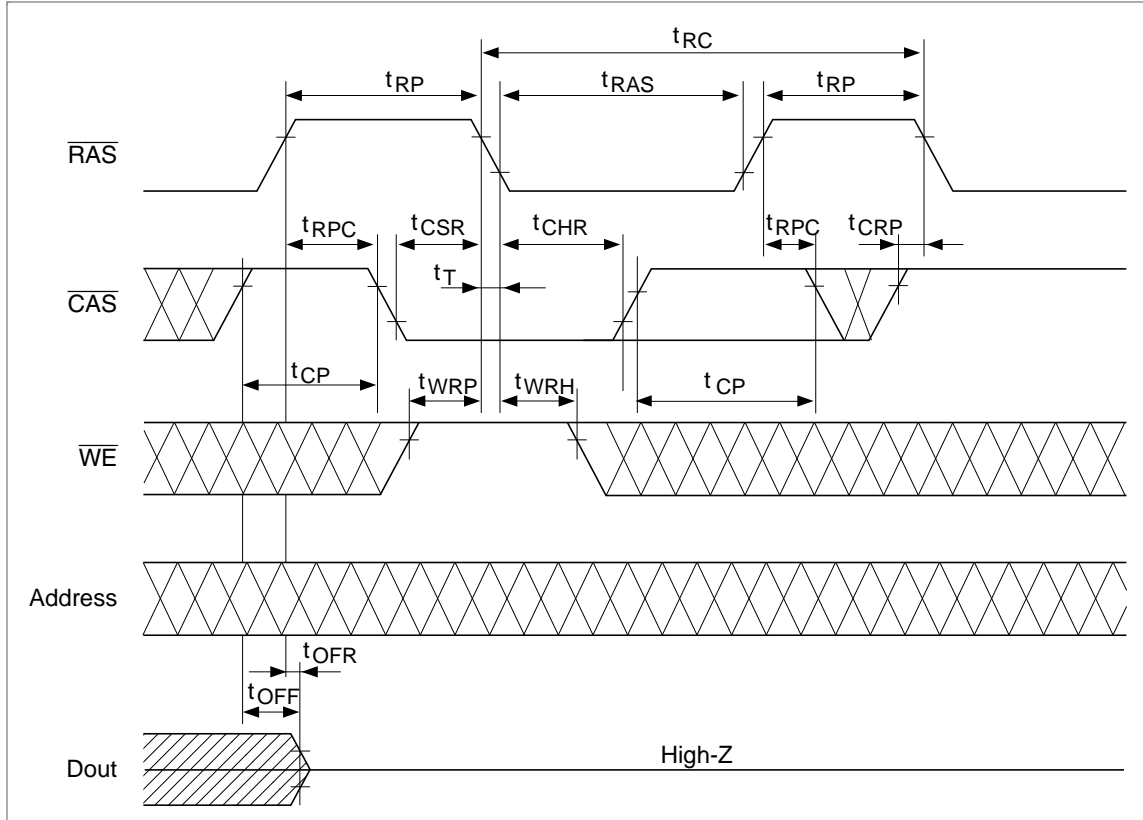
# HM5164805A Series, HM5165805A Series

## $\overline{\text{RAS}}$ -Only Refresh Cycle



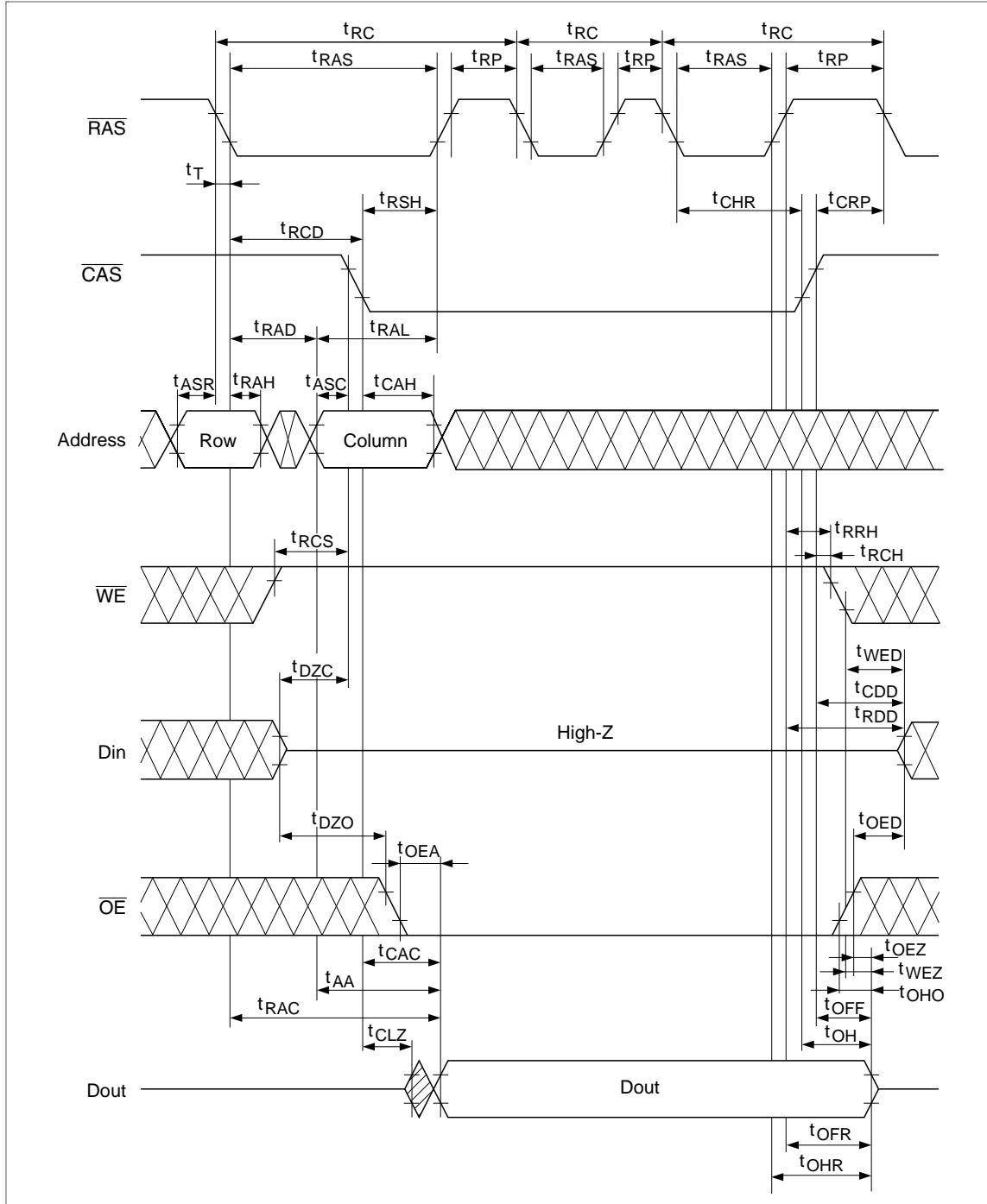
# HM5164805A Series, HM5165805A Series

## $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle



# HM5164805A Series, HM5165805A Series

## Hidden Refresh Cycle

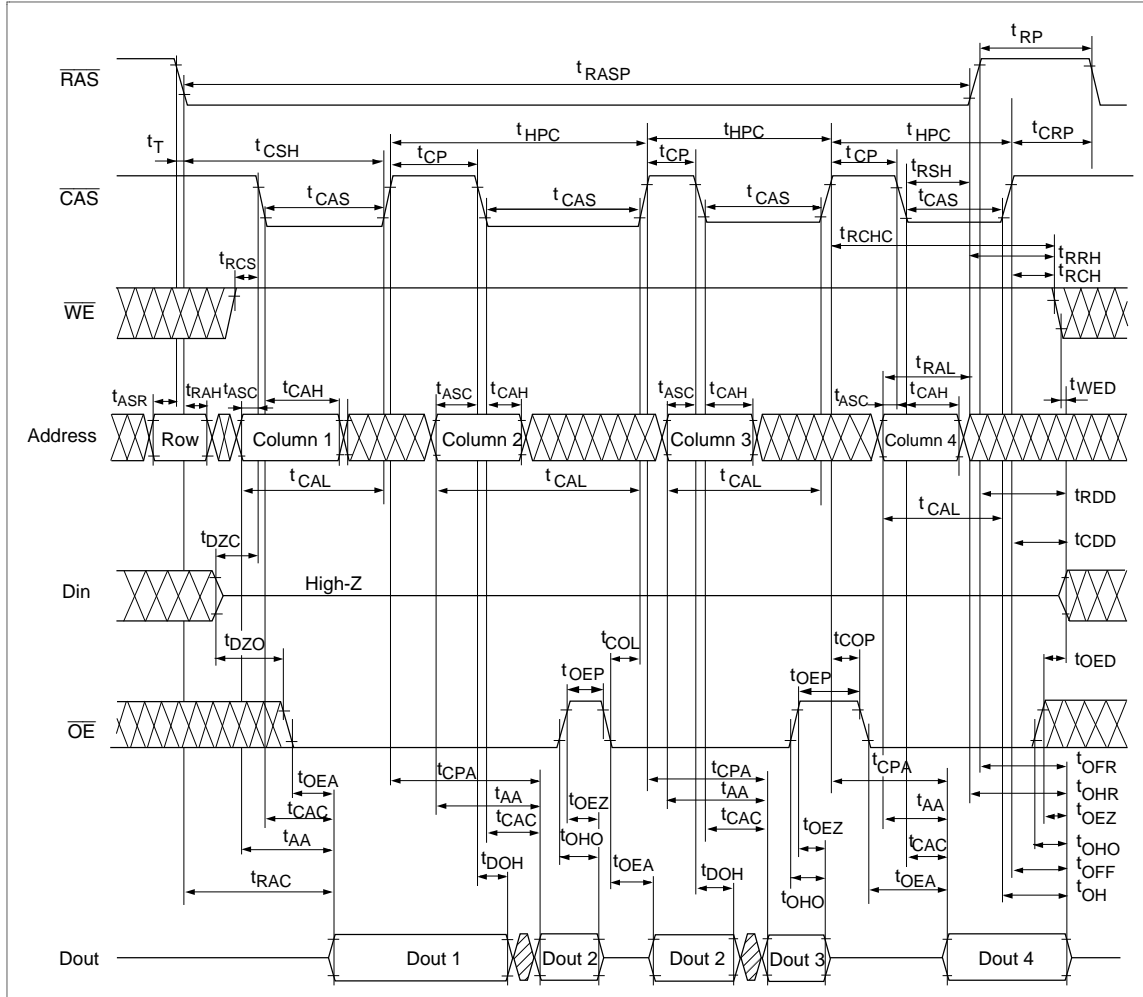






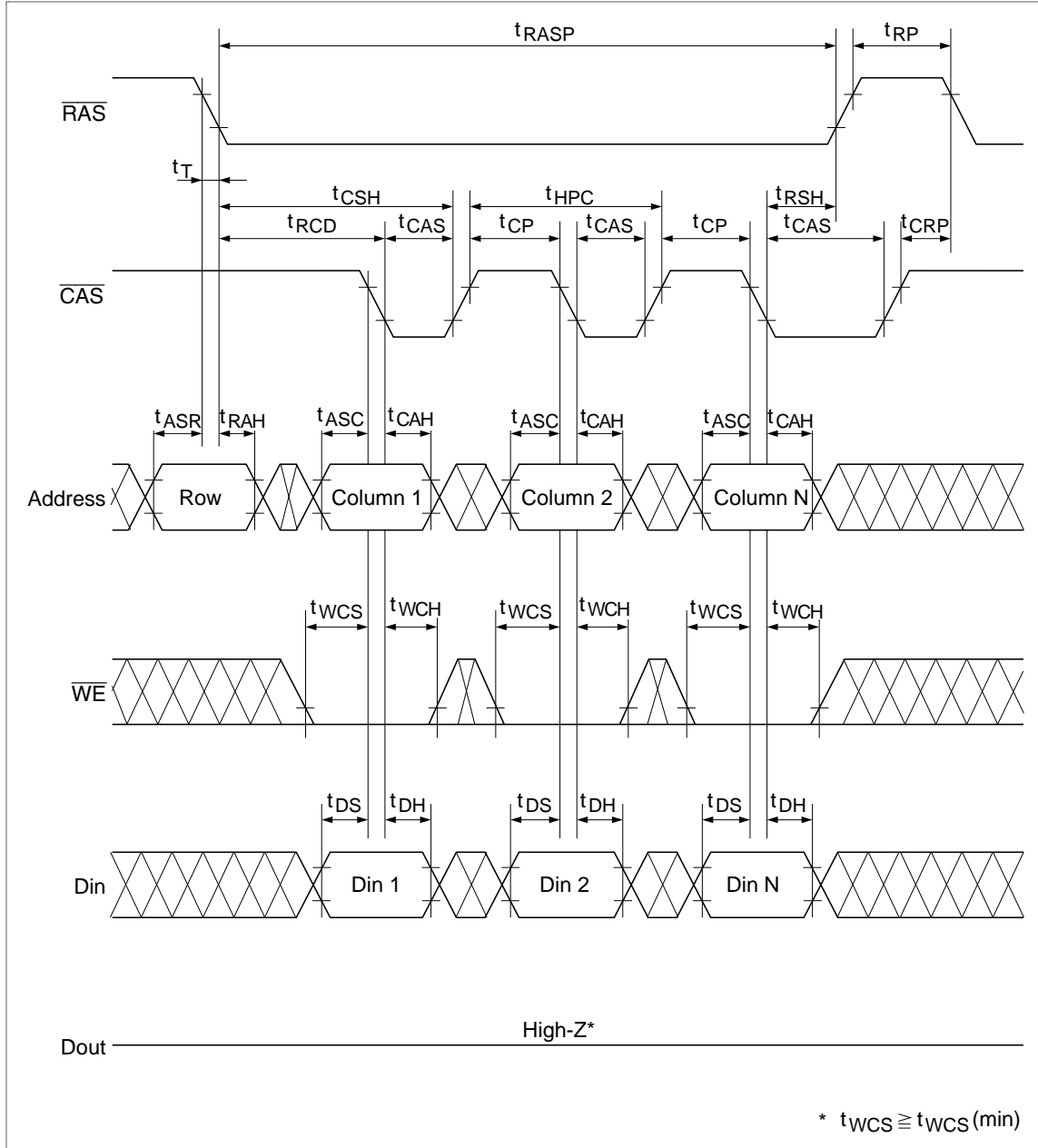
# HM5164805A Series, HM5165805A Series

## EDO Page Mode Read Cycle (2)



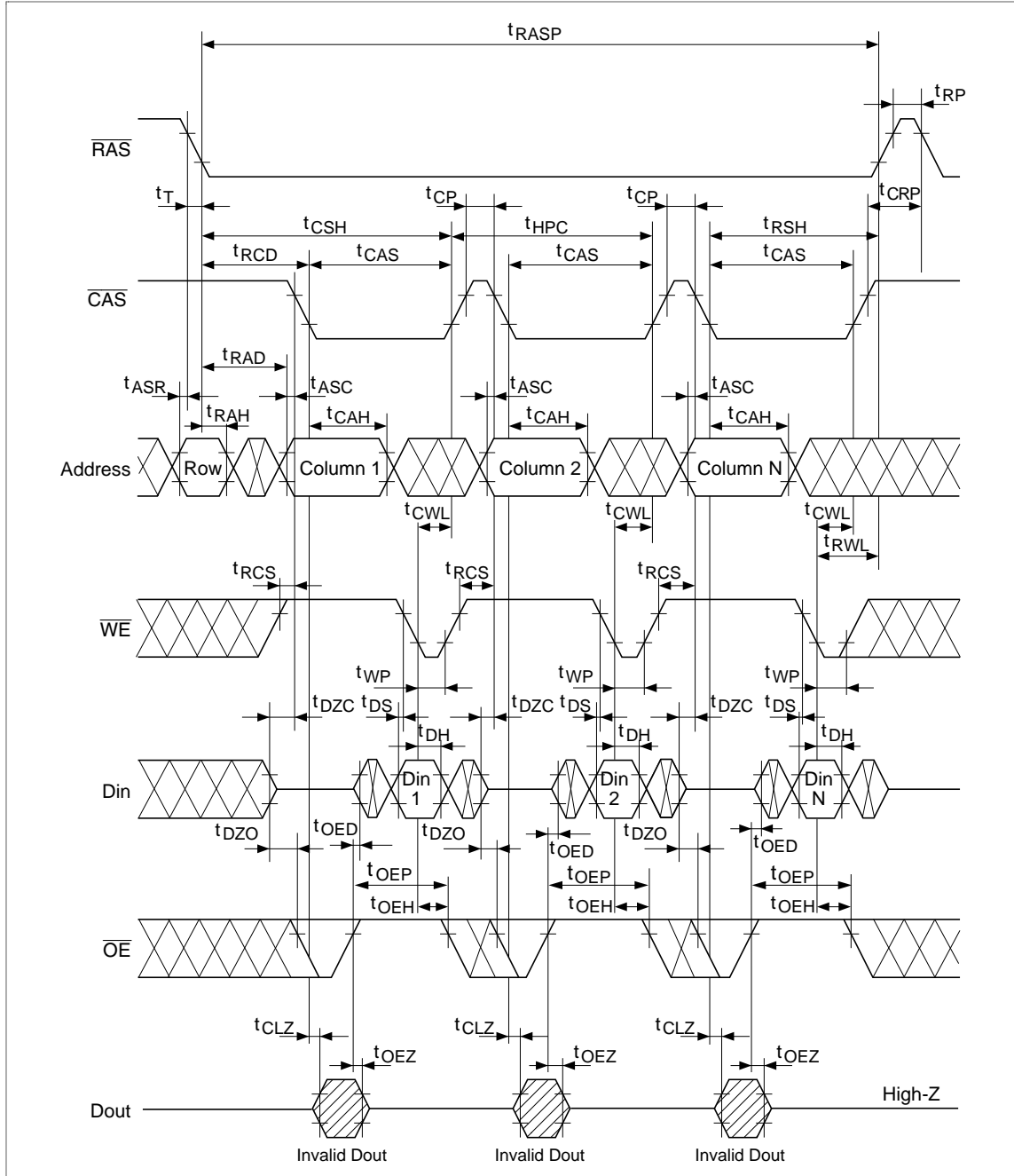
# HM5164805A Series, HM5165805A Series

## EDO Page Mode Early Write Cycle



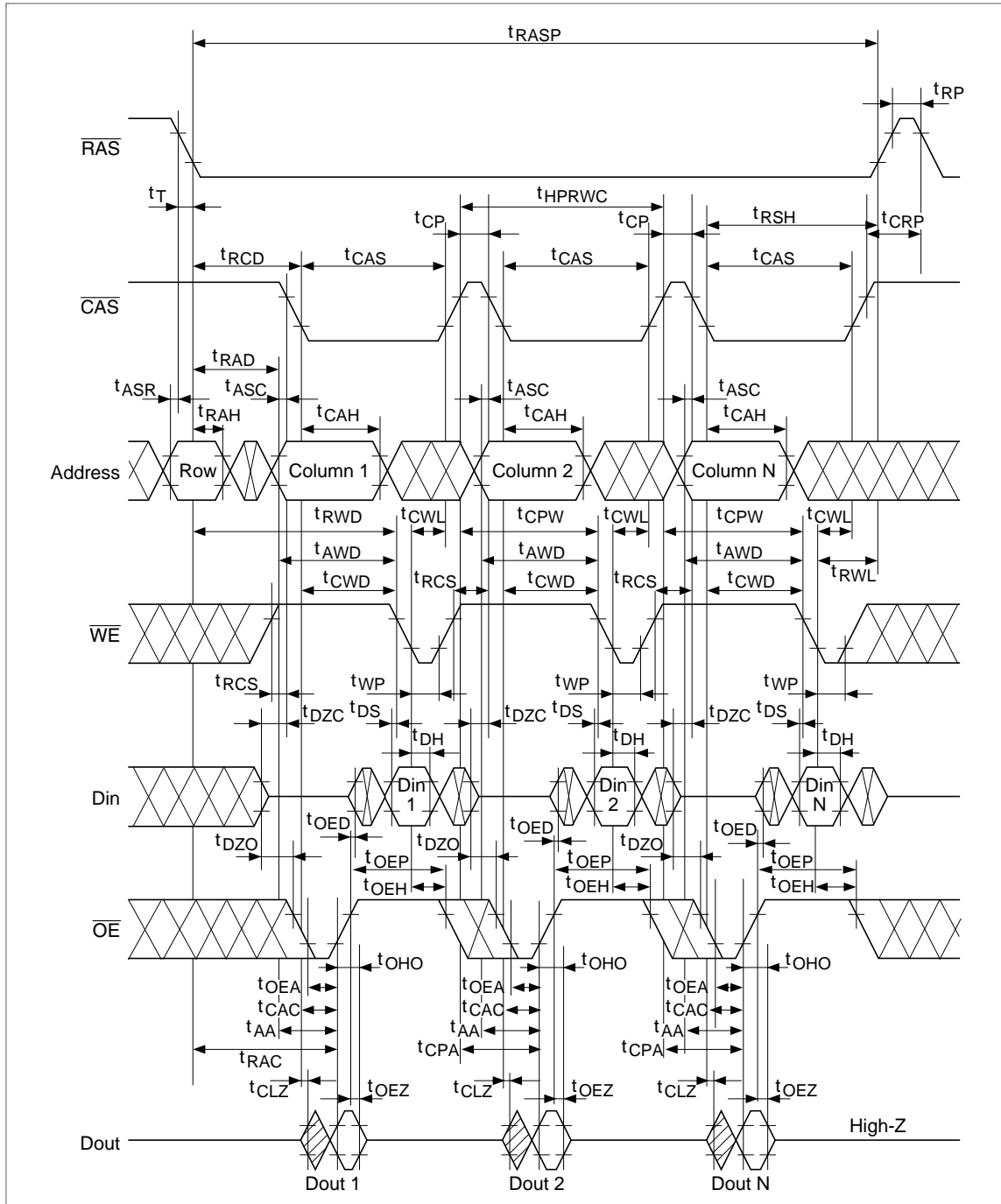
# HM5164805A Series, HM5165805A Series

## EDO Page Mode Delayed Write Cycle\*<sup>18</sup>



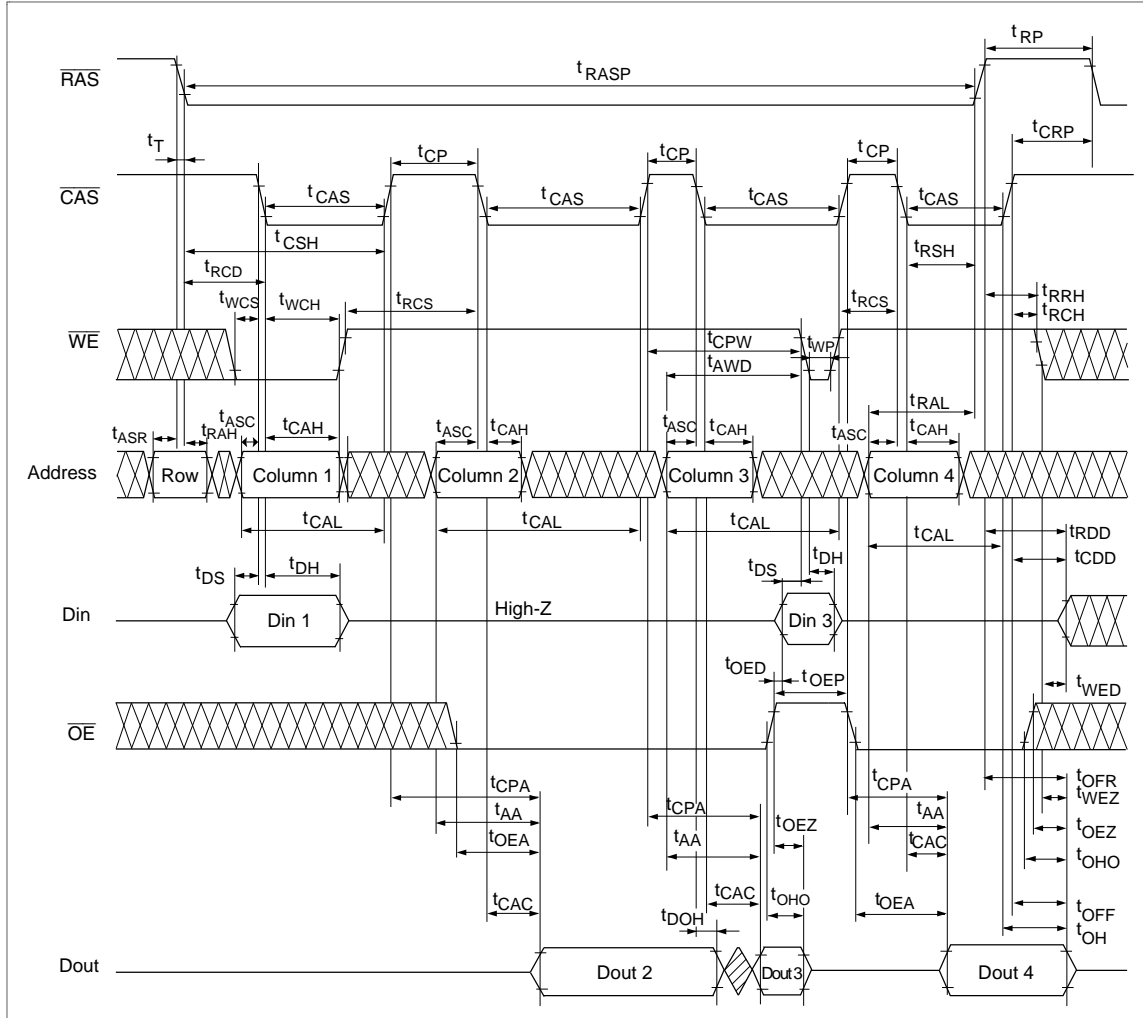
# HM5164805A Series, HM5165805A Series

## EDO Page Mode Read-Modify-Write Cycle\*18



# HM5164805A Series, HM5165805A Series

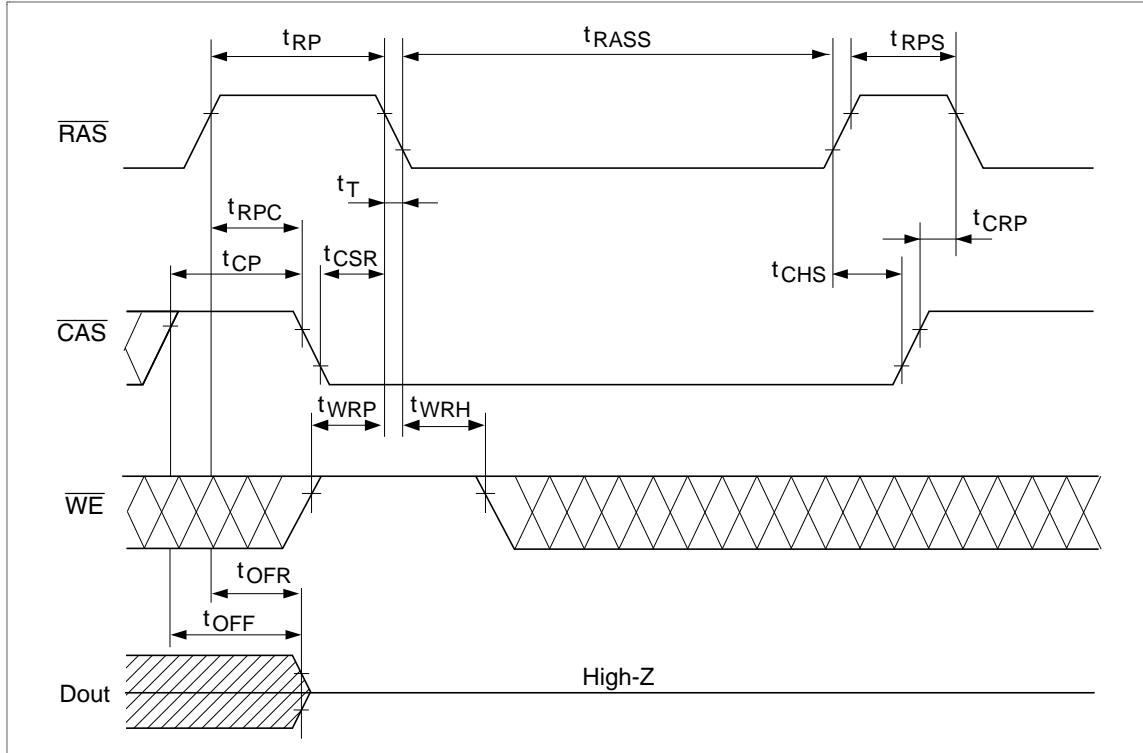
## EDO Page Mode Mix Cycle (1)





# HM5164805A Series, HM5165805A Series

## Self-Refresh Cycle (L-version)\*22, 23, 24



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## HM5164805A Series, HM5165805A Series

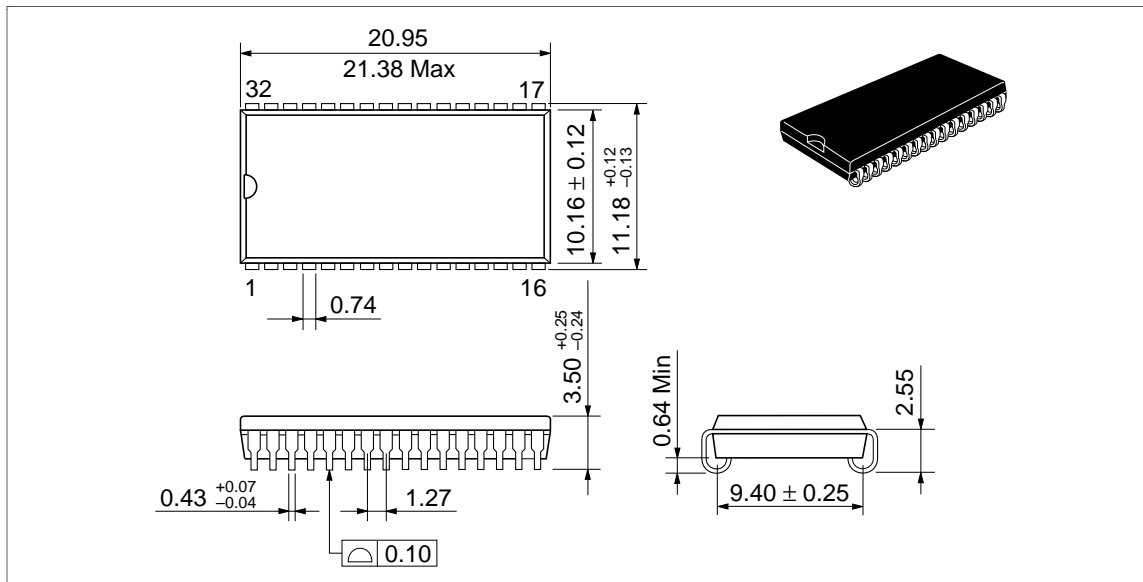
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### Package Dimensions

HM5164805AJ/ ALJ Series

HM5165805AJ/ ALJ Series (CP-32DC)

Unit: mm



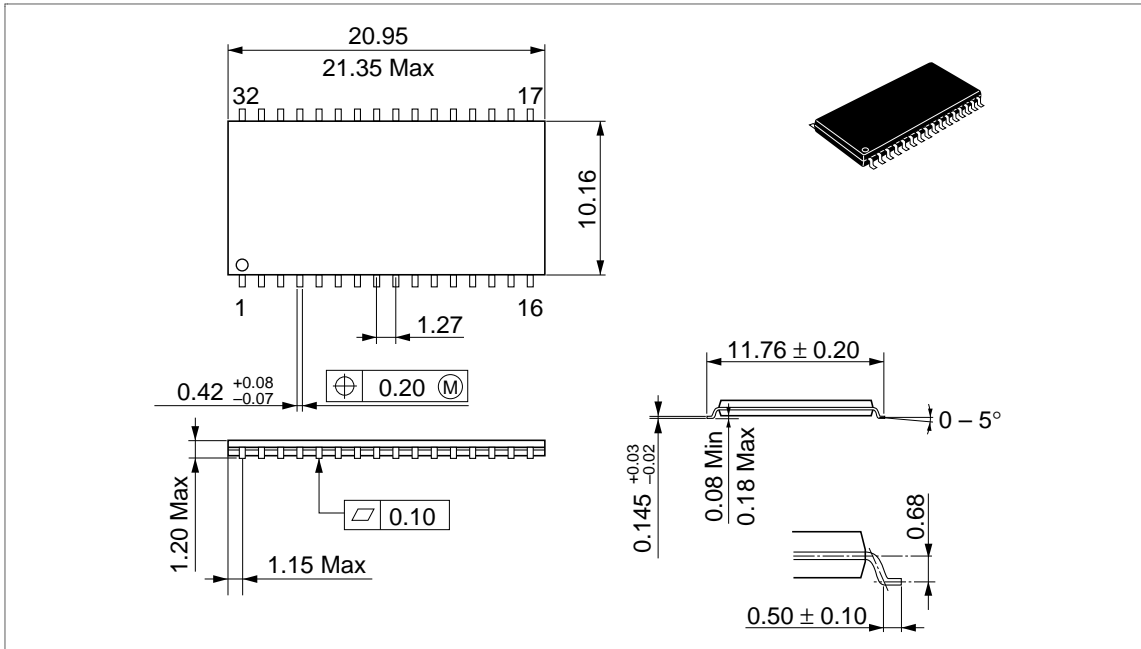


# HM5164805A Series, HM5165805A Series

HM5164805ATT/ALTT Series

HM5165805ATT/ALTT Series (TTP-32DC)

Unit: mm



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## HM5164805A Series, HM5165805A Series

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# HITACHI

## Hitachi, Ltd.

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

### For further information write to:

Hitachi America, Ltd.  
Semiconductor & IC Div.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1835  
U S A  
Tel: 415-589-8300  
Fax: 415-583-4207

Hitachi Europe GmbH  
Electronic Components Group  
Continental Europe  
Dornacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 0628-585000  
Fax: 0628-778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 0104  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071

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## HM5164805A Series, HM5165805A Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 13, 1995	Initial issue	S. Ikenaga	J. Kitano
0.1	Apr. 30, 1996	Change format Unification of HM5164805A Series and HM5165805A Series Addition of HM5164805A/HM5165805A-5 Series Addition of HM5164805AJ/ALJ Series, HM5165805AJ/ALJ Series (CP-32DC) Pin Descriptions Addition of Row/Refresh address and Column address to address input Addition of Block Diagrams DC Characteristics (HM5164805A) $I_{CC1}$ max: 105/95 mA to TBD/135/115 mA $I_{CC3}$ max: 105/95 mA to TBD/135/115 mA $I_{CC6}$ max: 105/95 mA to TBD/150/130 mA $I_{CC7}$ max: 105/95 mA to TBD/145/125 mA Addition of note 4 DC Characteristics (HM5165805A) $I_{CC1}$ max: 145/135 mA to TBD/185/165 mA $I_{CC3}$ max: 125/110 mA to TBD/185/165 mA $I_{CC6}$ max: 125/110 mA to TBD/150/130 mA $I_{CC7}$ max: 125/110 mA to TBD/145/125 mA Addition of note 4 AC Characteristics $t_{RCD}$ max: 38/45 ns to TBD/45/52 ns $t_{COP}$ min: 5/5 ns to TBD/10/10 ns Addition of $t_{WPE}$ and $t_{OEP}$ $t_{HPRWC}$ min: 79/90 ns to TBD/68/79 ns Addition of notes 20 to 24 Change of notes 3 and 13 Timing waveforms Addition of $t_{WPE}$ and $t_{OEP}$ timings Deletion of note: $t_{OEH} \geq t_{CWL}$	S. Ikenaga	J. Kitano
0.2	Jun. 12, 1996	AC Characteristics Change of notes 18 and 25 Timing waveforms Deletion of notes about undefined pins		

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