HM5117805 Series

2,097,152-word × 8-bit Dynamic RAM

HITACHI

ADE-203-630B (Z)
Rev. 2.0
Nov. 8, 1996

Description

The Hitachi HM5117805 is a CMOS dynamic RAM organized 2,097,152-word × 8-bits. It uses the most advanced CMOS technology for high performance and low power. The HM5117805 offers extended data out (EDO) page mode as a high speed access mode. Multiplexed address input lets the HM5117805 use standard 28-pin plastic SOJ and 28-pin TSOP packaging.

Features

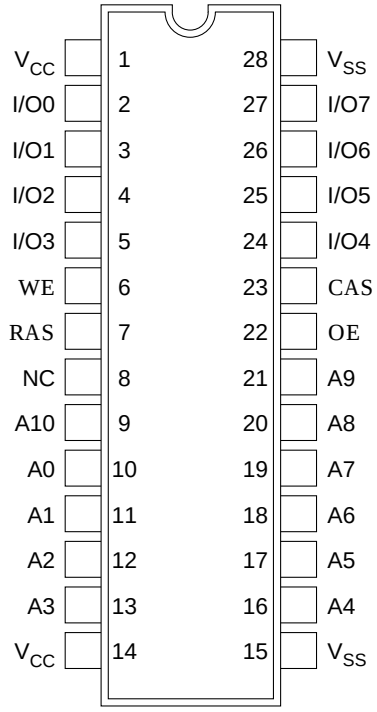
- Single 5 V (±10%)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation:
  - Active mode: 605 mW/550 mW/495 mW (max)
  - Standby mode:
    - 11 mW (max)
    - 0.83 mW (max) (L-version)
- EDO page mode capability
- Long refresh period; 2048 refresh cycles:
  - 32 ms
  - 128 ms (L-version)
- Four variations of refresh:
  - RAS-only refresh
  - CAS-before-RAS refresh
  - Hidden refresh
  - Self refresh (L-version)
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM5117805J-5 HM5117805J-6 HM5117805J-7	50 ns 60 ns 70 ns	400-mil 28-pin plastic SOJ (CP-28DA)
HM5117805LJ-5 HM5117805LJ -6 HM5117805LJ -7	50 ns 60 ns 70 ns	400-mil 28-pin plastic SOJ (CP-28DA)
HM5117805S-5 HM5117805S-6 HM5117805S-7	50 ns 60 ns 70 ns	300-mil 28-pin plastic SOJ (CP-28DNA)
HM5117805LS-5 HM5117805LS-6 HM5117805LS-7	50 ns 60 ns 70 ns	300-mil 28-pin plastic SOJ (CP-28DNA)
HM5117805TT-5 HM5117805TT-6 HM5117805TT-7	50 ns 60 ns 70 ns	400-mil 28-pin plastic TSOP II (TTP-28DA)
HM5117805LTT-5 HM5117805LTT-6 HM5117805LTT-7	50 ns 60 ns 70 ns	400-mil 28-pin plastic TSOP II (TTP-28DA)
HM5117805TS-5 HM5117805TS-6 HM5117805TS-7	50 ns 60 ns 70 ns	300-mil 28-pin plastic TSOP II (TTP-28DB)
HM5117805LTS-5 HM5117805LTS-6 HM5117805LTS-7	50 ns 60 ns 70 ns	300-mil 28-pin plastic TSOP II (TTP-28DB)

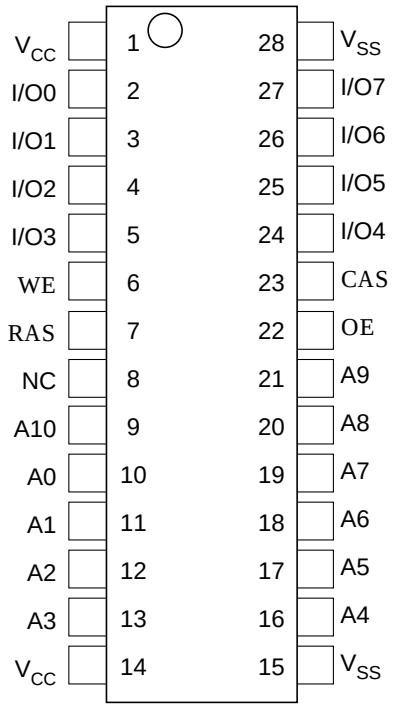
Pin Arrangement

HM5117805J/LJ Series
HM5117805S/LS Series



(Top view)

HM5117805TT/LTT Series
HM5117805TS/LTS Series

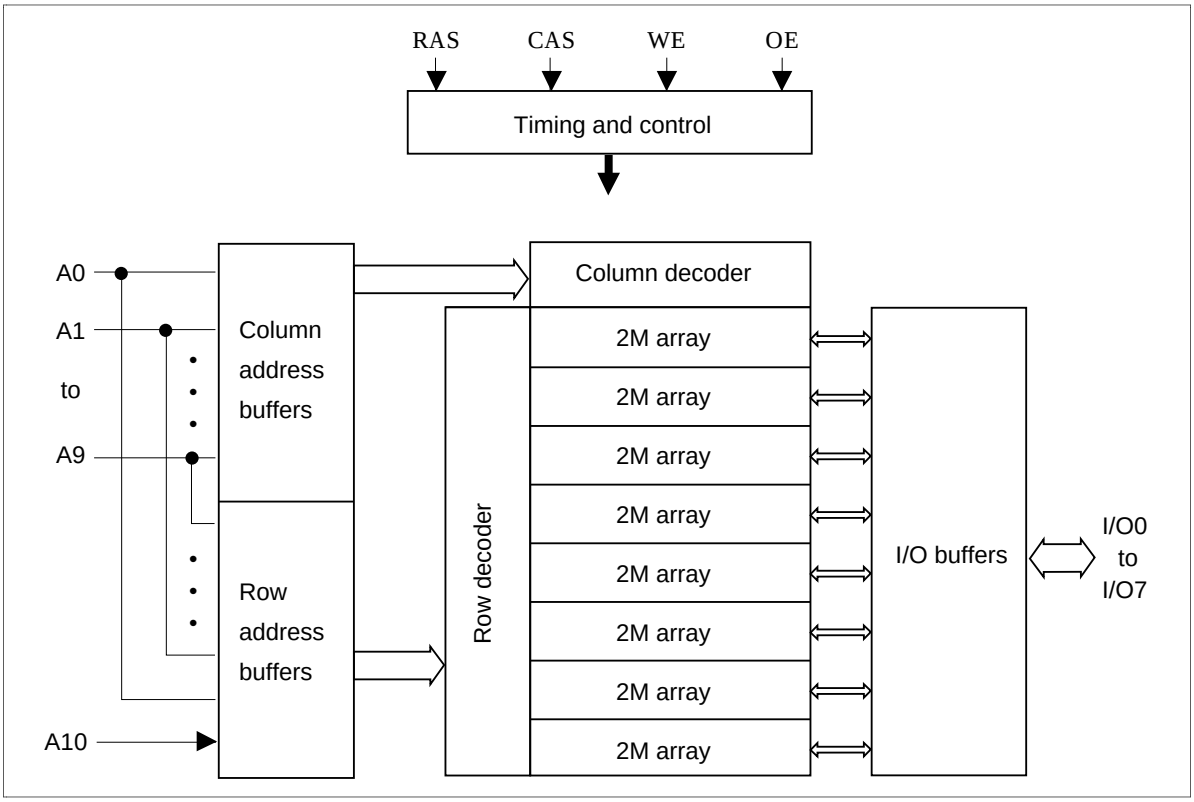


(Top view)

Pin Description

Pin name	Function
A0 to A10	Address input: • Row/Refresh address: A0 to A10 • Column address: A0 to A9
I/O0 to I/O7	Data input/data output
RAS	Row address strobe
CAS	Column address strobe
WE	Read/Write enable
OE	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	—	6.5	V
Input low voltage	V_{IL}	–1.0	—	0.8	V

Note: All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM5117805							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current*[1, *2]	I_{CC1}	—	110	—	100	—	90	mA	t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
Standby current	I_{CC2}	—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	150	—	150	—	150	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
$\overline{RAS}$-only refresh current*[2]	I_{CC3}	—	110	—	100	—	90	mA	t_{RC} = min
Standby current*[1]	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	110	—	100	—	90	mA	t_{RC} = min
EDO page mode current*[1, *3]	I_{CC7}	—	100	—	90	—	85	mA	t_{HPC} = min
Battery backup current*[4] (Standby with CBR refresh) (L-version)	I_{CC10}	—	500	—	500	—	500	µA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 62.5 µs t_{RAS} ≤ 0.3 µs
Self refresh mode current (L-version)	I_{CC11}	—	300	—	300	—	300	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≤ 0.2V Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $\overline{CAS}$ = L (≤ 0.2 V) while $\overline{RAS}$ = L (≤ 0.2 V).

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton meter or other effective method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)[*1, *2, *18]

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (including scope and jig)

Read, Write, Read-Modify-Write, and Refresh Cycles (Common Parameters)

		HM5117805							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
RAS precharge time	t_{RP}	30	—	40	—	50	—	ns	
CAS precharge time	t_{CP}	7	—	10	—	13	—	ns	
RAS pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
CAS pulse width	t_{CAS}	7	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	7	—	10	—	13	—	ns	
RAS to CAS delay time	t_{RCD}	11	37	14	45	14	52	ns	3
RAS to column address delay time	t_{RAD}	9	25	12	30	12	35	ns	4
RAS hold time	t_{RSH}	10	—	13	—	13	—	ns	
CAS hold time	t_{CSH}	35	—	40	—	45	—	ns	
CAS to RAS precharge time	t_{CRP}	5	—	5	—	5	—	ns	
OE to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
OE delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
CAS delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7

Read Cycle

		HM5117805							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from RAS	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from CAS	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17
Access time from OE	t_{OEA}	—	13	—	15	—	18	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to CAS	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from RAS	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to RAS	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to RAS lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to CAS lead time	t_{CAL}	15	—	18	—	23	—	ns	
CAS to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	20
Output data hold time from OE	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13, 20
Output buffer turn-off to OE	t_{OEZ}	—	13	—	15	—	15	ns	13
CAS to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5
Output data hold time from RAS	t_{OHR}	3	—	3	—	3	—	ns	20
Output buffer turn-off to RAS	t_{OFR}	—	13	—	15	—	15	ns	20
Output buffer turn-off to WE	t_{WEZ}	—	13	—	15	—	15	ns	
WE to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
RAS to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
RAS next CAS delay time	t_{RNCD}	50	—	60	—	70	—	ns	

Write Cycle

		HM5117805							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	7	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	7	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7	—	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	7	—	10	—	13	—	ns	15

Read-Modify-Write Cycle

		HM5117805							
		-5		-6		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	13	—	15	—	18	—	ns	

Refresh Cycle

		HM5117805						
		-5		-6		-7		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	7	—	10	—	10	—	ns
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	7	—	10	—	10	—	ns
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns

EDO Page Mode Cycle

		HM5117805							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	19
EDO page mode RAS pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from CAS precharge	t_{CPA}	—	28	—	35	—	40	ns	9, 17
RAS hold time from CAS precharge	t_{CPRH}	28	—	35	—	40	—	ns	
Output data hold time from CAS low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
CAS hold time referred OE	t_{COL}	7	—	10	—	13	—	ns	
CAS to OE setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from CAS precharge	t_{RCHC}	28	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HM5117805							
		-5		-6		-7			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	t_{HPRWC}	57	—	68	—	79		ns	
WE delay time from CAS precharge	t_{CPW}	45	—	54	—	62		ns	14

Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	32	ms	2048 cycles
Refresh period (L-version)	t_{REF}	128	ms	2048 cycles

Self Refresh Mode (L-version)

		HM5117805L						
		-5		-6		-7		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	100	—	µs
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	90	—	110	—	130	—	ns
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met; t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met; t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters; they are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open-circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{CPA}.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in an EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), the minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified t_{HPC} (min) value. The value of the $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).

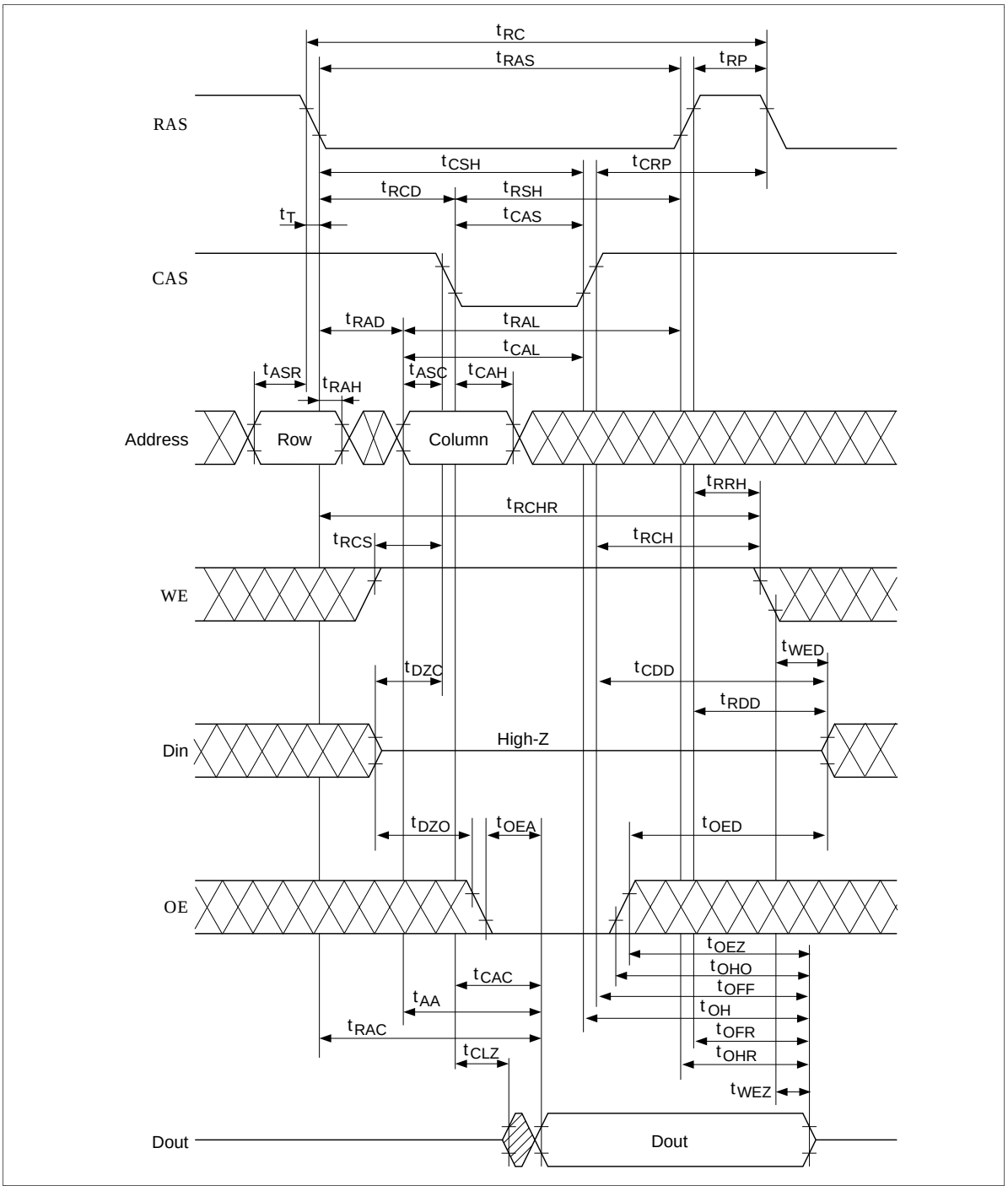
20. Data output turns off and becomes high-impedance from the later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn-off time are specified by the timing specifications of the later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between t_{OHR} and t_{OH} and between t_{OFR} and t_{OFF}.
21. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self-refresh mode. If t_{RASS} ≥ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
22. If you use $\overline{RAS}$-only refresh or CBR burst refresh mode in normal read/write cycles, 2048 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 32 ms immediately after exiting from and before entering into the self-refresh mode.
23. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
24. Repetitive self-refresh mode without refreshing all memory is not allowed. Once you exit from self-refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
25. XXX: H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

    ///////: Invalid Dout

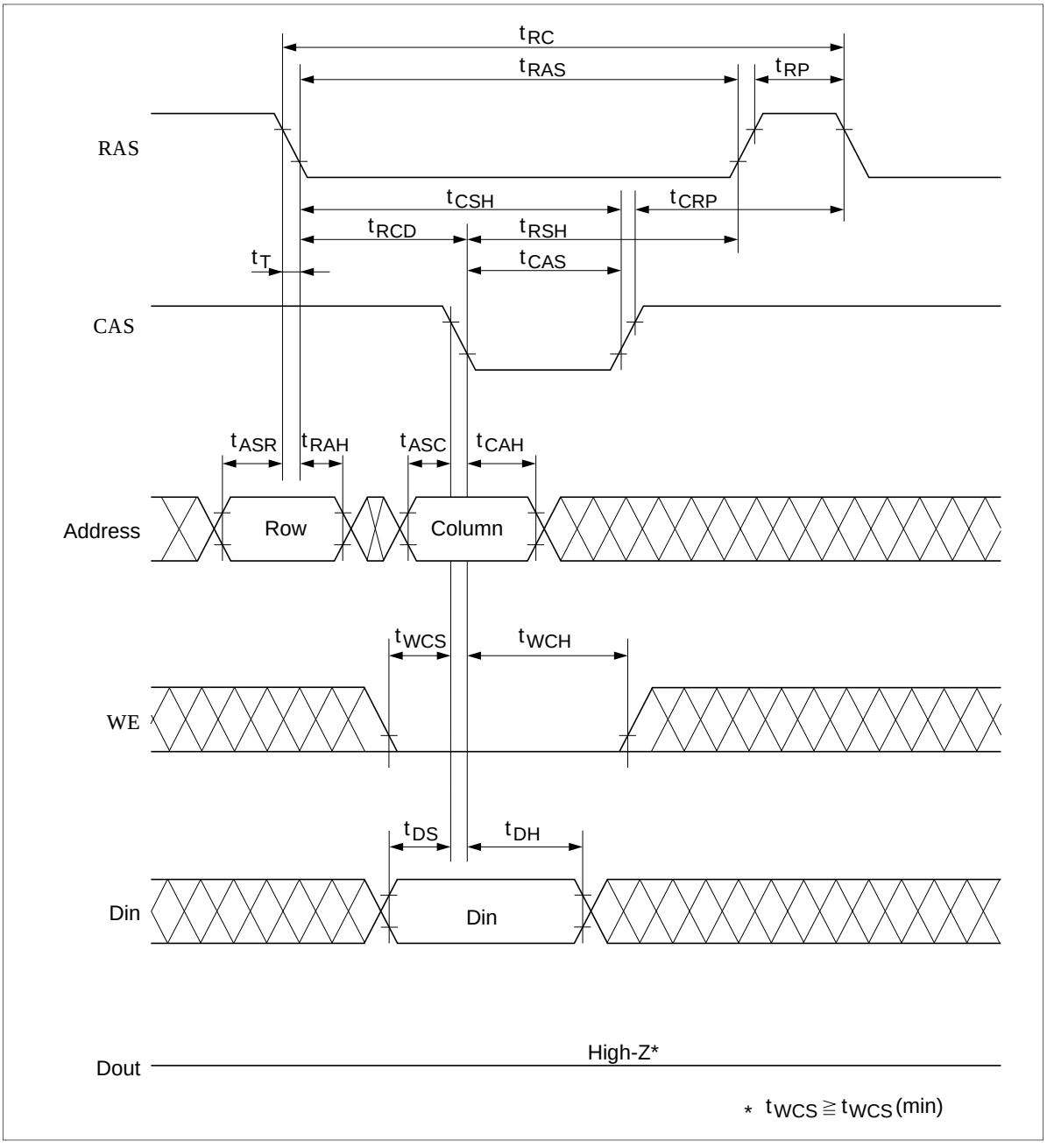
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

Timing Waveforms[*25]

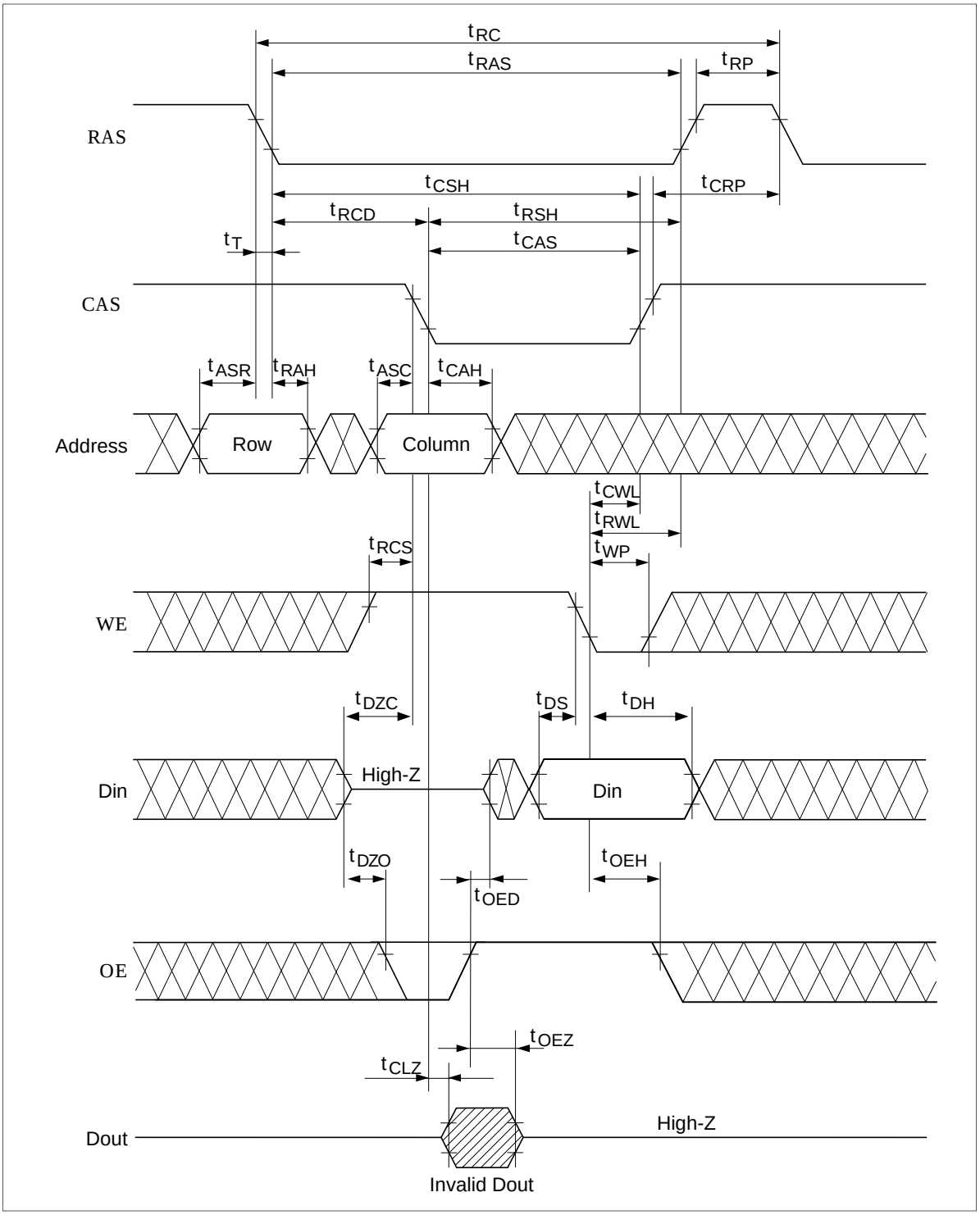
Read Cycle



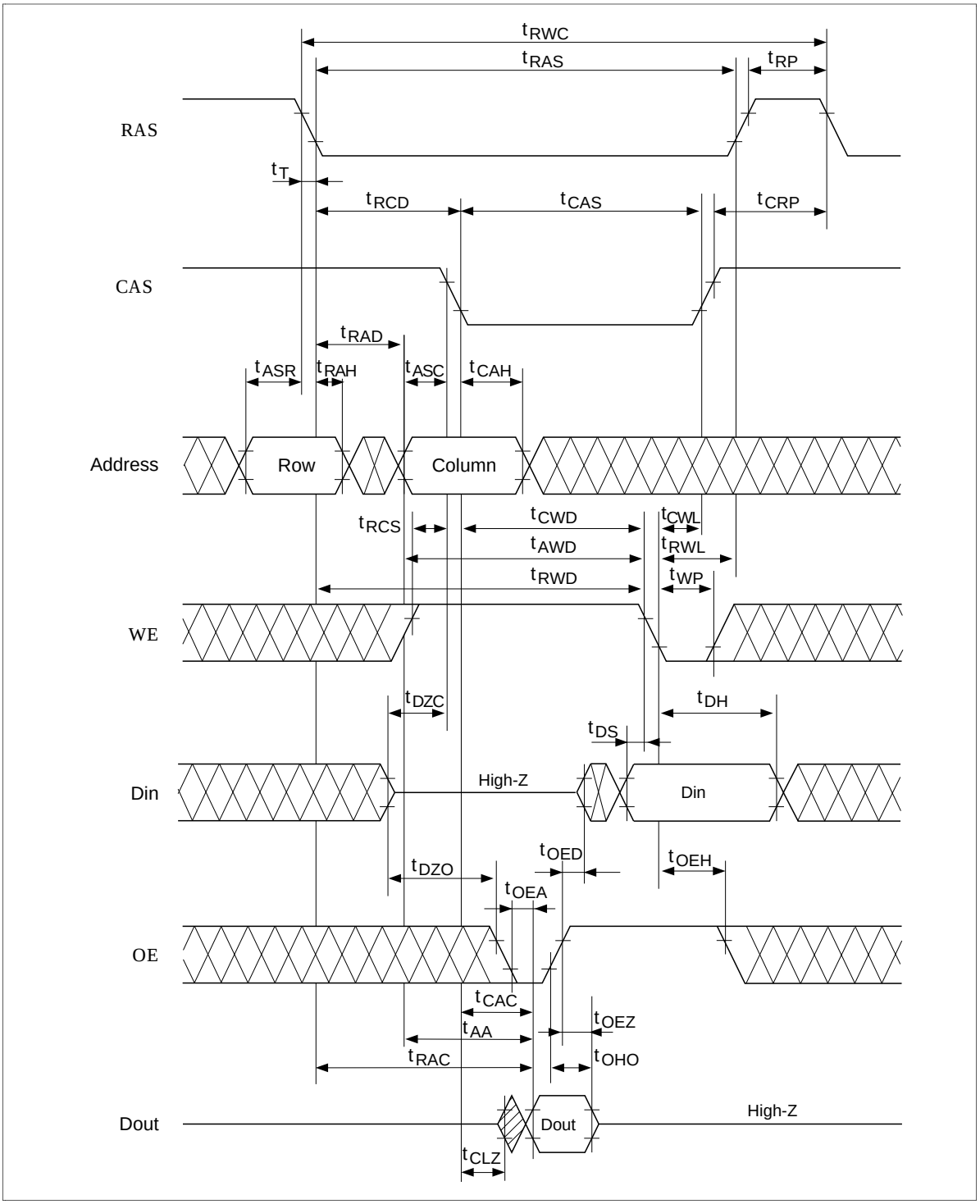
Early Write Cycle



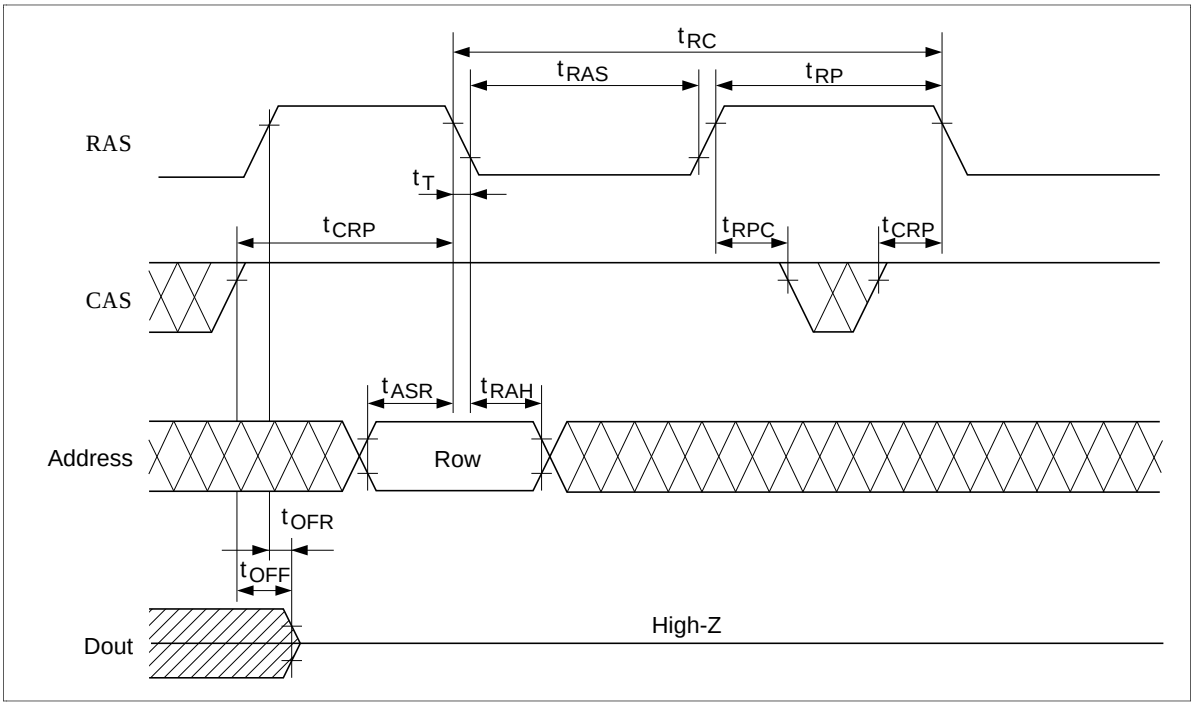
Delayed Write Cycle[*18]



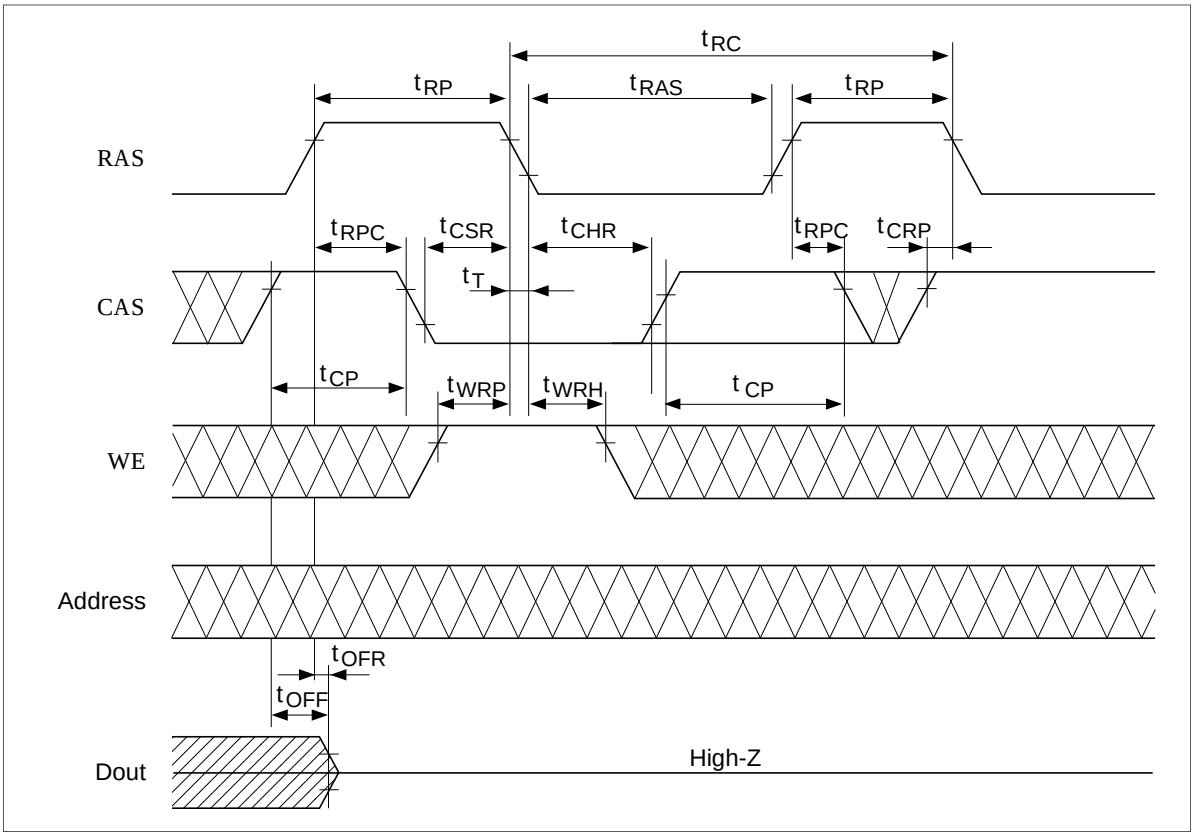
Read-Modify-Write Cycle[*18]



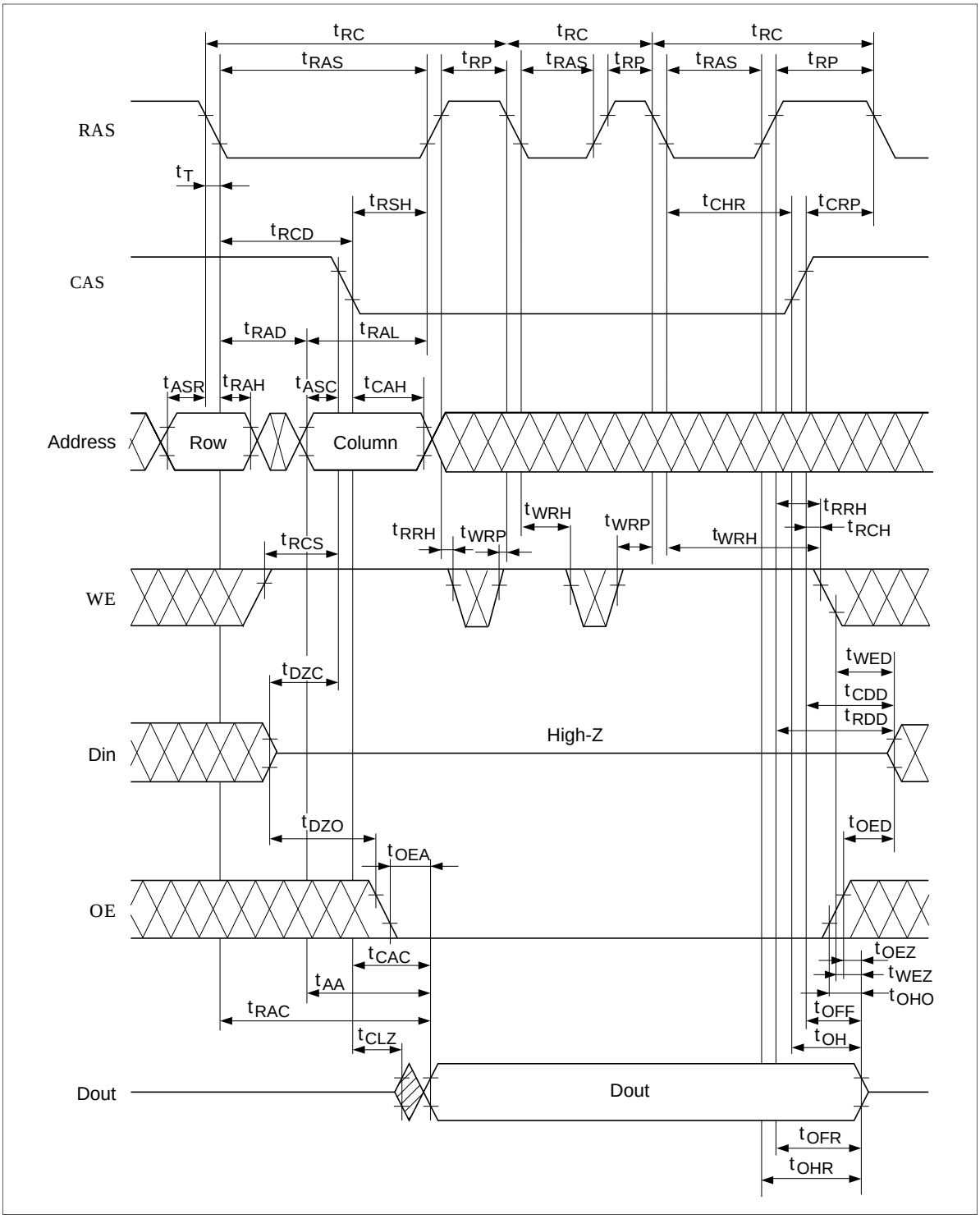
RAS-Only Refresh Cycle



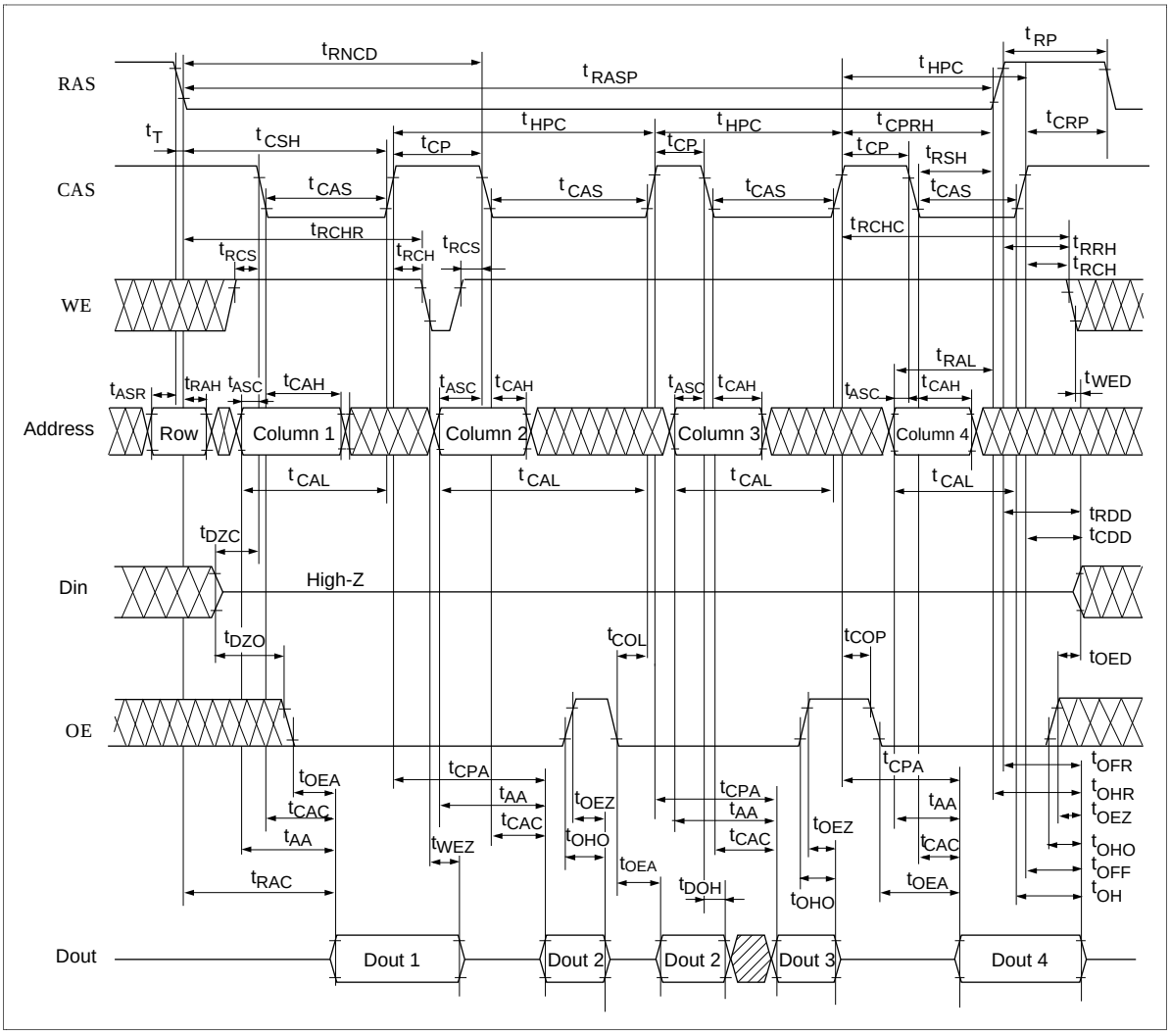
CAS-Before-RAS Refresh Cycle



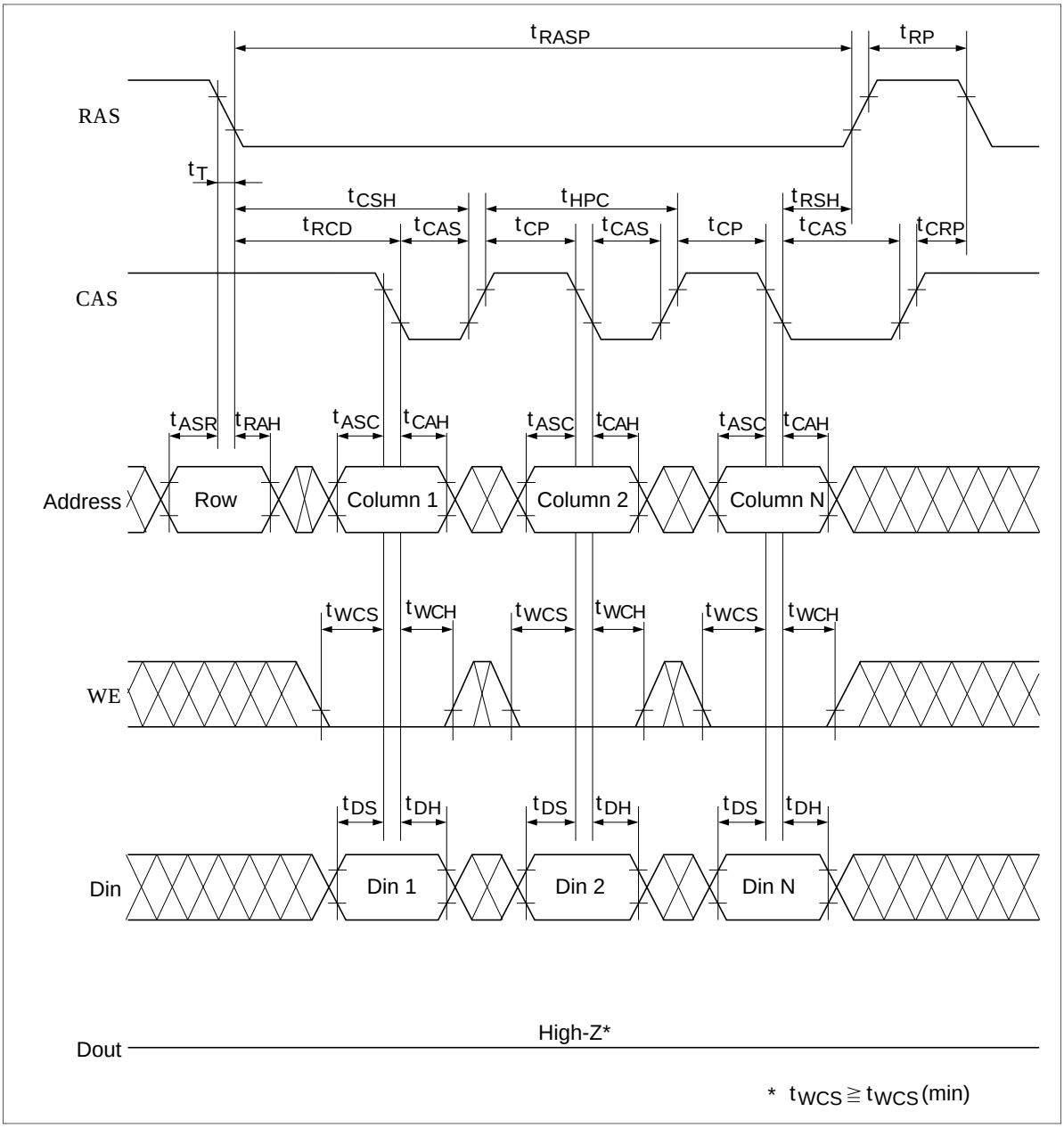
Hidden Refresh Cycle



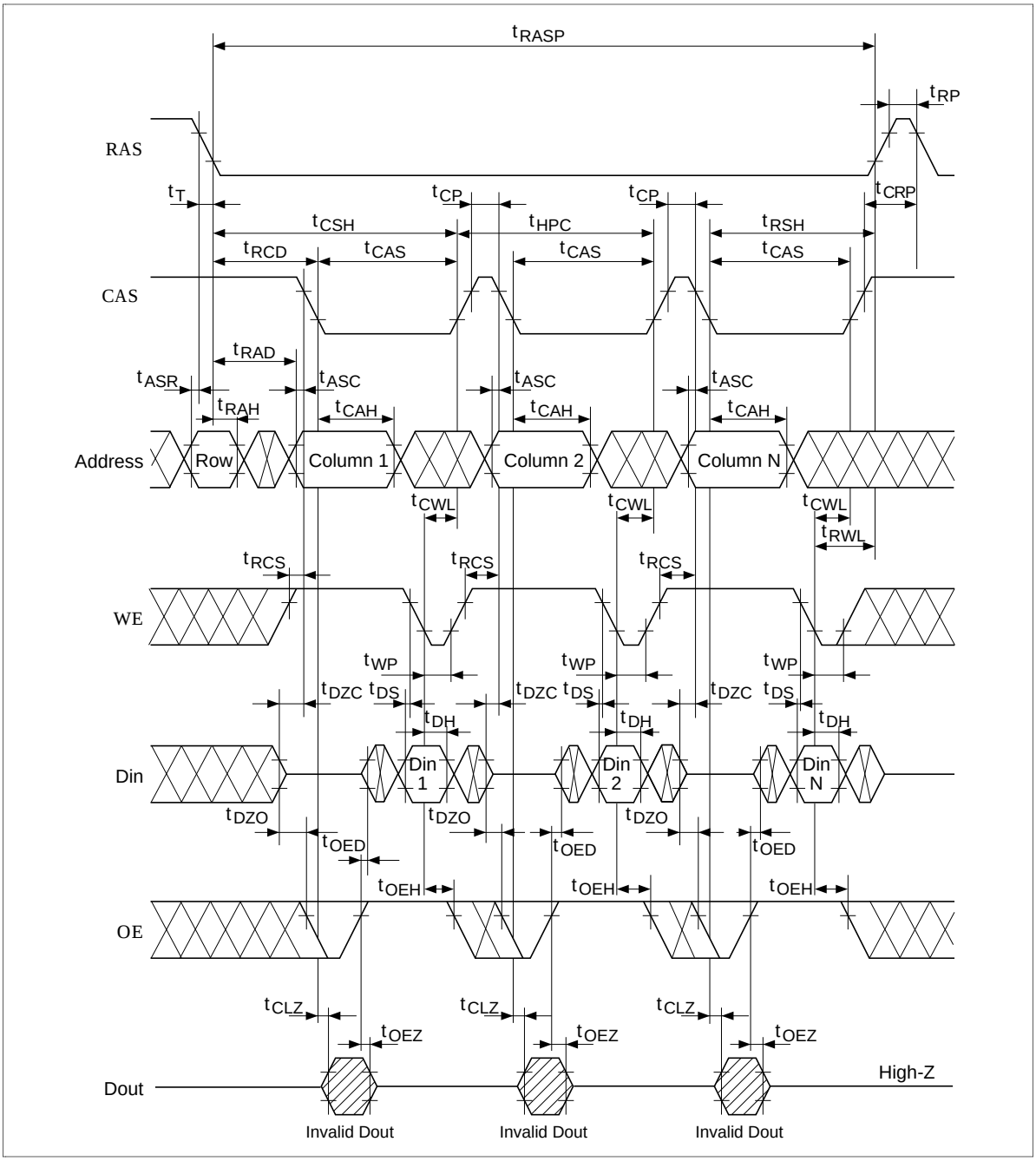
EDO Page Mode Read Cycle



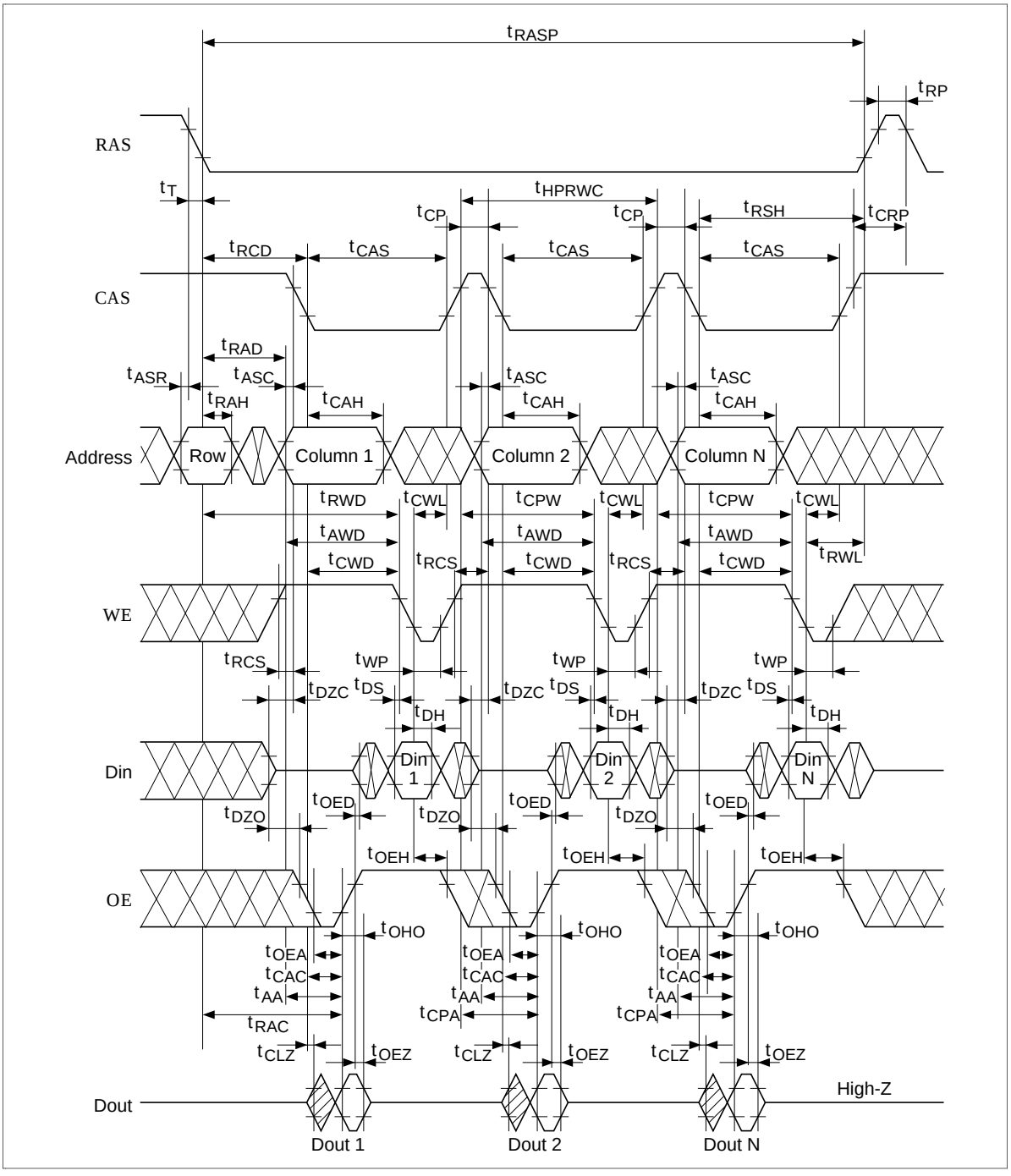
EDO Page Mode Early Write Cycle



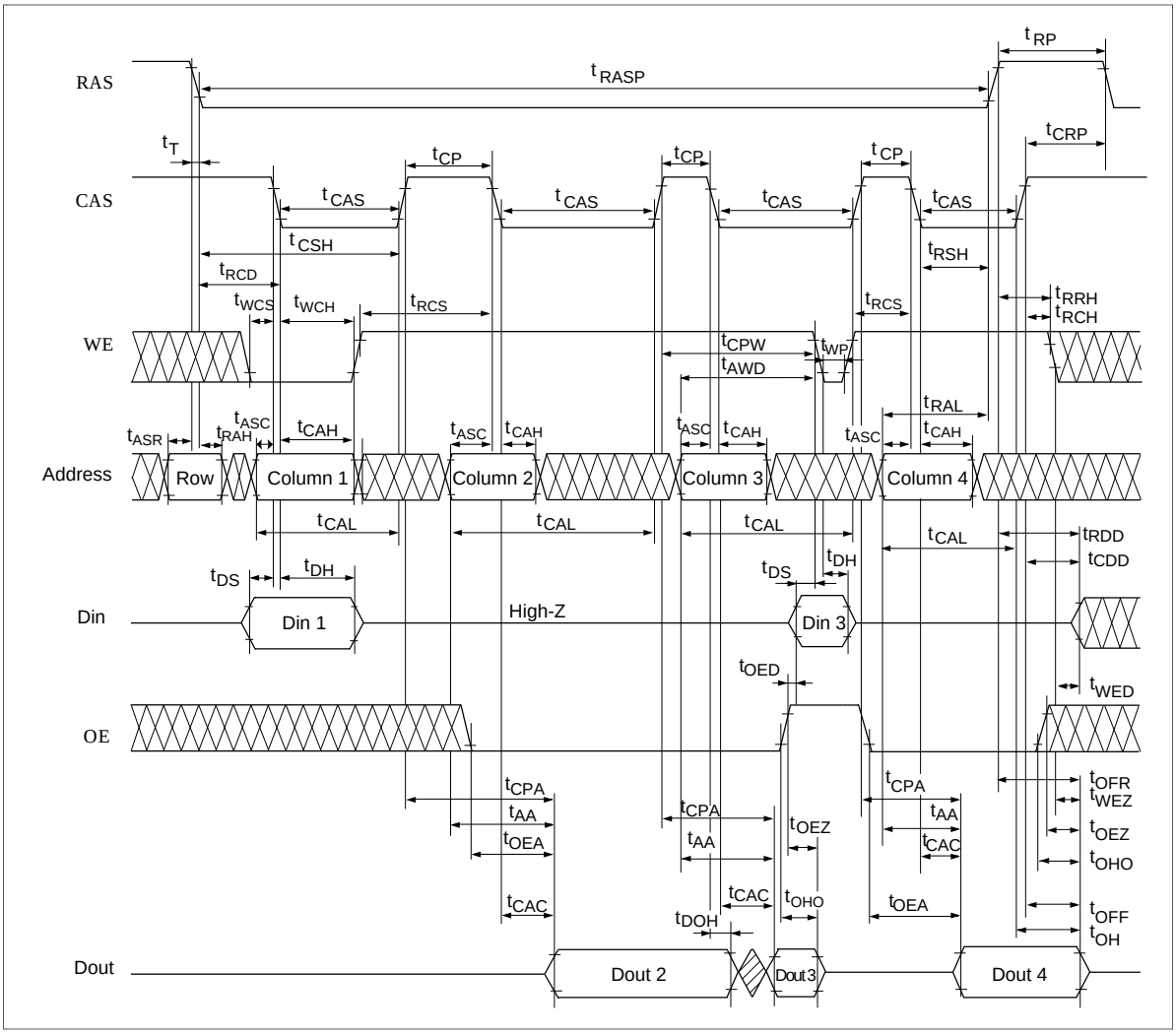
EDO Page Mode Delayed Write Cycle[*18]



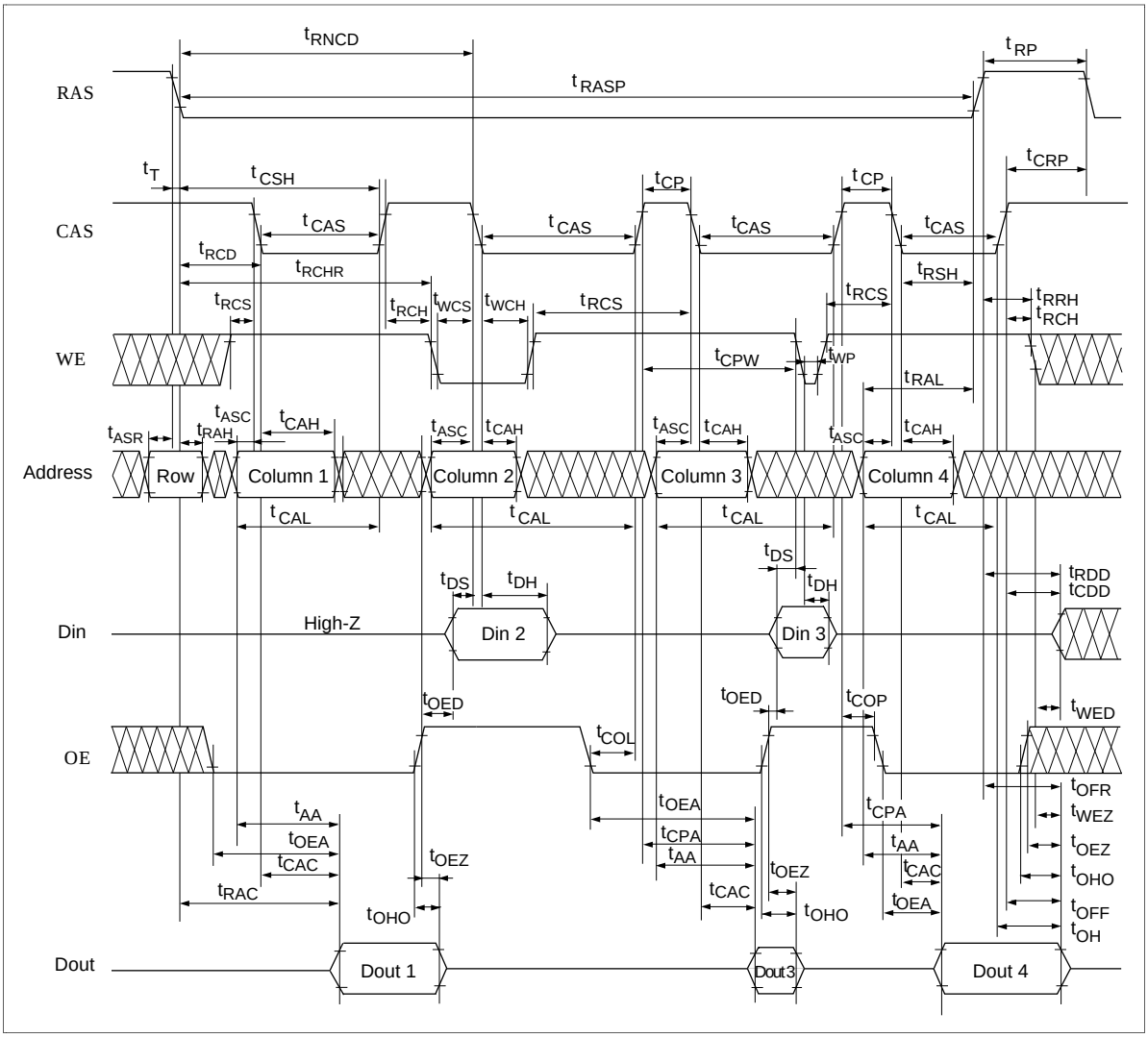
EDO Page Mode Read-Modify-Write Cycle[*18]



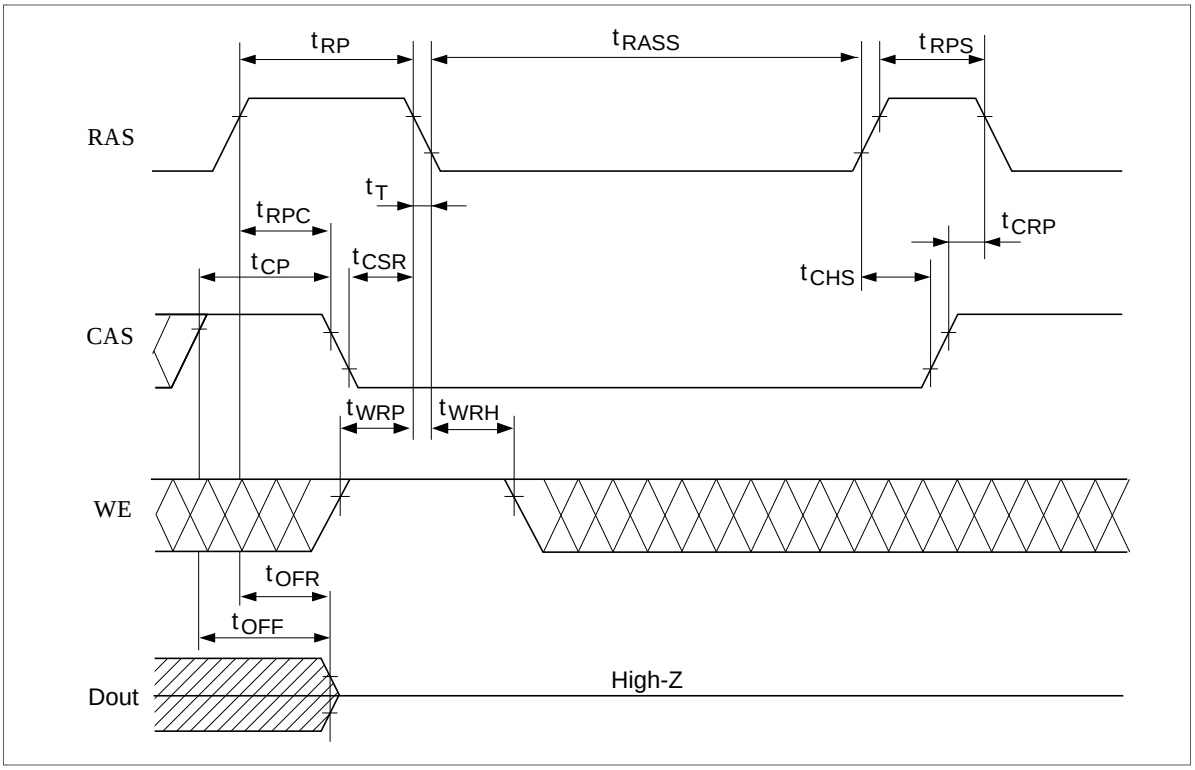
EDO Page Mode Mix Cycle (1)



EDO Page Mode Mix Cycle (2)



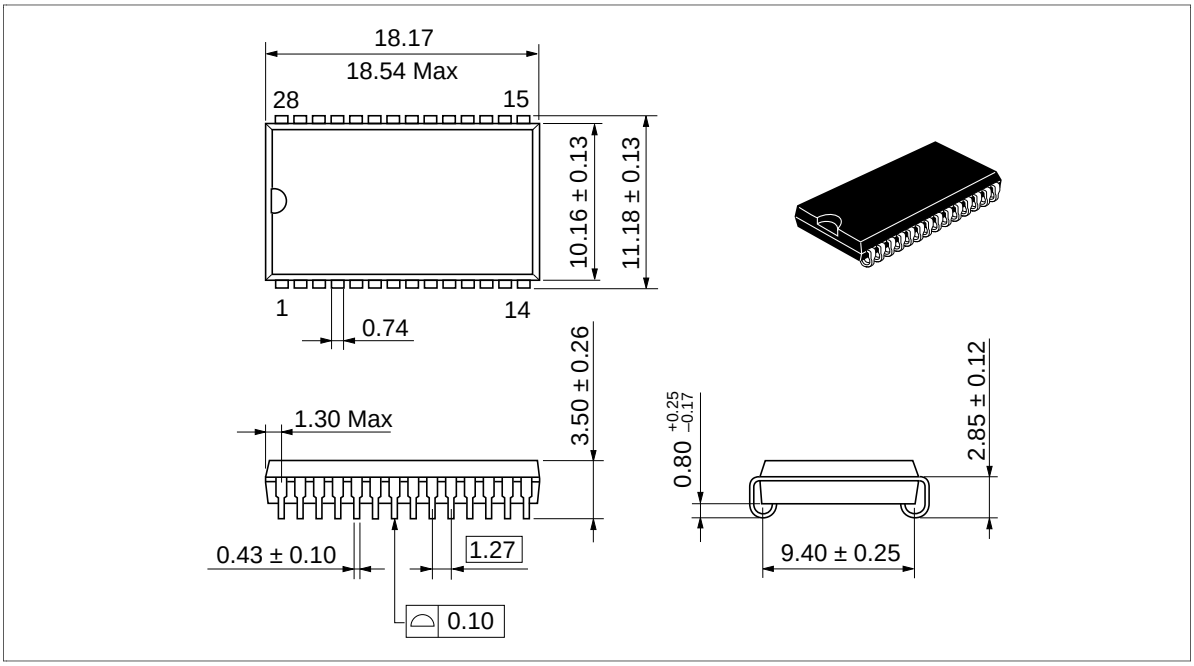
Self Refresh Cycle (L-version) [*21, 22, 23, 24]



Package Dimensions

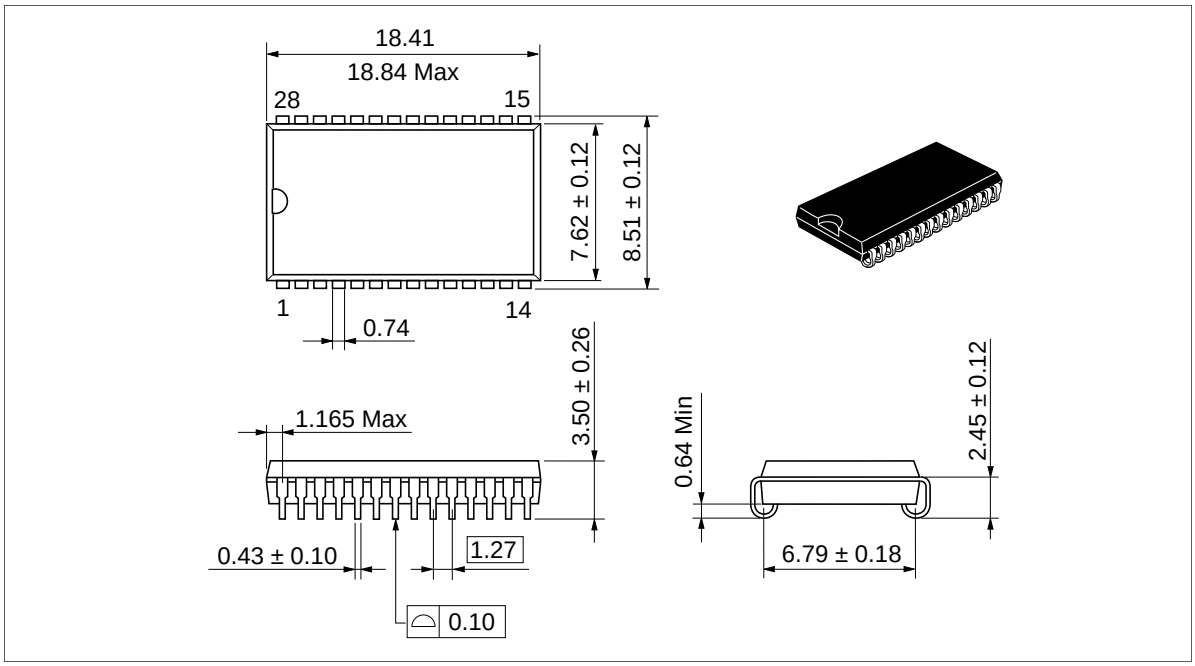
HM5117805J/LJ Series (CP-28DA)

Unit: mm



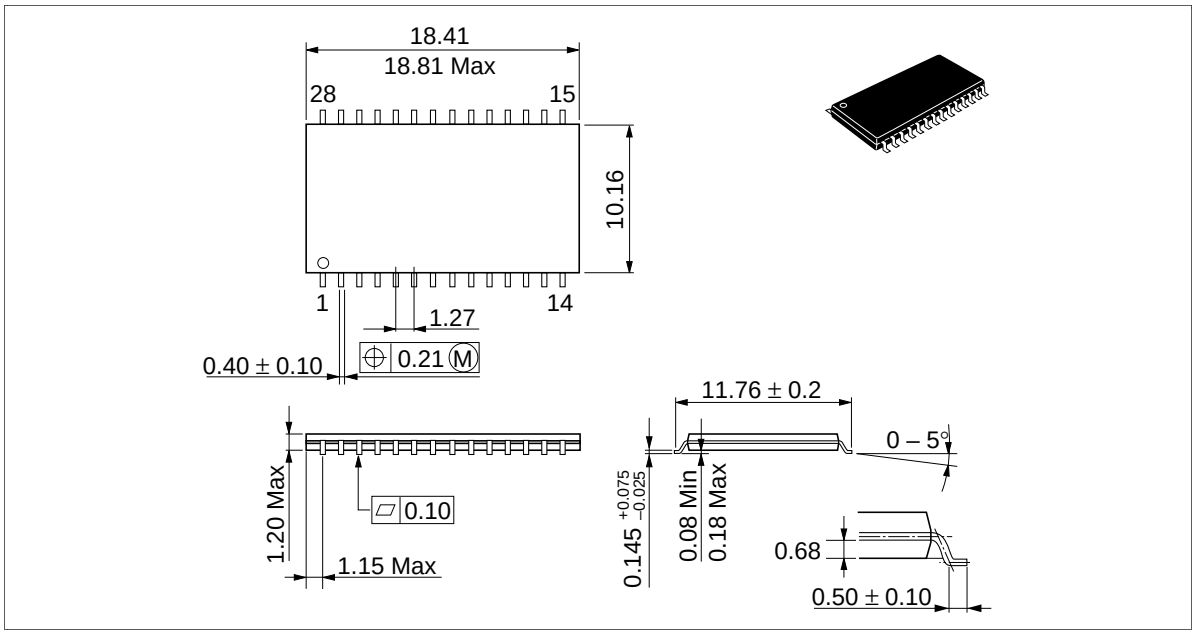
HM5117805S/LS Series (CP-28DNA)

Unit: mm



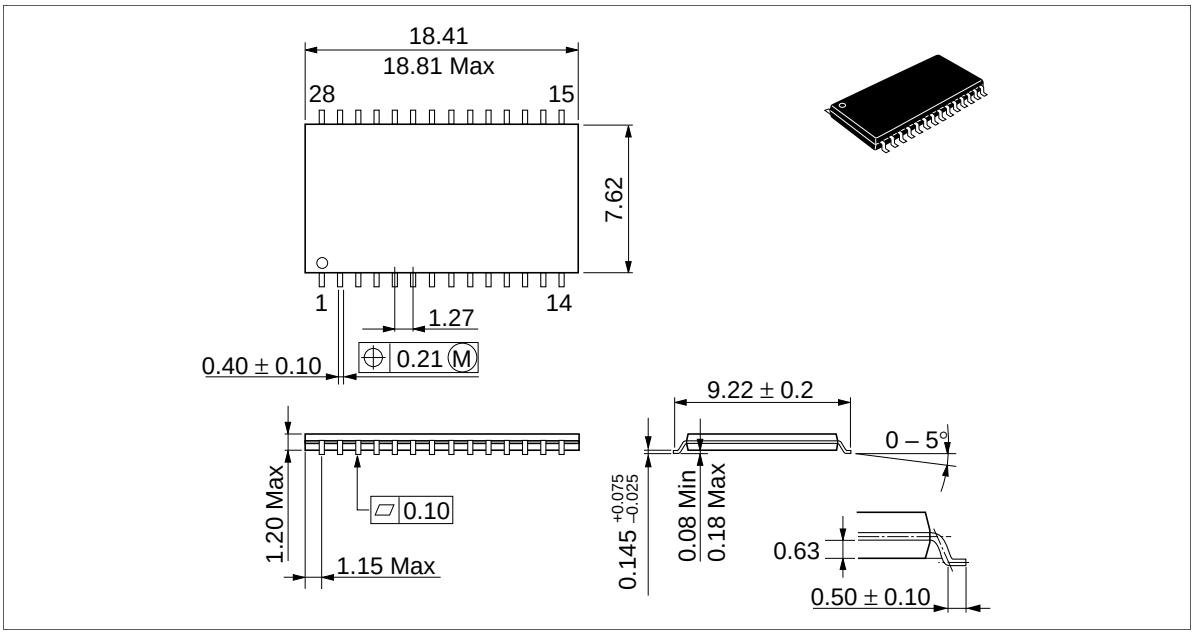
HM5117805TT/LTT Series (TTP-28DA)

Unit: mm



HM5117805TS/LTS Series (TTP-28DB)

Unit: mm



Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Oct. 1, 1996	Initial issue	Y. Kasama	M. Mishima
2.0	Nov. 8, 1996	Addition of HM5117805-5 Series Addition of HM5117805S/LS Series (CP-28DNA) Addition of HM5117805TS/LTS Series (TTP-28DB) Power dissipation (active) 660/605 mW(max) to 605/550/495 mW (max) DC Characteristics I_{CC1} max: 120/110 mA to 110/100/90 mA I_{CC3} max: 120/110 mA to 110/100/90 mA I_{CC6} max: 120/110 mA to 110/100/90 mA I_{CC7} max: 120/110 mA to 100/90/85 mA AC Characteristics t_{RCD} min: 20/20 ns to 11/14/14 ns t_{RAD} min: 15/15 ns to 9/12/12 ns t_{RSH} min: 15/18 ns to 10/13/13 ns t_{RRH} min: 0/0 ns to 5/5/5 ns t_{RWC} min: 149/175 ns to 111/135/161 ns t_{RWD} min: 82/95 ns to 67/79/92 ns t_{CWD} min: 37/43 ns to 30/34/40 ns t_{AWD} min: 52/60 ns to 42/49/57 ns t_{RPC} min: 0/0 ns to 5/5/5 ns t_{HPRWC} min: 79/90 ns to 57/68/79 ns Timing Waveforms Addition of t_{RNCD} timing to EDO page mode mix cycle (2)		

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