HM71V832 Series

32768-word x 8-bit Nonvolatile Ferroelectric RAM

HITACHI

Preliminary
Rev. 0.0
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Description

The HM71V832 is a ferroelectric RAM, or FARM® memory, organized as 32k-word x 8-bit. FRAM® memory products from Hitachi combine the read/write characteristics of semiconductor RAM with nonvolatile storage. This product is manufactured in a 0.8 micron silicon gate CMOS technology with the addition of integrated thin film ferroelectric storage cells developed. The ferroelectric cells are polarized on each read or write cycle, therefore no special store or recall sequence is required. The memory is always static and nonvolatile. Hitachi's FRAM® products operate from a single 3 V power supply and are CMOS compatible on all inputs and outputs. The HM71V832 utilizes the JEDEC standard bytewide SRAM pinout.

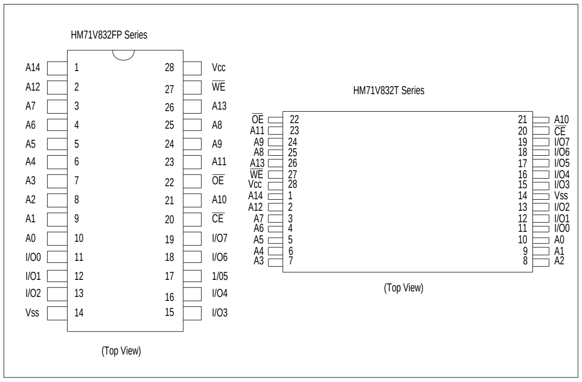
Features

- Single 3 V power supply (2.7 V to 3.6 V)
- Fully synchronous operation
  - — 150 ns Read access
  - — 235 ns Read/write cycle time
  - — 10^{12} Read/write cycle endurance
- Low power consumption
  - — Active: 20 mA (typ)
  - — Standby: 15 µA (typ)
- JEDEC standard 21-C write protection (Entire memory) and Selectable 4K byte write protection
- 10 year data retention
- CMOS compatible I/O pins
- 28 pin SOP and TSOP packages
- 0° to +70°C ambient operating temperature range

Ordering Information

Type No.	Access time	Package
HM71V832FP-15	150 ns	450 mil 28-pin plastic SOP (FP-28DA)
HM71V832T-15	150 ns	8 mm x 13.4 mm 28-pin TSOP (TFP-28DB)

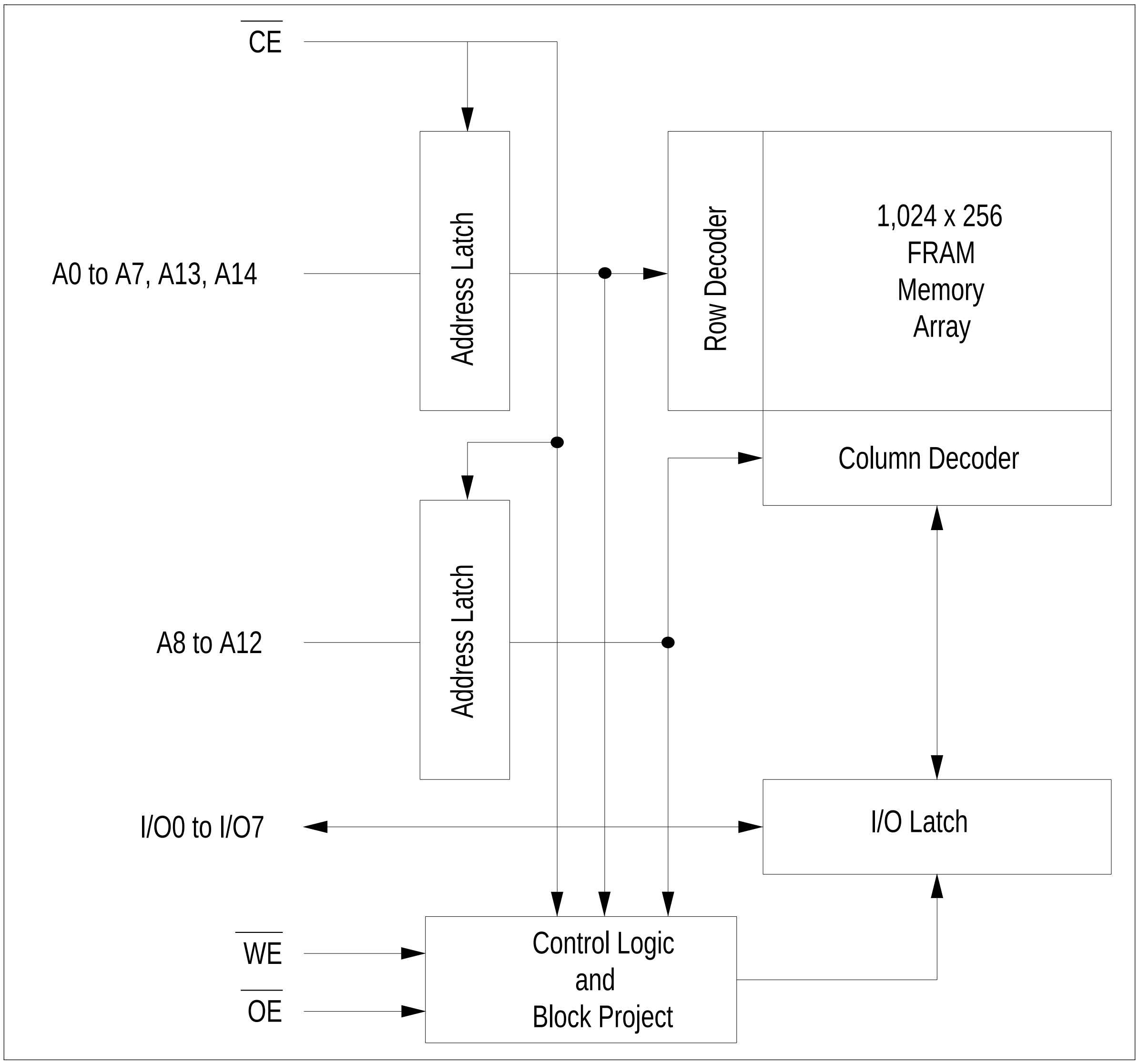
Pin Arrangement



Pin Description

Pin name	Function
A0 to A14	Address inputs
I/O0 to I/O7	Data input/output
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Device Operation

- Read operation:

  When $\overline{CE}$ is low and $\overline{WE}$ is high a read operation is performed by the FRAM® memory. On the falling edge of $\overline{CE}$, all address bits (A0 to A14) are latched into the part and the cycle is started. Data will appear on the output pins a maximum access time (t_{CE}) after the beginning of the cycle. The designer should ensure that there are no address transitions from t_{AS} (setup time) before the falling edge of $\overline{CE}$ to t_{AH} (hold time) after it. After t_{AH}, the address pins are ignored for the remainder of the cycle. It is equally important that $\overline{CE}$ be generated such that unwanted glitches or pulses, of any duration, be prevented. After the read has completed, $\overline{CE}$ should be brought high for the precharge interval (t_{PC}). During this period data is restored in the internal memory cells and the chip is prepared for the next read or write cycle. The HM71V832 will not operate in systems in which $\overline{CE}$ does not toggle with every access. The $\overline{OE}$ pin may be used to avoid bus conflicts on the system bus. Only when both $\overline{CE}$ and $\overline{OE}$ are low will the FRAM® memory drive its outputs. Under all other circumstances, the output drivers are held in a high impedance (High-Z) condition. Note that the internal read operation is performed regardless of the state of the $\overline{OE}$ pin.

- Write operation:

  When $\overline{CE}$ falls while $\overline{WE}$ is low, or $\overline{WE}$ falls while $\overline{CE}$ is low, a write operation will be performed by the FRAM® memory. On the falling edge of $\overline{CE}$, as in the read cycle, the address will be latched into the part with the same setup and hold requirements. As in the read cycle, $\overline{CE}$ must be held high for a precharge interval (t_{PC}) between each access. Data needs to be set up t_{DS} minimum on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Write operations take place regardless of the state of $\overline{OE}$, however, it may need to be driven high by the system at the beginning of the cycle in order to avoid bus conflicts.

  Data is immediately nonvolatile and power may be removed from the part upon completion of the precharge interval following the write. For better noise immunity, a 10 ns (typ) glitch protection is built into the $\overline{WE}$ signal.

- Write protection:

  The HM71V832 FRAM® memory uses a superset of JEDEC Standard 21-C for software data protection. The standard allows for the entire memory array to be protected or unprotected via software control. Hitachi enhanced the standard to allow each of the 4K word blocks on the HM71V832 to be individually protected or unprotected. The protection data map is stored in the nonvolatile block protection register. This data can be recalled at any time via the enhanced standard to restore the previously stored block protection map. The configuration data may also be modified via the enhanced standard.

- Standard JEDEC protection:

  Upon power up, the entire memory array is write protected as per the JEDEC standard. If desired, the entire memory array can be unprotected by executing the JEDEC disable sequence shown in Table 1. The entire memory array can be write protected by executing the JEDEC enable sequence shown in Table 1. Any time these two sequences are executed, the respective operation will be performed i.e. one should insure that these sequence of addresses is only executed if enabling or disabling write protection.

Table 1 JEDEC Write Protect Sequence

Cycle	Disable Sequence	Enable Sequence	Mode
1	1823 Hex	1823 Hex	Read
2	1820 Hex	1820 Hex	Read
3	1822 Hex	1822 Hex	Read
4	0418 Hex	0418 Hex	Read
5	041BHex	041B Hex	Read
6	0419 Hex	0419 Hex	Read
7	041A Hex	040A Hex	Read

- Enhanced block protection:

  Hitachi added capability to the HM71V832 to allow any of the eight 4K blocks to be individually protected or unprotected. This feature is enabled by adding one additional unique address to the standard JEDEC disable sequence as shown in Table 1. To write a specific block protect map to the HM71V832, the access to this added address should be a "WRITE" access as shown in Table 2. Each bit of the data word has a one to one correlation with a specific 4K block as shown in Table 4. A data of "1" enables write protection. A data of "0" allows writing to that block. It should be noted that data written on this sequence is written to the block protect register and not to address 040FH. If the previously configured block protection map is to be restored, then the access to 040FH address should be a "READ" cycle as shown in Table 3. The data on the I/O pins after an access time will be the data contained in the block protect register that is being restored, not the data at address 040FH. On the next rising edge of $\overline{CE}$ after executing the address sequence, in Table 2 or 3 the part will be placed into the write protected mode. The memory blocks that will be write protected will be those either written to the block protect register during that sequence or those restored from the previous contents the block protect register. For example, if the block protect register contained the following data 10011000, addresses 3000H to 4FFFH and 7000H to 7FFFH would be write protected, i.e. Blocks 3, 4 and 7. On a $\overline{WE}$ controlled write operation where $\overline{WE}$ rises prior to $\overline{CE}$, the data I/O outputs will become active a t_{WX} after $\overline{WE}$ rises. The data on the outputs mirror the data just written to the addressed location so no bus contention should arise. However, the addition of write protection required that the I/O outputs perform differently if a write to a protected location was attempted. If a write operation is attempted to a protected location, the I/O outputs remain high impedance after $\overline{WE}$ returns high. This is done to prevent any bus contention that might arise due to the data driven on the I/O lines externally and the data at the accessed memory location being different. The I/O outputs will remain high impedance until the next memory cycle.

Table 2 Extended Write Protect Sequence

Cycle	Sequence	I/O	Mode
1	1823 Hex	Data	Read
2	1820 Hex	Data	Read
3	1822 Hex	Data	Read
4	0418 Hex	Data	Read
5	041B Hex	Data	Read
6	0419 Hex	Data	Read
7	041A Hex	Data	Read
8	040F Hex	New block protect data	Write

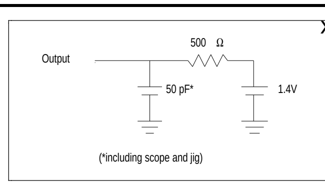
Table 3 Extended Restore Protect Sequence

Cycle	Sequence	I/O	Mode
1	1823 Hex	Data	Read
2	1820 Hex	Data	Read
3	1822 Hex	Data	Read
4	0418 Hex	Data	Read
5	041B Hex	Data	Read
6	0419 Hex	Data	Read
7	041A Hex	Data	Read
8	040F Hex	Restore block protect data	Read

Table 4 Block Number To I/O Correlation

4K Block Number	A14	A13	A12	I/O#
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

Function Truth Table

Function (Mode)	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$
Standby/Precharge	H	x	x
Latch address		x	x
Read	L	H	L
Write	L	L	x

Notes: H means logic HIGH. L means logic LOW. x means H or L.

Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Power supply voltage	Vcc	-0.5 to +5.0	V
Voltage on any pin relative to Vss	V_T	-0.5 to +5.0	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +85	°C

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	$0.7V_{CC}$	–	V_{CC} + 0.3	V
	V_{IL}	-0.3	–	$0.2V_{CC}$	V

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6V, V_{SS} = 0 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	–	–	10	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	–	–	10	µA	Vout = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	–	20	30	mA	V_{CC} = Max, $\overline{CE}$ cycling at minimum cycle time $I_{I/O}$ = 0 mA; $\overline{OE}$, $\overline{WE}$, AX = CMOS input levels
Standby power supply current	I_{SB}	–	15	25	µA	V_{CC} = Max, $\overline{CE}$ = V_{CC} input levels = V_{CC} or GND $I_{I/O}$ = 0 mA
Output low voltage	V_{OL}	–	–	0.2	V	I_{OL} = 100 µA
		–	–	0.4	v	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	V_{CC} -0.2	–	–	V	I_{OH} = -100 µA
		2.4	–	–	V	I_{OH} = -2.0 mA

Capacitance (Ta = 25°C, f = 1.0 MHz, V_{CC} = 3.0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
input capacitance	Cin	–	–	6	pF	$V_{I/O}$ = 0 V	1
input/output capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} =2.7 V to 3.6 V, V_{SS} = 0 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input rise and fall time:≤ 10 ns
- Input and output timing reference levels: 1.5 V

Function Truth Table

Function (Mode)	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$
Standby/Precharge	H	x	x
Latch adderss		x	x
Read	L	H	L
Write	L	L	x

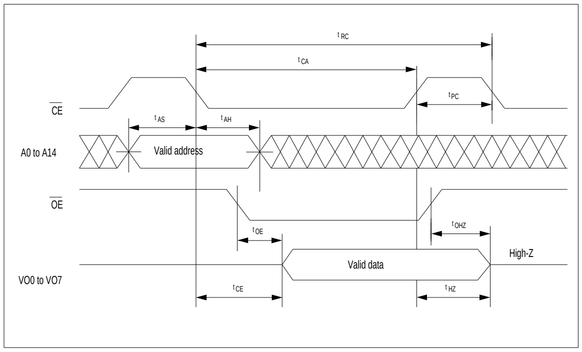
Notes : H means logic HIGH. L means logic LOW. x means H or L.

Read Cycle

			HM71V832-15			
Parameter	**Symbol**	**JEDEC Symbol**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	t_{ELEL}	235	–	ns	
Chip enable active time	t_{CA}	t_{ELEH}	150	10000	ns	
Precharge time	t_{PC}	t_{EHEL}	85	–	ns	
Address setup time	t_{AS}	t_{AVEL}	0	–	ns	
Address hold time	t_{AH}	t_{ELAX}	15	–	ns	
Chip enable access time	t_{CE}	t_{ELQV}	–	150	ns	
Output enable access time	t_{OE}	t_{OLQV}	–	25	ns	
Chip enable to output High-Z	t_{HZ}	t_{EHQZ}	–	25	ns	1
Output enable to output Hihg-z	t_{OHZ}	t_{OHQZ}	–	25	ns	1

Note: 1. This parameter is periodically sampled and not 100% tested.

Read Timing Waveform

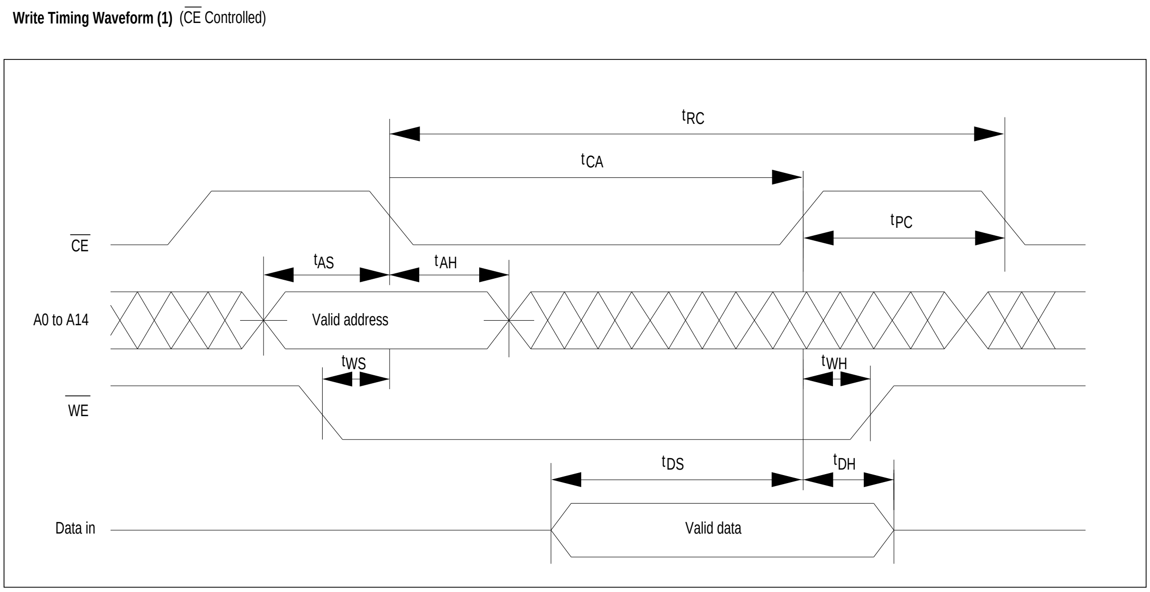


Write Cycle

			HM71V832-15			
Parameter	**Symbol**	**JEDEC Symobl**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	t_{ELEL}	235	–	ns	
Chip enable active time	t_{CA}	t_{ELEH}	150	10000	ns	
Chip enable to write High	t_{CW}	t_{ELWH}	150	–	ns	
Precharge time	t_{PC}	t_{EHEL}	85	–	ns	
Address setup time	t_{AS}	t_{AVEL}	0	–	ns	
Address hold time	t_{AH}	t_{ELAX}	15	–	ns	
Write enable pulse width	t_{WP}	t_{WLWH}	50	–	ns	
Data setup time	t_{DS}	t_{DVWH}	50	–	ns	
Data hold time	t_{DH}	t_{WHDX}	0	–	ns	
Write enable Low to output High-Z	t_{WZ}	t_{WLQZ}	–	25	ns	1
Write enable High to output driven	t_{WX}	t_{WHQX}	10	–	ns	1
Chip enable to output High-Z	t_{HZ}	t_{EHQZ}	–	25	ns	1
Write setup	t_{WS}	t_{CLWL}	0	–	ns	2
Write hold	t_{WH}	t_{WHCH}	0	–	ns	2

Notes: 1. This parameter is periodically sampled and not 100% tested.
2. Not a device specification, merely distinguished $\overline{CE}$ and $\overline{WE}$ controlled accesses.

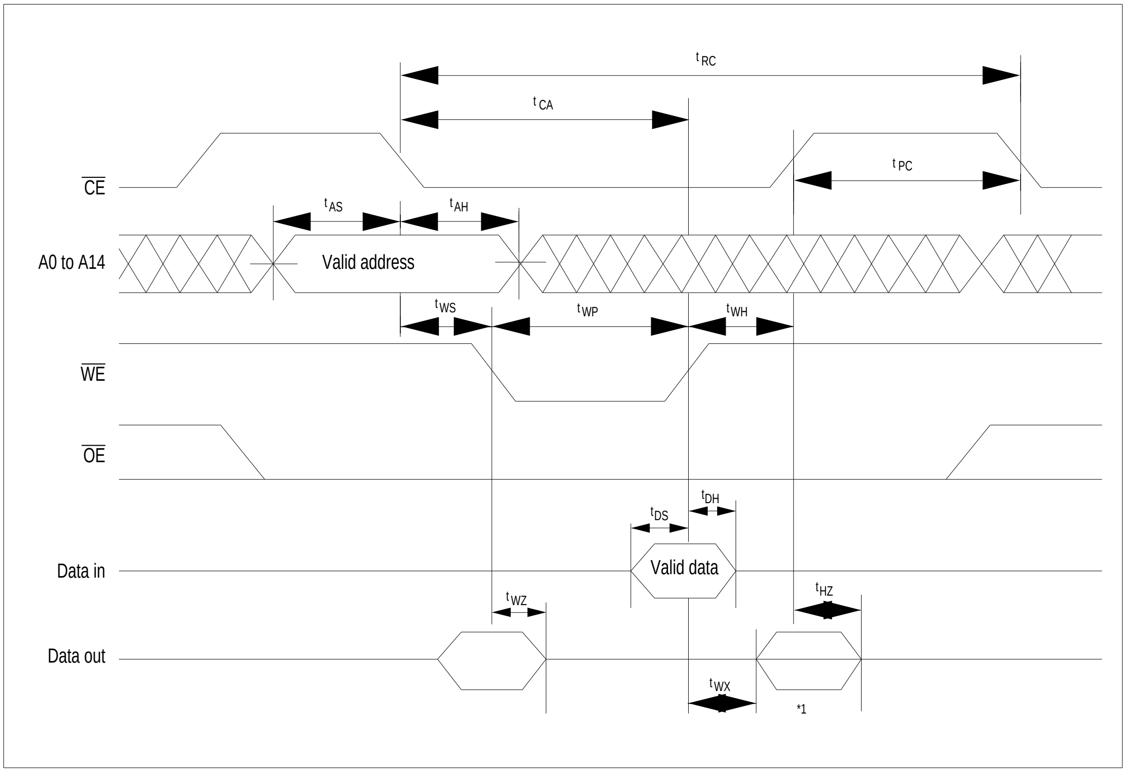
Write Timing Waveform (1) ($\overline{\text{CE}}$ Controlled)



Note: State of $\overline{\text{OE}}$ does not affect operation to device for this cycle.

Write Timing Waveform (2) ($\overline{\text{WE}}$ Controlled)

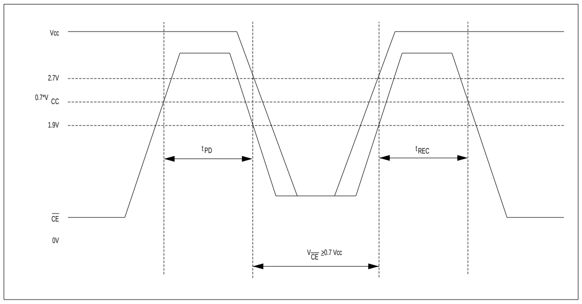
Write Timing Waveform (2) ($\overline{WE}$ Controlled)



Note: 1. Output remains high impedance after write attempt to a protected memory location

Power Down/Power Up Conditions

Care must be taken during power sequencing to prevent data loss resulting from memory operations during out of spec voltage conditions. This is managed by detecting power failure with sufficient time t_{PD} to disable memory operation prior to V_{CC} dropping below its lower specification, 2.7 V. During power up, the memory operation should be disabled until time t_{REC} after V_{CC} reaches its minimum operating Voltage, 2.7 V.

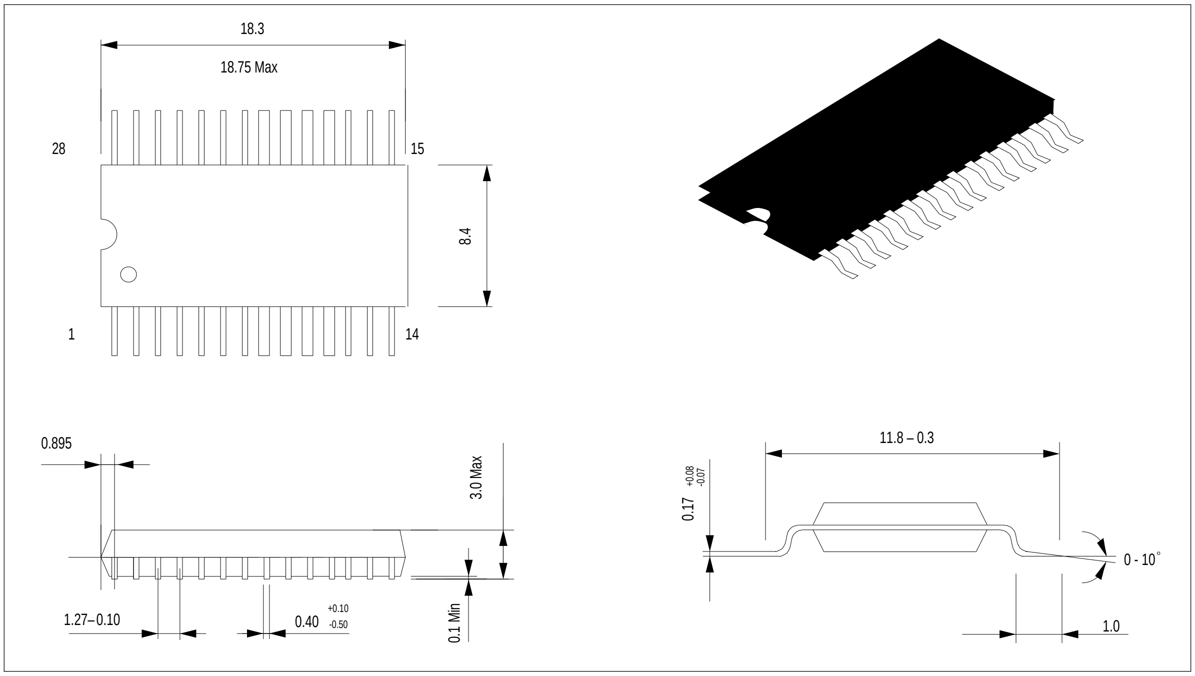


Power Up/Power Down Cycle

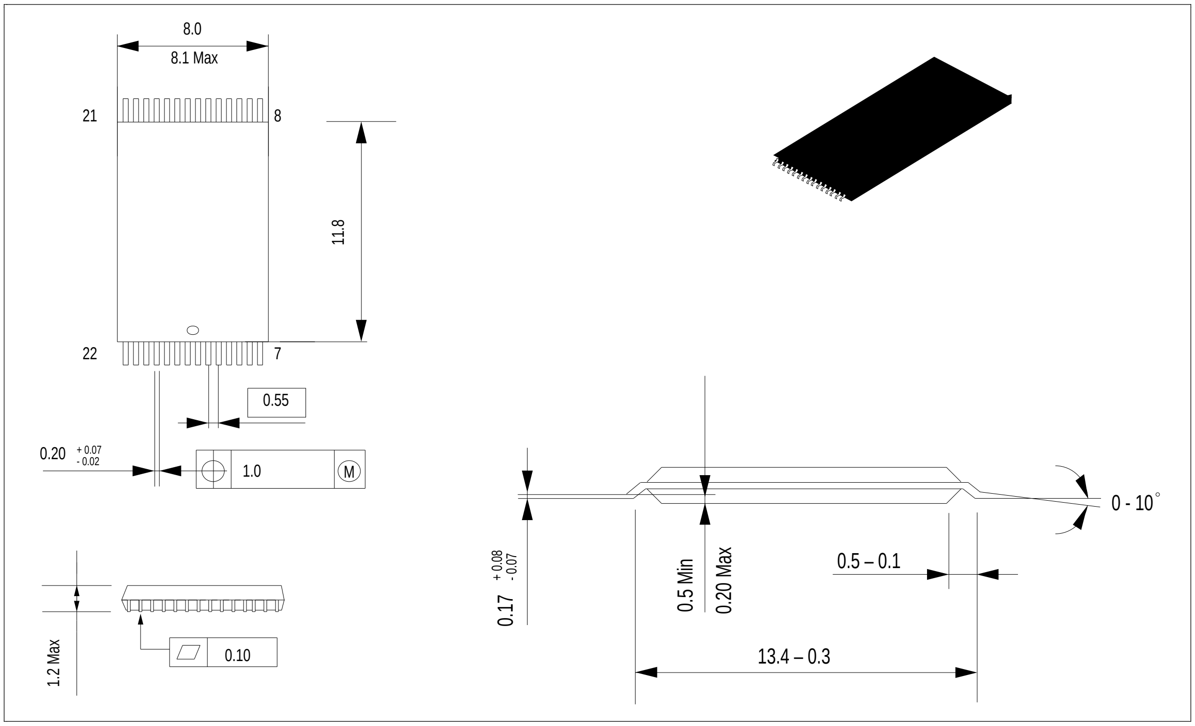
		HM71V832-15			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
$\overline{CE}$ signal stable to power down	t_{PD}	85	–	–	ns
Power up to operation	t_{REC}	85	–	–	ns

Package Dimensions

HM71V832FP Series (FP-28DA) Unit: mm



HM71V832T Series (TFP-28DB) Unit: mm


8.0
8.1 Max
21
8
22
7
11.8
0.55
0.20 + 0.07 - 0.02
1.0
M
1.2 Max
0.10
0 - 10°
0.17 + 0.08 - 0.07
0.5 Min
0.20 Max
0.5 – 0.1
13.4 – 0.3