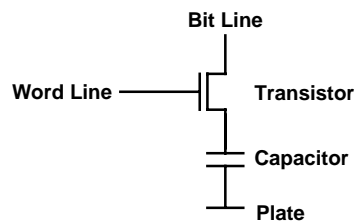

7 DRAM TECHNOLOGY

OVERVIEW

DRAM (Dynamic Random Access Memory) is the main memory used for all desktop and larger computers. Each elementary DRAM cell is made up of a single MOS transistor and a storage capacitor (Figure 7-1). Each storage cell contains one bit of information. This charge, however, leaks off the capacitor due to the sub-threshold current of the cell transistor. Therefore, the charge must be refreshed several times each second.



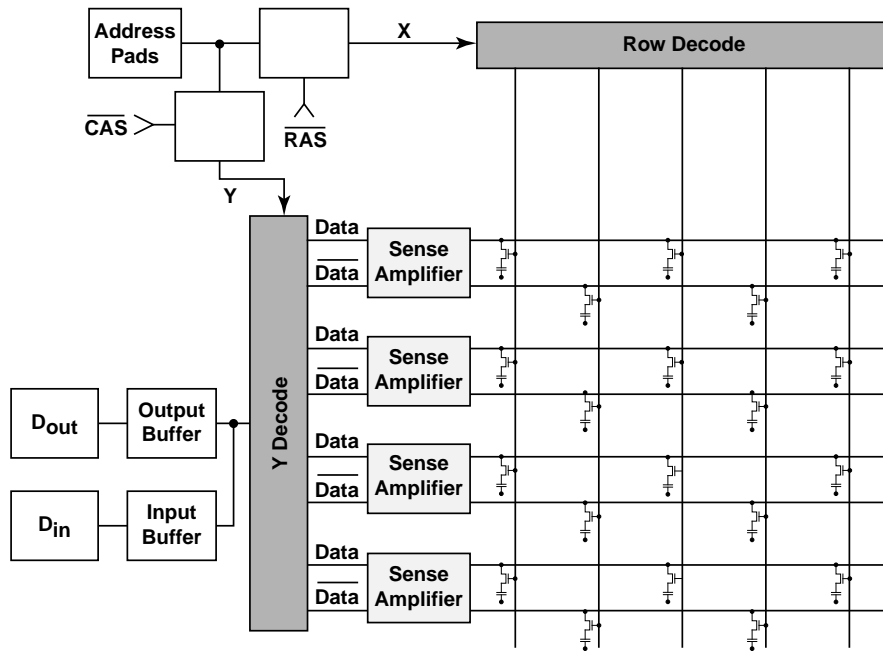
Source: ICE, "Memory 1997" 19941

Figure 7-1. DRAM Cell

HOW THE DEVICE WORKS

The memory cell is written to by placing a "1" or "0" charge into the capacitor cell. This is done during a write cycle by opening the cell transistor (gate to power supply or V_{CC}) and presenting either V_{CC} or 0V (ground) at the capacitor. The word line (gate of the transistor) is then held at ground to isolate the capacitor charge. This capacitor will be accessed for either a new write, a read, or a refresh.

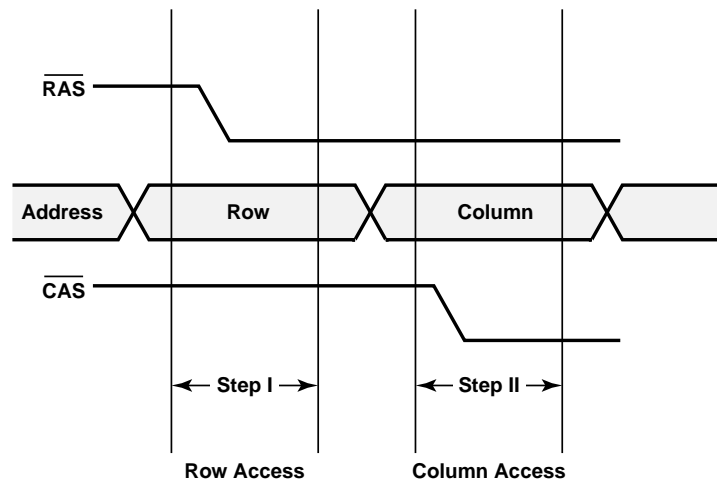
Figure 7-2 shows a simplified DRAM diagram. The gates of the memory cells are tied to the rows. The read (or write) of a DRAM is done in two main steps as illustrated in Figure 7-3. The row (X) and column (Y) addresses are presented on the same pads and multiplexed. The first step consists of validating the row addresses and the second step consists of validating the column addresses.



Source: ICE, "Memory 1997"

22430

Figure 7-2. Simplified DRAM Diagram



Source: ICE, "Memory 1997"

22431

Figure 7-3. DRAM Access Timing

First Step: Row Addresses

Row addresses are present on address pads and are internally validated by the \overline{RAS} (Row Address Access) clock. A bar on top of the signal name means this signal is active when it is at a low level. The X addresses select one row through the row decode, while all the other non-selected rows remain at 0V. Each cell of the selected row is tied to a sense amplifier. A sense amplifier is a circuit that is able to recognize if a charge has been loaded into the capacitor of the memory cell, and to translate this charge or lack of charge into a 1 or 0. There are as many sense amplifiers as there are cells on a row. Each sense amplifier is connected to a column (Y address). In this first step all the cells of the entire row are read by the sense amplifier. This step is long and critical because the row has a high time constant due to the fact that it is formed by the gates of the memory cells. Also, the sense amplifier has to read a very weak charge (approximately 30 femtoFarads or 30fF).

Second Step: Column Addresses

Following the first step, column addresses are present on the address pads and are internally validated by the Column Address Access (\overline{CAS}) clock. Each selected memory cell has its data validated in a sense amplifier. Column access is fast. This step consists of transferring data present in the sense amplifier to the D_{out} pin through the column decode and the output buffer. On memory data sheets, the access time from \overline{RAS} is termed t_{RAC} and the access time from \overline{CAS} is listed as t_{CAC} . On a typical standard DRAM of 60ns access time, $t_{RAC} = 60ns$ and $t_{CAC} = 15ns$.

Refresh

To maintain data integrity, it is necessary to refresh each DRAM memory cell. Each row of cells is refreshed every cycle. For example, if the product specification states, "Refresh cycle = 512 cycles per 8ms," then there are 512 rows and each individual row must be refreshed every eight milliseconds.

As explained above, during the row access step, all the cells from the same row are read by the sense amplifier. The sense amplifier has two roles. Since it holds information within the cell, it is able to transmit this data to the output buffer if it is selected by the column address. The sense amplifier is also able to re-transmit (write) the information into the memory cell. In this case, it "refreshes" the memory cell. When one row is selected, all the cells of that row are read by the sense amplifiers and all these cells are refreshed one at a time.

Burst or distributed refresh methods can be used. Burst refresh is done by performing a series of refresh cycles until all rows have been accessed. For the example given above, this is done every 8ms. During the refresh, other commands are not allowed. Using the distributed method and the above example, a refresh is done every 12.6 μ s (8ms divided by 512). Figure 7-4 shows these two modes.

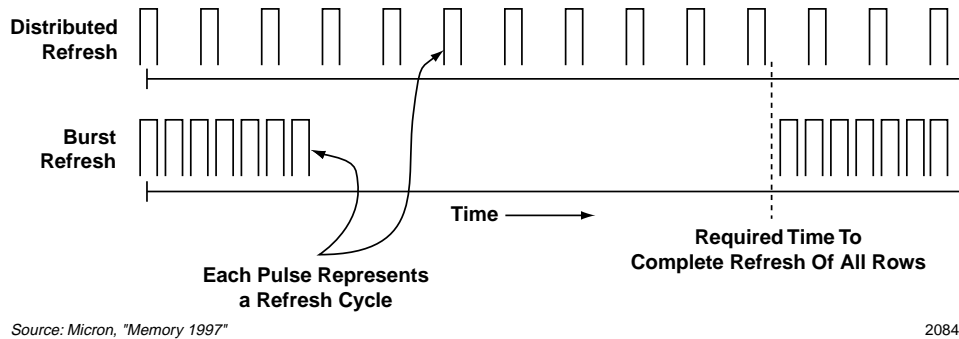


Figure 7-4. Burst and Distributed Refresh

For standard DRAMs there are three ways to perform refresh cycles. They are RAS-only refresh, CAS-before-RAS refresh, and hidden refresh. To perform a RAS-only refresh, a row address is put on the address lines and then RAS goes low. To perform a CAS-before-RAS refresh, CAS first goes low and then a refresh cycle is performed each time RAS goes low. To perform a hidden refresh the user does a read or write cycle and then brings RAS high and then low.

MEMORY CELL

A great deal of design effort has been made to shrink the cell area, particularly, the size of the DRAM capacitor. As memory density increases, the cell size must decrease. Designers have managed to shrink overall cell size. However, due to factors such as noise sensitivity and speed, it has been a challenge to reduce the capacitance. The capacitance must stay in the range of 30fF.

The charge (Q) stored in a capacitor is equal to capacitance times voltage ($Q = C \times V$). Over the years, DRAM operating voltage has decreased (i.e., 12V to 5V to 3.3V). As voltage decreases, the stored charge will also decrease. Design improvements allow for the decrease in the cell charge as long as the capacitance remains in the range of 30fF.

Two main developments are used to reduce capacitor area without reducing its value. These are the use of new capacitor shapes to fit into a minimum chip surface area and increasing the dielectric constant.

Memory Cell Shape

The 1Mbit DRAM generation was the first to abandon the classical planar capacitor and replace it with a trench or a stacked capacitor. Figure 7-5 shows the feature sizes of some of the DRAM devices that ICE analyzed in its laboratory these two last years. Trench capacitors are not widely used in spite of continual research and development on that type of design. As shown, the major 64Mbit DRAMs available on the market are today made of stacked capacitors.

Name	Density	Date Code	Cell Area μm^2	Die Area mm^2	Gate Length	Cell Type
Fujitsu	16M	9532	1.4	97.8	0.30	Stacked
Mosel-Vitellic	4M	9518	4.0	65.0	0.55	Stacked
NEC	64M	9621	1.0	161.0	0.35	Stacked
IBM/Siemens	64M	9539	1.5	197.0	0.25	Trench
Samsung	64M	9552	1.2	159.3	0.35	Crown
Mitsubishi	16M	1995	3.0	100.1	0.45	Stacked
Hitachi	64M	9351	1.6	229.4	0.35	Stacked

Source: ICE, "Memory 1997"

22432

Figure 7-5. Physical Dimensions of DRAMs

Cross sections of 64Mbit DRAMs analyzed by ICE's laboratory illustrate three major choices for manufacturing DRAM memory cells. Hitachi uses a stacked, multi-layer capacitor for its 64Mbit DRAM (Figure 7-6). The trench capacitor (Figure 7-7) is used by IBM/Siemens, and the simple stack capacitor (Figure 7-8, and 7-9) is preferred by Samsung and NEC.

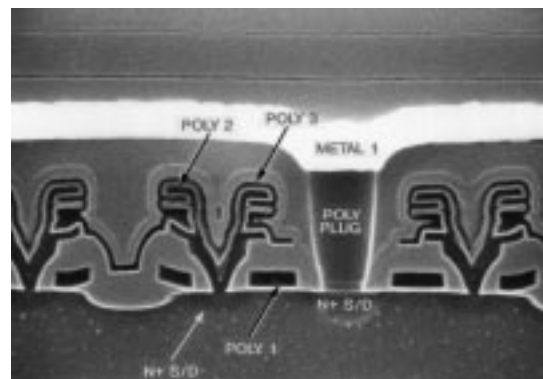


Photo by ICE, "Memory 1997"

19814

Figure 7-6. Hitachi 64Mbit DRAM Cross Section

Figure 7-10 shows how size cell improvements will be necessary for the next DRAM generations. Figure 7-11 illustrates the stacked capacitor structure evolution. The decrease of cell size without decreasing capacitor value results in increasing complexity of memory cell technology. Most leading DRAM manufacturers are working on 1Gbit cells. Their goal is to decrease the size of the cell without compromising the value of the capacitor.

Two types of 1Gbit cell developments are shown in the next figures. Toshiba tried to improve the trench capacitor concept by creating a bottle-shape trench design (Figure 7-12). Hitachi tried to improve the stack concept with a vertical and circular capacitor (Figure 7-13). NEC received a patent from the U.S. Patent Office for its proprietary HSG (hemispherical-grain) silicon technology.

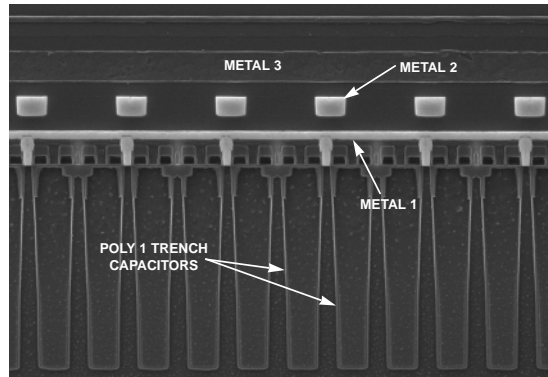


Photo by ICE, "Memory 1997"

22433

Figure 7-7. IBM/Siemens 64Mbit DRAM Cross Section

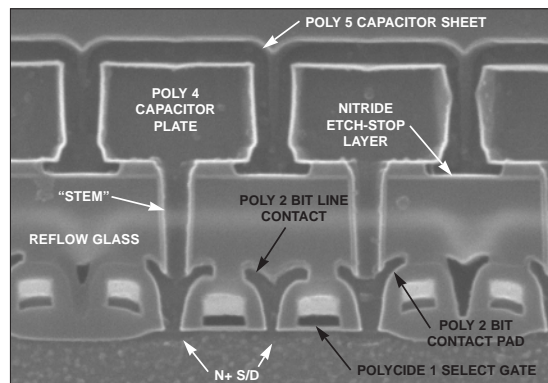


Photo by ICE, "Memory 1997"

20844

Figure 7-8. Samsung 64Mbit DRAM Cross Section

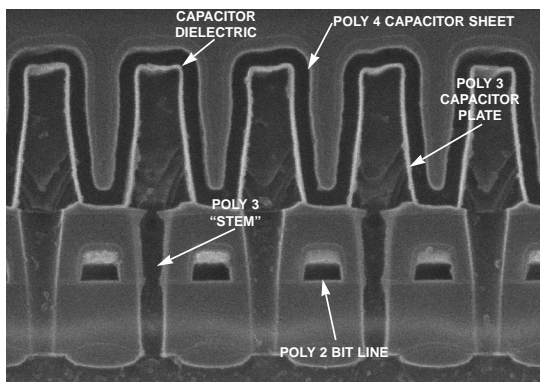
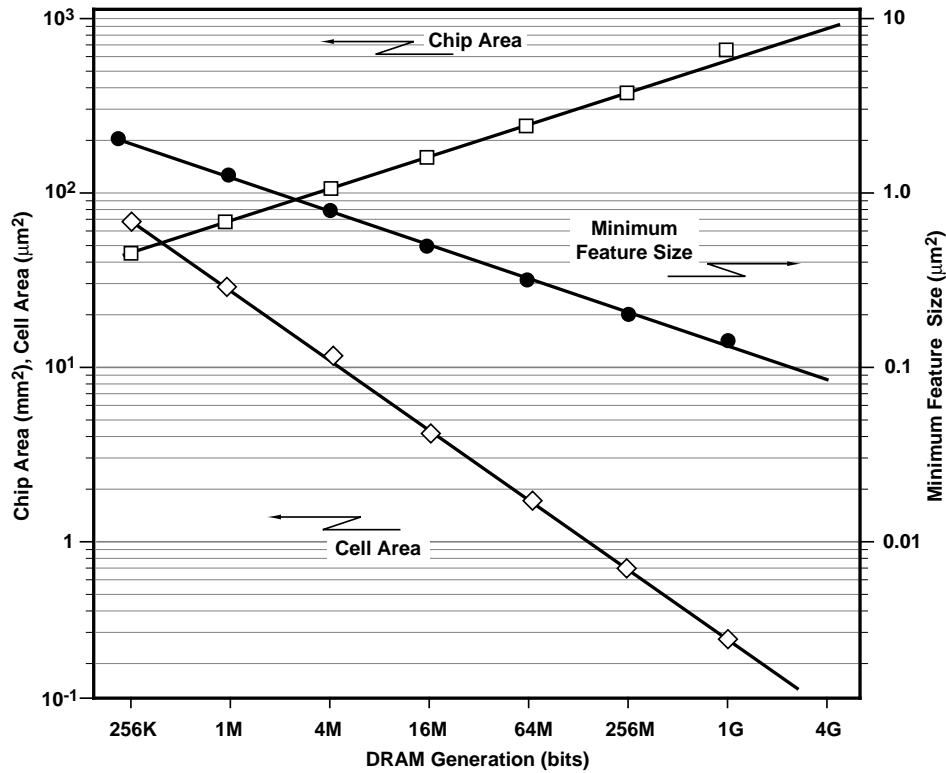


Photo by ICE, "Memory 1997"

22434

Figure 7-9. NEC 64Mbit DRAM Cross Section



Source: Hitachi/ICE, "Memory 1997"

20775A

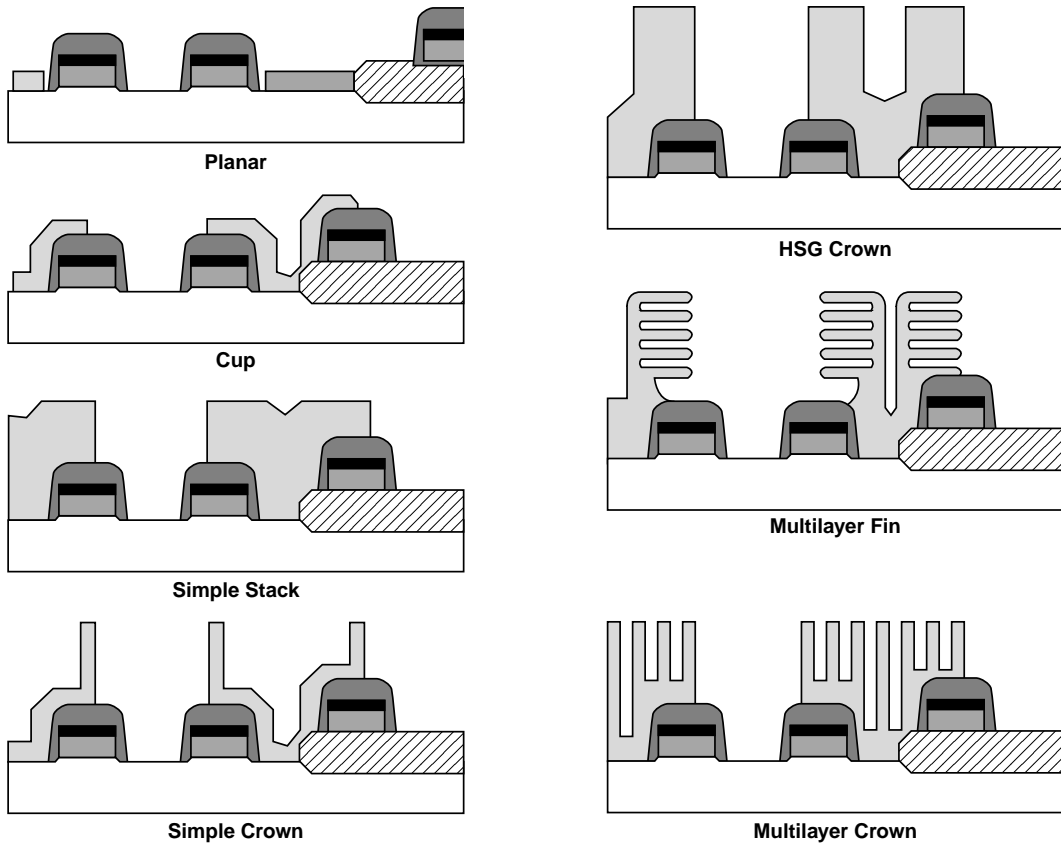
Figure 7-10. DRAM Technology Trend

CAPACITOR DIELECTRICS

The inability to scale the capacitor value has led to the consideration of new dielectric materials for the capacitor. It is likely that materials with higher dielectrics will see more use. Many of the materials have proven track records through their use as dielectrics in discrete capacitors. Therefore, the main challenge is the introduction of these materials into the IC process. Figure 7-14 shows some of the materials under consideration. Tantalum Pentoxide (Ta₂O₅) has been viewed in several of the 64Mbit DRAMs analyzed by the ICE laboratory. Ta₂O₅ seems that it could serve as a good dielectric since it can easily be integrated into conventional stack capacitor structure. However, it requires higher dielectric thickness, resulting in only a marginal improvement in capacitance.

PERFORMANCE

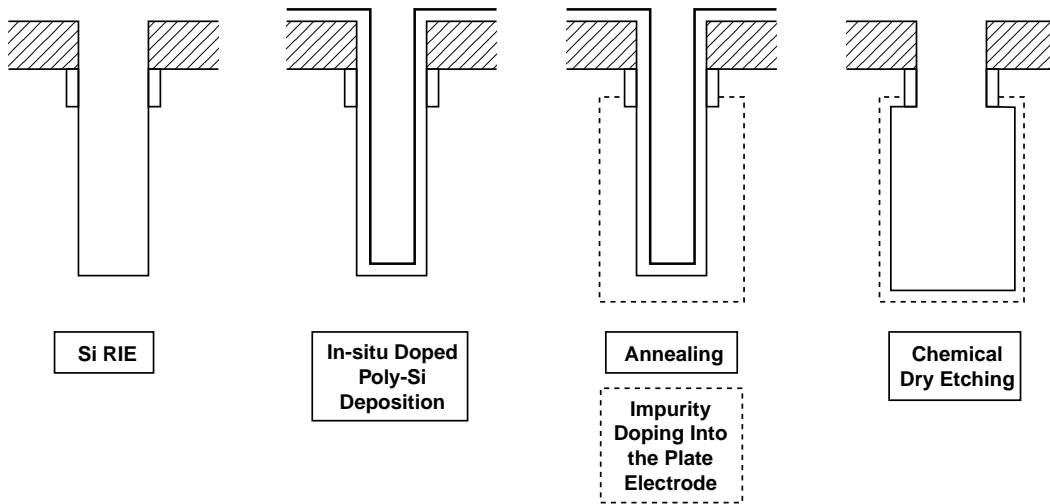
Compared with other memory ICs, DRAMs suffer from a speed problem. The on-chip circuitry required to read the data from each cell is inherently slow. As such, DRAM speeds have not kept pace with the increased clock speed of CPUs.



Source: IBM/Semiconductor International/ICE, "Memory 1997"

22435

Figure 7-11. Stack Capacitor Structure Evolution



Source: Toshiba/ICE, "Memory 1997"

20767

Figure 7-12. Capacitor Manufacturing Process

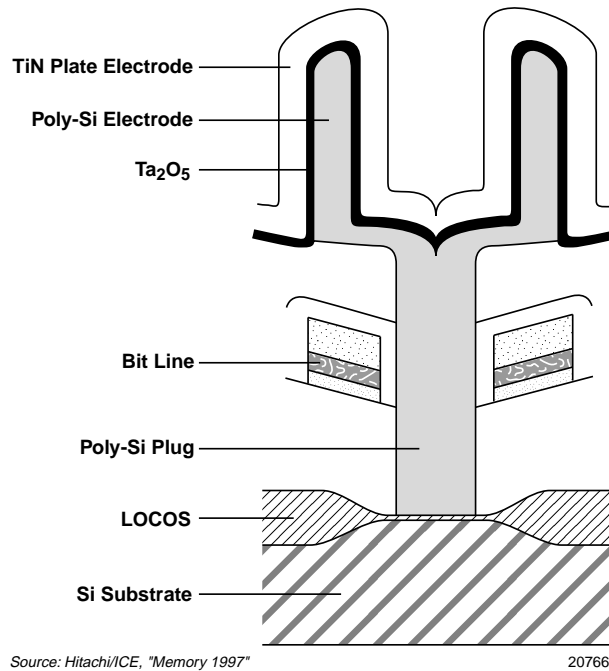


Figure 7-13. Schematic Cross-Sectional View of CROWN-Type Memory Cell

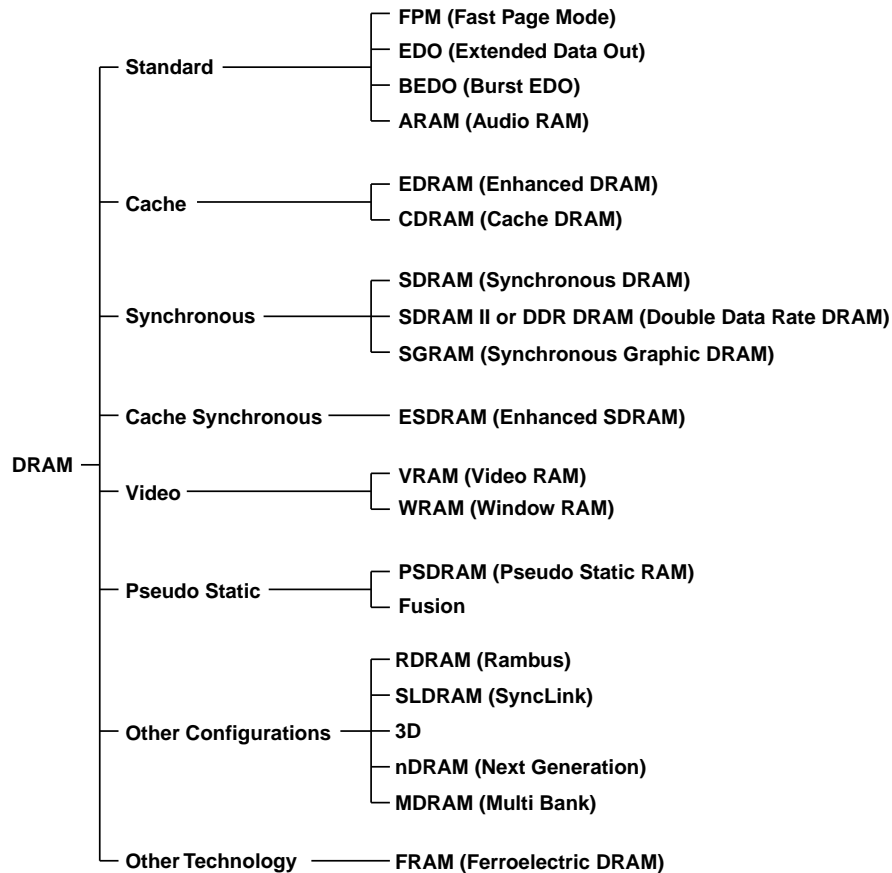
Material	ϵ_r
SiO ₂	3.8
SiN ₄	7.9
Ta ₂ O ₅	20 - 30
BaTiO ₃	15 - 30
SrTiO ₃	15 - 30
TiO ₂	35 - 50
Polyimide	2 - 2.6

Source: ICE, "Memory 1997" 18741

Figure 7-14. Capacitor Dielectric Constants

Early microprocessor systems were introduced with clock speeds of 1MHz (one million cycles per second). Today, CPUs in desktop PCs are 200MHz and faster, at least a 200x improvement. Early DRAMs had access cycle times (the time required for the DRAM chip to supply the data back to the CPU) of 250 nanoseconds (ns). The fastest DRAM units today are about 50ns, a five-fold improvement.

To face this speed discrepancy, DRAMs have branched into many sub-categories. Each features a variation of system interface circuitry with the intent of enhancing performance. Furthermore, each design attempts to answer needs of specific applications. Current offerings are shown Figure 7-15.



Source: ICE, "Memory 1997"

22450

Figure 7-15. Current DRAM Varieties

Fast Page Mode DRAMs

To access DRAM data, a row address is applied, followed by a column address. The addresses of a DRAM are multiplexed on the same package pins. When requested data is stored in the same row as previously requested data, merely changing the column address allows access to this new data. Therefore, with fast page mode, the data of the same row can be accessed by changing only the column address.

As an example, consider a 1Mbit DRAM that has an array organization of 1,024 x 1,024 bits. 1,024 bits of data belong to the same row. This data will be accessible through fast page mode (a row is considered a page). This mode is available on all the standard DRAMs. As described previously, this access time is as fast as the data available in the sense amplifier.

Static column mode is similar to page mode except that only the column address needs to be changed to obtain the new data, and no CAS pulse is needed. Nibble mode groups memory cells in “four bits per nibble” so that whenever one bit is selected, four serial bits appear. This mode is no longer widely used.

Extended Data Out (EDO) DRAMs

Extended data out DRAMs (EDO DRAMs), also called hyper-page-mode DRAMs, represent a small design change in the output buffer relative to a standard fast page mode DRAM. The old data is latched at the output while new data is addressed. EDO shortens the effective page mode cycle time as the valid data output time is extended.

For the same technology, a product in standard mode may have a cycle time of 110ns (access time of 60ns). This cycle time will be reduced to 40ns in fast page mode and to 25ns in EDO mode.

Burst EDO DRAMs

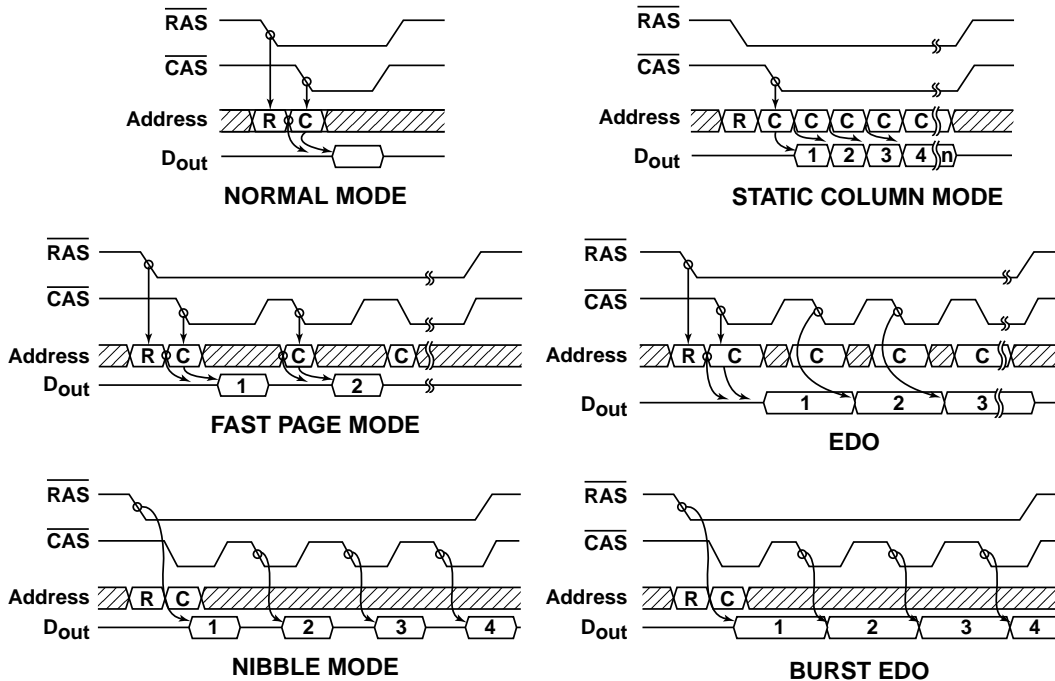
Several vendors offer burst versions of the EDO DRAM. The “burst” refers to the fact that all read and write cycles occur in bursts of four, automatically sequenced by the memory chip. To accomplish that, a special pipeline stage and a two-bit counter are added.

The Burst EDO DRAM read access time differs from EDO DRAM in two ways. First, as the output latch is replaced by a special pipeline stage (register), the latency will be higher but the bandwidth will be better. Second, as the Burst EDO DRAM includes an internal address counter, only the initial address in a burst of four needs to be provided.

Manufacturers may use the same mask set for their fast page mode EDO and burst EDO DRAMs. A wire bond option determines which product is in the final package. Figure 7-16 shows timing differences between the various standard DRAMs. Figure 7-17 shows speed differences.

Audio DRAMs

Due to process defects during wafer probe, some DRAMs wind up with a few failed storage cells that cannot be effectively repaired (or replaced) by the redundancy mechanism. These cannot be sold as good devices to PC OEMs. However, a few defective bits do not affect an audio application where there is a tolerance for error. For this reason manufacturers may sell parts with few bad cells for use in audio applications. These devices are called Audio DRAM (ARAM). The client can buy ARAMs cheaper than a standard DRAM.



R: Row Address
C: Column Address

Source: ICE, "Memory 1997"

22436

Figure 7-16. Comparison of Dynamic RAM High Speed Access Modes

DRAM Speed (t _{RAC})	DRAM Type		
	Fast Page Mode	EDO	Burst EDO
70ns	25MHz	33MHz	50MHz
60ns	28MHz	40MHz	60MHz
50ns	33MHz	50MHz	66MHz

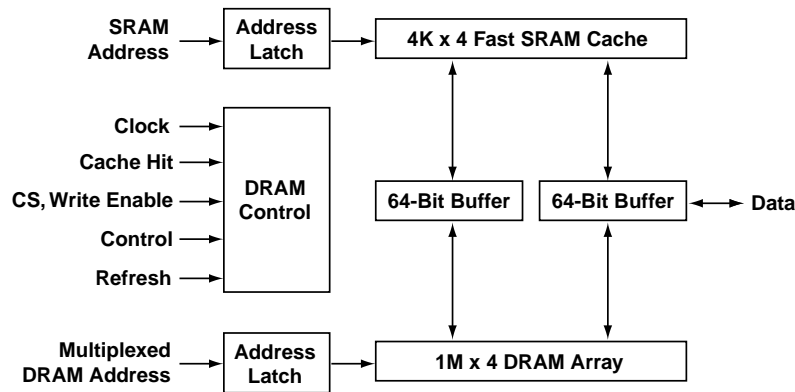
Source: Micron/ICE, "Memory 1997"

19992A

Figure 7-17. Comparison of Standard DRAM Performances

Cache DRAMs

Another DRAM alternative is the cache DRAM (CDRAM) developed by Mitsubishi. This device integrates a 16Mbit DRAM and a L2 (level two) SRAM cache memory (16Kbit SRAM) on the same chip. The transfer between the DRAM and the SRAM is performed in one clock cycle through a buffer of 8 x 16 bits. The SRAM is a six-transistor cell. The SRAM access/cycle time is 15ns. Currently, Mitsubishi and Samsung offer CDRAM devices. Figure 7-18 shows the chip organization of a CDRAM.



Source: EBN/ICE, "Memory 1997"

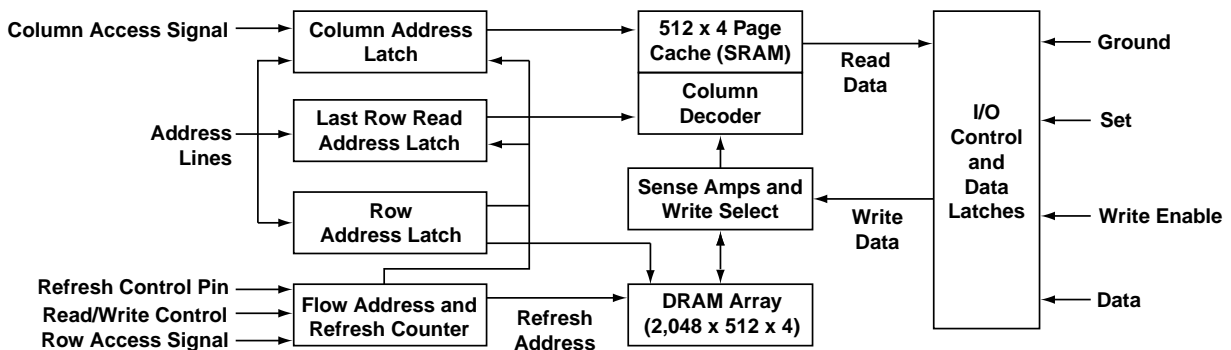
20756

Figure 7-18. Cache DRAM

Enhanced DRAMs

Enhanced DRAMs (EDRAMs) were developed by Ramtron Corporation. The EDRAM is also sold by IBM (3.3V and 5V parts), as IBM and Ramtron have a second source agreement for this product. The EDRAM architecture is similar to a standard 4Mbit page mode or static column DRAM with the addition of an integrated L2 SRAM cache and internal control. Technically, the EDRAM is a cache DRAM (CDRAM). Rather than integrate a separate SRAM cache, the EDRAM takes advantage of the internal architecture of a standard fast page mode DRAM, which has sense amplifiers that act like a 2Kbit SRAM cache when reading and accessing data.

Memory read cycles always occur from the cache. When the comparator detects a hit, only the SRAM is addressed where data is available in 15ns. When a miss is detected, the entire cache is updated and data is available at the output within a single 35ns access. Figure 7-19 shows the chip organization of an EDRAM.



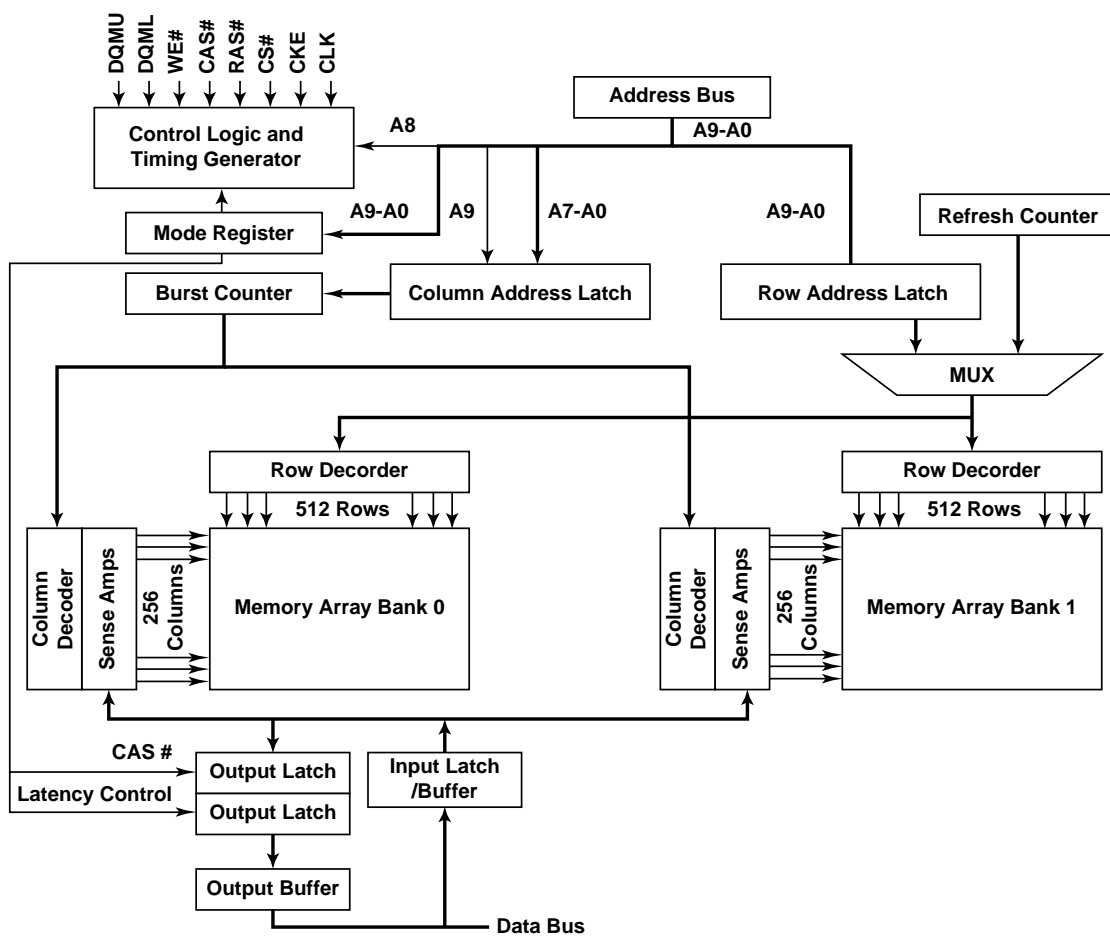
Source: EBN/ICE, "Memory 1997"

20757

Figure 7-19. Enhanced DRAM (EDRAM)

Synchronous DRAMs

Synchronous DRAMs represent the next step in the evolution of the industry standard DRAM architecture. Synchronous DRAMs (SDRAMs) have their read and write cycles synchronized with the processor clock. The SDRAM is designed with two separate banks. These two independent banks allow each bank to have different rows active at the same time. This allows concurrent access/refresh and recharge operations. Figure 7-20 presents a block diagram organization of an SDRAM.

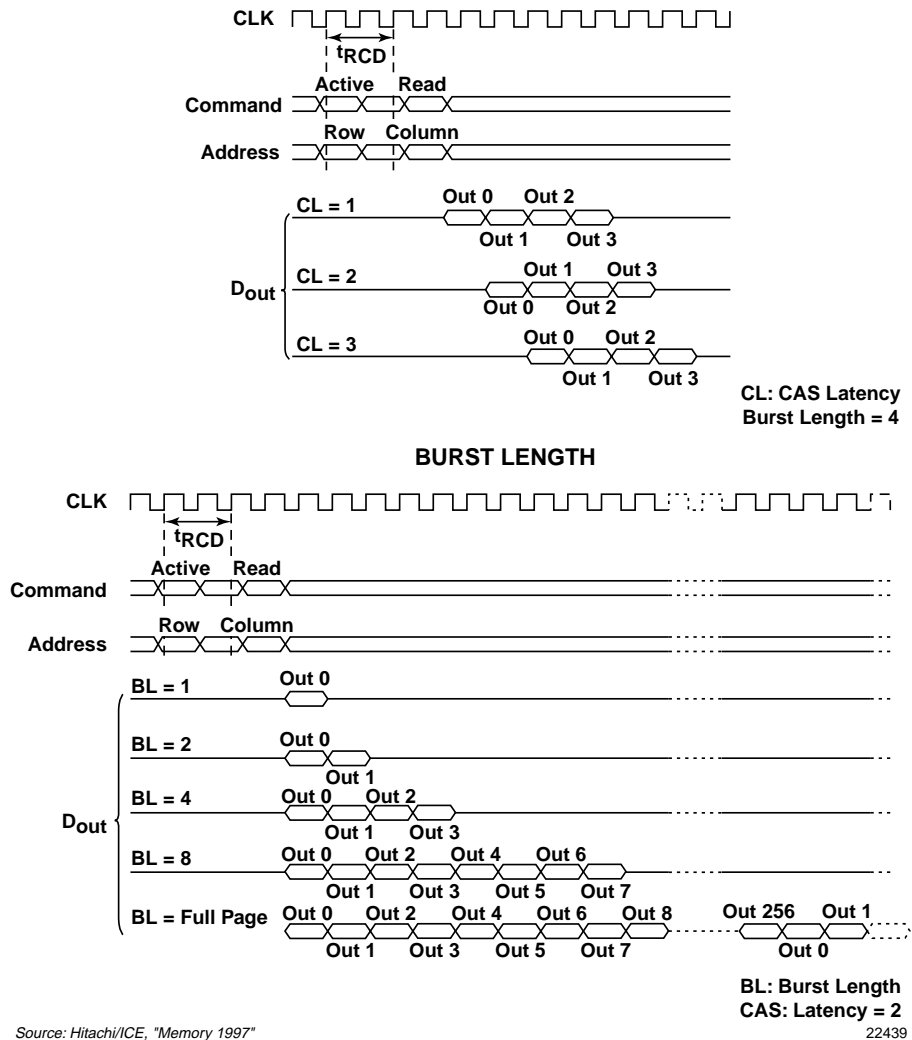


Source: Hitachi/ICE, "Memory 1997"

22437

Figure 7-20. 4Mbit SDRAM Block Diagram

The SDRAM is programmed using a mode register. The programmable features include burst length (1, 2, 4, 8, full page), wrap sequence (sequential/interleave), and CAS latency (1, 2, 3). Figure 7-21 shows an SDRAM timing sequence. This timing illustrates the different possibilities of CAS latency and of burst length.



Source: Hitachi/ICE, "Memory 1997"

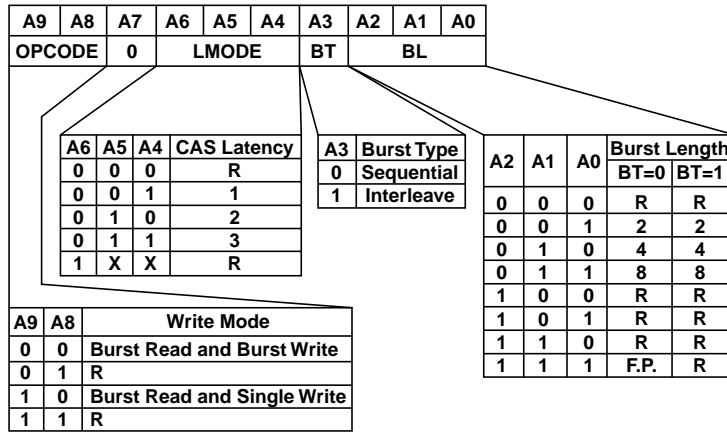
22439

Figure 7-21. SDRAM Timing

The size of the mode register is equivalent to the number of address pins on the device and is written during a mode register set cycle. This mode register must be reprogrammed each time any of the programmable features have to be modified. Figure 7-22 illustrates the content of a register for a 4Mbit SDRAM. Figure 7-23 shows a summary of the SDRAM functionality.

SDRAM-II or DDR DRAMs (Double Data Rate DRAMs)

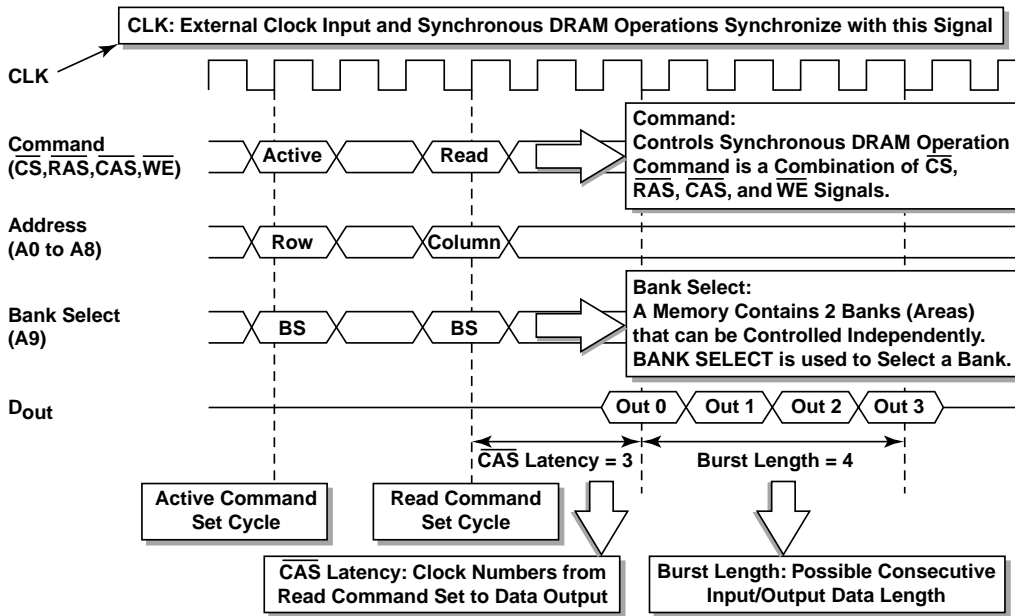
The purpose of the DDR DRAM is to read data of an SDRAM at two times the frequency clock. The device delivers data on both edges of the clock, doubling effective bandwidth at a given frequency.



F.P. = Full Page
 R = Reserved (inhibit)
 Source: Hitachi/ICE, "Memory 1997"

22438

Figure 7-22. Register Content of a 4Mbit SDRAM



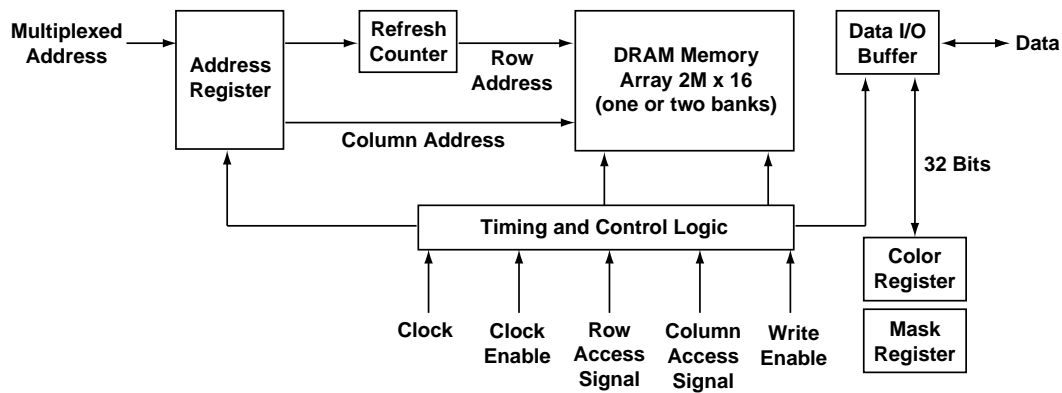
Source: Hitachi/ICE, "Memory 1997"

22440

Figure 7-23. SDRAM Functionality

Synchronous Graphics RAMs

Synchronous Graphics RAMs (SGRAMs) target video applications. SGRAMs differ from Synchronous DRAMs (SDRAMs) in that they provide features traditionally associated with video DRAMs such as 32-bit-wide bus and graphics-specific features such as block write mode and a masked write mode. Figure 7-24 shows the chip organization of an SGRAM.



Source: EBN/ICE, "Memory 1997"

20763

Figure 7-24. Synchronous Graphic DRAM

Enhanced Synchronous DRAMs

Enhanced Memory Systems Inc., a subsidiary of Ramtron, developed its Enhanced Synchronous DRAMs (ESDRAM). This memory combines the features of SDRAM plus cache SRAM on the same chip. 16Mbit ESDRAM combines two banks of 8Mbit SDRAM plus two banks of 4Kbit SRAM.

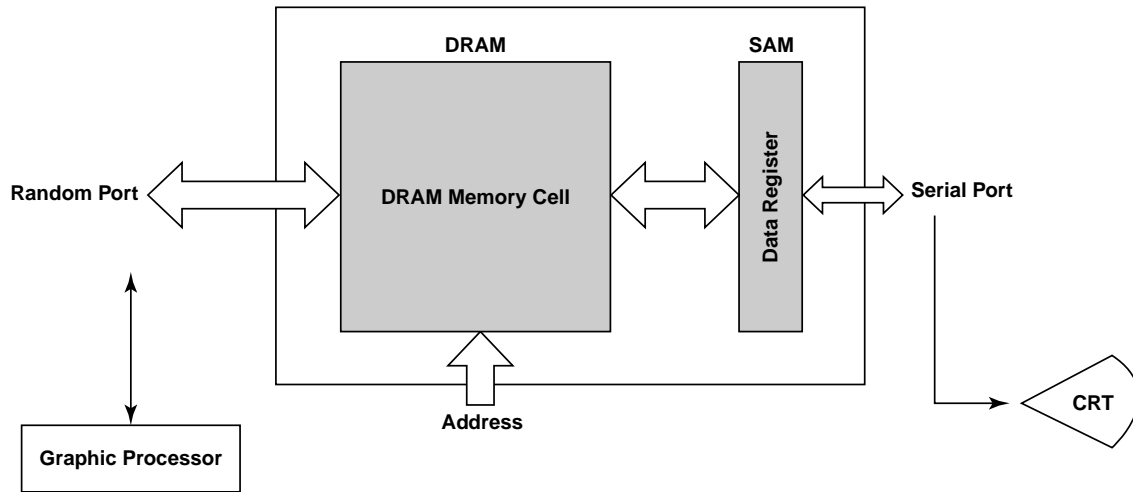
Video DRAMs

Video DRAMs (VRAMs) are also called Dual-Port DRAMs. VRAMs are almost exclusively used for video applications. Since the standard DRAM is inherently parallel and video data is inherently serial, graphics systems have always needed parallel to serial shift registers. A VRAM has separate parallel and serial interfaces. For example, a 4Mbit DRAM may be organized as:

DRAM: 262,144 Words X 16 bits

SAM (Serial Access Memory): 256 Words X 16 bits

The transfer of parallel data to serial data is accomplished by an on-chip parallel-to-serial shift register. The register may be divided into two halves. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads during CRT retrace periods), the full register mode of operation is retained to simplify system design. Figure 7-25 illustrates a general concept of Video DRAM.



Source: Hitachi/ICE, "Memory 1997"

22441

Figure 7-25. A General Concept of Video Ram

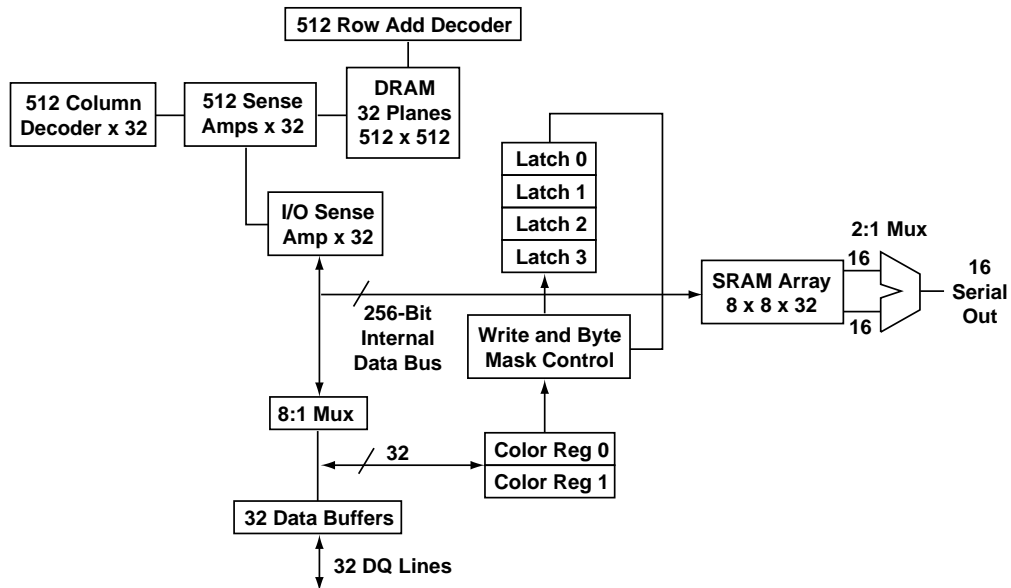
Window DRAMs

A window DRAM (WRAM) is a dual-ported VRAM with a number of added features. WRAMs incorporate EDO and fast page mode traits, have a 32-bit random access port and a 256-bit internal bus. Figure 7-26 shows the chip organization of a WRAM.

Pseudo SRAMs

Pseudo Static Random Access Memories (PSRAMs) were developed to minimize power consumption (relative to a DRAM) at the expense of speed. They incorporate the storage mechanism of a DRAM, but have additional on-chip circuitry that makes the chip perform like an SRAM. All storage cell refresh is performed internally. The chip size of a PSRAM is about 20 percent larger than a standard DRAM. The increase in size is due to additional pads from the different pin configuration, and extra internal circuitry for refresh.

The main markets for PSRAMs are portable PCs, laptops, and handheld machines. The PSRAM is packaged like an SRAM, typically in a x8 or wider data path in and out, and without multiplexed address inputs. SRAMs and PSRAMs are pin compatible. However, the PSRAM has an additional signal to tell the system when the chip is busy performing its internal refresh.



Source: EBN/ICE, "Memory 1997"

20755

Figure 7-26. Window DRAM

Although they have been available for more than 15 years, the PSRAMs market has never grown strongly. Moreover, it seems that the PSRAM market may be shriveling as Hitachi and Toshiba, the two major suppliers withdraw support. Figure 7-27 provides a comparison of PSRAMs and low-power SRAMs.

	4M SRAM	4M PSRAM
Access Time	55ns	80ns
Operating Current	90mA	75mA
Data Retention Power	15µa @ 2V	15µa @ 3V
Relative per Bit Cost (DRAM = 1)	4x	1.2x

Source: ICE, "Memory 1997"

18742

Figure 7-27. Static and Pseudo Static RAM Comparison

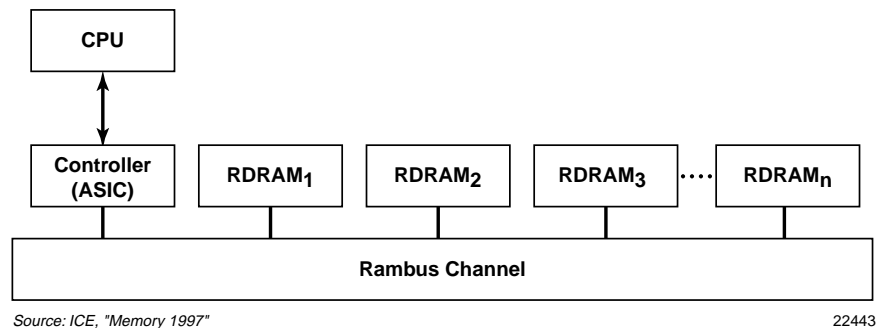
Fusion Memories

Integrated Device Technology (IDT) developed a pseudo static DRAM and SRAM and labeled it fusion memory. IDT claims that fusion memory is the first architecture to fuse together SRAM performance at DRAM density and cost.

Rambus DRAMs

Rambus technology is based on very high speed, chip-to-chip interface that is incorporated on a new DRAM architecture and on processors or controllers. The Rambus architecture achieves a performance level more than ten times greater than conventional DRAMs. Rambus Inc. does not manufacture products but licenses its design of Rambus DRAMs (RDRAMs) and controllers. To date, Rambus has licensed over one dozen of the world's largest semiconductor companies to jointly develop and bring to market a wide range of memory and logic products. Further, it won the support of Intel for the next-generation of DRAM architecture in PC systems.

Unlike other approaches that have focused on increasing the speed of individual DRAMs, Rambus provides a complete system-level solution by integrating fast components with an innovative high-speed interface technology. Figure 7-28 shows the Rambus technology elements. This architecture is comprised of three main elements that include the Rambus Channel, the Rambus Interface (controller), and the RDRAMs.



Source: ICE, "Memory 1997"

22443

Figure 7-28. Typical Rambus Configuration

The Rambus Channel

Figures 7-29 through 7-31 show the configuration and the main characteristics of the Rambus Channel. The Rambus Channel is the core of Rambus' architecture. The goal of this channel is to transmit information at a very high rate. For that to occur, the conventional TTL level signals are replaced by small swing (600mV) signals plus an additional reference signal (V_{ref}) set to be the mid-point of the swing. These low-speed signals reduce bus power consumption, noise, and increase the speed transfer.

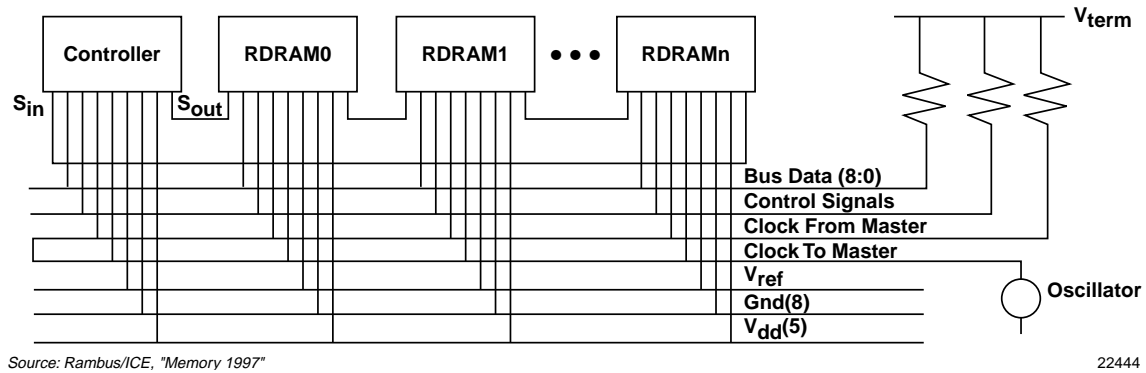


Figure 7-29. Rambus Channel

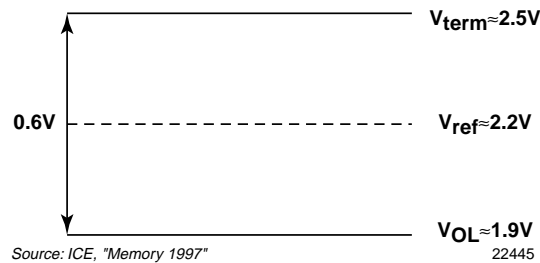


Figure 7-30. Rambus Channel Swing Signal

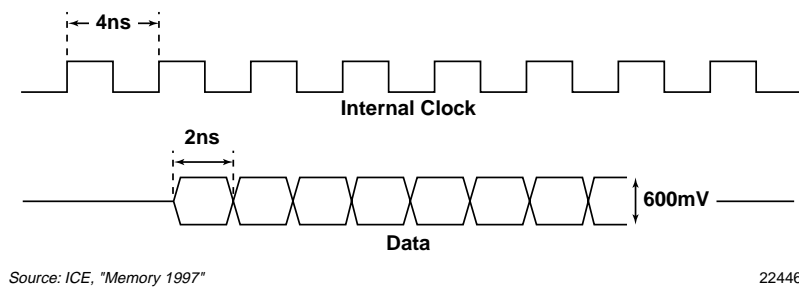
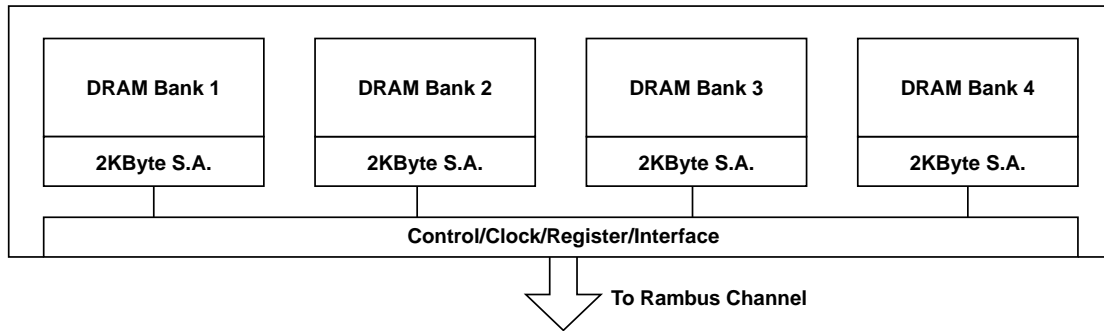


Figure 7-31. Rambus Channel Speed

The RDRAM

RDRAMs use conventional DRAM processes and manufacturing technology. Due to the Rambus interface, an RDRAM consumes 14 percent more silicon than a conventional DRAM. Figure 7-32 shows a 64Mbit Rambus DRAM chip organization. The RDRAM is divided in two parts: the interface logic and the DRAM core. The interface logic includes the high speed I/O interface, clock circuitry, and protocol control logic. The sense amplifiers act as cache memory. Like standard DRAMs, the RDRAM cells have to be refreshed. RDRAMs have a self-refresh capability built in.



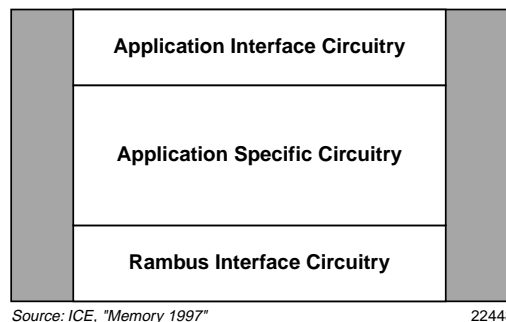
Source: ICE, "Memory 1997"

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Figure 7-32. 64Mbit RDRAM Architecture

The Rambus Controller

The block diagram of a Rambus controller is shown Figure 7-33. This controller serves as the interface between the Rambus Channel and the application. The Rambus Interface circuitry consists of serial-to-parallel and parallel-to-serial conversion plus clock recovery. This interface can be either made of an ASIC I/O cell or as a full custom cell obtained from Rambus Inc.



Source: ICE, "Memory 1997"

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Figure 7-33. Rambus Controller

Rambus also developed its own package design. This development includes a standard socket, a short fixed bus length, and specific memory modules. Figure 7-34 shows the physical layout of a Rambus-based system.

SyncLink DRAM (SLDRAM)

A DRAM architecture competing against Rambus is SyncLink. A group from the IEEE Computer Society worked on the general specifications. The concept uses a very high-speed unidirectional point-to-point interface rather than the more conventional bus. Multiple chips are located in series along the RamLink and tied to a common controller for output to the CPU. The SyncLink consortium expects to deliver prototypes in early 1998. Figure 7-35 shows the SLDRAM architecture.

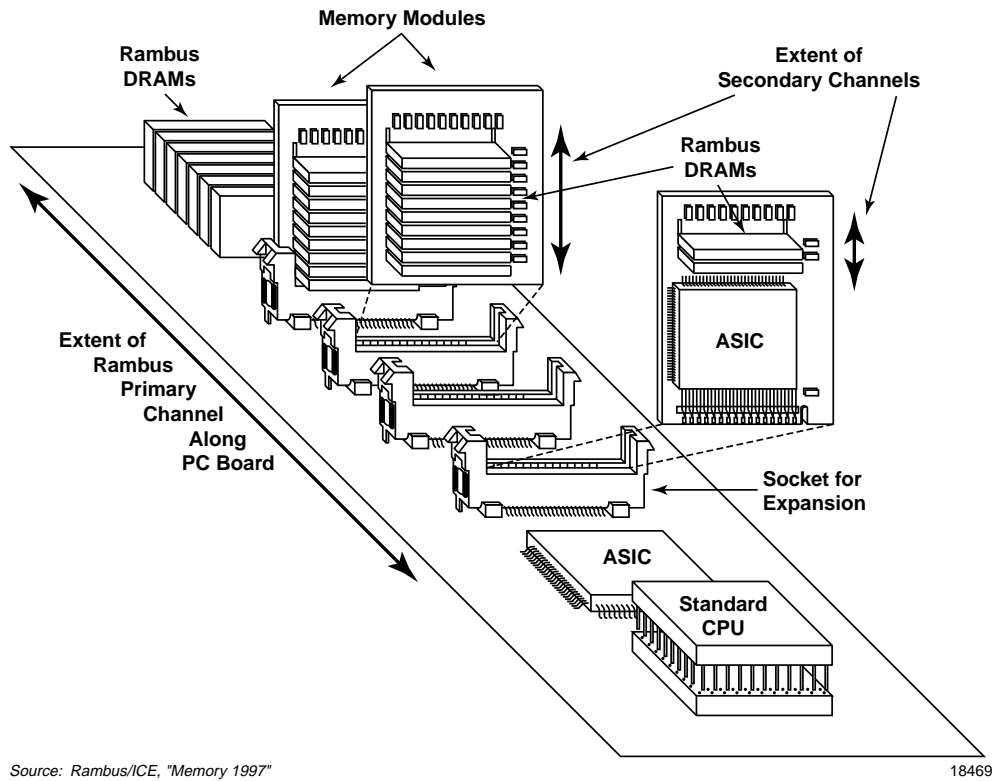


Figure 7-34. Physical Organization of a Rambus-Based System

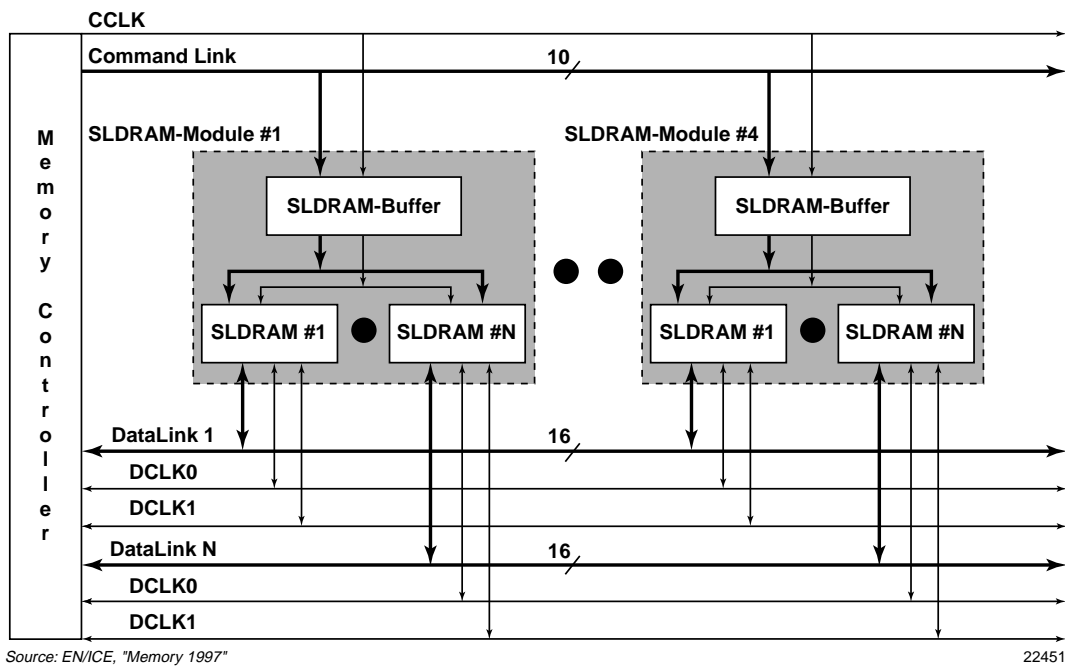
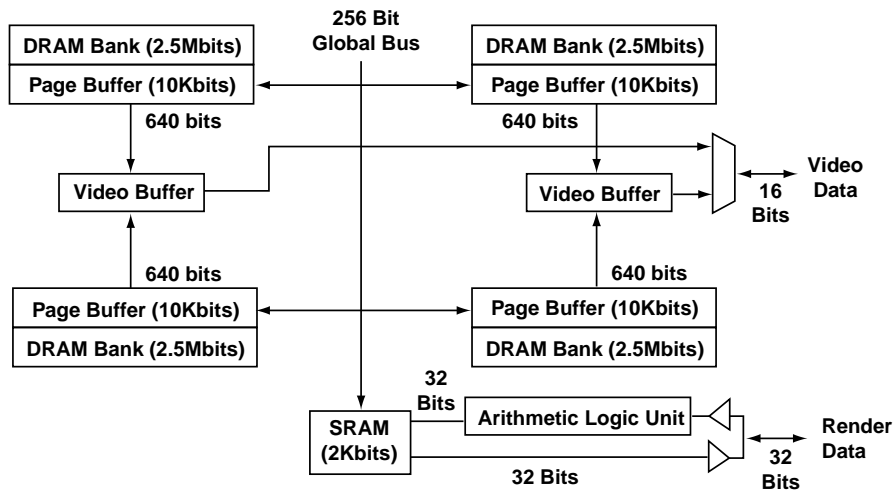


Figure 7-35. SyncLink DRAM Architecture

3D RAMs

3D RAMs, developed by Mitsubishi, are based on the cache DRAM (CDRAM) architecture. A block diagram of the architecture is shown in Figure 7-36. There are four major functional blocks in a 3D RAM. These include four independent DRAM banks of 2.5Mbits each, two video buffers, a 256-bit-wide global bus and a tri-ported SRAM buffer of 2Kbits. IBM and Toshiba announced that they will start joint production of the chips in the U.S. in the second half of 1997.



Source: EBN/ICE, "Memory 1997"

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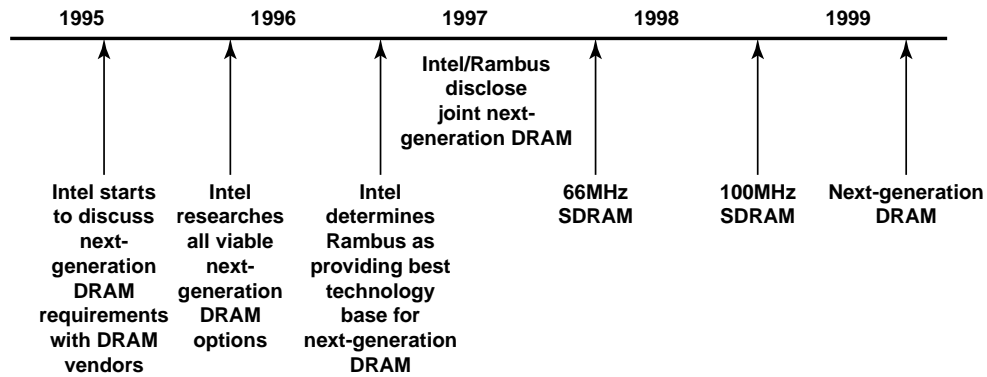
Figure 7-36. 3D DRAM

nDRAM (next-generation DRAM)

Intel and Rambus have agreed to collaborate on a new DRAM based on the RDRAM architecture. This new DRAM, called next generation DRAM (nDRAM), will not be available before 1999. Figure 7-37 shows the Intel/Rambus relationship roadmap. Currently, the RDRAM gets its speed by using a narrow 8-bit channel. The nDRAM may use two parallel 8-bit channels and reach a speed of 1.6Gbytes per seconds.

Multibank DRAM

MoSys, a 1991 fabless startup based in San Jose, California, developed the multibank DRAM (MDRAM). MoSys argues that the penalty for using DRAMs in graphics applications is not the bandwidth but the latency between two bursts. Developing a DRAM with 32 banks reduces this latency (Figure 7-38).



Source: Intel Corp./ICE, "Memory 1997"

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Figure 7-37. Intel/Rambus DRAM Cooperation

Memory Type	Page-Hit Latency (ns)	Page-Miss Latency ¹ (ns)	Row-Access Latency (ns)	I/O Data Rate (MHz)	Peak Bandwidth ² (Mbytes/s)	Interleaved Bank Bandwidth ² (Mbytes/s)	Sustained Bandwidth ² (Mbytes/s)
Fast-Page Mode	30	110	60	25	200	N/A	139
CDRAM ³	10	70	70	100	800	N/A	320
EDRAM ³	10	75	25	100	800	N/A	582
EDO	30	90	60	40	320	N/A	194
Fast EDO	20	60	35	66	533	N/A	305
Burst EDO	25	90	53	66	533	N/A	237
SDRAM ³	30	70	60	100	800	800	320
SGRAM	30	90	60	100	800	800	267
RDRAM ⁴	39	99	73	600	1,200	1,077	285
MDRAM	24	90	64	200	1,600	1,600	305
Multibank EDO EDRAM	12	30	25	100	800	N/A	582
Multibank Burst-EDO EDRAM	12	30	30	100	800	N/A	533
ESDRAM ⁵	12	12	30	133	1,064	1,064	853

¹ Page-miss latency is time to access next random data after data burst.

² Bandwidth assumes 64-bit memory bus, except for RDRAM.

³ Page-miss latency reduced by hidden precharge.

⁴ Bandwidth for two parallel Rambus channels.

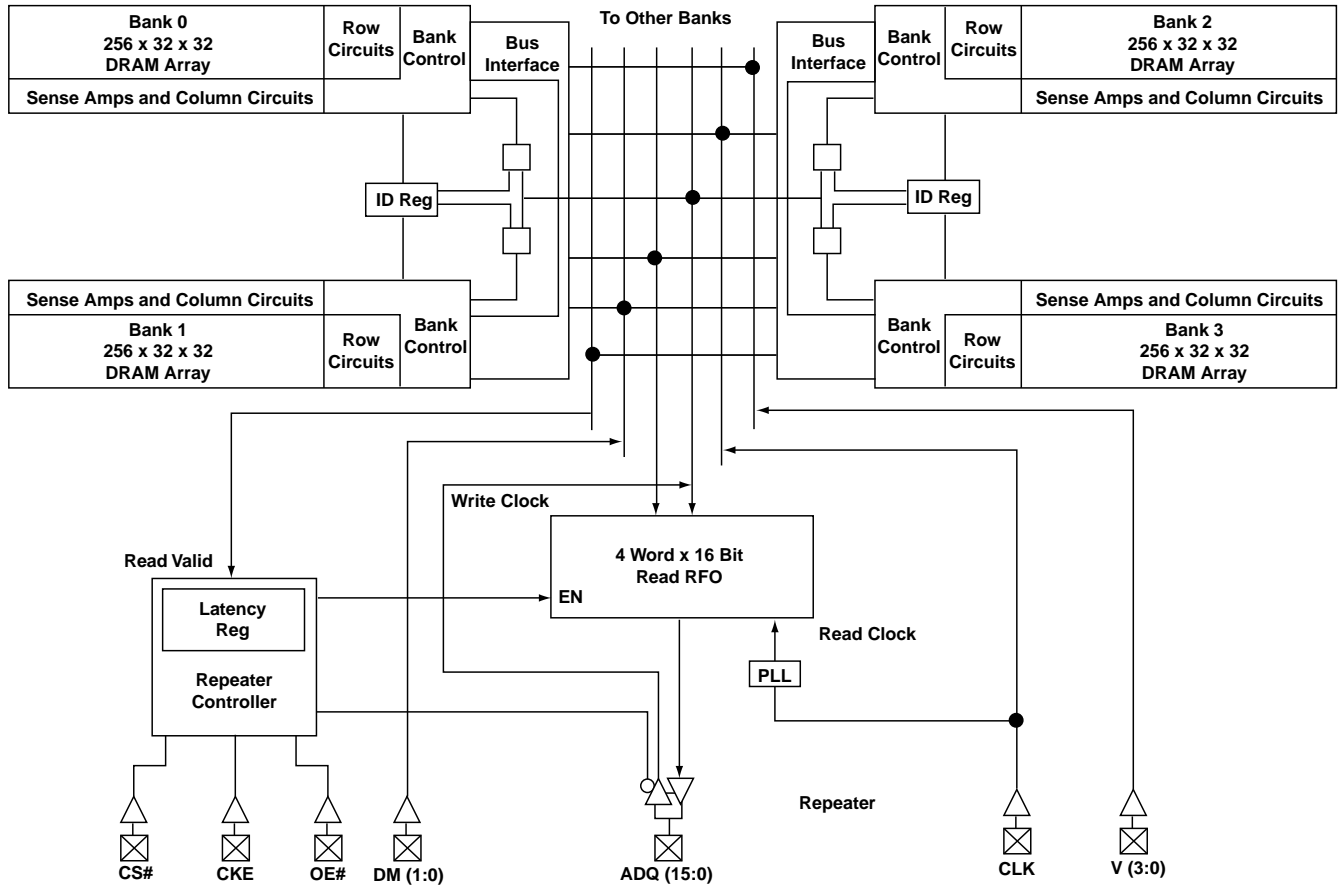
⁵ Page-miss latency reduced by hidden precharge and random access.

Source: Electronic Products/ICE, "Memory 1997"

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Figure 7-38. Performance of New Memories

All of the advanced next-generation DRAMs now coming to market are multibank DRAMs. What makes the multibank DRAM from MoSys different from previous DRAM technologies is that it is the first to give full access to any or all of the banks—each bank being a fully independent unit of memory. This gives the MDRAM a degree of memory granularity unmatched by most other DRAM alternatives. Figure 7-39 shows the MDRAM chip organization.



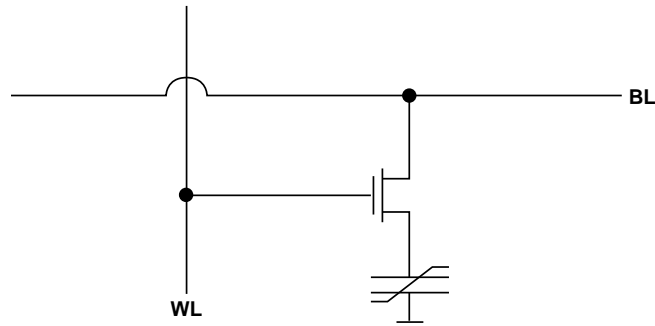
Source: EBN/ICE, "Memory 1997"

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Figure 7-39. Multibank DRAM

Non-Volatile Ferroelectric DRAM

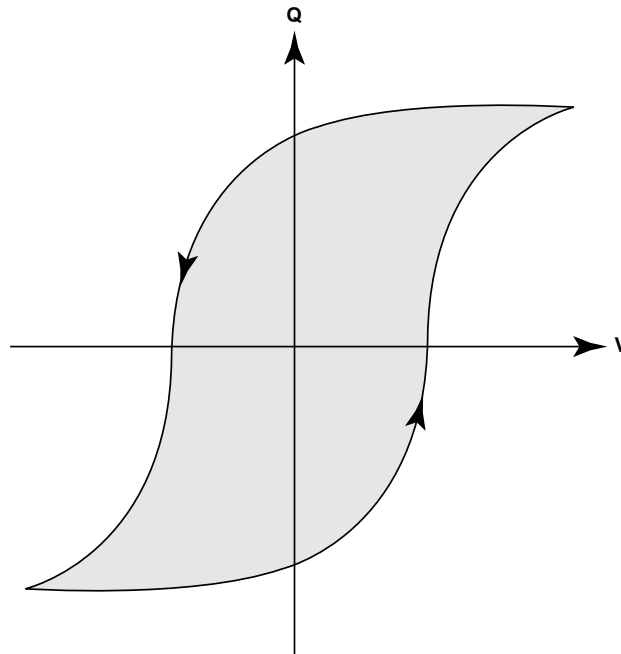
The non-volatile ferroelectric DRAM (FRAM) cell is comprised of one capacitor and one transistor. The film of the capacitor uses a ferroelectric material, typically a ceramic film of PZT (lead zirconium titanate), to provide non-volatile data storage. The memory cell functions like a DRAM when power is applied, except no refresh is needed. When power is removed, data is retained. Figure 7-40 shows the electrical schematic of a ferroelectric cell and Figure 7-41 shows the hysteresis curve of a ferroelectric capacitor.



Source: ICE, "Memory 1997"

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Figure 7-40. Ferroelectric Cell



Source: ICE, "Memory 1997"

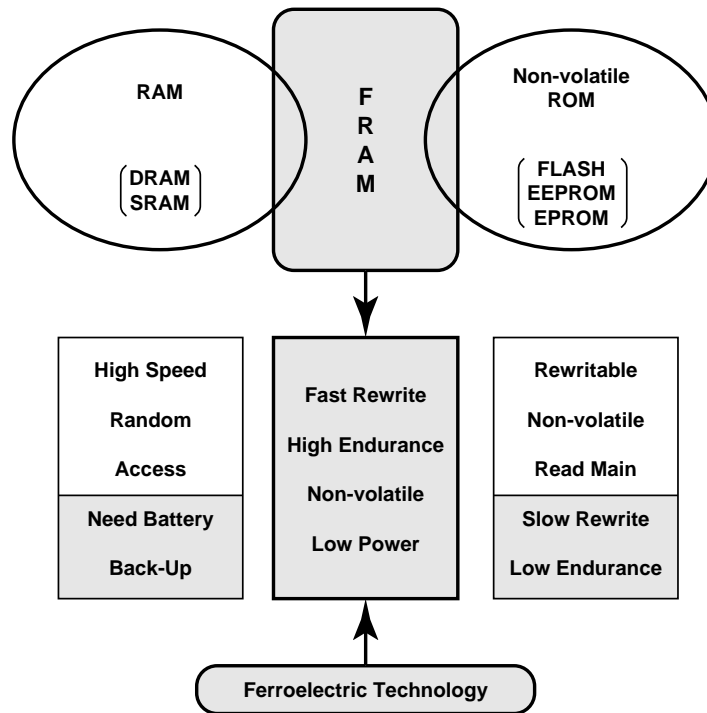
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Figure 7-41. Hysteresis Curve of FRAM Cell Capacitor

FRAMs can operate and program from a single power supply. In addition, ferroelectric materials typically exhibit dielectric constants much larger than that of SiO_2 .

Ramtron Corporation first presented the FRAM concept at the 1988 ISSCC. In early 1995, Ramtron announced the immediate availability of eight new FRAMs. These products are all offered in the x8-bit configuration, in 4Kbit, 8Kbit, or 16Kbit densities. Several manufacturers joined Ramtron as partners for developing next-generation FRAMs. The list includes Rohm, Hitachi, Toshiba, Fujitsu and more recently (January 1997), Samsung and SGS-Thomson.

This product is still in the introduction phase of its life cycle. Figure 7-42 shows the advantages of the FRAM over the other types of memories.



Source: Hitachi/ICE, "Memory 1997"

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Figure 7-42. FRAM Application

Cycle Time	100ns
Power Supply	3.3V
t _{AA}	60ns
Active Current	50mA
Stand-By Current	10μA
Cell Size	6.2 x 5.6μm ²
Chip Size	15.7 x 5.75mm ²
Capacitor Dielectric	SrBi ₂ Ta ₂ O ₉
Dielectric Remanent Polarization (Pr)	5μC/cm ²
Minimum Metal Width	1μm

Source: NEC/ICE, "Memory 1997"

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Figure 7-43. NEC's 1Mbit FDRAM

In the 1996 ISSCC conference, NEC presented a 3.3V 1Mbit FRAM. The device used an oxide of Strontium-Bismuth-Tantalum (SBT) as capacitor dielectric and had a cell size of 34.72μm². Figure 7-43 summarizes the main characteristics of this device.

FRAM technology is still in the development stages, but is finally emerging after years of R&D and limited production. Most companies are working at the 1Mbit density and plan to move toward development of 16Mbit devices.

The highest FRAM density currently available in the market is a 256Kbit proposed by Hitachi. The dielectric of this FRAM is made of lead zirconium titanate. Hitachi said it expects to produce 1Mbit and 4Mbit FRAM devices between 1998 and 1999.

At the 1996 IEDM conference, Toshiba presented a paper on a Ferroelectric Epitaxial (Ba,Sr) TiO₃ (BST) capacitor for deep sub-micron FRAM.

Figure 7-44 samples several DRAM vendors and provides a quick reference of the architectures each supports.

Vendor	DRAM Architectures Offered	Rambus Licensee	SyncLink Consortium Member
Fujitsu	SGRAM, SDRAM	—	•
Hitachi	SGRAM, SDRAM, EDO DRAM	•	•
Hyundai	EDO DRAM	•	•
IBM	SRAM, SDRAM, EDO DRAM	—	•
LG Semicon	—	•	•
Micron	SGRAM, EDO DRAM	—	•
Mitsubishi	3-D RAM, cache DRAM, SDRAM, EDO DRAM	—	•
Mosel-Vitelic	EDO DRAM	—	•
NEC	SGRAM, SDRAM, Rambus DRAM, EDO DRAM	•	•
Oki	EDO DRAM, VRAM	•	•
Ramtron	Enhanced DRAM	—	—
Silicon Magic	EDO DRAM	—	—
Samsung	SGRAM, SDRAM, Windows RAM, EDO DRAM	•	•
Texas Instruments	SDRAM, VRAM, EDO DRAM	—	•
Toshiba	EDO DRAM, SDRAM, Rambus DRAM, VRAM	•	•

Source: Computer Design/ICE, "Memory 1997"

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Figure 7-44. DRAM Vendors Support Many Architectures