FAIRCHILD SEMICONDUCTOR™

November 1992
Revised March 1999

74VHC245
Octal Bidirectional Transceiver with 3-STATE Outputs

General Description

The VHC245 is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC245 is intended for bidirectional asynchronous communication between data busses. The direction of data transmission is determined by the level of the T/$\overline{R}$ input. The enable input can be used to disable the device so that the busses are effectively isolated. All inputs are equipped with protection circuits against static discharge.

Features

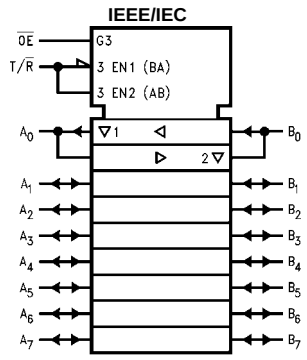
- High Speed: t_{PD} = 4.0 ns (typ) at V_{CC} = 5V
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power Down Protection is provided on all inputs
- Low Noise: V_{OLP} = 0.9V (typ)
- Low Power Dissipation:
  I_{CC} = 4 μA (Max) @ T_A = 25°C
- Pin and Function Compatible with 74HC245

Ordering Code:

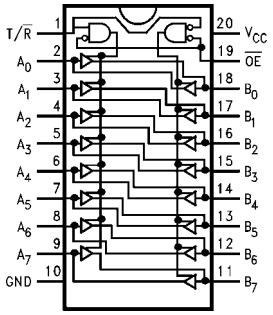
Order Number	Package Number	Package Description
74VHC245M	M20B	20-Lead Small Outline Integrated Package (SOIC), JEDEC MS-013, 0.300" Wide
74VHC245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC245N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Description

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial
Any unused bus terminals during HIGH-Z State must be held HIGH or LOW.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN}) (T/$\overline{R}$, $\overline{OE}$)	−0.5V to 7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK}) (T/$\overline{R}$, $\overline{OE}$)	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})(T/$\overline{R}$, $\overline{OE}$)	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs or I/O pins must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	µA	V_{IN} = V_{CC} or GND; V_{OUT} = V_{CC} or GND; V_{IN} $\overline{OE}$ = V_{IH} or V_{IL}	
I_{IN} (T/$\overline{R}$, $\overline{OE}$)	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 3)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.2	V	$C_L = 50$ pF
V_{OLV} (Note 3)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.9	−1.2	V	$C_L = 50$ pF
V_{IHD} (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50$ pF
V_{ILD} (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50$ pF

Note 3: Parameter guaranteed by design.

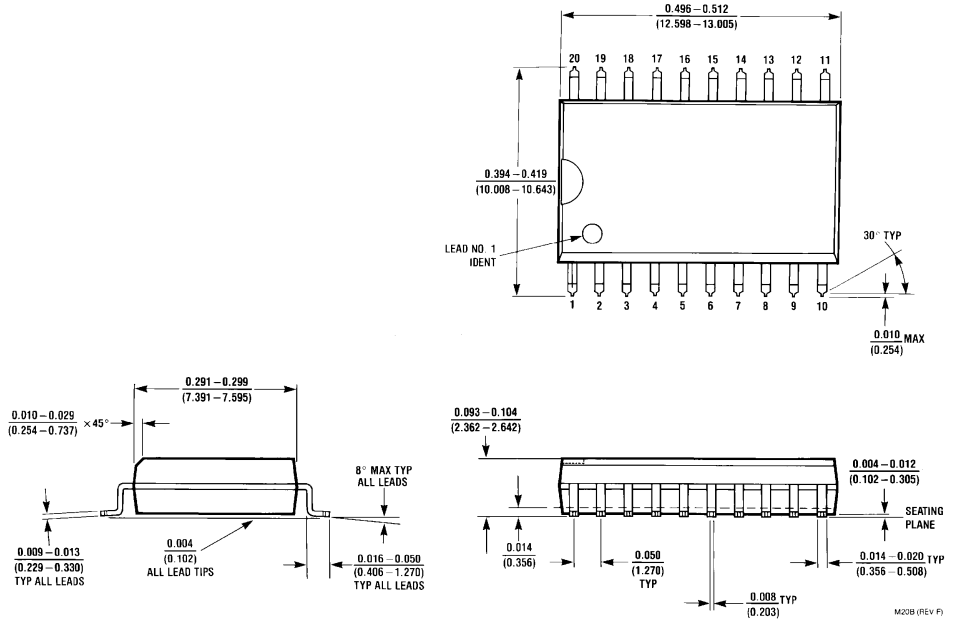
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Time	3.3 ± 0.3		5.8	8.4	1.0	10.0	ns		$C_L = 15$ pF
				8.3	11.9	1.0	13.5			$C_L = 50$ pF
		5.0 ± 0.5		4.0	5.5	1.0	6.5	ns		$C_L = 15$ pF
				5.5	7.5	1.0	8.5			$C_L = 50$ pF
t_{PZL} t_{PZH}	3-STATE Output Enable Time	3.3 ± 0.3		8.5	13.2	1.0	15.5	ns	$R_L = 1$ kΩ	$C_L = 15$ pF
				11.0	16.7	1.0	19.0			$C_L = 50$ pF
		5.0 ± 0.5		5.8	8.5	1.0	10.0	ns		$C_L = 15$ pF
				7.3	10.6	1.0	12.0			$C_L = 50$ pF
t_{PLZ} t_{PHZ}	3-STATE Output Disable Time	3.3 ± 0.3		11.5	15.8	1.0	18.0	ns	$R_L = 1$ kΩ	$C_L = 50$ pF
		5.0 ± 0.5		7.0	9.7	1.0	11.0			$C_L = 50$ pF
t_{OSLH} t_{OSHL}	Output to Output Skew	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	$C_L = 50$ pF
		5.0 ± 0.5			1.0		1.0			$C_L = 50$ pF
C_{IN} ($T/\overline{R}$, $\overline{OE}$)	Input Capacitance			4	10		10	pF	V_{CC} = Open	
$C_{I/O}$	Output Capacitance			8				pF	$V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance			21				pF	(Note 5)	

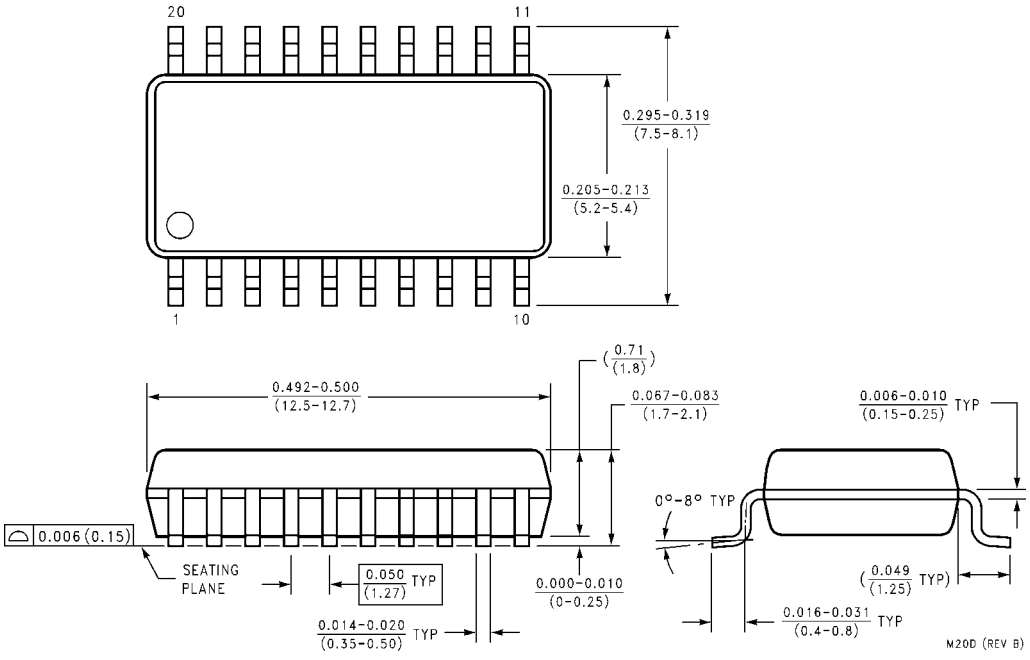
Note 4: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per Bit).

Physical Dimensions inches (millimeters) unless otherwise noted

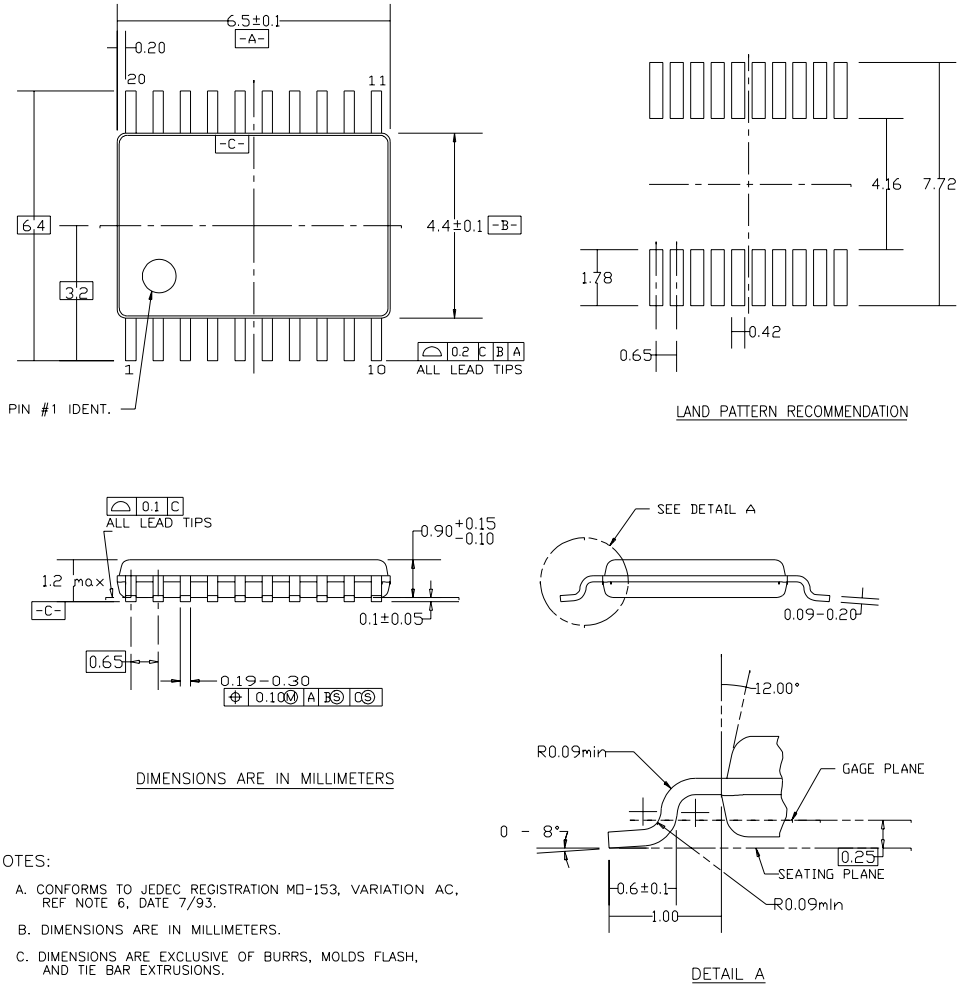


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

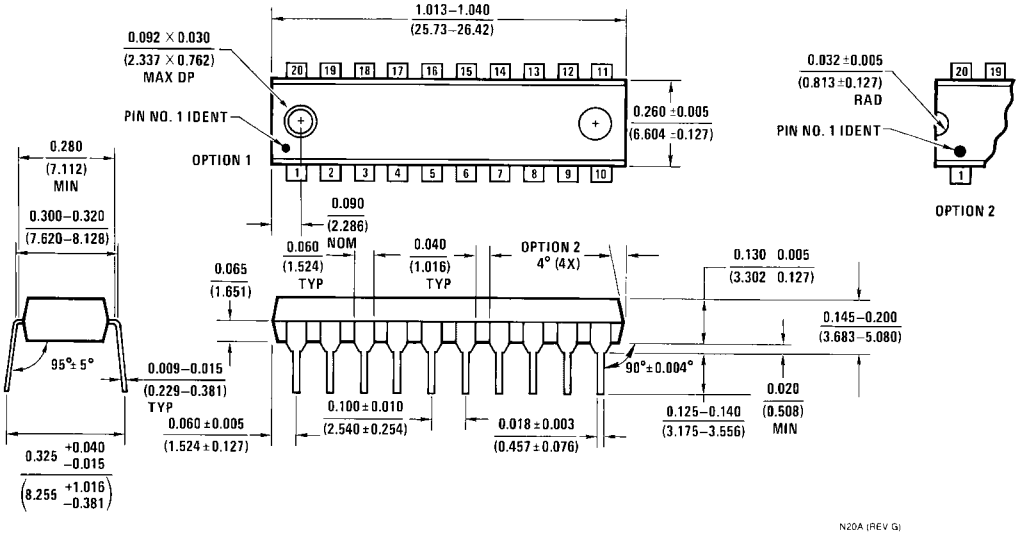
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A