

## 54F/74F545 Octal Bidirectional Transceiver with TRI-STATE® Outputs

### General Description

The 54F545 is an 8-bit, TRI-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA (20 mA Mil) bus drive capability on the A ports and 64 mA (48 mA Mil) bus drive capability on the B ports.

One input, Transmit/Receive (T/R) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a TRI-STATE condition.

### Features

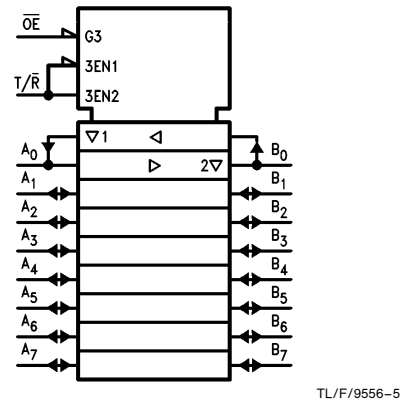
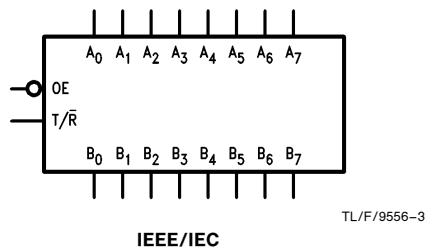
- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- TRI-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA (20 mA Mil) and 64 mA (48 mA Mil) bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection
- Pin for Pin compatible with Intel 8286

Commercial	Military	Package Number	Package Description
74F545PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F545DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F545SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F545SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F545FM (Note 2)	W20A	20-Lead Cerpack
	54F545LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

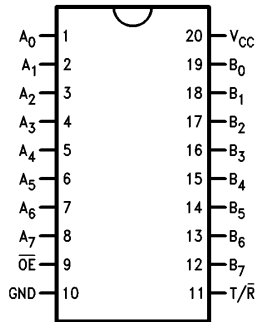
### Logic Symbols



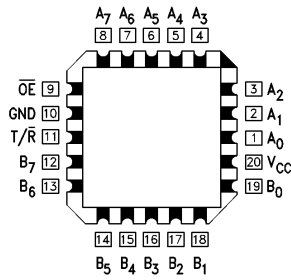
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## Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



Pin Assignment  
for LCC



TL/F/9556-2

TL/F/9556-1

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu A$ / -1.2 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/2.0	20 $\mu A$ / -1.2 mA
$A_0$ - $A_7$	Side A TRI-STATE Inputs or TRI-STATE Outputs	3.5/1.083	70 $\mu A$ / -650 $\mu A$
$B_0$ - $B_7$	Side B TRI-STATE Inputs or TRI-STATE Outputs	150/40 (33.3)	-3 mA/24 mA (20 mA)
		3.5/1.083	70 $\mu A$ / -650 $\mu A$
		600/106.6 (80)	-12 mA/64 mA (48 mA)

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V <sub>CC</sub>	Conditions
			Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage					V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2			V	Min	I <sub>IN</sub> = -18 mA ( $\overline{OE}$ , T/ $\overline{R}$ )
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5			V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> ) I <sub>OH</sub> = -12 mA (B <sub>n</sub> ) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> ) I <sub>OH</sub> = -15 mA (B <sub>n</sub> ) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> )
		54F 10% V <sub>CC</sub>	2.4					
		54F 10% V <sub>CC</sub>	2.0					
		74F 10% V <sub>CC</sub>	2.5					
		74F 10% V <sub>CC</sub>	2.4					
		74F 10% V <sub>CC</sub>	2.0					
		74F 5% V <sub>CC</sub>	2.7					
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA (A <sub>n</sub> ) I <sub>OL</sub> = 48 mA (B <sub>n</sub> ) I <sub>OL</sub> = 24 mA (A <sub>n</sub> ) I <sub>OL</sub> = 64 mA (B <sub>n</sub> )	
		54F 10% V <sub>CC</sub>		0.55				
		74F 10% V <sub>CC</sub>		0.5				
		74F 10% V <sub>CC</sub>		0.55				
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V ( $\overline{OE}$ , T/ $\overline{R}$ )	
		74F		5.0				
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE}$ , T/ $\overline{R}$ )	
		74F		7.0				
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F		1.0	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )	
		74F		0.5				
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
		74F		50				
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded	
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded	
I <sub>IL</sub>	Input LOW Current			-1.2	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , T/ $\overline{R}$ )	
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )	
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )	
			-100	-225				

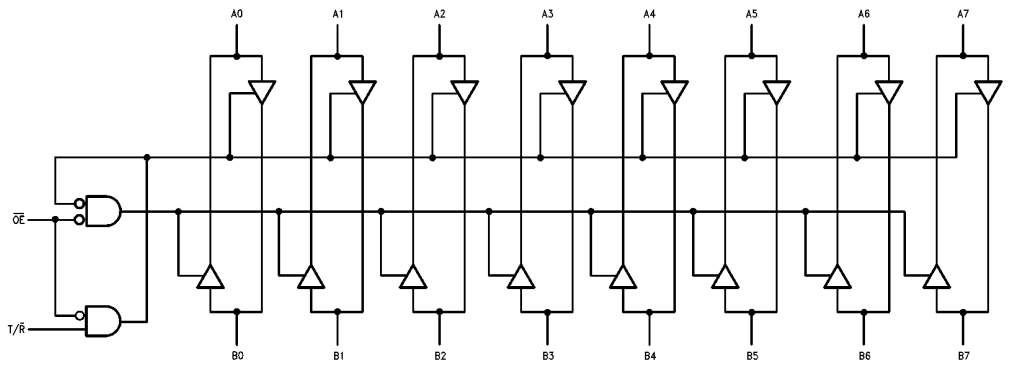
## DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		70	90	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		95	120	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		85	110	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	2.5	4.6	6.0	2.0	7.5	2.5	7.0	
t <sub>PZH</sub>	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns
t <sub>PZL</sub>		3.5	6.0	8.0	3.0	10.0	3.5	9.0	
t <sub>PHZ</sub>	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5	ns
t <sub>PLZ</sub>		2.0	5.0	6.5	2.0	10.0	2.0	7.5	

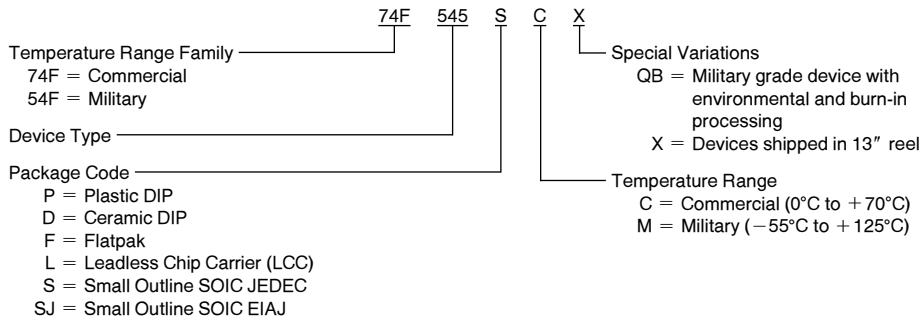
## Logic Diagram



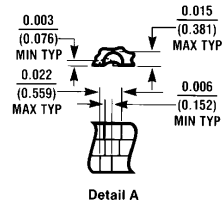
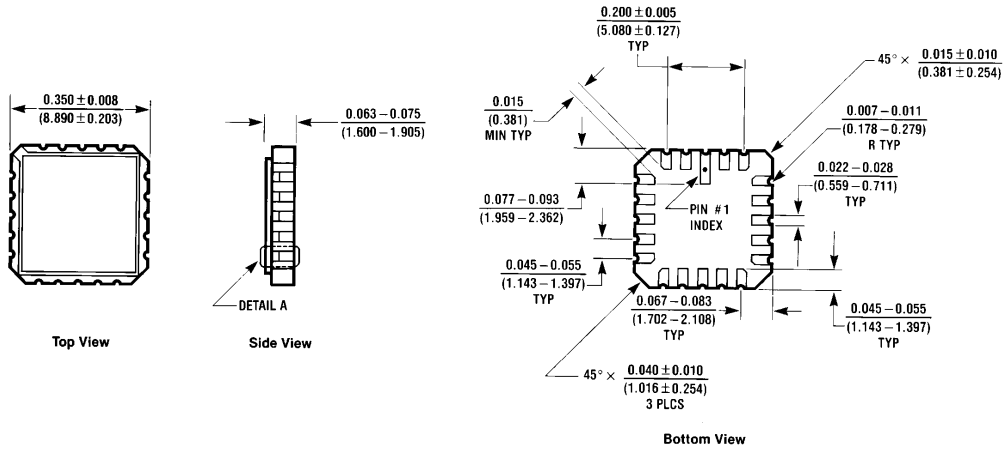
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

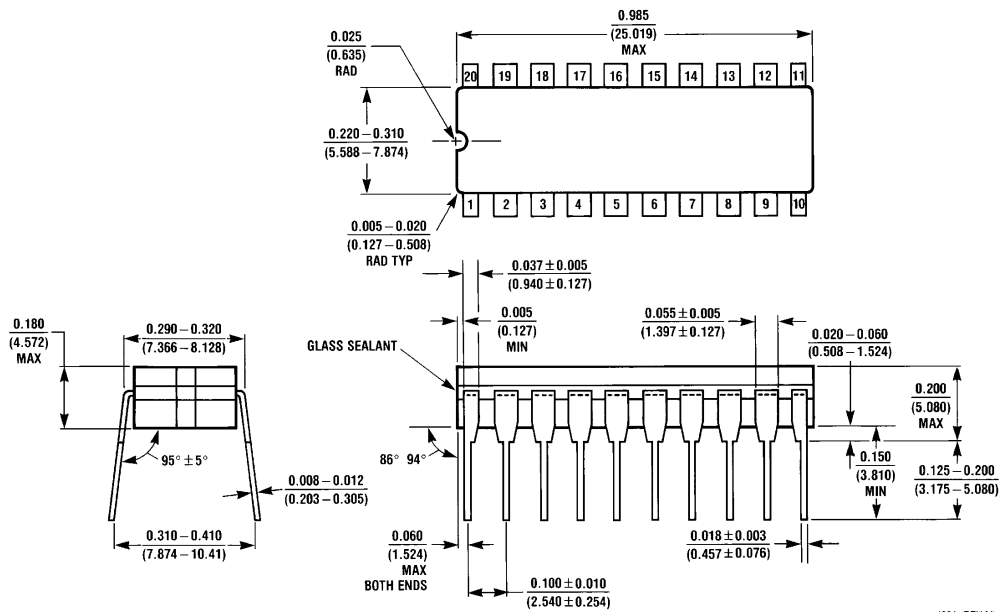


**Physical Dimensions** inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)**  
**NS Package Number E20A**

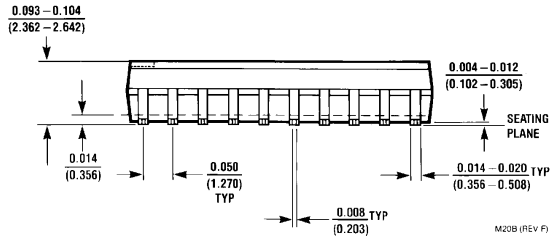
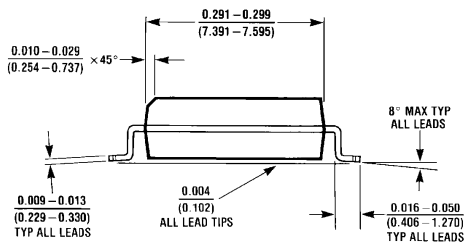
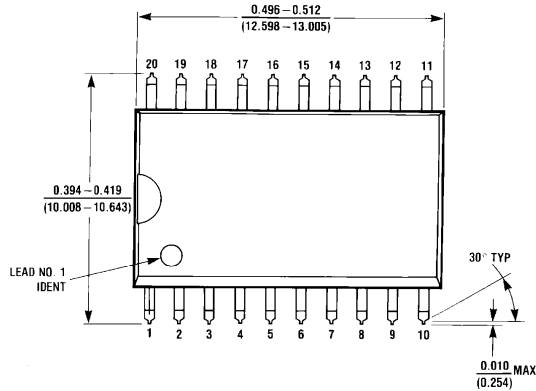
E20A (REV D)



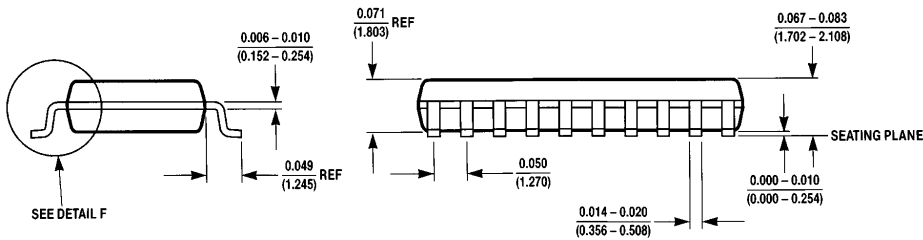
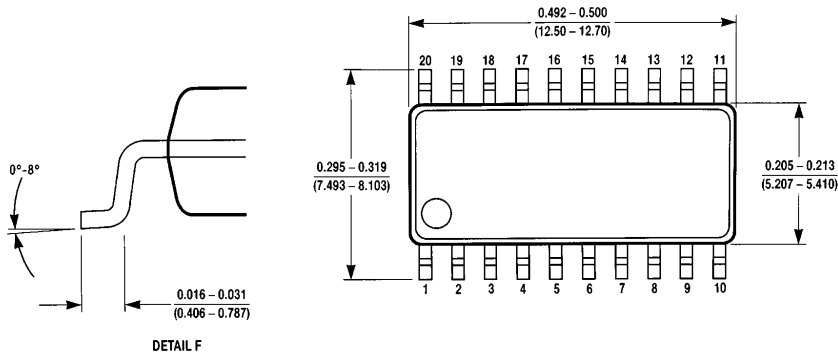
**20-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J20A**

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M20B**



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ  
NS Package Number M20D**



**Physical Dimensions** inches (millimeters) (Continued)



W20A (REV E)

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