■ DESCRIPTION

The SED1520 is a dot matrix LCD driver LSI intended for display of characters and graphics. The bit-addressable display data which is sent from a microcomputer is stored in a built-in display data RAM and generates the LCD drive signal.

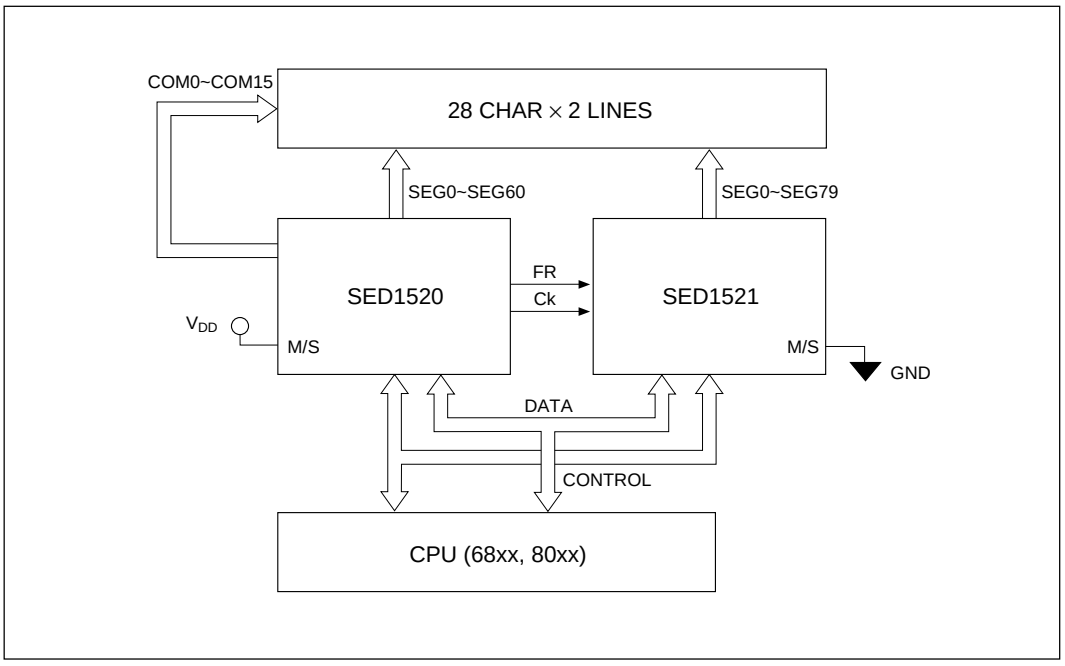
The SED1520 incorporates innovative circuit design strategies to assure very low current dissipation and a wide range of operating voltages. With these features, the SED1520 permits the user to implement high-performance handy systems operating from a miniature battery.

In order for the user to adaptively configure his system, the SED1520 family offers two application forms. One form allows an LCD display of 12 characters × 2 lines with an indicator with a single chip. The other is dedicated to driving a total of 80 segments, enabling a medium-size display to be achieved by using a minimum number of drivers.

■ FEATURES

- Low-power CMOS technology
- Fast CPU 8-bit data interface (80xx, 68xx)
- Segment output ..... 61 outputs
- Common output ..... 16 outputs
- Duty cycle ..... SED1520 ..... 1/16 to 1/32
  SED1521 ..... 1/8 to 1/32
- Built-in display data RAM ..... 2560 bits
- Rich display command setting
- On-chip CR oscillation circuit
- Recommended expansion segment driver: 80 bit
- Master/slave operation is supported
- Low power consumption 30μW
- LCD voltage ..... 3.5 to 13V
- Single power supply ..... 2.4 to 7.0V
- Package ..... QFP5-100 pin (F_{0A}, F_{AA})
  QFP15-100 pin (F_{0C}, F_{AC})
  Al pad (D_{0A}, D_{AA})
  Au bump (D_{0B}, D_{AB})
  TAB (T_{0A})

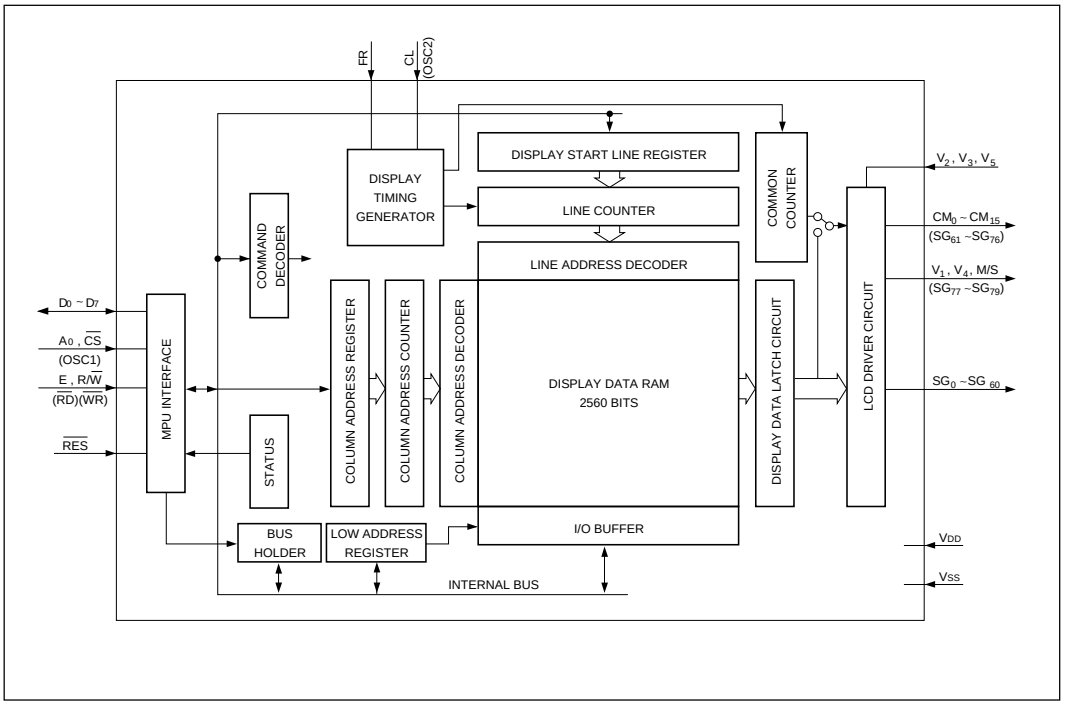
■ SYSTEM BLOCK DIAGRAM



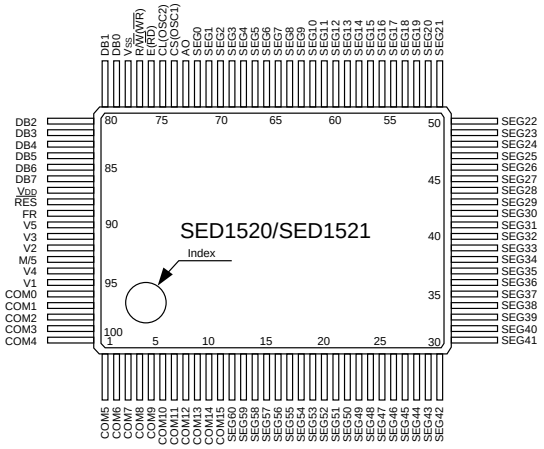
● SED1520 family specifications:

Product Name	Clock Frequency		Applicable Driver	No. of SEG Drivers	No. of COM Drivers
	On Chip	External			
SED1520F$_{OA}$	18kHz	18kHz	SED1520F$_{OA}$, SED1521F$_{OA}$	61	16
SED1521F$_{OA}$	—	18kHz		80	0
SED1520F$_{AA}$	—	2kHz	SED1520F$_{AA}$, SED1521F$_{AA}$, HD44103CH	61	16
SED1521F$_{AA}$	—	2kHz		80	0

■ BLOCK DIAGRAM



■ PINOUT



Model Name	Terminal No.	
	74	75
SED1520FO*	OSC1	OSC2
SED1520FA*	CS	CL

The Common output COM0 to COM15 of the Master LSI corresponds COM31 to COM16 on the Slave LSI.

■ PIN DESCRIPTION

Terminal Name	Function
DB0~DB7	Data input
A0	Selects display data or instructions. HIGH: Display data. LOW: Instructions.
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH: 68-port MPU interface. LOW: 80-port MPU interface.
$\overline{CS}$	Chip Select input. LOW: Active level sensing.
E ($\overline{RD}$)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/$\overline{W}$ ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH: Read Select LOW: Write Select (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input (only effective with external clock types).
FR	LCD Frame (AC-conversion) signal input/output.
SEG0~SEG60	Segment output for driving the LCD.
COM0~COM15 (COM31~COM16)	Common output for driving the LCD.
M/S	Master/Slave Select signal
V_{DD}	5V power supply.
V_{SS}	0V power supply (GND level).
V1, V2, V3, V4, V5	Power supplies for driving the LCD. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

■ MODEL CLASSIFICATION

Model Name	Operating Clock		Connectable Drivers	SEG Driver	COM driver
	Internal oscillator	External clock			
SED1520FO*	18 KHz	18 kHz	SED1520FO*, SED1521FO*	61 ports	16 ports
SED1520FA*	—	2 KHz	SED1520FA*, SED1521FA*	61 ports	16 ports

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD} = 0V, $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–8.0 to 0.3	V
Supply voltage (2)	V5	–16.5 to 0.3	V
Supply voltage (3)	V1, V4 V2, V3	V5 to 0.3	V
Input voltage	V_I	V_{SS}–0.3 to 0.3	V
Output voltage	V_O	V_{SS}–0.3 to 0.3	V
Permissible loss	P_D	250	mV
Operating temperature	T_{opr}	–30 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature	T_{sol}	260°C for 10 s (at leads)	—

- **DC Characteristics**

V_{DD} = 0V, T_a = –20 to 75°C

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Applicable Pin
Operating voltage (1)*1	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Potential				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V5			–13.0	—	–3.5	V	V5
	Potential				–13.0	—	—		
	Potential	V1, V2			0.6×V5	—	V_{DD}	V	V1, V2
	Potential	V3, V4			V5	—	0.4xV_{DD}	V	V3, V4
HIGH input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	*2
		V_{IHC}			0.2×V_{SS}	—	V_{DD}	V	*3
LOW input voltage		V_{ILT}			V_{SS}	—	V_{SS}+0.8	V	*2
		T_{ILC}			V_{SS}	—	0.8×V_{SS}	V	*3
HIGH output voltage		V_{OHT}	I_{OH}= –3.0mA		V_{SS}+2.4	—	—	V	D0~D7 pins
		V_{OHC1}	I_{OH}= –2.0mA		V_{SS}+2.4	—	—	V	FR pins
		V_{OHC2}	I_{OH}= –120µA		0.2×V_{SS}	—	—	V	OSC2
LOW output voltage		V_{OLT}	I_{OL}=3.0mA		—	—	V_{SS}+0.4	V	D0~D7, FR pins
		V_{OLC1}	I_{OL}=2.0mA		—	—	V_{SS}+0.4	V	FR pins
		V_{OLC2}	I_{OL}=120µA		—	—	0.8×V_{SS}	V	OSC2
Input leak current		I_{LI}			–1.0	—	1.0	µA	*4
Output leak current		I_{LO}	Applicable when FR is in a high-impedance state		–3.0	—	3.0	µA	D0~D7, FR pins
LCD driver ON resistance		R_{ON}	T_a=25°C	V5=–5.0V	—	5.0	7.5	kΩ	SEG0~60
				V5=–3.5V	—	10.0	50.0		COM0~15
Static current consumption		I_{DDQ}	$\overline{CS}$=CL=V_{DD}		—	0.05	1.0	µA	V_{DD}
Dynamic current dissipation	External CLK Oscillator	During $I_{DD(1)}$	f_{CL}=2kHz display	—	2.0	5.0		µA	V_{DD}
				R_f=1MΩ	—	9.5	15.0		
				f_{CL}=18kHz	—	5.0	10.0		
		$I_{DD(2)}$	During access t_{cyc}=200kHz		—	300	500	µA	V_{DD}
Input terminal capacity		C_{IN}	T_a=25°C f=1MHz		—	5.0	8.0	pF	All input terminals
Oscillation frequency		f_{OSC}	Rf=1.0MΩ±2%	V_{SS}= –5.0V	15	18	21	kHz	
			Rf=1.0MΩ±2%	V_{SS}= –3.0V	11	16	21		
Reset time		t_R			1.0	—	1000	µs	$\overline{RES}$

Notes:

*1. A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

*2. A0, D0~D7, E, R/$\overline{W}$ and $\overline{CS}$ pins.

*3. CL, FR, M/$\overline{S}$ and $\overline{RES}$ pins.

*4. A0, E, R/$\overline{W}$, $\overline{CS}$, CL, $\overline{RES}$, M/$\overline{S}$ pins.

● **AC Characteristics**

○ **Read/Write timing for the 80-port MPU**

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
Address hold time	A0, $\overline{CS}$	t_{AHB}		10	—	—	ns
Address set-up time		t_{AWB}		20	—	—	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0 ~ D7	t_{DS8}		80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100pF	—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

*2. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

○ **Read/Write timing for the 68-port MPU**

(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter		Signal	Symbol	Condition	Rating			Unit
					Min	Typ	Max	
System cycle time		A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *3		1000	—	—	ns
Address set-up time			t_{AW6}		20	—	—	ns
Address hold time			t_{AH6}		10	—	—	ns
Data set-up time		D0 ~ D7	t_{DS6}		80	—	—	ns
Data hold time			t_{DH6}		10	—	—	ns
Output disable time			t_{OH6}	C_L = 100pF	10	—	60	ns
Access time			t_{ACC6}		—	—	90	ns
Enable pulse width	READ	E	t_{EW}		100	—	—	ns
	WRITE				80	—	—	ns

*3. t_{CYC6} indicates the cycle during which $\overline{CS}$/$\overline{E}$ are HIGH; it does not indicate the cycle of the E signal.

*4. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

○ **Control timing for 80-port/68-port display**

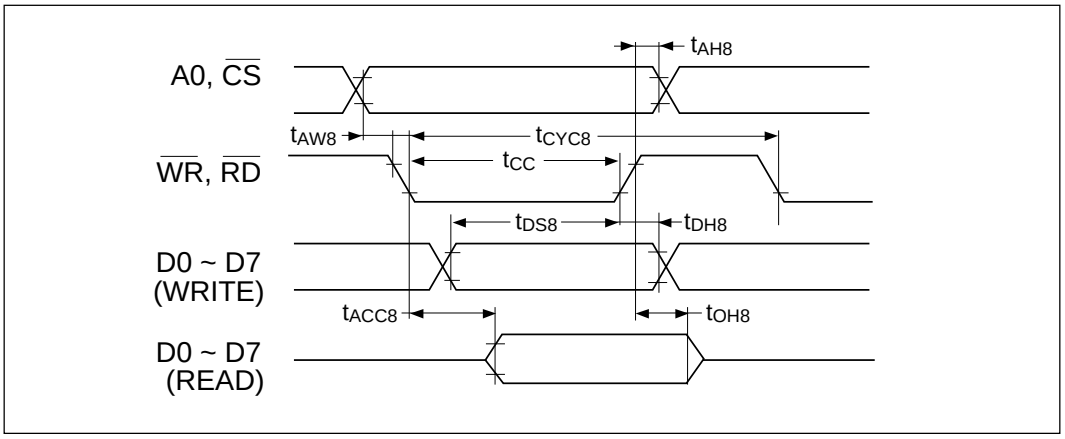
(T_a = –20 to 75°C, V_{SS} = –5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Typ	Max	
LOW pulse width	CL	t_{WLCL}		35	—	—	µs
HIGH pulse width		t_{WHCL}		35	—	—	µs
Rising time		t_r		—	30	150	ns
Falling time		t_f		—	30	150	ns
FR delay time	FR	t_{DFR}	(Input timing)	–2.0	0.2	2.0	µs
			(Output timing), C_L = 100pF	—	0.2	0.4	

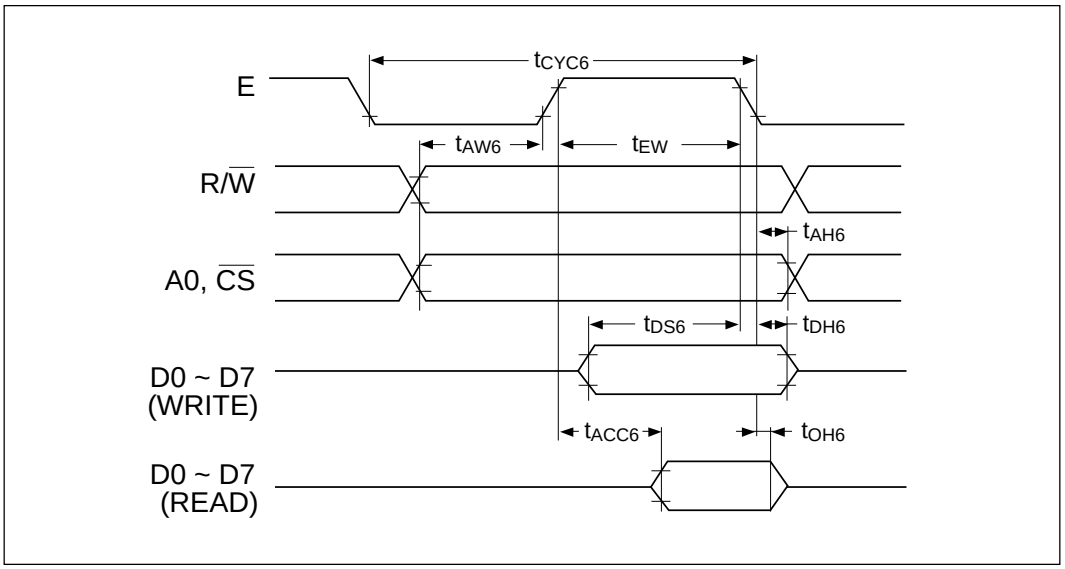
*5. The ratings when V_{SS} = –3.0V are approximately 100% higher than when V_{SS} = –5.0V.

*6. The input timing of the FR delay time is determined by the SED1520 (Slave).
The output timing of the FR delay time is determined by the SED1520 (Master).

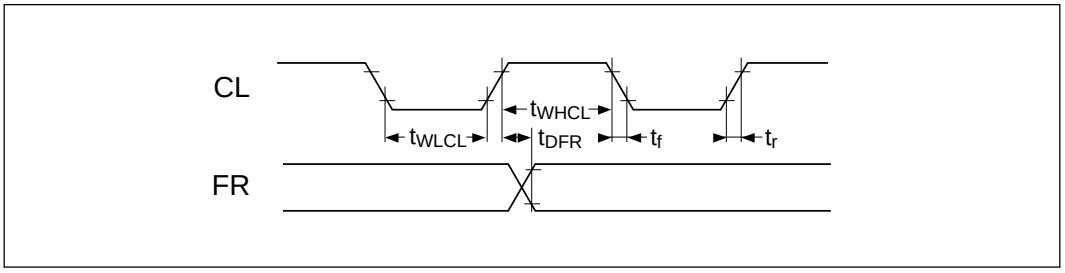
- **Timing Chart**
  - **Read/Write timing for the 80-port MPU**



  - **Read/Write timing for the 68-port MPU**



  - **Control timing for 80-port/68-port display**



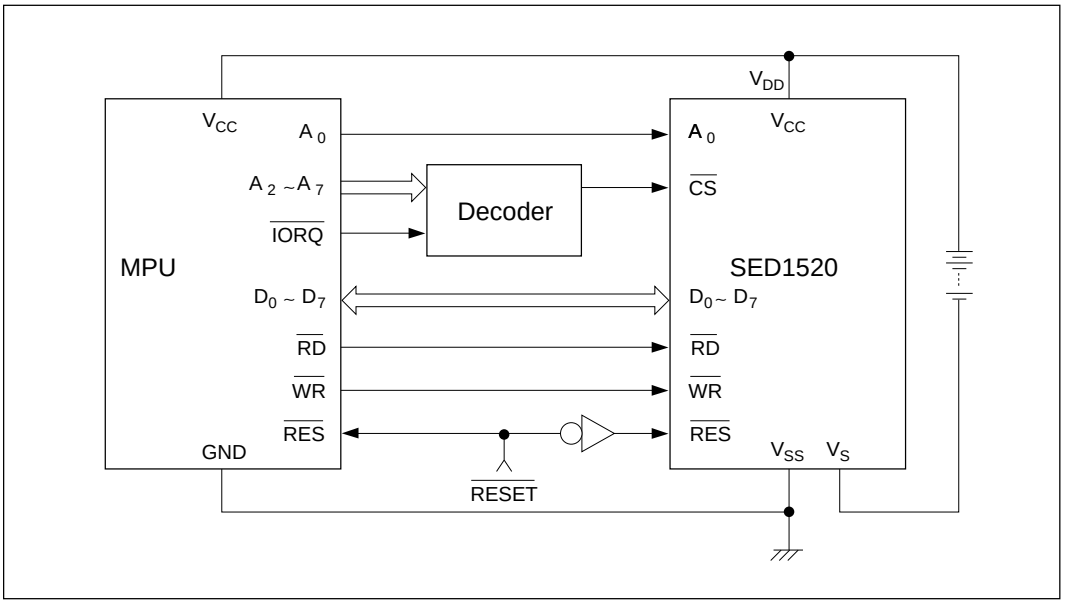
■ **DISPLAY COMMANDS**
(Based on the 80-port MPU; the $\overline{RD}$ and $\overline{WR}$ commands differ for the 68-port MPU.)

	Command	$\overline{RD}$	$\overline{WR}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Function
1	Display ON/OFF	1	0	0	1	0	1	0	1	1	1	0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *7
2	Display START Line	1	0	0	1	1	0	Display START address (0~31)					Determines the line of RAM data to be displayed at the display's top line (COM0).
3	Page Address Set	1	0	0	1	0	1	1	1	0	Page (0~3)		Sets the page of the Display RAM in the page address register.
4	Column (Segment) Address Set	1	0	0	0	Column address (0~79)							Sets the column address of the Display RAM in the column address register.
5	Status Read	0	1	0	BUSY	ACC	ON/OFF	RESET	0	0	0	0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1	0	1	Write Data								Writes the data on the data bus to RAM
7	Read Display Data	0	1	1	Read Data								Reads data from the Display RAM onto the data bus.
													These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
8	ADC Select	1	0	0	1	0	1	0	0	0	0	0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1	0	0	1	0	1	0	0	1	0	0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *7 0: Normal display operation
10	Duty Select	1	0	0	1	0	1	0	1	0	0	0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11	Read Modify Write	1	0	0	1	1	1	0	0	0	0	0	Increments the column address counter by one only when display data is written but not when it is read.
12	End	1	0	0	1	1	1	0	1	1	1	0	Cancels the Ready Modify Write mode.
13	Reset	1	0	0	1	1	1	0	0	0	1	0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

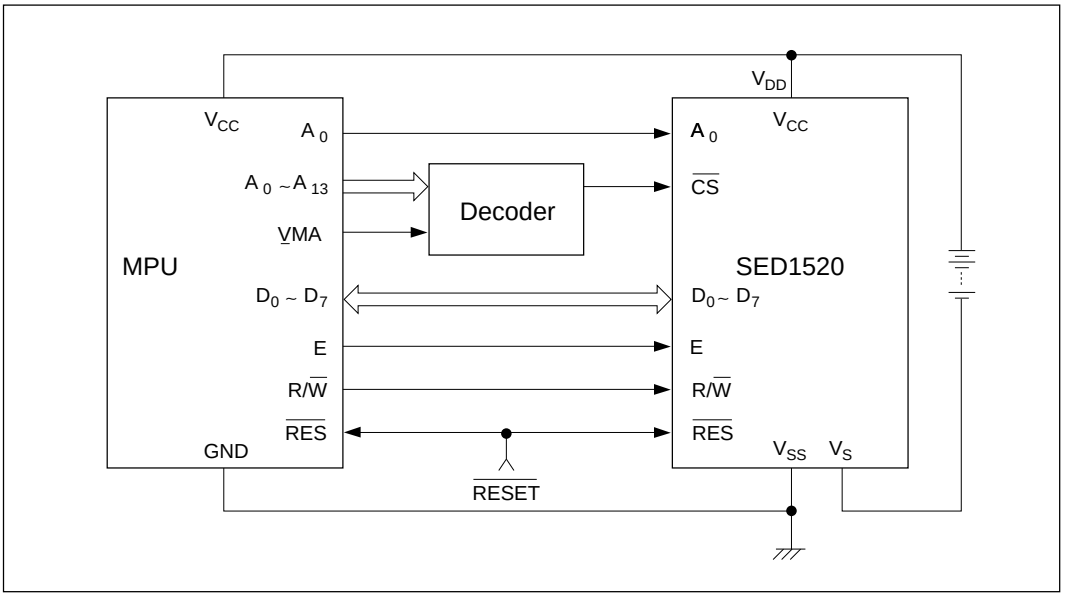
*7. Power Save mode is entered by selecting static drive in Display OFF status.

● **MPU INTERFACE (Reference)**

○ **(a) 80-family MPU**



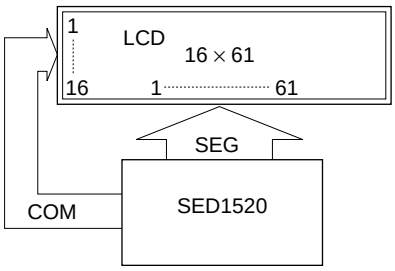
○ **(b) 68-family MPU**



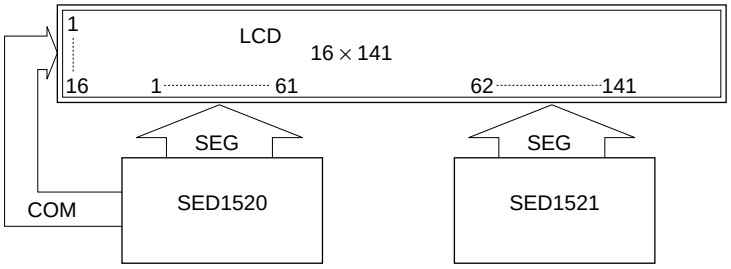
* The SED1520 (containing an oscillator) does not have pin $\overline{CS}$. The output ORed with $\overline{CS}$ must be applied to pins A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$).

- **Typical Connections With LCD Panel (Full dot LCD panel: 1 character = 6 × 8 dots)**

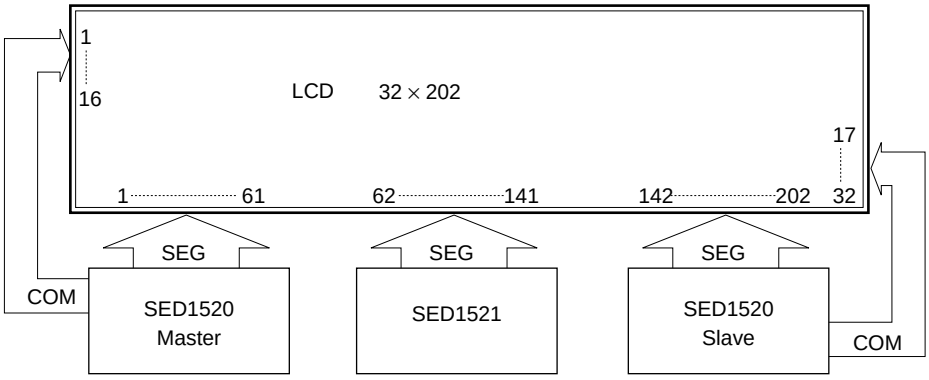
○ **(a) Duty 1/16, 10 characters × 2 lines**



○ **(b) Duty 1/16, 23 characters × 2 lines**



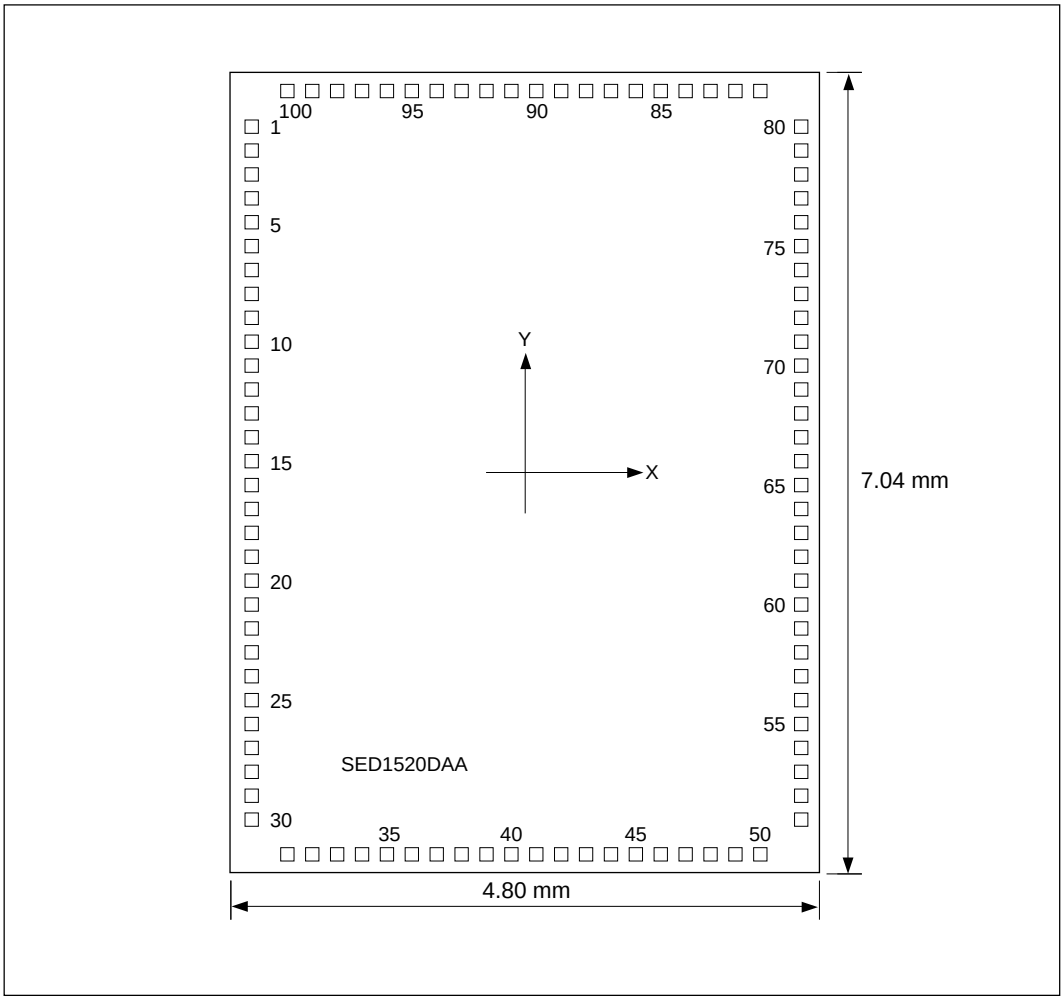
○ **(c) Duty 1/32, 33 characters × 4 lines**



* SED1521 may be omitted. If it is not used, the panel consists of 32 × 122 dots.

Note: Type AA (using external clock) and type 0A (containing an oscillator) cannot coexist for the same panel.

■ PAD LAYOUT (SED1520D/SED1521D)



● **Al pad**

Chip Specification	Dimensions (mm)
Chip size	7.04 × 4.80
Chip thickness	0.400 ± 0.025
Pad size	0.10 × 0.10

● **Au bump pad**

Chip Specification	Dimensions (mm)
Chip size	7.04 × 4.80
Chip thickness	0.525 ± 0.025
Pad size	0.132 × 0.111
Pad pitch	0.199 min
Bump height	0.020 +0.01 to –0.005

■ PAD COORDINATES (SED1520D$_{AB}$)

Pad		X	Y
No.	Name		
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159

Pad		X	Y
No.	Name		
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	2696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948

Pad		X	Y
No.	Name		
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	$\overline{CS}$	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V5	2699	6884
91	V3	2300	6884
92	V2	2100	6884
93	M/S	1901	6884
94	V4	1701	6884
95	V1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884