Airoha Technology Corp.

Application Note RDN_R6952

AR1000 Programming Guide (RevF)

HISTORY

Version	Change Summary	Date	Author
0.10	Created	07-Dec-06	KH Chen
0.20	For RevD Update	05-Mar-07	Purple Liu
0.30	Add description of the difference between RevD&E	12-Mar-07	Purple Liu
0.40	For RevE Update	04-May-07	Purple Liu
0.41	Errata	11-May-07	Purple Liu
0.60	Update volume control & register	09-July-07	Purple Liu
0.80	For RevF Update	30-July-07	Purple Liu
0.81	Errata & Update register value	22-Jan-08	Purple Liu

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1 Introduction

The AR1000 FM radio single chip integrates 2-wire and 3-wire interfaces for register read & write control from the host processor. The chip is controlled through register settings; the chip status and RDS/RBDS data can be read through registers, too. In this programming guide, the pin assignment of evaluation board hardware interfaces are first introduced. The register contents are described, and the initialization procedure of AR1000 is also presented. The detailed behaviors of 3-wire and 2-wire interface are presented. Finally a sample code of AR1000 is included.

The package of AR1000 (RevF) is 4x4 24-pin package. The register map is different from previous versions, such that the control software (FMTool) should be upgraded, too. However, the hardware interface definition of the EVB board is the same.

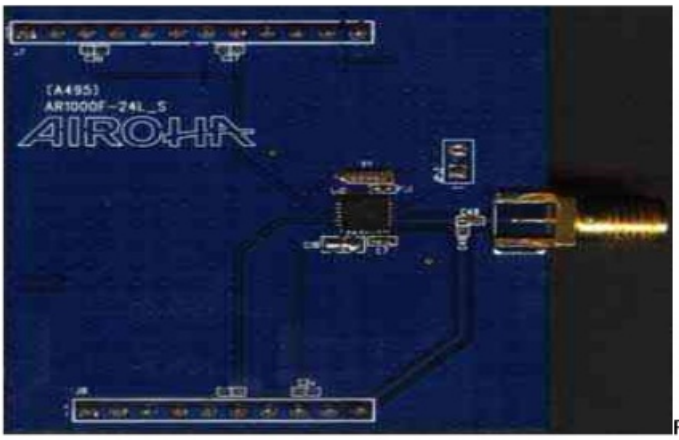


Figure 1.1: AR1000 RevF EVB

2 Hardware Interface

There are two connectors on the AR1000 EVB: J7 and J8. The pin definitions of the two connectors are listed as follows:

PIN #	PIN Name	Description
Connector J7		
1	NC	Not connected, Keep Floating
2	NC	Not connected, Keep Floating
3	BUSEN	Serial Interface
4	DATAIO	Serial Interface
5	GND	Ground
6	CLOCK	Serial Interface
7	GND	Ground
8	GPIO1	General I/O Port
9	GPIO3	General I/O Port
10	NC	Not connected, Keep Floating
11	GPIO2	General I/O Port
12	NC	Not Connected, Keep Floating
Connector J8		
1	VCCIO	Supply Voltage for I/O Ports
2	VDDD	Supply Voltage for Digital Circuits
3	GND	Ground
4	VANA	Supply Voltage for Analog Circuits
5	GND	Ground
6	L_OUT	Left Channel Audio Output
7	GND	Ground
8	R_OUT	Right Channel Audio Output
9	GND	Ground
10	NC	Not Connected, Keep Floating

Please note that the Supply Voltage of digital/analog circuits must be with the same voltage level. VCCIO should be with the same level as VCC supply voltage of the host controller I/O ports.

3 Register Programming Table

3.1 Register Map (RevF)

The register map is presented at the end of this document.

3.2 Register Table (RevF)

REG	Description
R0	
xo_en	Internal oscillator enable signal. Logic '0' for using external reference clock, logic '1' for enable the internal oscillator.
ENABLE	Analog and digital blocks enable signals.
R1	
rds_en	RDS enable signal.
rds_int_en	RDS interrupt enable. Logic '1'=Enable, logic '0'=Disable. If enabled, RDS will generate a 5-ms active low interrupt signal at GPIO2 every time when (1) RDS data group received successfully, and (2) R13_GPIO2<1:0>='01'.
stc_int_en	Seek tune complete enable signals. This signal will result in a 5-ms active low interrupt signal at GPIO2 after (1) seek or tune completed, and (2) R13_GPIO2<1:0>='01'.
deemp	De-emphasis. Logic '1' for 75-us de-emphasis, logic '0' for 50-us de-emphasis.
mono	Forced mono control signal. Logic '1' for mono; logic '0' depends on signal strength.
smute	Soft mute control signal. Logic '1' for enable; logic '0' for disable. Disable it when testing sensitivity.
hmute	Hard mute control signal. Logic '1' for enable; logic '0' for disable

R 2

TUNE	TUNE channel enable signals. '1' = Enable, '0' = Disable. Each tuning process must set this signal from '0' to '1' to get the enabling edge signal. The STC flag is cleared to '0' automatically if TUNE is set to '0'.
CHAN<8:0>	Channel setting control signals. From 9'd0 to 9'd511. The FM channel is mapped by the equation. Frequency (MHz) = 69 + 0.1 * CHAN.

R 3

SEEKUP	Seek direction control signals. Logic '1' for seek up, logic '0' for seek down.
SEEK	SEEK channel enable signals ('1' for enable, '0' for disable). Each seeking process must set this signal from '0' to '1' to get the enabling edge signal.
SPACE	Channel spacing setting signal for SEEK operation. Logic '1' for 100k, logic '0' for 200k. When the spacing is set at 200k, no matter what the band is, it just increases or decreases it by 200k spacing.
BAND<1:0>	Band control signal. 2'b0x: US/Europe band. Range from 87.5MHz to 108MHz 2'b10: JAPAN band. Range from 76MHz to 90MHz 2'b11: JAPAN wide band. Range from 76MHz to 108MHz
VOLUMN<3:0>	EAR amplifier analog gain control signals.
SEEKTH<6:0>	SEEK threshold control signals. Setting too high would result in channel missing.

R 10

seek_wrap	SEEK wrap enable signal 1:wrap 0:no wrap

R 11

hilo_side	AFC high side and low side injection control.
hiloctrl_b1	High side control bit 1
hiloctrl_b2	High side control bit 2

R 13

GPIO3<1:0>	General purpose IO 3 control signals 2'b00 for disable, 2'b01 for stereo indication 2'b10 for logic '0', 2'b11 for logic '1'

GPIO2<1:0>	General purpose IO 2 control signals 2'b00 for disable, 2'b01 for STC or RDS interrupt 2'b10 for logic '0', 2'b11 for logic '1'
GPIO1<1:0>	General purpose IO 1 control signals 2'b00 for disable, 2'b01 for reserved 2'b10 for logic '0', 2'b11 for logic '1'

R14

VOLUME2	Volume control 2

R15

rds_sta_en	RDS statistic data enable signal.
rds_mecc<1:0>	RDS Error Correction. 2'b0x disable error correction 2'b10 2-bit error correction 2'b11 5-bit error correction
rds_ctrl	RDS mode control Logic '0' for block mode. RDSR is asserted once 4 blocks are received. The data in blocks may not be correct. RBS1~RBS4 will present the status of each block. Logic '1' for group mode., RDSR is asserted when 4 blocks received without any error.

RSSI

RSSI<6:0>	RF input signal strength
IF_CNT<8:0>	IF frequency counter

STATUS

READCHAN<8:0>	Current Channel number
RDSR	RDS data ready flag. '1'=Ready, '0'=Not ready
STC	Seek/Tune complete flag, '1'=Complete, '0'=Incomplete
SF	Seek fail flag, '1'=Seek Fail, '0'=Successful

ST	Stereo flag, '1'=Stereo, '0'=Mono

RBS

RBS1<1:0>	RDS block status for block 1 00 : no error 01 : 1 ~ 2 bit errors in this block 10 : 3 ~ 5 bit errors in this block 11 : error is not correctable
RBS2<1:0>	RDS block status for block 2 00 : no error 01 : 1 ~ 2 bit errors in this block 10 : 3 ~ 5 bit errors in this block 11 : error is not correctable
RBS3<1:0>	RDS block status for block 3 00 : no error 01 : 1 ~ 2 bit errors in this block 10 : 3 ~ 5 bit errors in this block 11 : error is not correctable
RBS4<1:0>	RDS block status for block 4 00 : no error 01 : 1 ~ 2 bit errors in this block 10 : 3 ~ 5 bit errors in this block 11 : error is not correctable

RDS1

RDS1<15:0>	RDS1 data

RDS2

RDS2<15:0>	RDS2 data

RDS3

RDS3<15:0>	RDS3 data

RDS4

RDS4<15:0>	RDS4 data

RDS5

rds_dsc<15:0>	RDS correct data block statistics

RDS6

rds_dfc<15:0>	RDS wrong data block statistics

DEVID

VERSION<3:0>	FM radio version control (4'b0110)
MFID<11:0>	Manufacturer ID (12'h5B1)

CHIPID

CHIPNO<15:0>	FM radio IC No. (16'h1000 is for RDS version, 16'h1010 is No-RDS version)

Please notice that in AR1000 version F, register address from 00H~11H are control registers and could be READ or WRITE; register address from 12H~1CH are status registers and could be READ only.

3.3 RF Frequency Calculation

The RF frequency setting of AR1000 is calculated as follows:

RF Frequency (in KHz) = 690 + CHAN

while CHAN (in decimal) is D8~D0 of register R2.

The host processor can set RF frequency directly by changing CHAN values. The BAND bit (D12 of register R3) is used to indicate the valid frequency range for TUNE and SEEK functions of AR1000, 76~90MHz for Japan band and 87.5~108MHz for US/Europe band. Japan wideband (76~108MHz) is also supported.

3.4 Note about SEEK Function

Before a SEEK function is performed, host controller should set appropriate CHAN as the starting frequency to seek from. This value may be read from the previous seeking result in READCHAN<8:0> and be set onto CHAN<8:0>. After CHAN<8:0> is updated the SEEK function could then be enabled. STC flag should be used to check if SEEK operation is finished or not. When STC flag is set, SF flag indicates if this operation successes or not. If no station is found, SF is set to 1 which means "seek fail". The SEEK operation under way could be stopped by register setting.

3.5 Note about SEEK/TUNE with Auto Hi/Lo Side Selection

Cooperating with software driver, user can accomplish SEEK/TUNE with auto Hi-Lo Side selection. See also Chapter 6 Pseudo Code for implementation.

3.6 Default register values of AR1000 RevF (using crystal)

The default register values of AR1000 RevF is as follows: (V23_080123).

Symbol	Address	Value
R0	00H	0xFFFB
R1	01H	0x5B15
R2	02H	0xD0B9
R3	03H	0xA010
R4	04H	0x0780
R5	05H	0x28AB
R6	06H	0x6400
R7	07H	0x1EE7
R8	08H	0x7141
R9	09H	0x007D
R10	0AH	0x82C6
R11	0BH	0x4E55
R12	0CH	0x970C
R13	0DH	0xB845
R14	0EH	0xFC2D
R15	0FH	0x8097
R16	10H	0x04A1
R17	11H	0xDF6A

3.7 Default register values of AR1000 RevF (using external clock)

The default register values of AR1000 RevF is as follows: (V23_080123).

Symbol	Address	Value
R0	00H	0xFF7B
R1	01H	0x5B15
R2	02H	0xD0B9
R3	03H	0xA010
R4	04H	0x0780
R5	05H	0x28AB
R6	06H	0x6400
R7	07H	0x1EE7
R8	08H	0x7141
R9	09H	0x007D
R10	0AH	0x82C6
R11	0BH	0x4F55
R12	0CH	0x970C
R13	0DH	0xB845
R14	0EH	0xFC2D
R15	0FH	0x8097
R16	10H	0x04A1
R17	11H	0xDF6A

3.8 Volume control of AR1000 RevF

The volume control of AR1000 could be set by sending registers. There are two volume control fields in registers: Volume in R3 (D7~D10), Volume2 in R14 (D12~D15). The following table presents 19 recommended combinations to increasing the gain of L/R audio outputs.

Step	Volume2	Volume
0	0	F
1	C	F
2	D	F
3	F	F
4	C	B
5	D	B
6	F	B
7	F	A
8	F	9
9	F	8
10	F	7
11	D	6
12	E	6
13	F	6
14	E	3
15	F	3
16	F	2
17	F	1
18	F	0

4 Initialization Procedure

The serial interface is built by BUSEN, CLOCK and DATA. The 3-wire mode is selected if BUSMOD is HIGH, and the 2-wire mode is selected if BUSMODE is LOW.

Register Feeding Sequence of Power-on Initialization:

At the Register Setting Stage of AR1000 after the Reset State, the register feeding sequence must be in the following order:

AR1000 RevF: (START) 01H → 02H → ⋯ → 11H → 00H (END)

And then enter the Calibration State. This order must be followed no matter 2-wire or 3-wire interface is used.

When AR1000 finishes its Calibration State, the STC flag will be set. The control software must wait for this flag before the first tune.

The timing diagrams are shown in figure 4.1 and 4.2.

Figure 4.1: Procedure for 2-wire mode initialization in AR1000 RevF

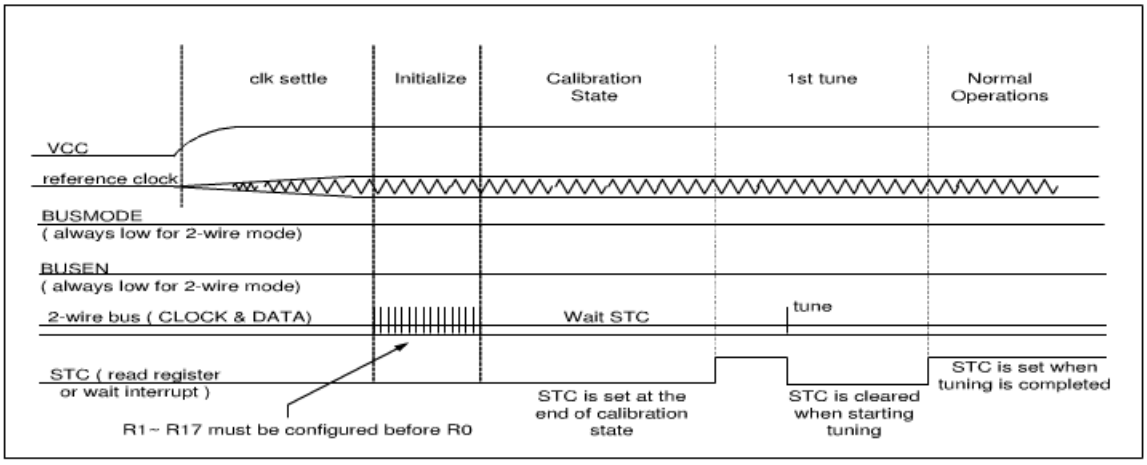
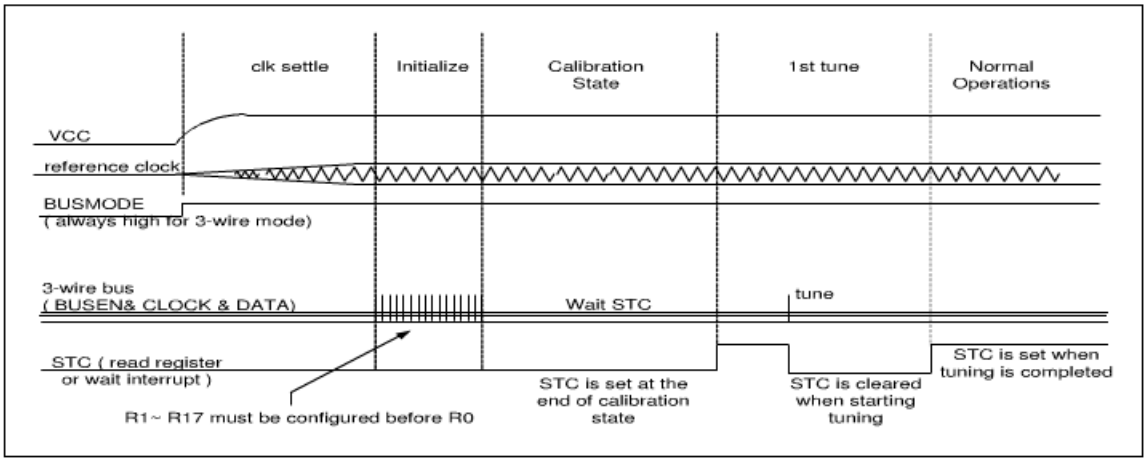


Figure 4.2: Procedure for 3-wire mode initialization in AR1000 RevF



5 Serial Interface

5.1 The 3-Wire Interface

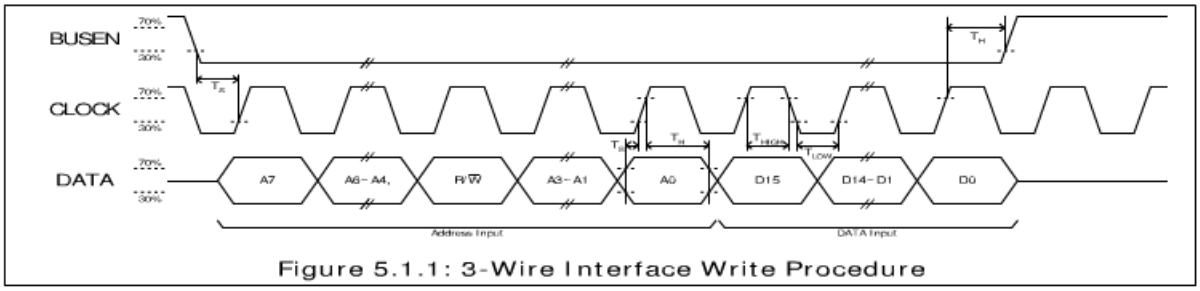


Figure 5.1.1: 3-Wire Interface Write Procedure

Figure 5.1.1 shows the WRITE procedure of 3-wire interface. The BUSEN of 3-wire interface is active low, so it should be kept at HIGH if 3-wire interface is inactive. When BUSEN set to "0", the 3-wire interface is activated, and the Master (host processor) will send 26 CLOCK signals in a WRITE process. BUSEN must be set to "1" before the last (the 26th) CLOCK to end this transmission.

A7~A0 is the register address, while R/$\bar{W}$ indicates the READ or WRITE procedure (R/$\bar{W}$ = "0" means WRITE procedure). D15~D0 is the 16-bit data of that register. At the last (26th) CLOCK, AR1000 will update the received data into the register and complete the WRITE process.

Figure 5.1.2 shows the READ procedure of 3-wire interface. When BUSEN is set to "0", the 3-wire interface is activated, and the Master (host processor) will send 26 CLOCK signals in a READ process. BUSEN must be set to "1" before the last (the 26th) CLOCK to end this transmission.

A7~A0 is the register address, while R/$\bar{W}$ indicates the READ or WRITE

procedure (R/$\bar{W}$ = "1" means READ procedure). A 1/2 clock cycle duration is inserted after the address bits for bus turn-around. D15~D0 is the 16-bit data of that register, feeding by AR1000. At the last (26th) CLOCK, AR1000 will complete the READ process.

The detailed timing spec of Figure 5.1.1 and 5.1.2 are listed in Table 5.1.1.

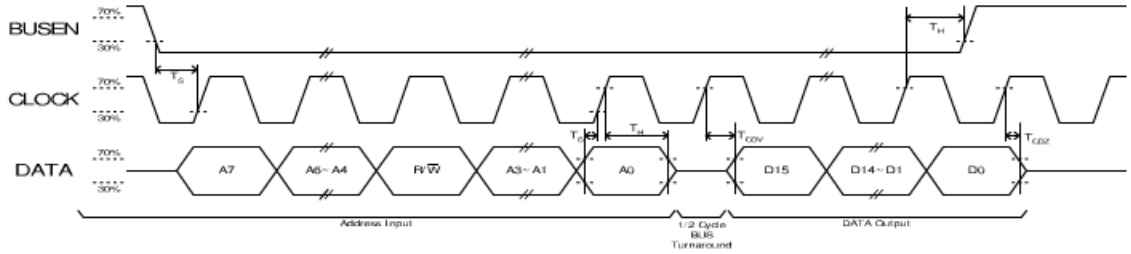


Figure 5.1.2: 3-Wire Interface Read Procedure

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		2.5	MHz
T_S	DATA In, BUSEN to CLOCK P-edge Setup time	20			ns
T_H	DATA In, BUSEN to CLOCK P-edge Hold time	10			ns
T_{HIGH}	CLOCK HIGH duration	25			ns
T_{LOW}	CLOCK LOW duration	25			ns
T_{DV}	CLOCK P-edge to DATA OUT Valid time	2		25	ns
T_{DZ}	CLOCK P-edge to DATA OUT High-Z time	2		25	ns

Table 5.1.1: Timing spec of 3-wire interface

5.2 The 2-Wire Interface

As shown in figure 5.2.1, the data length is 8-bits long for one data transfer on 2-wire interface. Each data transfer is followed by an ACK bit from receiver side. Data is transferred with the most significant bit (MSB) first.

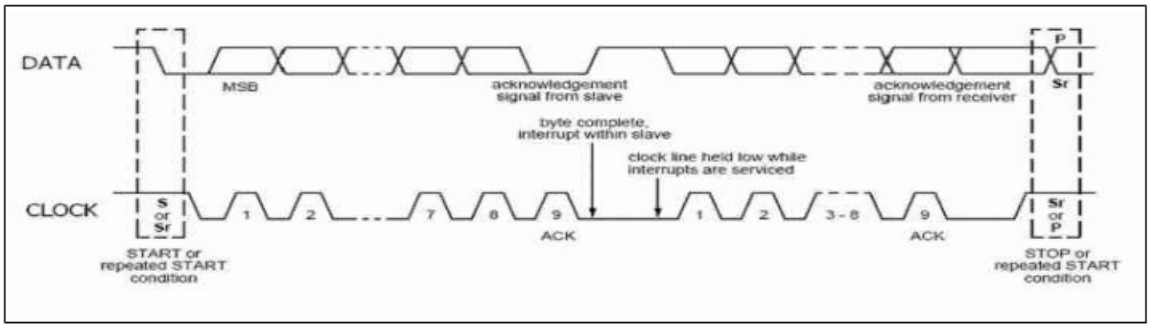


Figure 5.2.1: Data transfer on 2-wire interface

In a "READ" mode, as shown in figure 5.2.2, the receiver should send an ACK (="0") signal to transmitter at the end of each 8-bit data transfer, and the transmitter will send the following data. On the other hand, if the receiver sends a NACK (="1") signal to transmitter, the READ mode will be terminated.

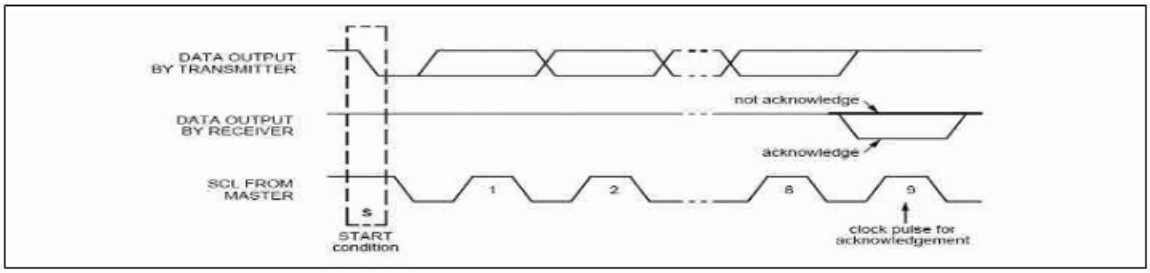


Figure 5.2.2: ACK/ NACK of the 2-wire interface

In a WRITE mode, the host processor is the "master-transmitter" while AR1000 is the "slave-receiver". In a "READ" mode, the host processor is the "master-receiver" while AR1000 is the "slave-transmitter". The device address of AR1000 in 2-wire mode is 7b'001_0000.

Write a register into AR1000 through 2-wire interface

To write a register data into AR1000, as shown in Figure 5.2.3, the master-transmitter should at first initiate a start condition followed by the 7-bit 2-wire-mode slave address and a WRITE bit ($R/\bar{W}$="0" which means this is a WRITE process) to indicate that AR1000 should be into WRITE mode now. The slave-receiver (AR1000) then returns an ACK to master-transmitter.

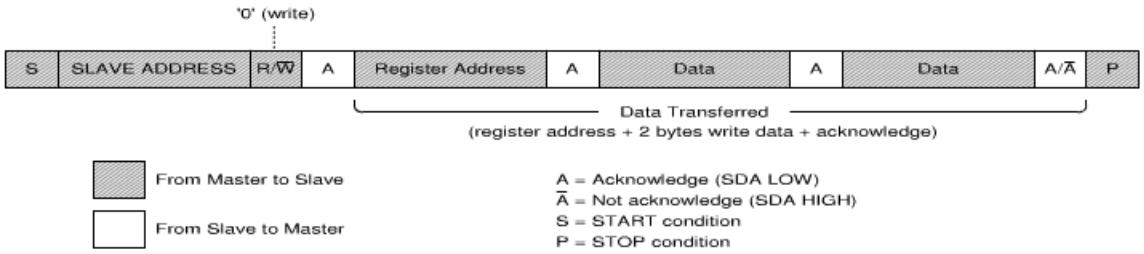


Figure 5.2.3: WRITE mode of 2-wire interface

Then master-transmitter transmits the target register address into slave-receiver, and slave-receiver returns an ACK again. The register content (16-bit length) is separated into two bytes data and sent into the slave-receiver, and slave-receiver should send back two ACK correspondingly. The whole WRITE Register process is then terminated by a STOP condition from master-transmitter.

The whole WRITE ONE REGISTER process could be designed as follows:

1. Master (Host processor) initiates a START condition.
2. Master writes the device address of the slave (AR1000), and then followed a WRITE bit. Slave sends back an ACK.
3. Master writes the register address of AR1000. Slave sends back an ACK.
4. Master writes 2-byte data to complete a register, and then sends a STOP condition to end the write procedure.

Read a register from AR1000 through 2-wire interface

To read a register data from AR1000, as shown in Figure 5.2.4, the process is separated into two partitions. At first the master-receiver initiates a start condition followed by the 7-bit 2-wire-mode slave address and a WRITE bit (R/$\bar{W}$="0" which means this is a WRITE process), and the slave-transmitter returns an ACK. Then master-receiver transmits the target register address into slave-transmitter, and slave-transmitter returns an ACK again.

Figure 5.2.4: READ mode of 2-wire interface

After the target register address sent into AR1000, the master-receiver then re-initiates a start condition with the 7-bit 2-wire-mode slave address, but followed with a READ bit (R/$\bar{W}$="1" which means this is a READ process), and the slave-transmitter returns an ACK. Then master-receiver sends CLOCK signal into slave-transmitter, and slave-transmitter outputs associated bit data at DATA pin. Master should send ACK at the end of each byte data. After the two-byte data transmitted completely, the READ mode could be terminated by a STOP condition or a NACK from the master-receiver.

The whole READ ONE REGISTER process could be designed as follows:

1. Master (Host processor) initiates a START condition.
2. Master writes the device address of the slave (AR1000), and then followed a WRITE bit. Slave sends back an ACK.
3. Master writes the register address of AR1000. Slave sends back an ACK.
4. Master re-initiates a start condition.
5. Master writes the device address of the slave (AR1000) again, and then followed a READ bit. Slave sends back an ACK.
6. Master sends CLOCK signal into slave, and slave outputs associated bit data at DATA pin. Master sends ACK at the end of each byte data.
7. After 2 bytes data read from slave, master sends a STOP condition to end the read procedure.

Conjunctive Read/ Write Registers on AR1000

AR1000 also allows conjunctive register read/write through the 2-wire interface. Once a write or read process is started, the first register address is fed into AR1000. After 2-byte data transferred, the internal register address of AR1000 will automatically accumulated by 1. If the master does not send a STOP condition, the write/read process could be continued for further data transfer. The conjunctive R/W process would be terminated when master sends a STOP condition to slave. Slave could not terminate the R/W process itself. If the register address reaches the last one, then the address will automatically get back to the first one in the next transfer (wrap-around). The *LAST ADDRESS* is different from READ to WRITE process, and different from version D to version E. Please notice that the register of AR1000 is 16-bit long, thus 2-byte data transfer is needed to complete one register's read/write process.

Figure 5.2.5 shows a conjunctive READ process of AR1000. Figure 5.2.6 shows a single READ/WRITE process of 2-wire interface. Figure 5.2.7 shows the timing parameters of 2-wire interface in READ/WRITE mode. The associated timing spec is shown in table 5.2.1.

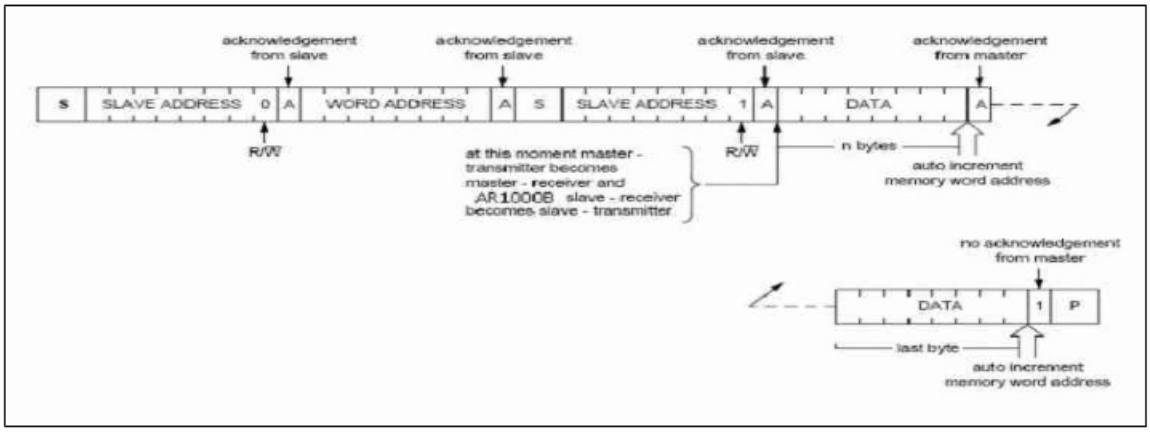


Figure 5.2.5: Conjunctive READ mode

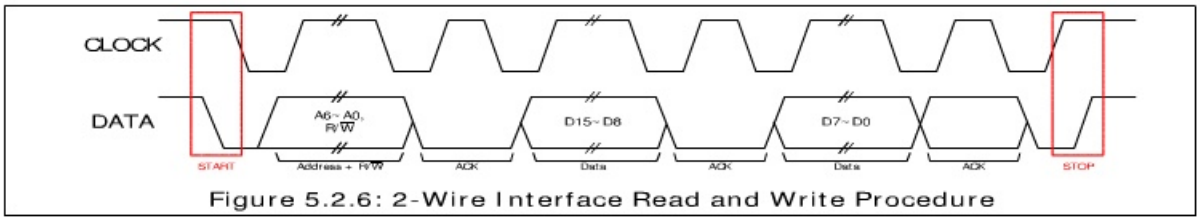


Figure 5.2.6: 2-Wire Interface Read and Write Procedure

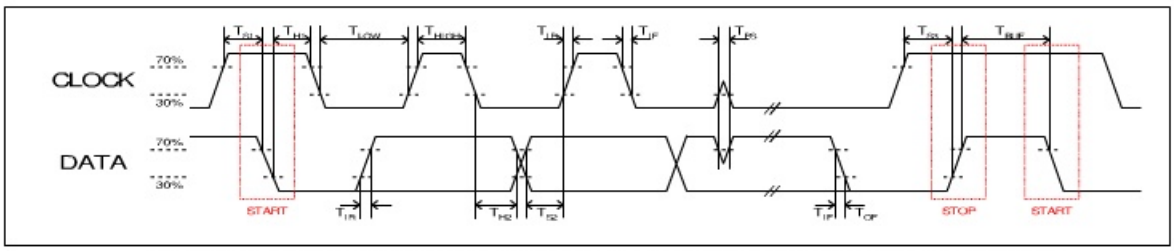


Figure 5.2.7: 2-Wire Interface Read and Write Timing Parameters

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		400	KHz
T_{S1}	CLOCK Input to DATA N-edge Setup time (START)	600			ns
T_{H1}	CLOCK Input to DATA N-edge Hold time (START)	600			ns
T_{S2}	DATA Input to CLOCK P-edge Setup time	100			ns
T_{H2}	DATA Input to CLOCK N-edge Hold time	0		900	ns
T_{S3}	CLOCK Input to DATA P-edge Setup time (STOP)	600			ns
T_{BUF}	STOP to START time	1300			ns
T_{OF}	DATA Output Fall time	20		250	ns
T_{IR}	DATA Input & CLOCK Rise time	20		300	ns
T_{IF}	DATA Input & CLOCK Fall time	20		300	ns
T_{HIGH}	CLOCK HIGH duration	600			ns
T_{LOW}	CLOCK LOW duration	1300			ns
T_{PS}	Input Filter Pulse Suppression			50	ns

Table 5.2.1: Timing parameter specs of 2-wire interface

6 Pseudo code

1. Tune

(1) Set hmute Bit
(2) Clear TUNE Bit
(3) Clear SEEK Bit
(4) Set BAND/SPACE/CHAN Bits
(5) Enable TUNE Bit
(6) Wait STC flag (Seek/Tune Complete, in "Status" register)
(7) Clear hmute Bit
(8) Update Functions (optional)

2. Tune with Auto Hi/ Lo

(1) Set hmute Bit
(2) Clear TUNE Bit
(3) Clear SEEK Bit
(4) Set BAND/SPACE/CHAN Bits
(5) Read Low-side LO Injection

1. Set R11 (clear D15, clear D0/D2)
2. Enable TUNE Bit
3. Wait STC flag (Seek/Tune Complete, in "Status" register)
4. Get RSSI (RSSI1)
5. Clear TUNE Bit

(6) Read High-side LO Injection

1. Set R11(set D15, set D0/D2)
2. Enable TUNE Bit
3. Wait STC flag (Seek/Tune Complete, in "Status" register)
4. Get RSSI (RSSI2)
5. Clear TUNE Bit

(7) Compare Hi/Lo Side Signal Strength

1. If (RSSI1 > RSSI2) Set R11(clear D15, set D0/D2), else Set R11(set D15, clear D0/D2)

(8) Enable TUNE Bit

(9) Wait STC flag (Seek/Tune Complete, in "Status" register)
(10) Clear hmute Bit
(11) Update Functions (optional)

3. Seek

(1) Set hmute Bit
(2) Clear TUNE Bit
(3) Set CHAN Bits
(4) Clear SEEK Bit
(5) Set SEEKUP/SPACE/BAND/SEEKTH Bits
(6) Enable SEEK Bit
(7) Wait STC flag (Seek/Tune Complete, in "Status" register)
(8) Clear hmute Bit
(9) Update Functions (optional, but remember to update CHAN with the seek result in READCHAN before next seek)

4. Seek with Auto Hi/ Lo

(1) Set hmute Bit
(2) Clear TUNE Bit
(3) Set CHAN Bits
(4) Clear SEEK Bit
(5) Set SEEKUP/SPACE/BAND/SEEKTH Bits
(6) Enable SEEK Bit
(7) Wait STC flag (Seek/Tune Complete, in "Status" register)
(8) If SF is not set, tune with auto Hi/Lo (using the seek result in READCHAN as CHAN)
(9) Clear hmute Bit
(10) Update Functions (optional)

5. Update

(1) Get RSSI Bits for signal strength
(10) Get IF_CNT Bits for IF counter (ideal IF_CNT should be 250 ± 27)
(11) Get READCHAN Bits for current tuning channel
(12) Get SF Bit for Seek Failed
(13) Get ST Bit for Stereo indicator

6. Power Down (Standby mode)

(1) Set ENABLE bit=0 (in register R0)

**Note: Being set ENABLE to 0, AR1000 will switch to standby mode with only very few current consumption. Setting ENABLE to 1 can wakeup AR1000 again. After ENABLE is set to 1, users must wait for STC flag before tunning to the wanted frequency.

AR1000F Register Table

Address	Alias	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H	R0									xo_en							ENABLE
01H	R1			rds_en							rds_int_en	stc_int_en	deemp	mono	smute	hmute	
02H	R2							TUNE	CHAN<8:0>								
03H	R3	SEEKUP	SEEK	SPACE	BAND<1:0>			VOLUME<3:0>			SEEKTH<6:0>						
04H	R4																
05H	R5																
06H	R6																
07H	R7																
08H	R8																
09H	R9																
0AH	R10													seek_wrap			
0BH	R11	hilo_side													hiloctrl_b1		hiloctrl_b2
0CH	R12																
0DH	R13											GPIO3<1:0>		GPIO2<1:0>		GPIO1<1:0>	
0EH	R14	VOLUME2<3:0>															
0FH	R15											rds_sta_en	rds_mecc<1:0>				rds_ctrl
10H	R16																
11H	R17																
12H	RSSI	RSSI<6:0>							IF_CNT<8:0>								
13H	STATUS	READCHAN<8:0>									RDSR	STC	SF	ST			
14H	RBS	RBS1<1:0>		RBS2<1:0>		RBS3<1:0>		RBS4<1:0>									
15H	RDS1	RDS1<15:0>															
16H	RDS2	RDS2<15:0>															
17H	RDS3	RDS3<15:0>															
18H	RDS4	RDS4<15:0>															
19H	RDS5	rds_dsc<15:0>															
1AH	RDS6	rds_cfc<15:0>															
1BH	DEVID	VERSION<3:0>				MFID<11:0>											
1CH	CHIPID	CHIPNO<15:0>															
																	2007/4/13

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01H	R1			rds_en							rds_int_en	stc_int_en	deemp	mono	smute	hmute	
02H	R2							TUNE	CHAN<8:0>								
03H	R3	SEEKUP	SEEK	SPACE	BAND<1:0>		VOLUME<3:0>				SEEKTH<6:0>						
04H	R4																
05H	R5																
06H	R6																
07H	R7																
08H	R8																
09H	R9																
0AH	R10													seek_wrap			
0BH	R11	hilo_side													hiloctrl_b1		hiloctrl_b2
0CH	R12																
0DH	R13											GPIO3<1:0>		GPIO2<1:0>		GPIO1<1:0>	
0EH	R14	VOLUME2<3:0>															
0FH	R15											rds_sta_en	rds_mecc<1:0>				rds_ctrl
10H	R16																
11H	R17																
12H	RSSI	RSSI<6:0>							IF_CNT<8:0>								
13H	STATUS	READCHAN<8:0>									RDSR	STC	SF	ST			
14H	RBS	RBS1<1:0>		RBS2<1:0>		RBS3<1:0>		RBS4<1:0>									
15H	RDS1	RDS1<15:0>															
16H	RDS2	RDS2<15:0>															
17H	RDS3	RDS3<15:0>															
18H	RDS4	RDS4<15:0>															
19H	RDS5	rds_dsc<15:0>															
1AH	RDS6	rds_dfc<15:0>															
1BH	DEVID	VERSION<3:0>					MFID<11:0>										
1CH	CHIPID	CHIPNO<15:0>															
																	2007/4/13