Spartan-3 FPGA Family: Introduction and Ordering Information

DS099-1 (v1.2) December 24, 2003

Advance Product Specification

Introduction

The Spartan™-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to five million system gates, as shown in Table 1.

The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from state-of-the-art Virtex™-II technology. These Spartan-3 enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Revolutionary 90-nanometer process technology
- Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
  - Densities as high as 74,880 logic cells
  - 326 MHz system clock rate
  - Three power rails: for core (1.2V), I/Os (1.2V to 3.3V), and auxiliary purposes (2.5V)
- SelectIO™ signaling
  - Up to 784 I/O pins
  - 622 Mb/s data transfer rate per I/O
  - Seventeen single-ended signal standards
  - Seven differential signal standards including LVDS
  - Termination by Digitally Controlled Impedance
  - Signal swing ranging from 1.14V to 3.45V
  - Double Data Rate (DDR) support
- Logic resources
  - Abundant logic cells with shift register capability
  - Wide multiplexers
  - Fast look-ahead carry logic
  - Dedicated 18 x 18 multipliers
  - JTAG logic compatible with IEEE 1149.1/1532 specifications
- SelectRAM™ hierarchical memory
  - Up to 1,872 Kbits of total block RAM
  - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by Xilinx ISE development system
  - Synthesis, mapping, placement and routing
- MicroBlaze processor, PCI, and other cores

Table 1: **Summary of Spartan-3 FPGA Attributes**

Device	System Gates	Logic Cells	CLB Array (One CLB = Four Slices)			Distributed RAM (bits[1])	Block RAM (bits[1])	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	712	312
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	784	344

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.

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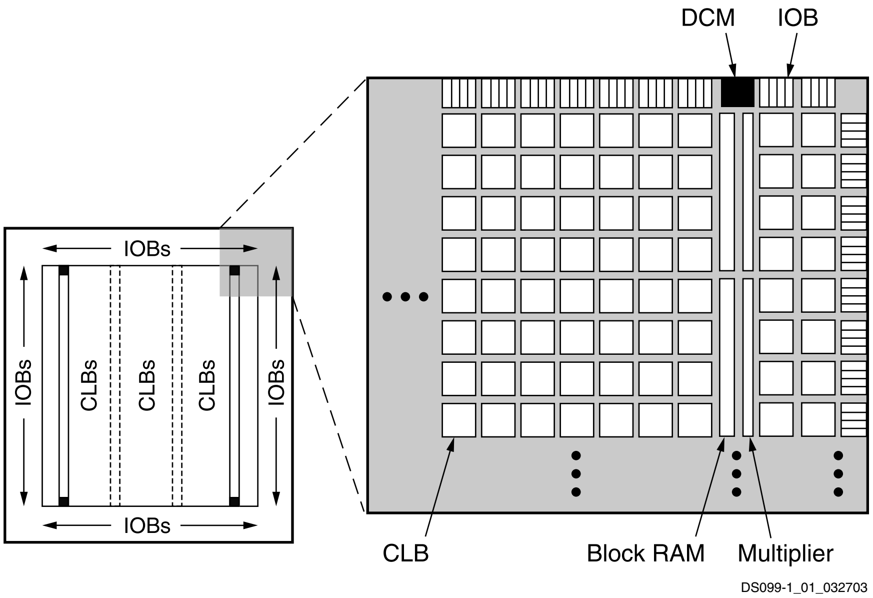
Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

- Configurable Logic Blocks (CLBs) contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Input/Output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-four different signal standards, including seven high-performance differential standards, are available as shown in Table 2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
- Block RAM provides data storage in the form of 18-Kbit dual-port blocks.
- Multiplier blocks accept two 18-bit binary numbers as inputs and calculate the product.
- Digital Clock Manager (DCM) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure 1. A ring of IOBs surrounds a regular array of CLBs. The XC3S50 has a single column of block RAM embedded in the array. Those devices ranging from the XC3S200 to the XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 devices have four RAM columns. Each column is made up of several 18K-bit RAM blocks; each block is associated with a dedicated multiplier. The DCMs are positioned at the ends of the outer block RAM columns.

The Spartan-3 family features a rich network of traces and switches that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The two additional block RAM columns of the XC3S4000 and XC3S5000 devices are shown with dashed lines. The XC3S50 has only the block RAM column on the far left.

Figure 1: **Spartan-3 Family Architecture**

Configuration

Spartan-3 FPGAs are programmed by loading configuration data into robust static memory cells that collectively control all functional elements and routing resources. Before powering on the FPGA, configuration data is stored externally in a PROM or some other nonvolatile medium either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes: Master Parallel, Slave Parallel, Master Serial, Slave Serial and Boundary Scan (JTAG). The Master and Slave Parallel modes use an 8-bit wide SelectMAP™ port.

The recommended memory for storing the configuration data is the low-cost Xilinx Platform Flash PROM family, which includes the XCF00S PROMs for serial configuration and the higher density XCF00P PROMs for parallel or serial configuration.

I/O Capabilities

The SelectIO feature of Spartan-3 devices supports 17 single-ended standards and seven differential standards as listed in Table 2. Many standards support the DCI feature, which uses integrated terminations to eliminate unwanted signal reflections. Table 3 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination.

Table 2: **Signal Standards Supported by the Spartan-3 Family**

Standard Category	Description	V_{CCO} (V)	Class	Symbol	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A	SSTL18_I	Yes
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT	Lightning Data Transport (HyperTransport™)	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
			Ultra	ULVDS_25	No
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No

Table 3: **Spartan-3 I/O Chart**

Device	Available User I/Os and Differential (Diff) I/O Pairs																	
	VQ100		**TQ144**		**PQ208**		**FT256**		**FG320**		**FG456**		**FG676**		**FG900**		**FG1156**	
	User	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50	63	29	97	46	124	56	-	-	-	-	-	-	-	-	-	-	-	-
XC3S200	63	29	97	46	141	62	173	76	-	-	-	-	-	-	-	-	-	-
XC3S400	-	-	97	46	141	62	173	76	221	100	264	116	-	-	-	-	-	-
XC3S1000	-	-	-	-	-	-	173	76	221	100	333	149	391	175	-	-	-	-
XC3S1500	-	-	-	-	-	-	-	-	221	100	333	149	487	221	-	-	-	-
XC3S2000	-	-	-	-	-	-	-	-	-	-	-	-	489	221	565	270	-	-
XC3S4000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	633	300	712	312
XC3S5000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	633	300	784	344

Notes:

1. All device options listed in a given package column are pin-compatible.

Product Ordering and Availability

Table 4 shows all valid device ordering combinations of device density, speed grade, package, and temperature range parameters for the Spartan-3 family as well as the availability status of those combinations.

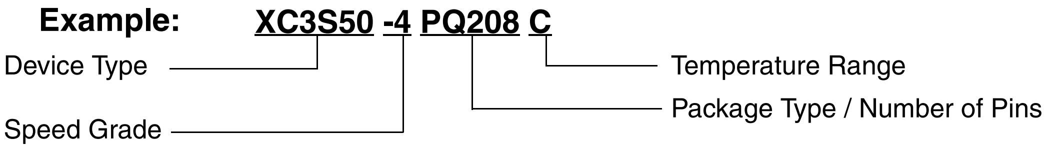
Table 4: **Spartan-3 Device Availability**

Package Type(1):	**VQFP**	**TQFP**	**PQFP**	**FTBGA**	**FBGA**				
Code:	**VQ100**	**TQ144**	**PQ208**	**FT256**	**FG320**	**FG456**	**FG676**	**FG900**	**FG1156**
Device									
XC3S50	(C, I)	(C, I)	(C, I)	-	-	-	-	-	-
XC3S200	(C, I)	(C, I)	(C, I)	(C, I)	-	-	-	-	-
XC3S400	-	(C, I)	(C, I)	(C, I)	(C, I)	(C, I)	-	-	-
XC3S1000	-	-	-	(C, I)	(C, I)	(C, I)	(C, I)	-	-
XC3S1500	-	-	-	-	(C, I)	(C, I)	(C, I)	-	-
XC3S2000	-	-	-	-	-	-	(C, I)	(C, I)	-
XC3S4000	-	-	-	-	-	-	-	(C, I)	(C, I)
XC3S5000	-	-	-	-	-	-	-	(C, I)	(C, I)

Notes:

1. Package types are explained in **Ordering Information**, page 5.
2. Commercial devices are offered in the -4 and -5 speed grades; industrial devices are only in the -4 speed grade.
3. C = Commercial, T_J = 0° to +85° C; I = Industrial, T_J = –40° C to +100° C.
4. Parentheses indicate that a given device is not yet released to production. Contact your local sales office for availability information.

Ordering Information


Example:
XC3S50 -4 PQ208 C
Device Type
Speed Grade
Temperature Range
Package Type / Number of Pins

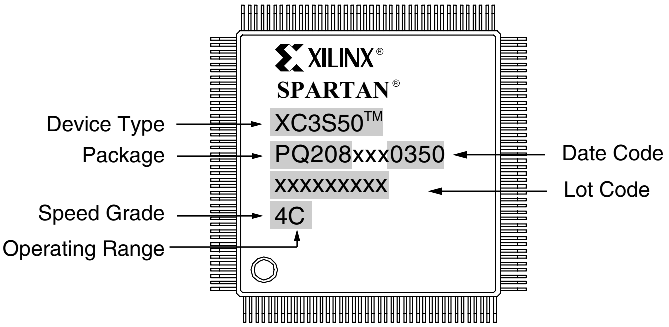
Device
XC3S50
XC3S200
XC3S400
XC3S1000
XC3S1500
XC3S2000
XC3S4000
XC3S5000

Speed Grade	
-4	Standard Performance
-5	High Performance

Package Type / Number of Pins	
VQ100	100-pin Very Thin Quad Flat Pack (VQFP)
TQ144	144-pin Thin Quad Flat Pack (TQFP)
PQ208	208-pin Plastic Quad Flat Pack (PQFP)
FT256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)
FG320	320-ball Fine-Pitch Ball Grid Array (FBGA)
FG456	456-ball Fine-Pitch Ball Grid Array (FBGA)
FG676	676-ball Fine-Pitch Ball Grid Array (FBGA)
FG900	900-ball Fine-Pitch Ball Grid Array (FBGA)
FG1156	1156-ball Fine-Pitch Ball Grid Array (FBGA)

Temperature Range (T_J)	
C	Commercial (0°C to 85°C)
I	Industrial (–40°C to 100°C)

Package Marking


XILINX®
SPARTAN®
XC3S50™
PQ208xxx0350
xxxxxxxxx
4C
Device Type
Package
Speed Grade
Operating Range
Date Code
Lot Code

ds099-1_02_122403

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release.
04/24/03	1.1	Updated block RAM, DCM, and multiplier counts for the XC3S50.
12/24/03	1.2	Added the FG320 package.

The Spartan-3 Family Data Sheet

DS099-1, ***Spartan-3 FPGA Family: Introduction and Ordering Information*** (Module 1)

DS099-2, ***Spartan-3 FPGA Family: Functional Description*** (Module 2)

DS099-3, ***Spartan-3 FPGA Family: DC and Switching Characteristics*** (Module 3)

DS099-4, ***Spartan-3 FPGA Family: Pinout Descriptions*** (Module 4)