XAPP751 (v1.0) March 4, 2004

Setting the Correct Differential Bias Voltages for Spartan-3 FPGAs

Summary

This application note describes how to set the voltage bias circuitry within a Spartan-3™ I/O bank to guarantee the differential output voltages specified in the Spartan-3 data sheet. These special settings are required until new default settings are included in a future Xilinx ISE development software release.

Introduction

Each Spartan-3 I/O bank contains a special voltage bias circuit that controls the differential output voltage and the common-mode voltage for differential outputs. Memory cells loaded during FPGA configuration control the bias circuitry, and the default memory settings are included automatically in the generated FPGA programming file.

Each specific version of the Xilinx ISE development software controls the default settings. All current versions of the ISE software produce the incorrect settings for the differential bias circuitry.

Until corrected in a future version of ISE, this application note describes how to override the default settings to guarantee the differential output levels described in the Spartan-3 data sheet.

Setting the Differential Bias Circuitry

BLVDS_25 and LVPECL_25 differential outputs do not require special settings. However, to guarantee the differential output voltages for the other differential standards described in the Spartan-3 data sheet, use the special bitstream option settings provided below. The settings shown in Figure 1 set the proper levels for the LVDS_25, LVDS_25_DCI, LVDSEXT_25, LVDSEXT_25_DCI, and RSDS_25 I/O standards. The LDT_25 and ULVDS_25 I/O standards require different bitstream option settings that are not yet available.

These settings overwrite the default values generated by the Xilinx ISE software.

```
-g lvdsbias_opt0_x:1
-g lvdsbias_opt1_x:1
-g lvdsbias_opt2_x:0
-g lvdsbias_opt3_x:0
-g lvdsbias_opt4_x:0
-g lvdsbias_opt5_x:0
-g lvdsbias_opt6_x:0
-g lvdsbias_opt7_x:0
-g lvdsbias_opt8_x:1
-g lvdsbias_opt9_x:0
-g lvdsbias_opt11_x:0
-g lvdsbias_opt12_x:1
```

Figure 1: **Special Bitstream Generator Settings to Guarantee the Differential Output Voltages for LVDS_25, LVDS_25_DCI, LVDSEXT_25, and RSDS_25 Standards**

To set the proper output levels for a specific bank, insert the following additional bitstream generation options. In Figure 1, **x** is an I/O bank number ranging from 0 to 7, inclusive. No special settings are required for **lvdsbias_opt10**. Despite the name “lvdsbias”, these settings apply to all differential output settings.

If differential outputs are required in multiple I/O banks, then the options must be set for each bank with differential outputs. However, setting the options for a bank that does not have differential outputs might cause the bitstream generation software to fail.

There are two methods to generate a programming file:

1. With the BitGen command-line function
2. Within the ISE Project Navigator

BitGen Command

If generating the FPGA configuration bitstream using the BitGen command-line function, add the special option settings shown in Figure 1. Due to the complexity of the settings, create a batch file or use the BitGen command file option described below.

For example, include all the bias voltage settings for all the I/O banks in a single BitGen command file. The name of the command file is user defined, but this example uses the **bias_opt.txt** file provided with this application note. Modify **bias_opt.txt** as appropriate for the specific application. Remember only specify the bias voltage settings for those I/O banks that contain differential output drivers. Then, instead of a complicated command line, merely run the following command:

```
bitgen -f bias_opt.txt <other_BitGen_arguments>
```

ISE Project Navigator

If using the ISE Project Navigator, position the cursor over the **Generate Programming File** item in the **Processes for Current Source** panel and right-click the mouse, as shown in Figure 2.

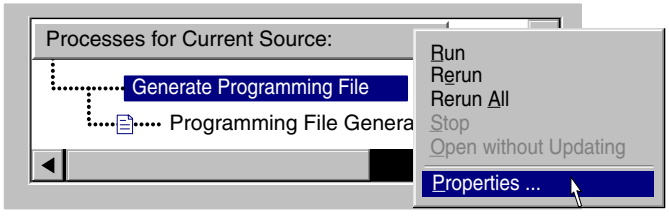

Figure 2: **Setting Bitstream Generator (BitGen) Options in Project Navigator**

As shown in Figure 3, click the **General Options** tab and enter the special BitGen settings from Figure 1 in the **Other Bitgen Command Line Options** text box. Again, if there are differential outputs in multiple I/O banks, enter a complete set of option settings per each bank. Unfortunately, the command file method used in the “BitGen Command” section is not allowed here. When finished, click **OK**. Be sure to rerun the **Generate Programming File** process.

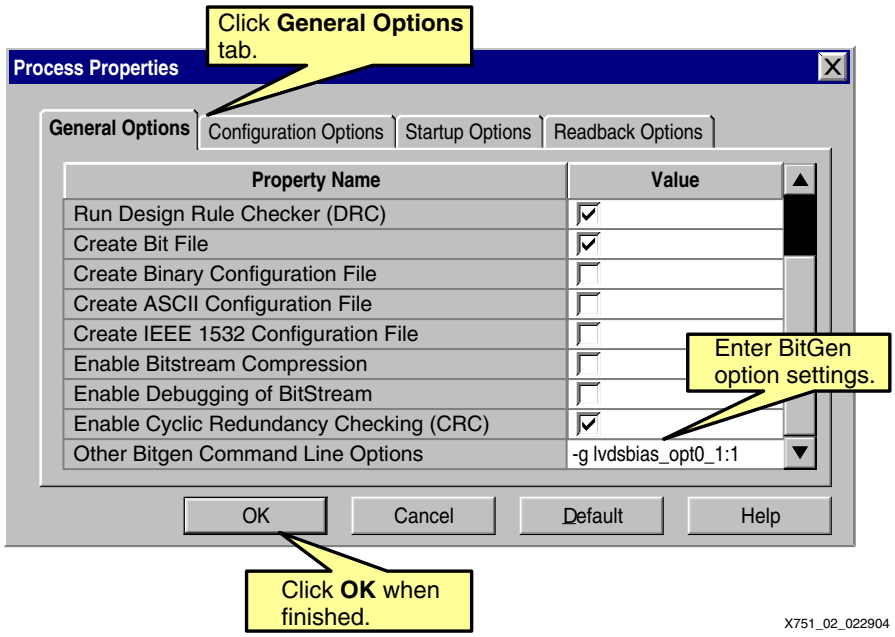

Figure 3: **BitGen Option Settings in ISE Project Navigator**

Related File

The example BitGen command file (`bias_opt.txt`) is located at the following location. This file currently supports the LVDS_25, LVDS_25_DCI, LVDSEXT_25, LVDSEXT_25_DCI, and RSDS_25 output standards.
http://www.xilinx.com/bvdocs/appnotes/xapp751.zip

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/04/04	1.0	Initial release.