XAPP259 (v1.0) April 28, 2003

System Interface Timing Parameters

Author: Sean Koontz, Maria George, and Markus Adhiwiyogo

Summary

This application note defines timing parameters required for the timing analysis of source synchronous and system synchronous applications. The parameters discussed in this application note are listed in Module 3 of the Virtex™-II and Virtex-II Pro™ data sheets. This application note explains the DCM clock phase accuracy parameters, system-synchronous pin-to-pin setup/hold with DCM parameters (T_{PSDCM} and T_{PHDCM}), and all source-synchronous parameters. Memory interfaces and the XGMII interface analyses are provided as examples.

Introduction

The fundamental modules in any system interface are the transmitter and receiver. A timing analysis is required to determine the performance of these modules. The timing parameters required for analysis are defined in the following sections. This is followed by an analysis of memory interfaces for transmitter (write to memory) and receiver (read from memory) modules, and the XGMII interface.

DCM Phase Error

Almost all FPGA designs use the Digital Clock Manager (DCM) for clock de-skew and/or clock synthesis. This section discusses the phase error introduced by the DCMs.

Two parameters contribute to DCM output phase error; CLKOUT_PHASE and CLKIN_CLKFB_PHASE. The existing software (ISE 5.2i) timing analysis does not use these timing parameters. Therefore, they must be manually factored into the capture window timing analysis.

CLKOUT_PHASE

CLKOUT_PHASE specifies the phase relationship between the DCM outputs of the same DCM. This parameter is specified as ±140 ps. The ± only indicates whether one output is ahead of or behind another output. The magnitude (280 ps) must not be used in a calculation because the phase difference between any two outputs of a DCM can only be a maximum of 140 ps. This is the case as long as the DCM is locked. CLKOUT_PHASE is relevant when any DCM output other than the feedback clock (CLK0 or CLK2X) is used in the design.

CLKIN_CLKFB_PHASE

CLKIN_CLKFB_PHASE defines the amount of phase offset between the clock input and the feedback input of the same DCM. Although this parameter is specified as ±50 ps the magnitude (100 ps) must not be used in timing analysis for designs using a single DCM. The maximum phase offset between the clock input and clock feedback input of a DCM can be either +50 ps or –50 ps (a tap delay) at any time and stays at that value as long as the DCM is locked. All the DCM parameters in the data sheet are specified at the inputs and outputs of the DCM, including this parameter. In the source synchronous data sheet all the DCM related parameters are specified at an IOB flip-flop.

Circuits with associated timing diagrams using DCMs are described in the Appendix. Each of these circuits shows a possible use of one or two DCMs to clock two flip-flops. Each case describes the worst case value of the clock phase difference.

Setup/Hold Adjustment for Mixed I/O Standards

Setup/Hold times must be adjusted whenever data and clock use different (mixed) I/O standards. The software version ISE 5.1i calculates setup/hold times, and clock-to-out when a different I/O standard other than the default (LVTTL) is used. Earlier versions need to have the adjustment calculated manually. The adjustment for setup/hold times is determined by the following equation.

Setup/Hold Adjustment = Data Path Delay Adjustment – Clock Path Delay Adjustment

A longer clock delay reduces setup time and increases hold time by the same amount, thus shifting the capture window to the right. The capture window does not increase. A longer data delay increases setup time and reduces hold time by the same amount, thus shifting the capture window to the left. The capture window does not increase.

For any input clock buffer using an I/O standard slower than the LVTTL input clock buffer, setup time is reduced by the I/O standard input adjustment. The example in Figure 1 illustrates this point.

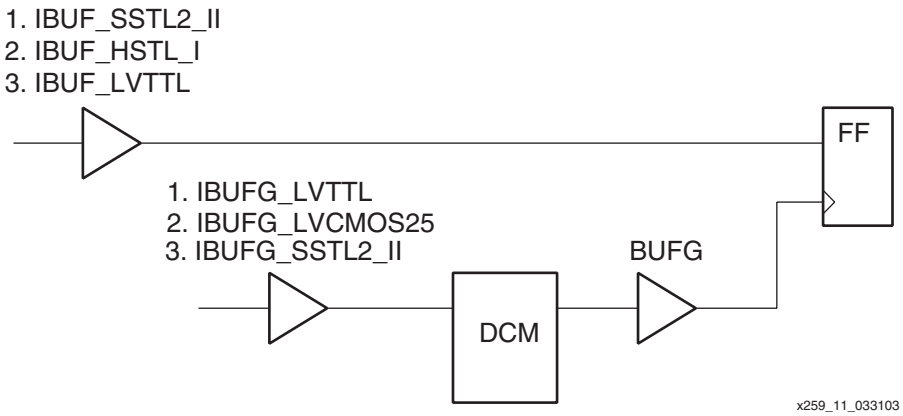


Figure 1: **Setup/Hold I/O Standard Adjustment**

Case 1: Data input buffer SSTL2_II and clock input buffer LVTTL

Setup/Hold Adjustment = TISSTL2_II – 0 = 0.42 ns

The setup time increases by 0.42ns and the hold time is reduced by 0.42 ns

Case 2: Data input buffer HSTL_I and clock input buffer LVCMOS25

Setup/Hold Adjustment = TIHSTL_I – TILVCMOS25 = 0.42 ns – 0.11 ns = 0.31 ns

The setup time increases by 0.31ns and the hold time is reduced by 0.31 ns

Case 3: Data input buffer LVTTL and clock input buffer SSTL2_II

Setup/Hold Adjustment = TILVTTL – TISSTL2_II = 0 – 0.42 ns = –0.42 ns

The setup time reduces by 0.42 ns and the hold time is increased by 0.42 ns

Jitter

This section describes the jitter introduced by the DCM due to the periodic selection of discrete tap delays. If the data is clocked by CLK0 of the DCM at the DDR IOBs, then CLKOUT_PER_JITT_0, specified as ±100 ps, must be used in the timing calculations. In this case the worst-case jitter magnitude is 100 x 2 = 200 ps.

Package Skew

The package skew values ($T_{PKGSKEW}$) represent the layout netlists worst-case skew between any two balls of the package. These values are measured by extracting the trace lengths from the package layout netlists. The dielectric material is characterized using time-domain reflectometry, and its variation is specified in the source-synchronous data sheet.

The values listed in the source-synchronous data sheet represent the worst-case value for all pins and the slowest dielectric. Individual trace lengths for each pin, in all flip-chip packages, are available in a separate set of spreadsheets. These Virtex-II and Virtex-II Pro "Package Flight Time" data spreadsheets are available on the Xilinx web site by entering the SPICE Suite at http://www.xilinx.com/support/software/spice/spice-request.htm. Once registered, access the SPICE models, simulation kits, characterization reports, and package flight time data. Flight times for each pin can then be calculated using the dielectric characteristic constants (time/distance) specified in the spreadsheets.

Clock Tree Skew

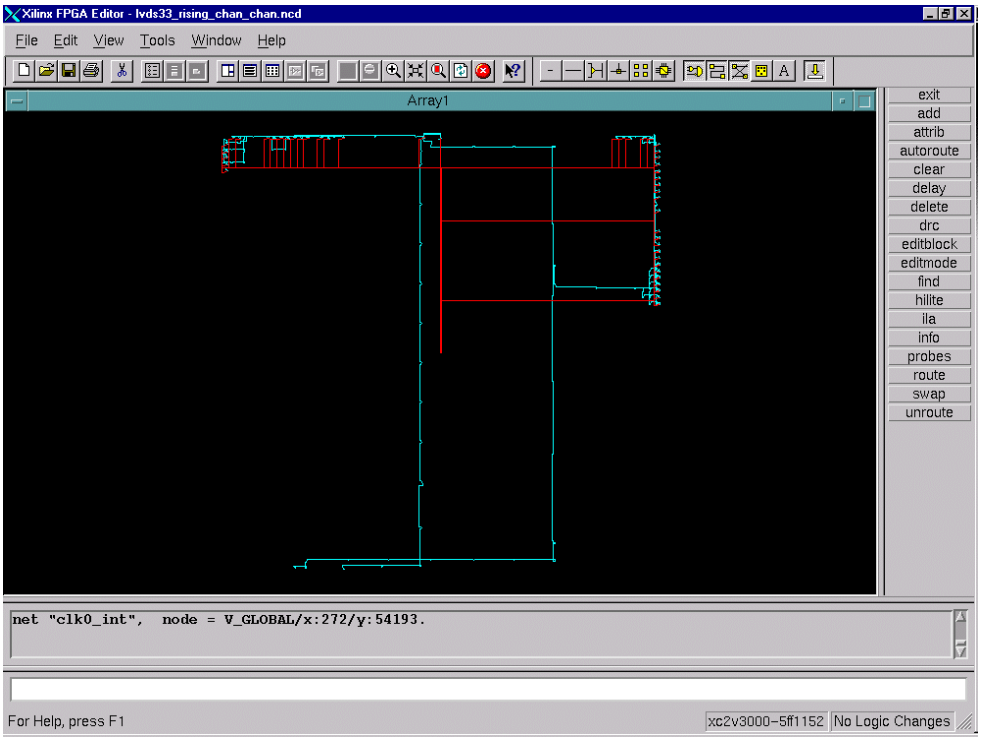
The global clock tree skew values (T_{CKSKEW}) represent the worst-case clock-tree skew observable between IOB sequential elements (input flip-flops). The test patterns used to measure global clock tree skew use a single BUFG, DDR output registers configured for clock forwarding, and LVDS drivers. See the Virtex-II/Virtex-II Pro user guides, Chapter 2, "Using DDR I/O" for details on this circuit.

The skew is the measured output delay difference between the closest pin (with corresponding IOB flip-flops) to the clock source (BUFG) and the farthest pin (with corresponding IOB flip-flops) from the clock source (BUFG). This is the worst case for all IOBs. Significantly less clock-tree skew exists for I/O registers close to each other and fed by identical or adjacent clock-tree branches.

Experiments to determine the behavior of the clock-tree skew across each bank have produced the following results:

1. Top and bottom banks: The skew increases logarithmically from the center of the die to the corner of the die. This is reported in the source-synchronous data sheet as the maximum possible clock tree skew.
2. Left and right banks: The function used to represent the skew is a periodic wave with very little variation.

For source-synchronous designs, it is recommended to place all the I/Os associated with any one bus (including the forwarded clock) close to each other and to use either the left or right banks to prevent excessive channel-to-channel clock-tree skew. Figure 2 shows a typical Virtex-II clock tree.



x259_12_033103

Figure 2: **Clock Tree**

DCM Deskew Adjust

Attribute Name	Element Controlled	Default Setting
DESKEW_ADJUST	DCM feedback delay element	System Synchronous

Example UCF Syntax

```
INST DEMO DESKEW_ADJUST = SOURCE_SYNCHRONOUS;
```

The DESKEW_ADJUST attribute sets the value for a configurable, variable-tap delay element to control the amount of delay added to the DCM feedback path (Figure 3). This delay element allows adjustment of the effective clock delay between the clock source and CLK0 to guarantee non-positive hold times of any flip-flop in the device. Adding more delay to the DCM feedback path decreases the effective delay of the actual clock path from the FPGA clock input pin to the clock input of any flip-flop. Decreasing the clock delay increases the setup time represented in the input flip-flop, and reduces any positive hold times required. The clock path delay includes the delay through the IBUFG, route, DCM, BUFG, clock-tree, to the destination flip-flop. If the feedback delay equals the clock-path delay, the effective clock-path delay will be zero.

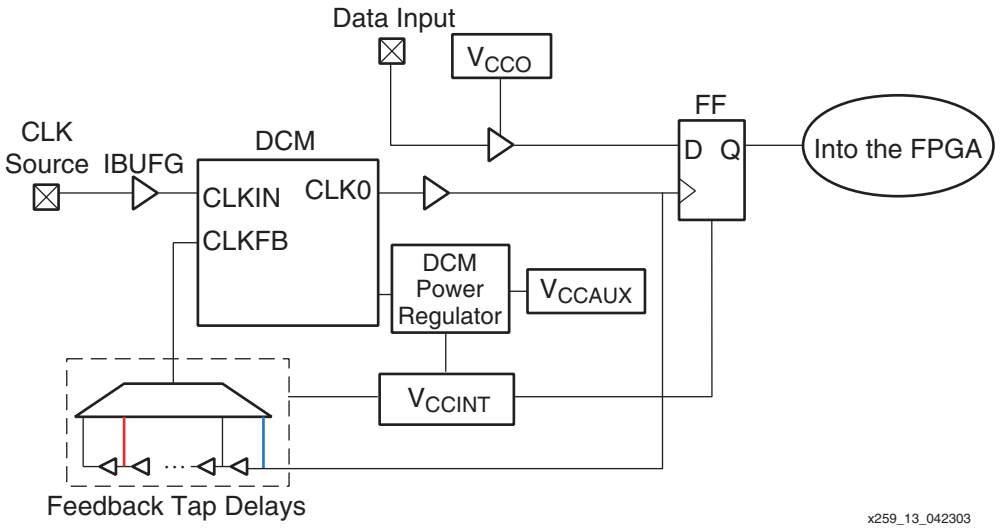


Figure 3: **DCM and Variable-Tap Delay Element**

System-Synchronous Setting (Default)

By default the feedback delay is set to system-synchronous. The primary timing requirements for a system-synchronous system are non-positive hold times (or minimally positive hold times) and minimal clock-to-out and setup times. Faster clock-to-out and setup times allow shorter system clock periods. Ideally, the purpose of a DLL is to zero-out the clock delay to produce faster clock-to-out and hold times. The system synchronous setting (default) for DESKEW_ADJUST configures the feedback delay element to add approximately 1.5 ns delay to the feedback path. As shown in Figure 3, the feedback path includes tap delays in the default setting (red line). The pin-to-pin timing parameters (with DCM) on the Virtex-II/Virtex-II Pro data sheets (Module 3) reflects the setup/hold, and clock-to-out times when the DCM is in "system-synchronous" mode.

Source-Synchronous Setting

When DESKEW_ADJUST is set to source-synchronous, the DCM feedback delay element is set to zero. As shown in Figure 3, in source-synchronous mode, the DCM clock feedback bypasses the tap delays in the DCM feedback delay element (blue line). This results in am extra clock path delay of approximately 1.5 ns (depending on the array size), a positive hold time, and larger clock-to-outs. However, in source-synchronous (clock-forwarded) interfaces this is not a problem. The sampling error is now minimized since any possible clock delay variations (due to V_{CCINT} variation) through the feedback tap delays is removed. The source-synchronous switching characteristics section in the Virtex-II/Virtex-II Pro data sheets (Module 3) reflect the various timing parameters for the source-synchronous design when the DCM is in "source-synchronous" mode.

Duty-Cycle Distortion

The source-synchronous data sheet parameters (T_{DCD_CLK0}/T_{DCD_CLK180}) specify the duty-cycle distortion of the clock at the output of the IOB DDR flip-flop; accounting for DCM, BUFG, global clock tree, and IOB DDR flip-flop contributions to the overall duty-cycle distortion. T_{DCD_CLK0} and T_{DCD_CLK180} represent the worst-case duty-cycle distortion observable on the device pads. These values are measured using LVDS drivers. The LVDS drivers are found to contribute negligible amounts of duty-cycle distortion with respect to the rest of the circuit. For cases where other I/O standards are used, IBIS simulation can be used to predict duty-cycle distortion contributed by specific drivers and PCB/loading conditions (asymmetrical rise and fall times). Any additional duty-cycle distortion found through simulation should be added to T_{DCD_CLK0} and T_{DCD_CLK180}.

T_{DCD_CLK0}

This is the worst-case duty-cycle distortion observed when CLK0 or any other DCM quadrature clock output (90,180, 270) is used with local inversion in the IOB to clock input or output DDR flip-flops, as shown in Figure 4, Circuit 1.

T_{DCD_CLK180}

This is the worst-case duty-cycle distortion observed when CLK0 and CLK180 (or CLK90 and CLK270) outputs of the DCM (and two BUFGs) are used to clock input or output DDR flip-flops. Shown in Figure 4, Circuit 2.

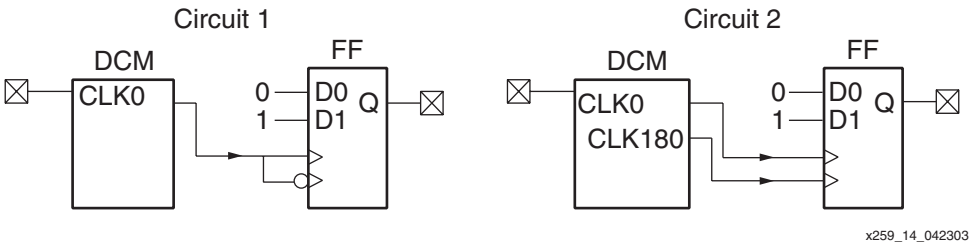


Figure 4: **Duty-Cycle Distortion**

Pin-to-Pin Setup/Hold, and Sampling Window

Setup time is the minimum time data must be available before the clock edge order to be captured (Figure 5).

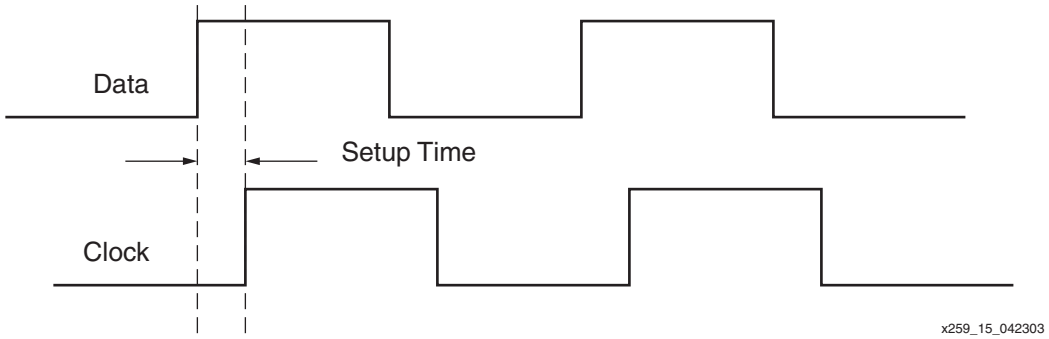


Figure 5: **Illustration of Setup Time**

Typically, setup time is a measure of the difference between the data path delay and the clock path delay. The data path is from the input pin of the device, through the input buffer, to the D input of the flip-flop (or DDR IOB input flip-flop). The clock path is from the input pin of the device, through the clock input buffer, through the global clock distribution (with or without DCM), to the clock input of the flip-flop (or DDR IOB input flip-flop).

Setup_Time = Data_Path_Delay – Clock_Path_Delay

Assuming that both data and clock signals arrive at the pins of the FPGA at the same time a positive setup time suggests that the clock signal reaches the pin of the input flip-flop before the data signal (Data_Path_Delay > Clock_Path_Delay). A negative setup time suggests that the clock signal reaches the pin of the input flip-flop after the data signal (Data_Path_Delay < Clock_Path_Delay).

Hold time is the minimum time a data-bit must remain stable after a clock-edge in order to capture that data-bit with that clock-edge (Figure 6).

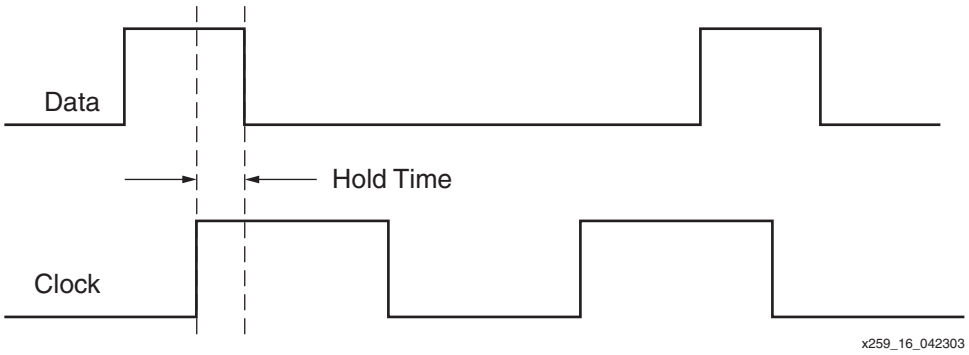


Figure 6: **Illustration of Hold Time**

Based on these definitions and the illustrations, the minimum data valid time required for a clock-edge to sample a data-bit is the sum of the setup time and hold time. This value indicates the total sampling error (or sample window) for a given device (across all pins).

Pin-to-Pin Setup/Hold Times in Virtex-II/Virtex-II Pro Devices:

T_{PSDCM}/T_{PHDCM}: System-Synchronous Mode

T_{PSSDCM}/T_{PHSDCM}: Source-Synchronous Mode

The circuit in Figure 7 is used to measure setup/hold times in Virtex-II/Virtex-II Pro devices.

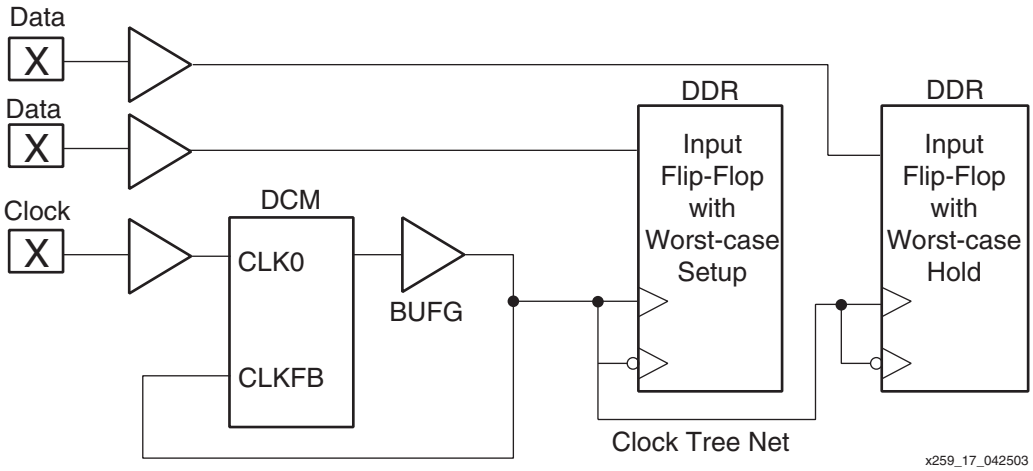


Figure 7: **System Synchronous Pin-to-Pin Setup/Hold Measurement Circuit**

System-synchronous pin-to-pin measurements are initially made on the bench over process, voltage, and temperature, using a pulse generator to provide stimulus (clock and data) and an oscilloscope to measure delay between clock and data (setup/hold). After initial measurements are made, pin-to-pin measurements are continued on a production tester using a similar test pattern. In this circuit, both data and clock signals (from the pulse generator) arrive at the pins of the FPGA at the same time. Data is then delayed (with respect to clock) until valid and stable at the output of the registers. Since the setup and hold measurements are made by measuring the average delay between the stimulus (clock and data) when Q is stable and valid (the output of the IOB registers), any jitter in the system (DCM jitter) is not captured. The average delay between the waveforms is used, when measured on an oscilloscope or production tester, in order to produce stable and consistent results. Since the average is used, any variation in the clock or data position (jitter) is not captured. System-synchronous pin-to-pin setup/hold

(T_{PSDCM}/T_{PHDCM}) are worst-case numbers guaranteed (and tested) over process, voltage, and temperature, including the following aspects of the Virtex-II/Virtex-II Pro architecture:

1. Clock-Tree Skew (worst-case)
2. Package Skew

Figure 8 illustrates the effect of the clock-path delay and data-path delay on the input clock and data signals. The 1.7 ns signifies the worst-case pin-to-pin setup time with the DCM in system-synchronous mode.

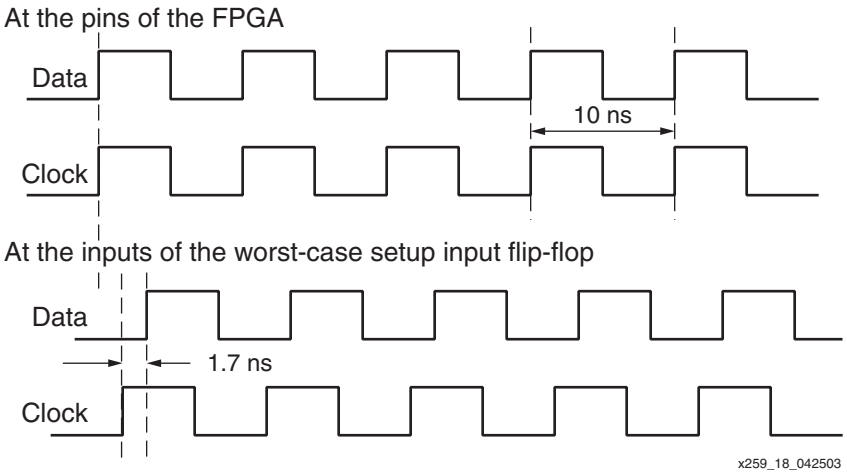


Figure 8: **Effects of Clock and Data Path Delay- System Synchronous**

Source-synchronous pin-to-pin measurements are made using a different technique; Built-in self test (BIST). This new test procedure was developed to make accurate measurements of setup/hold times and sample error. This technique uses the DCMs in the device under test (DUT) to provide stimulus (clock and data) to the setup/hold times of the input flip-flops being measured. One DCM is used (in variable phase shift mode) to phase shift data with respect to clock to create metastable events (invalid data). A state machine controls the DCMs and records the points where data is captured as valid and invalid. This effectively describes the data eye or defines the edges of the data valid window (setup plus hold). Once the "edges" of the data valid window are determined, the measurement is repeated many times (± 3 Σ) to capture the worst-case bounds due to any jitter on the stimulus. This is why jitter is included in the source-synchronous pin-to-pin specifications. Source-synchronous pin-to-pin setup/hold (T_{PSSDCM}/T_{PSHDCM}) are worst-case numbers guaranteed (and tested) over process, voltage, and temperature, including the following aspects of the Virtex-II/Virtex-II Pro architecture:

1. Clock-Tree Skew (worst-case)
2. Package Skew
3. DCM Jitter

Sample Window Parameter in Virtex-II/Virtex-II Pro Devices: T_{SAMP}

The sample window, also known as the sampling error, is the minimum data valid time required by the Virtex-II/Virtex-Pro receiver. The receiver is defined as the flip-flop, data-path, and clock network. All sources of error in these elements (variation in propagation delays or clock uncertainty) contribute to the total sampling error of the receiver. The sample window specifications are obtained by using the same data set collected for the source-synchronous pin-to-pin setup/hold numbers. T_{SAMP} is defined as the sum of the worst-case setup and hold times for any single input flip-flop in the device, when a DCM in source-synchronous mode (and both CLK0 and CLK180 are used for DDR applications) and global clock trees are used for clock distribution.

For a better understanding of the circuit used for source-synchronous sampling measurements see the "Active Phase Alignment" application note XAPP268. XAPP268 describes a circuit very similar to the one used for characterization.

Since T_{SAMP} is obtained in the same manner as the source-synchronous pin-to-pin specifications, it also includes DCM jitter. However, since T_{SAMP} represents the sum of setup and hold times for a single input flip-flop, it does not include package or clock-tree skew. This parameter should only be used in a static interface timing analysis when active phase alignment is used, or bench calibration is performed. Bench calibration is the process of centering the clock in the aggregate data eye (data eye for the entire source-synchronous bus) experimentally; by manually phase shifting the forwarded clock to "train" to the incoming data stream. Once the optimal phase shift value is determined, the total receiver sampling error for the particular source-synchronous interface will be T_{SAMP} + [(Clock-tree skew + package skew) for the particular pins used for the receiver interface]. The same equation applies if using active-phase alignment. If local clock inversion in the IOB is used as opposed to CLK0 and CLK180, an additional 90 ps should be added to compensate for the duty-cycle distortion difference (T_{DCD_CLK0} vs. T_{DCD_CLK180}).

In the circuit shown in Figure 9, the DCM is in variable phase-shift mode. The sampling window value (T_{samp}) is 500 ps.

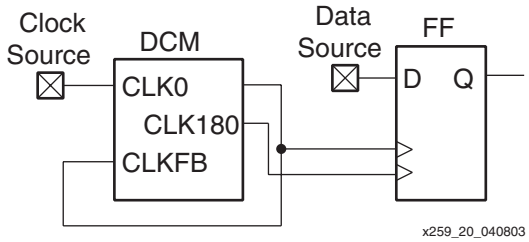


Figure 9: **Example Sampling Window Circuit**

As indicated in the previous diagrams, if clock and data signals arrive at the pin of the FPGA at the same time, then, at the input flip-flop the clock signal arrives 200 ps earlier than the data signal. To meet the Virtex-II/Virtex-II Pro setup time, if 1-bit clock and data signals arrive at the pin of the FPGA at the same time, the designer must delay the input clock by 200 ps. Delaying the input clock by at least this amount guarantees that the incoming data-bit will be sampled by the accompanying clock-edge.

For source-synchronous designs, it is always a good practice to center align the clock edge with respect to the data bit. The amount of delay required for 1-bit clock and 1-bit data signals is:

Delay_Amount = Setup_Time + (½ x Bit_Time)

Figure 10 illustrates the timing diagram for the Delay_Amount.

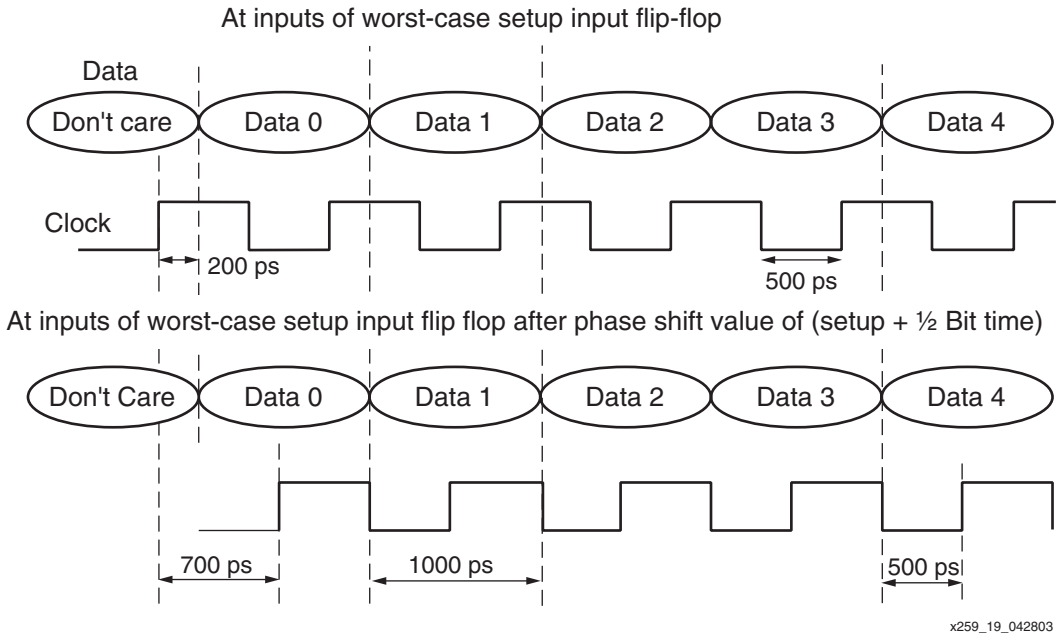


Figure 10: **Centering the Clock Edge With Respect To Data Bit**

Instead of calculating the delay amount for multiple data bits, Xilinx recommends using the "Auto Clock Data Alignment Circuit" outlined in XAPP225.

The setup time values are measured at the DDR flip-flop closest to the input clock pins and the hold time values are measured at the DDR flip-flop furthest from the input clock pins. These values are worst-case values, measured across process, voltage, and temperature, including the worst-case clock tree and package skew for a given device. However, this value does not include the DCM jitter, since it is a bench measurement using an oscilloscope.

The sampling error value for Virtex-II/Virtex-II Pro input flip-flops using the DCM in fixed phase-shift mode is produced by adding the setup time and hold time together. To calculate the timing budget (worst-case) for a circuit where the DCM is in fixed phase-shift mode, the sum of the sampling window, clock-tree skew, and package skew is substituted with the sum of the setup/hold.

If the input flip-flop uses local clock inversion as opposed to CLK180, the designer must add an additional 90 ps the window to compensate for the duty-cycle distortion difference (T_{DCD_CLK0} versus T_{DCD_CLK180}).

Example XGMII Timing Analysis (XC2V1000 FF896)

In the application note "XGMII" (XAPP606) the clock frequency is 156.25 MHz, and the system is DDR (312.5 MHz). This implies a bit time of 3.2 ns. The T_{SET} and T_{HOLD} are 960 ps each. This implies a data valid window of at least 1920 ps. This is outlined in Figure 3 of XAPP606.

Transmit

The transmit data valid window shown in XAPP606 (Figure 6) is described in the following equation.

Tx data valid window = Data Period – (Jitter + Duty-Cycle Distortion + Package Skew + Clock Skew + DCM Phase Offset)

Jitter

Based on the circuit describe in Figure 6 of XAPP606, the CLK0 output has a random jitter of ±100 ps. Additionally, by using another clock (CLK90), the jitter caused by this clock must be realized (±150 ps). In the case where multiple pins of the DCM are used, use the worst-case jitter (in this case, ±150 ps). Jitter is the only number in the timing budget defined with absolute magnitude; in this case the magnitude of the jitter is 300 ps.

Duty-Cycle Distortion

In the XGMII design, the CLK0 output of the DCM is used to clock the dual data-rate register, using local inversion. A value of 140 ps is used for T_{DCD_CLK0}.

Package Skew

The worst-case package skew $T_{PKGSKEW}$ using an XC2V1000 FF896 is 130 ps.

Clock Tree Skew

The clock tree skew, T_{CKSKEW} using an XC2V1000 is 80 ps.

CLKOUT_PHASE Error

With the clock forwarded using CLK90, there is a phase offset between the outputs (CLKOUT_PHASE) of ±140 ps. However, the magnitude of the offset is not doubled to 280 ps. After the DCM locks, there will be a phase difference of at most 140 ps among all outputs. A plus/minus indicates that all DCM outputs from one DCM can be either ahead or behind by 140 ps, but not both.

Tx Data Valid Window = 3200 – [300 + 140 + 130 + 80 + 140] = 2410 ps

Since the transmit data valid window of 2410 ps is greater than the required 1920 ps, this design meets the required XGMII timing budget specification.

Receive (From an External device, not a Xilinx Virtex-II or Virtex-II Pro FPGA)

The transmit data valid window shown in XAPP606 (Figure 7) is described by the following equation.

Receiver Sample Error = Sampling Error + Clock Skew + Package Skew + Jitter

Sampling Error

Since the circuit is implemented using the DCM in fixed phase-shift mode, the sampling error is simply the addition of the setup/hold times (700 ps). This value includes clock tree and package skew numbers. Since the circuit uses local inversion, 90 ps must be added to compensate for duty-cycle distortion differences.

Jitter

Based on the circuit described in Figure 7 of XAPP606,CLK0 is the output of the DCM. The DCM jitter value is listed as ±100 ps. Since jitter is magnitude, therefore, for the timing budget it is 200 ps.

Receiver Sample Error = 700 + 90 + 200 = 990ps

As long as the total sample error is less than the data valid window, the XGMII timing budget specification is met. Clearly, 990 ps is less than 1920 ps.

Shift Amount

For 1-bit clock and 1-bit data, the shift amount is the sum of the setup time and the half-bit time.

Example Timing Analysis of a DDR SDRAM Interface using Local Clocking for a (XC2V3000 -5 FF1152)

Introduction to the DDR SDRAM Interface

This DDR SDRAM interface uses the DQS issued by the memory to capture data during a read. Since the DQS is issued edge-aligned with the data during the READ, additional trace delay is added on the board on the DQS line to make the DQS signal center-aligned with data at the IOB registers. This additional delay needs to be taken care of while analyzing the Write side, since during a write the DQS needs to be center aligned with the data at the memory.

Transmit Side

The transmit (Write) interface is comprised of the data path with DDR IOB registers used to transmit data from the FPGA to the DDR SDRAM. The Write data is clocked at the DDR IOB register with CLK0, or with a phase-shifted clock to improve data margin at the memory. Figure 11 shows the transmit (Write) data path.

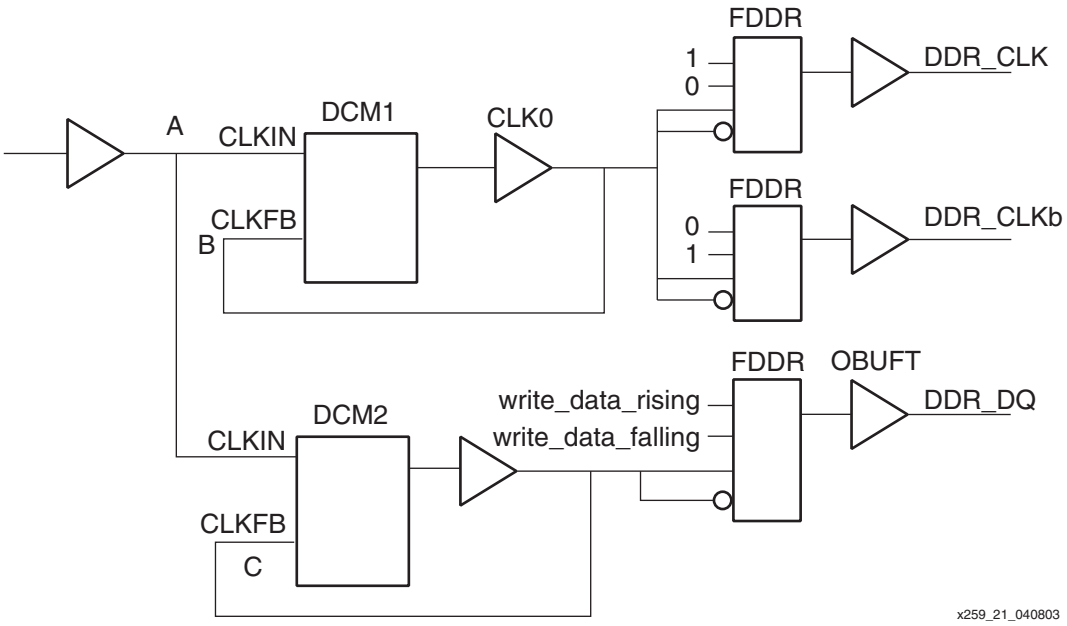


Figure 11: **Transmit (Write) Data Path**

Data Valid Window at the Pins of the FPGA

Data Valid Window at the Pins of the FPGA = Clock Period/2
$- (T_{PKGSKEW} + T_{CLKTREESKEW}$
$+ T_{DUTY\_CYCLE\_DISTORTION}$
$+ T_{Jitter}$ + CLKIN_CLKFB_PHASE for DCM1
+ CLKIN_CLKFB_PHASE for DCM2)
= 2.5 – (0.115 + 0.1 + 0.14 + 0.200 + 0.1)
= 1.845 ns

In Figure 11, clock and strobe to the DDR SDRAM is provided by DCM1. Since two DCMs with a common clock source are used in this circuit, the CLKIN_CLKFB_PHASE parameter must be used. For a worst-case timing analysis, consider the feedback input of DCM1 (B) to be ahead of the common clock source (A) by 50 ps. Consider the feedback input of DCM2 (C) to be behind the common clock source (A) by 50 ps. This results in a total of 100 ps of phase offset between the clocks at B and C. Also of note, all the DCM parameters in the module 3 of the Virtex-II/Virtex-II Pro data sheets are specified at the inputs and outputs of the DCM including this parameter. In the source-synchronous data sheet all the DCM related parameters are specified at the IOB flip-flop.

Receive Data Path

On the receive path, the DQS line is delayed externally on the board in order to meet setup/hold requirements at the IOB registers. Figure 12 comes from the DDR SDRAM application note XAPP253.

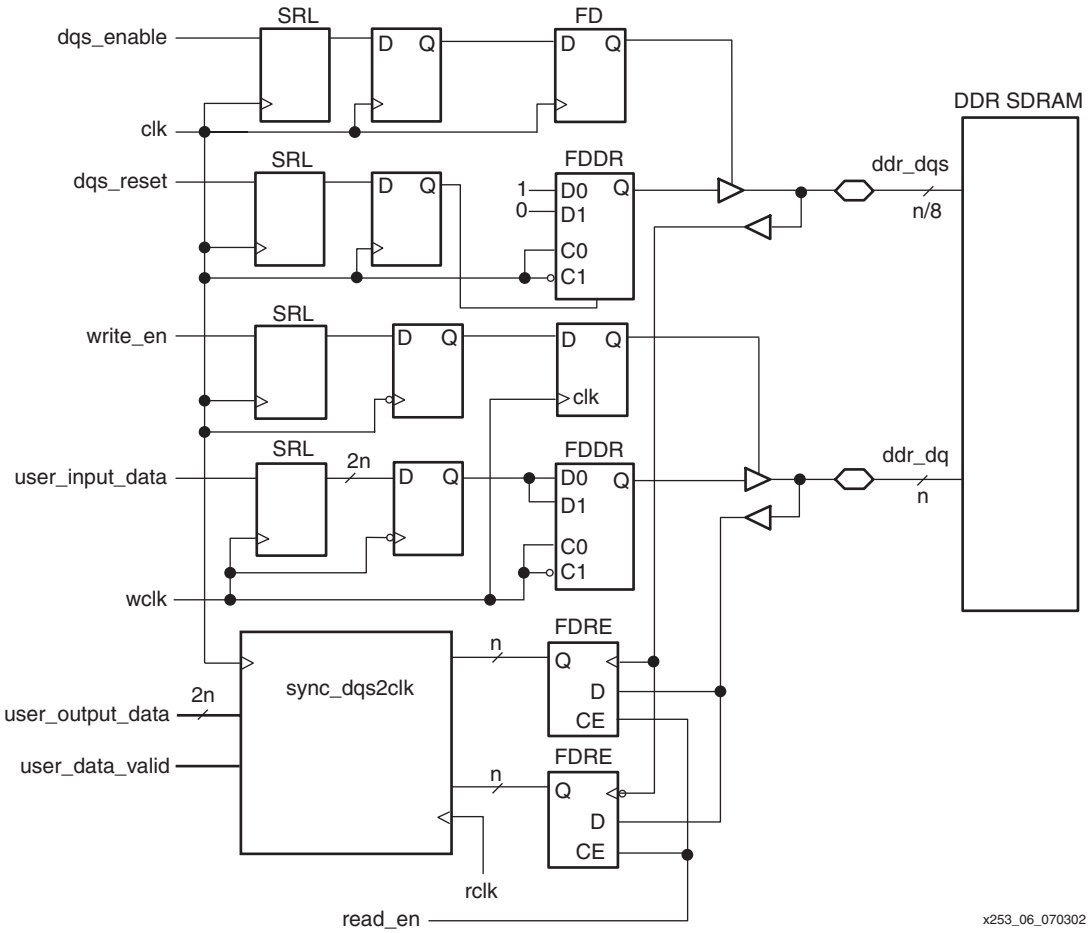


Figure 12: **DDR SDRAM Controller Data Path**

Data Valid Window at the Memory

Data valid window refers to the window of valid data window in the actual data period. For a 200 MHz interface, the clock period is 5 ns and the data period is 2.5 ns. It can also be referred to as the sum of the sampling error and data margin. The data valid window at the memory is calculated with respect to the timing specifications from the memory vendor. Data sheet numbers from Micron are used here.

Data valid window at the memory according to memory specifications
= $T_{QH} - t_{DQSQ}$ = 1.25 ns

Available Data Margin at the FPGA

Data margin refers to the margin of data available out of the actual data window received from the memory. This is calculated by eliminating all the worst-case factors that might affect the data window available from the memory. Board parameters can affect the data valid window; however, they are not taken into account in this analysis.

Available margin at the FPGA = Data valid window at memory
– (setup time at the DDR IOB + hold time at the DDR IOB
+ worst-case package skew
+ internal skew of DQS on the HEX lines
+ Duty-cycle distortion + jitter)
= 1.25 – (1.34 – 0.81 + 0.115 + 0.18 + 0.180 + 0.180)
= 0.029 ns

Setup/Hold Times

Setup/Hold times explain the relationship of the data with respect to the clock. These values are subtracted from the data window in order to ensure the Data Margin meets the setup/hold requirements at the DDR IOB registers. The T_{IOPICK}/T_{IOICKP} parameter is used in the calculation since these represent the setup/hold times with respect to a clock (not generated through a DCM) at the IOB input register. The clock path in the measurement of the T_{IOPICK}/T_{IOICKP} parameter is from the clock input pin of the IOB to the clock input of the Input IOB flip-flop. In this design, the clock at the IOB registers is the Data Strobe input to the FPGA from the DDR SDRAM memory routed on the HEX lines. The numbers represented in module 3 of the Virtex-II/Virtex-II Pro data sheets for these parameters represent the timing numbers measured for LVTTL standards. For the SSTL2_II standard, these numbers need adjustment.

Setup time = $T_{IOPICK} + T_{ISSTL2\_II} = 0.92 + 0.42 = 1.34$ ns

Hold time = $T_{IOICKP} - T_{ISSTL2\_II} = -0.37 - 0.42 = -0.79$ ns

DQS Internal Skew

The DQS internal skew refers to the worst skew existing on the HEX line. A worst-case skew of 180 ps is used for calculation.

Duty-Cycle Distortion on the Local Clock

This refers to the amount of worst-case duty-cycle distortion on the local clock. A worst-case number of 180 ps is used for calculation.

Example Timing Analysis of 100 MHz DDR SDRAM Interface Using Global Clock Resources to Capture Read Data (XC2V6000-5FF1152)

Transmit (Write to Memory)

In this example design two separate DCMs are being used, one internal DCM for the memory controller design inside the FPGA and the other external DCM to forward clocks to the external memory device. Although the write data strobe signal and the write data are both generated by the internal DCM, the data valid window calculations must account for phase offset between these two DCMs. This is because the memory device expects the data strobe signal forwarded by the FPGA during a write command to be in phase with the clock it receives at the memory pins.

Phase Offset Between System clock in FPGA Memory Controller and Clock Forwarded to Memory

The example in Figure 13 shows a memory interface clocking scheme.

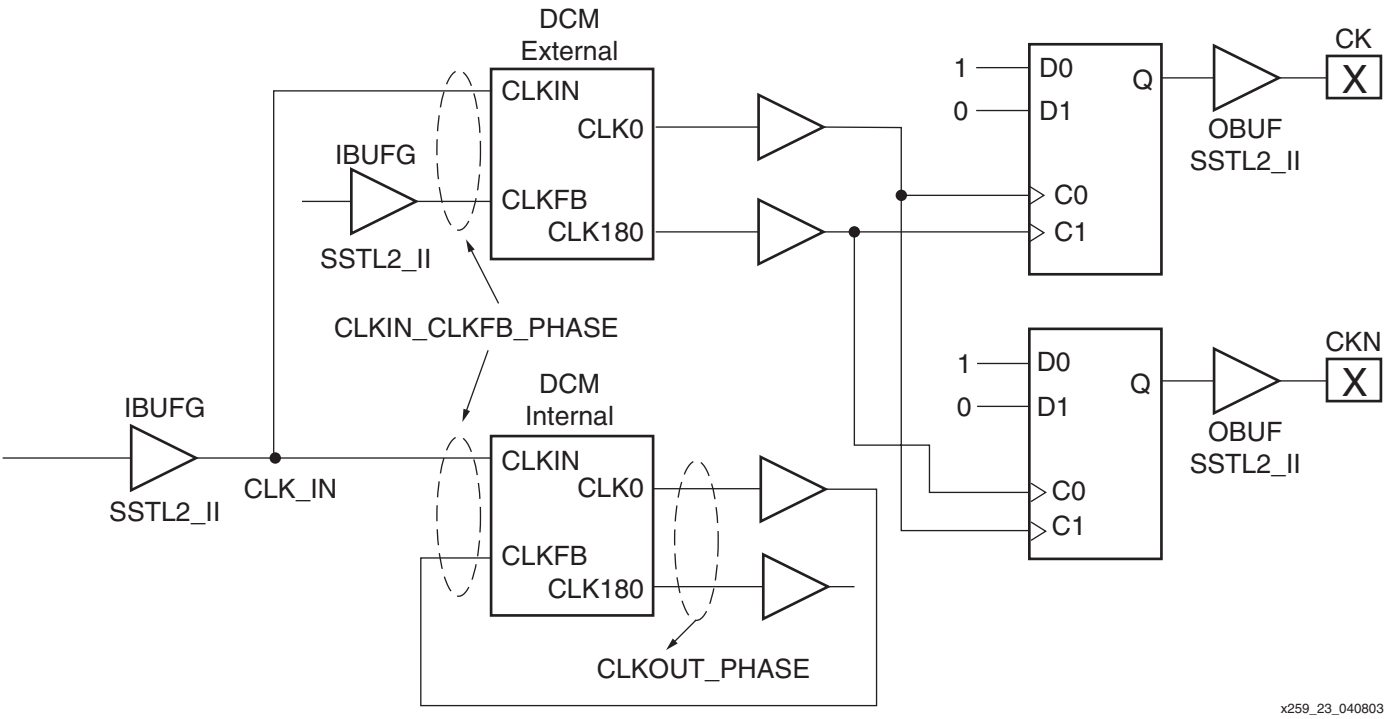


Figure 13: **Memory Interface Clocking Scheme**

Worst-Case Clock Phase Offset = CLKIN_CLKFB_PHASE for Internal DCM +
CLKIN_CLKFB_PHASE for External DCM +
CLKOUT_PHASE between outputs of Internal DCM +
Clock Tree Skew for XC2V6000-5 (T_{CKSKEW}) +
Output Clock Jitter (CLKOUT_PER_JITT_90)
= 50 ps + 50 ps + 140 ps + 500 ps + 300 ps
= 1040 ps

CLKIN_CLKFB_PHASE for Internal DCM and External DCM

For a worst-case analysis, consider the feedback input, CLKFB, of the internal DCM to be 50 ps behind the clock source, CLK_IN, and the feedback input, CLKFB, of the external DCM to be 50 ps ahead of CLK_IN. This results in a 100 ps phase offset between the CLK0 outputs of the internal and external DCMs.

CLKOUT_PHASE

For a worst-case analysis, consider the CLK90 output of the internal DCM to be 140 ps behind the CLK0 output of the internal DCM. This results in a 240 ps phase offset between the CLK0 output of the external DCM and the CLK90 output of the internal DCM.

Clock Tree Skew

The XC2V6000 FF1152 device has a worst-case clock tree skew of 500 ps as specified in the source-synchronous data sheet. For a worst-case analysis, it is assumed that the clock tree

skew between the DDR IOB flip-flop clocked by CLK0 output of the external DCM and the DDR IOB flip-flop clocked by the CLK90 output of the internal DCM is 500 ps.

Output Clock Jitter

This is the jitter introduced by the DCM due to the periodic selection of discrete tap delays. Since the data is clocked out by CLK90 of internal DCM at the DDR IOBs, CLKOUT_PER_JITT_90 specified as ±150 ps is used in these calculations. The worst-case jitter magnitude in this case is 150 x 2 = 300 ps.

Write Data Path

Transmit Data Valid Window at FPGA pin = Clock Period/2 – (Worst case clock phase offset + Duty-Cycle Distortion (T_{DCD_CLK0}) + Package Skew for XC2V6000/FF1152 ($T_{PKGSKEW}$))

= 5 ns – (1.04 ns + 0.14 ns + 0.09 ns)

= 5 ns – 1.27 ns

= 3.73 ns

Transmit Data Valid Window at Memory = Data Valid Window at FPGA pin – Board Trace Delay

Receive (Read from DDR Memory)

In the design in Figure 14, the read data strobe signal sent by the memory device along with the data is being ignored. Instead, the internal DCM phase shifted clock outputs are used to capture read data. Therefore, clock phase offset computed in the previous section, board trace delay, package skew, and duty-cycle distortion must all be subtracted from the data valid window.

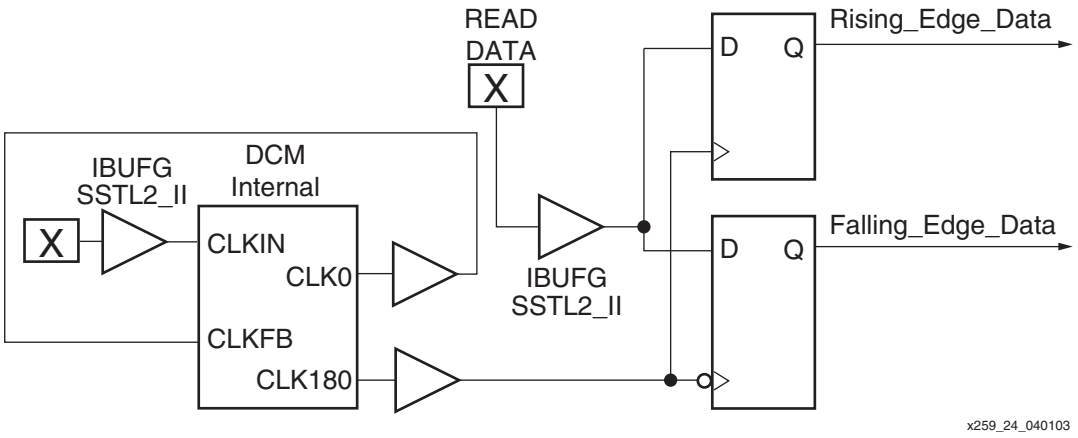


Figure 14: **Read Data Capture**

Read Data Path

Receive Data Valid Window at Memory = Clock Period/2 – Access Time specified by memory vendor
= 5 ns – 1.6 ns = 3.4 ns

Receive Data Valid Window at DDR IOB FF=3.4 ns – (Board Trace Delay + Package Skew + Worst case clock phase offset + Duty-Cycle Distortion)
= 3.4 ns – (0.6 ns + 0.09 ns + 1.04 ns + 0.14 ns)
= 1.53 ns

Board Trace Delay

The board trace delay is the propagation delay of data bits from memory device to FPGA. It is assumed that all the data bits in the data bus have matched trace lengths, and therefore the same trace delay.

Package Skew

The worst-case package skew for the XC2V6000 in an FF1152 package is considered in this worst-case calculation. The package skew can be reduced or eliminated by adjusting the trace delays of the data bits to compensate for package skew.

Duty-Cycle Distortion

The source synchronous data sheet parameter T_{DCD_CLK0} is used to calculate the duty-cycle distortion. This parameter is the duty-cycle distortion at the clock input pin of the flip-flop.

Worst-Case Clock Phase Offset

The calculation of worst-case clock phase offset is discussed in the transmit section. This parameter includes output jitter and CLKOUT_PHASE for CLK90.

The Margin at the DDR IOB Flip-Flop = 1.53 ns - (setup + hold)
= 1.53 ns - (T_{PSDCM} + T_{PHDCM})
= 1.53 ns - 0.8 ns = 0.73 ns

A setup/hold adjustment is not required because both the clock and data have the same I/O standard.

Global Clock SETUP an HOLD with DCM (T_{PSDCM}/T_{IOICKP})

This parameter must be used when using global clock resources to clock input IOB flip-flops. DCM output jitter is included in this parameter, therefore jitter need not be added in the timing analysis. The clock path in the measurement of this parameter (T_{PSDCM}/ T_{PHDCM}) is from the output of the DCM through the BUFG, the global clock tree to the clock input pin of the input IOB flip-flop. The parameter (T_{IOPICK}/T_{IOICKP}) must be used when using non-global clocking resources. The clock path in the measurement of the T_{IOPICK}/T_{IOICKP} parameter is from the clock input pin of the IOB to the clock input of the input IOB flip-flop.

Example Timing Analysis of a 200 MHz QDR SRAM Interface Using Global Clock Resources to Capture Read Data (XC2V1000-5FF896)

Transmit (Write to QDR Memory)

The board trace delay does not need to be subtracted from the data valid window since the forwarded data and forwarded clock have matched board trace lengths. As shown in Figure 15, these clock paths inside the FPGA are also matched. Only one DCM is being used to forward both the data and the clock, therefore the parameter CLKIN_CLKFB_PHASE is not used.

Transmit Data Valid Window at FPGA pin =Clock Period/2
– (Clock Tree Skew for XC2V1000 (T_{CKSKEW})
+ Pkg Skew for XC2V1000 FF896($T_{PKGSKEW}$)
+ Duty-Cycle Distortion (T_{DCD_CLK0})
+ Output Clock Jitter (CLKOUT_PER_JITT_0)
+ CLKOUT_PHASE

= 2.5 ns – (80 ps + 130 ps + 140 ps + 200 ps +140 ps
= 1.81 ns

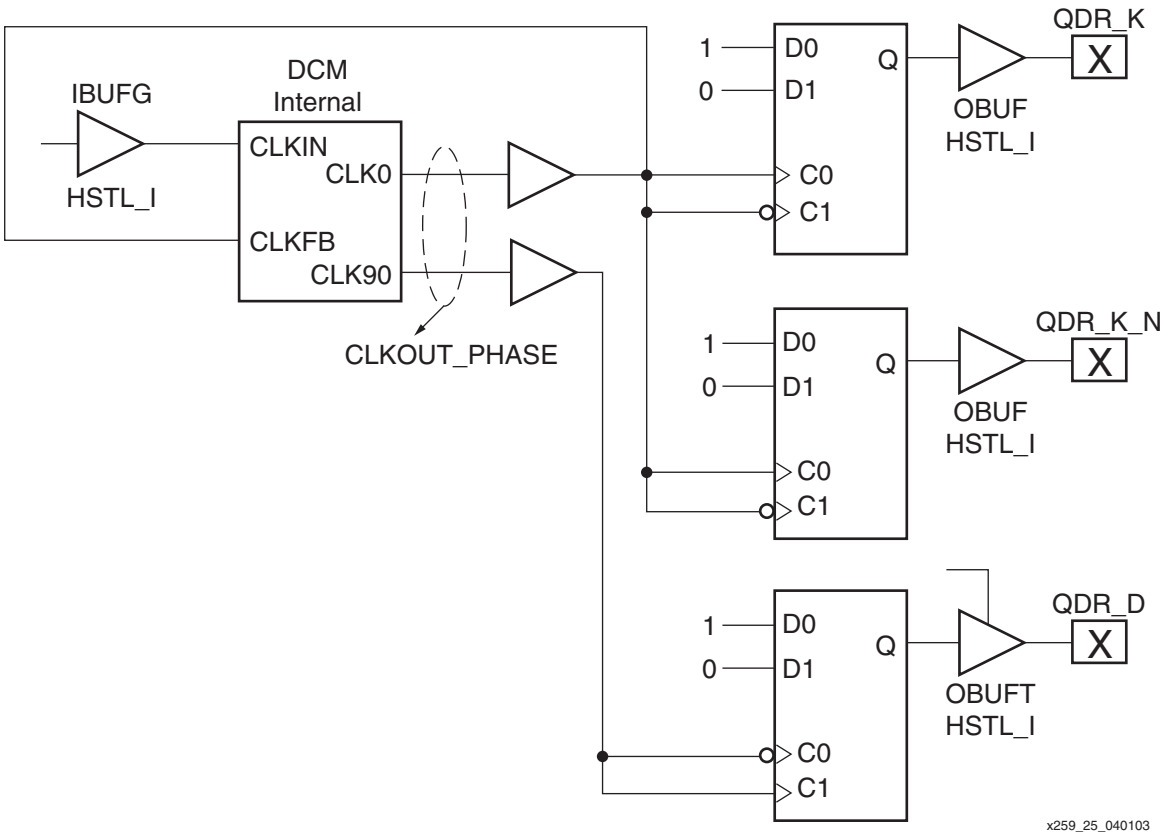


Figure 15: **Write Data and Clock Path**

Transmit Data Margin at QDR Memory = 1.81 – Memory Sample Window (provided by memory vendor)

$= 1.81 – (t_{DVKH\_200} + t_{KHDX\_200})$

= 1.81 – 1.2 ns = 0.6 ns

Receive (Read from QDR Memory)

Figure 16 shows the read data path.

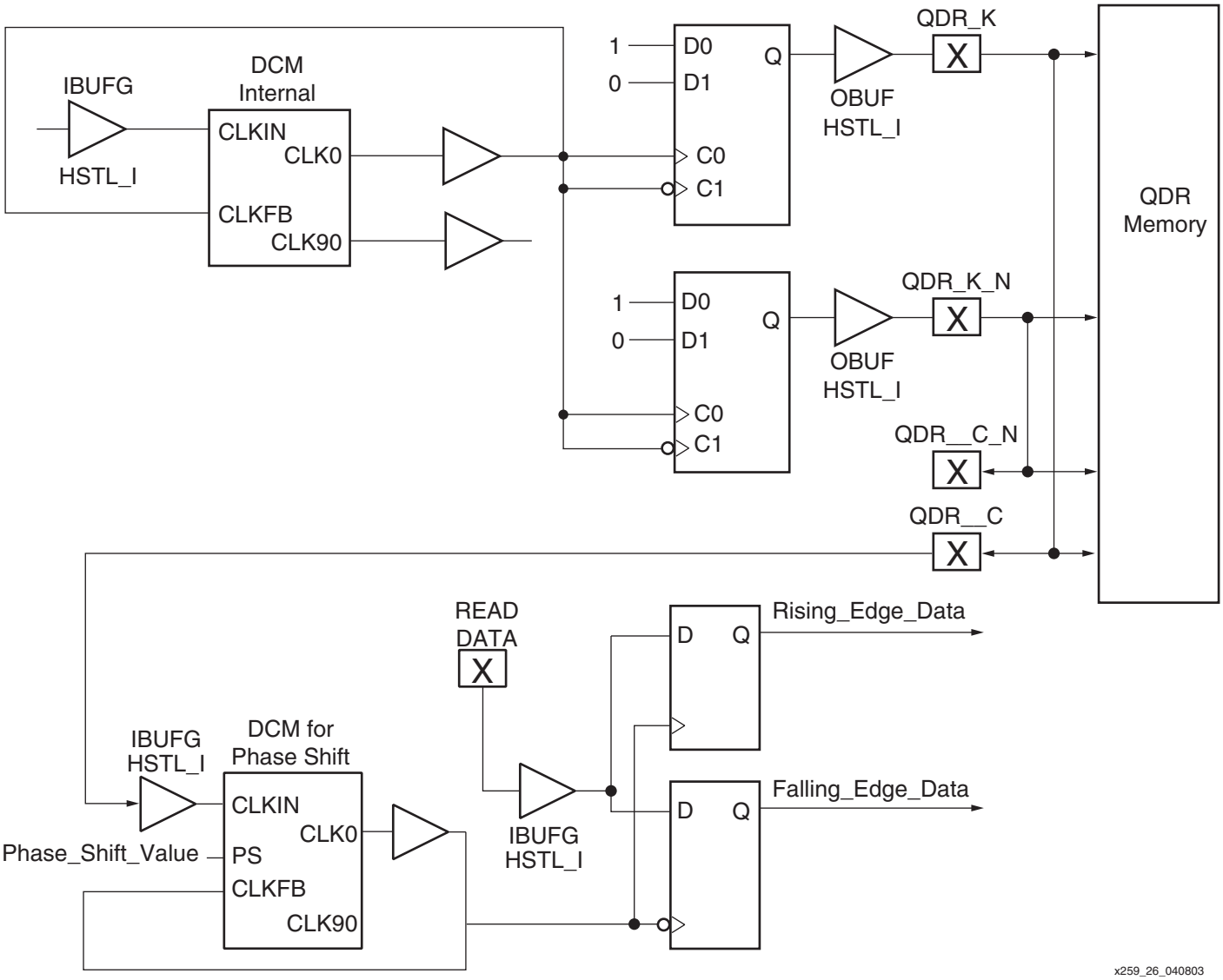


Figure 16: **Read Data and Clock Path**

Read Timing Analysis

This timing analysis assumes that both the K clock and C clock inputs at the QDR memory pins arrive at approximately the same time (i.e., the difference in board trace delays between the two paths is negligible). Another assumption is that the board trace delays for the data and the associated clock are matched. Based on these assumptions, the timing analysis does not consider board trace delays since both the data and the clock are delayed by the same amount.

QDR SRAMs send read data edge aligned with respect to the read clock (C clock). QDR SRAM vendors provide parameters (t_{CHQX} and t_{CHQVav}) to define the uncertainty of data availability with respect to the C clock edge. In order to capture this data inside the FPGA, the C clock DCM is phase shifted. This phase shift value is defined in the following equation.

$$T_{PHASESHIFT} = t_{CHQX} + t_{CHQVav} + t_{90PS} + T_{PSDCM\_HSTL} + T_{SAMPLE}/2$$

The 90° phase shift (t_{90PS}) is required to place the C clock edge in the middle of the theoretical data valid window.

Timing Margin Calculation for Read

Data Valid Window at the QDR SRAM = clock period / 2 – t_{CHQZ} + t_{CHQX}
= 2.5 – 2.2 + 1 = 1.3 ns

The parameters t_{CHQZ} and t_{CHQX} are provided by the memory vendor.

Data Valid Window at FPGA = clock period / 2 – (T_{SAMPLE} + T_{CKSKEW} (XC2V1000)
+ $T_{PKGSKEW}$ (XC2V1000 FF896)
+ Output Clock Jitter (CLKOUT_PER_JITT_0))
= 2.5 - (0.7 + 0.1 + 0.130 + 0.2) = 1.37 ns

Timing Margin = 1.3 ns – 1.13 ns = 0.17 ns

Conclusion

There are two parameters contributing to DCM phase error; CLKOUT_PHASE and CLKIN_CLKFB_PHASE. The CLKOUT_PHASE parameter is only used with the non-feedback output of the DCM. The CLKIN_CLKFB_PHASE parameter is used with multiple DCMs with a common clock source.

A setup/hold adjustment is required when the clock input buffer is a different I/O standard than the data input buffer.

Pin-to-pin setup/hold is used for timing budget and analysis of source-synchronous circuits when the DCM is configured in fixed phase-shift mode. T_{samp} is used for timing budget and analysis of source-synchronous circuits when the DCM is configured in variable phase-shift mode. Duty-cycle distortion differences must be taken into account.

Appendix

Example DCM Circuits with Associated Phase Error

A detailed analysis for each circuit is provided in this Appendix. For each circuit, a worst-case analysis results in the least capture window margin. Table 1 lists the example DCM circuits with links to the figures.

Table 1: **Example DCM Circuits with Associated Phase Error**

Example Circuits	Phase Error
DCM - Single Output using BUFG	Total Phase Error = 0 ps
DCM - Single Output Low Skew Line or Local	Total Phase Error = 0 ps
DCM/CLKFB and Second Output	Total Phase Error = 140 ps
DCM1/OUT1 and DCM2/OUT2	Total Phase Error = 100 ps
DCM1/CLKFB and DCM2/OUT	Total Phase Error = 240 ps
DCM1/OUT1 and DCM2/OUT2	Total Phase Error = 380 ps
BUFG and DCM/FB_OUT	Total Phase Error = 50 ps
BUFG and DCM/OUT	Total Phase Error = 190 ps
Cascaded DCMs with DCM2/FB_OUT2	Total Phase Error = 50 ps
Cascaded DCMs with DCM2/OUT2	Total Phase Error = 190 ps
DCM and Data Input	Total Phase Error = 140 ps

In Figure 17, the goal is to determine the phase error between the clock inputs to the flip-flops. The DCM output could be a feedback or any other non-feedback output. Since the same DCM output is used to clock both the flip-flops, the phase error introduced by the DCM is zero.

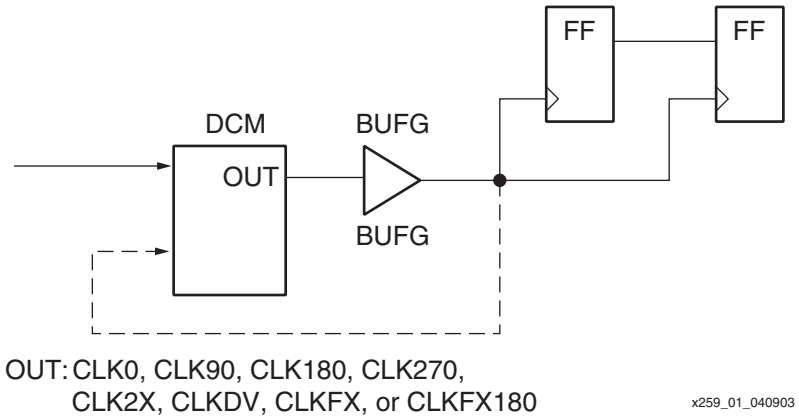


Figure 17: **DCM - Single Output using BUFG**

In Figure 18, the goal is to determine the phase error between the clock inputs to the flip-flops. The DCM output could be a feedback or any other non-feedback output. Since the same DCM output is used to clock both the flip-flops, the phase error introduced by the DCM is zero.

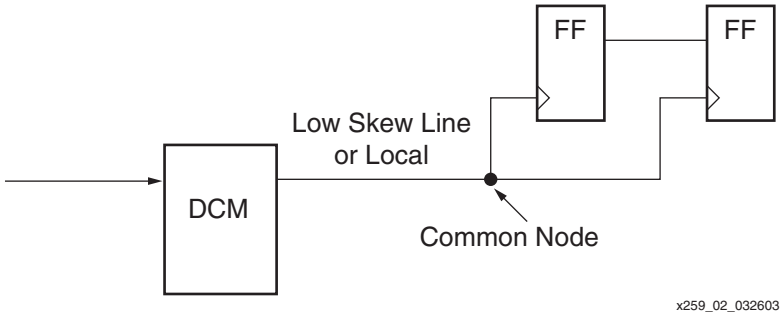


Figure 18: **DCM - Single Output Low Skew Line or Local**

In Figure 19, the goal is to determine the phase error between the clock inputs to the flip-flops. In this case two DCM outputs are used, one is the feedback output and the other is the non-feedback output. Therefore, the phase error introduced by the DCM is CLKOUT_PHASE = 140 ps. OUT_BUFG can be 140 ps ahead of or behind DCM_FB. For a worst-case timing analysis, consider the situation that provides the worst available margin in a system.

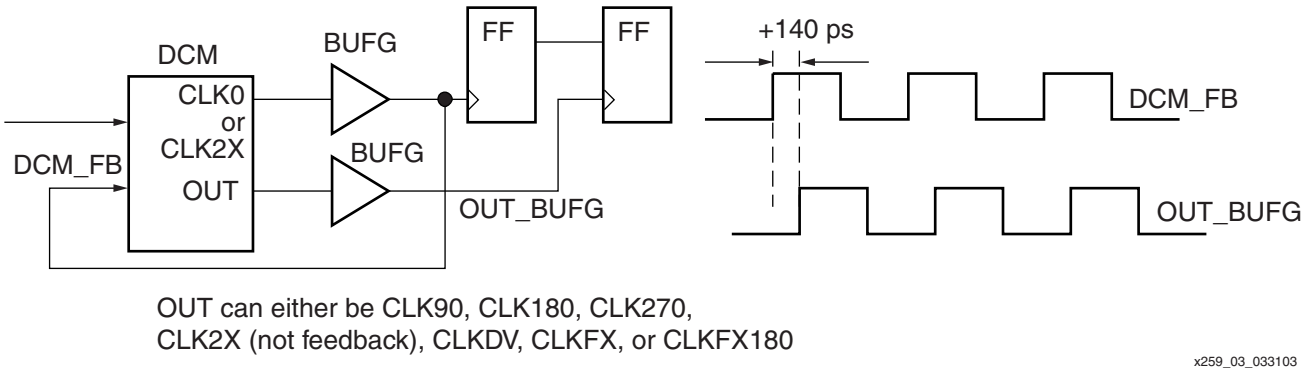


Figure 19: **DCM/CLKFB and Second Output**

In Figure 20, the goal is to determine the phase error between the clock inputs to the flip-flops. Only the feedback output is used in each DCM, therefore the CLKOUT_PHASE parameter must not be considered. In this circuit two DCMs with the same source clock are used. Therefore, the CLKIN_CLKFB_PHASE parameter must be used for each DCM. For a worst-case analysis, consider the feedback output of DCM1, DCM1_FB to be 50 ps ahead of CLKIN and the feedback output of DCM2, DCM2_FB to be 50 ps behind CLKIN. This results in a maximum phase error between the feedback outputs of the DCMs (or clock inputs of flip-flops) of 100 ps.

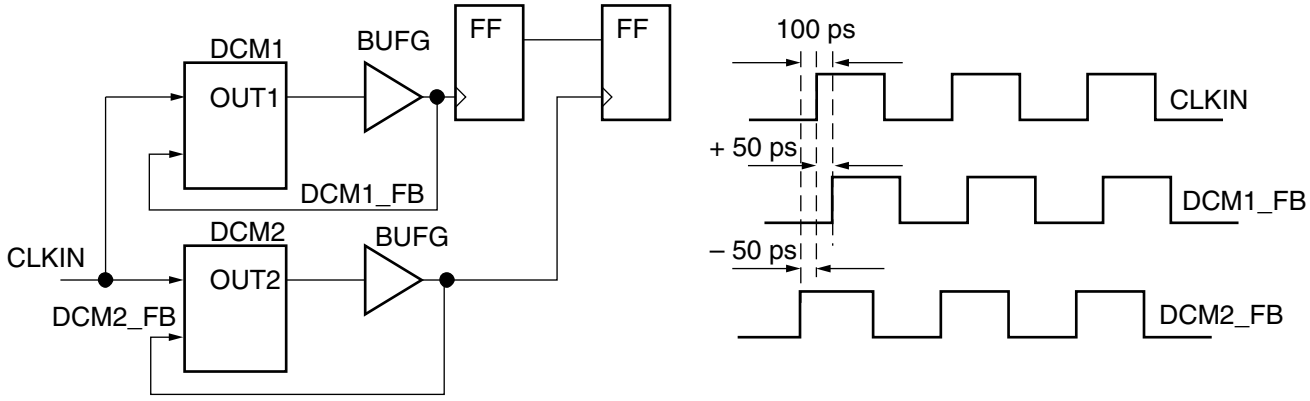
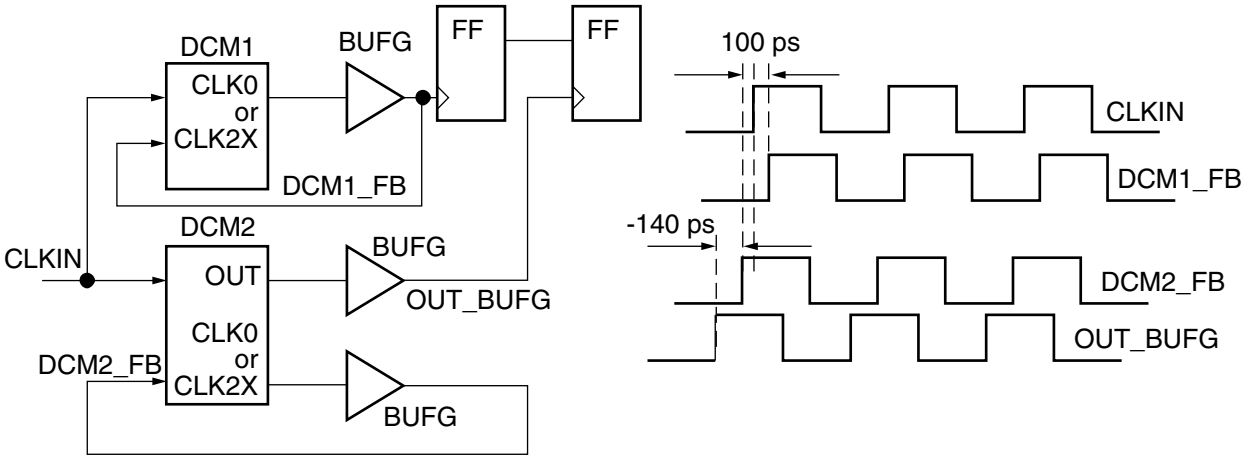


Figure 20: **DCM1/OUT1 and DCM2/OUT2**

In Figure 21, the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit two DCMs with the same source clock are used. Therefore, the CLKIN_CLKFB_PHASE parameter must be used for each DCM. For a worst case-analysis, consider the feedback output of DCM1 to be 50 ps ahead of CLKIN and the feedback output of DCM2 to be 50 ps behind CLKIN. This results in a maximum phase error between the feedback outputs of the DCMs of 100 ps. Only the feedback output is used to clock a flip-flop with DCM1, therefore the CLKOUT_PHASE parameter must not be considered for DCM1. However with DCM2, the non-feedback output, OUT is used to clock the flip-flop, therefore the CLKOUT_PHASE parameter must be used for DCM2. For a worst-case analysis, consider OUT_BUFG to be 140 ps behind DCM2_FB. This results in a total phase error between the flip-flop clock inputs of 240 ps.

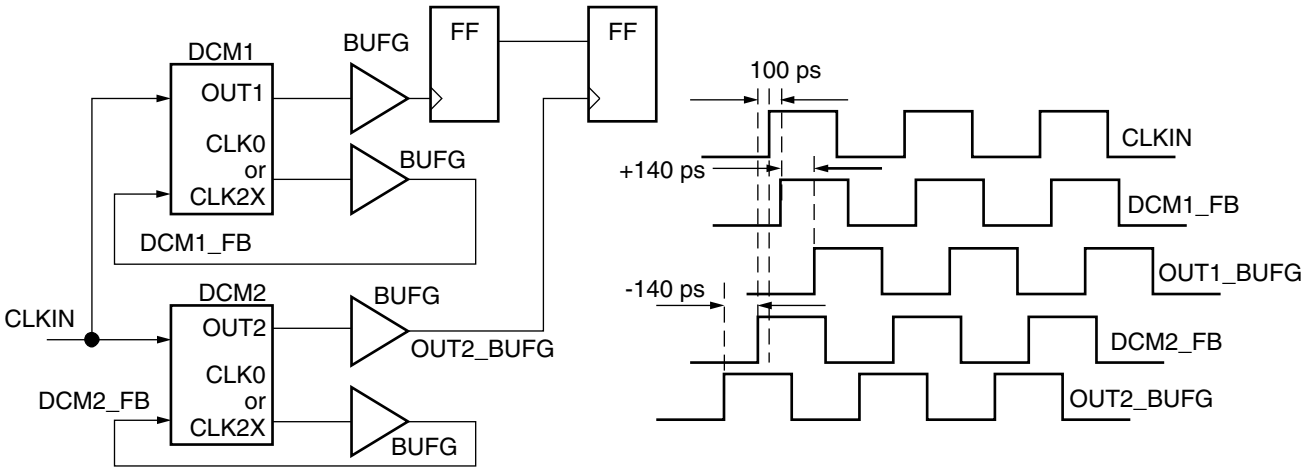


OUT can either be CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180
If CLKFB is not connected in DCM2,
then the phase relationship between CLKFX/CLKFX180 and CLKIN is not guaranteed

x259_05_033103

Figure 21: **DCM1/CLKFB and DCM2/OUT**

In Figure 22 the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit two DCMs with the same source clock are used. Therefore, the CLKIN_CLKFB_PHASE parameter must be used for each DCM. For a worst-case analysis, consider the feedback output of DCM1 to be 50 ps ahead of CLKIN and the feedback output of DCM2 to be 50 ps behind CLKIN. This results in a maximum phase error between the feedback outputs of the DCMs of 100 ps. The non-feedback output, OUT1 is used to clock a flip-flop with DCM1 therefore the CLKOUT_PHASE parameter is used for DCM1. For a worst-case analysis, consider OUT1_BUFG to be 140 ps ahead of its feedback output, DCM1_FB. In DCM2 the non-feedback output, OUT2 is used to clock the flip-flop, therefore the CLKOUT_PHASE parameter is used for DCM2. For a worst case analysis, consider OUT2_BUFG to be 140 ps behind its feedback output, DCM2_FB. This results in a total phase error between the flip-flop clock inputs of 380 ps.

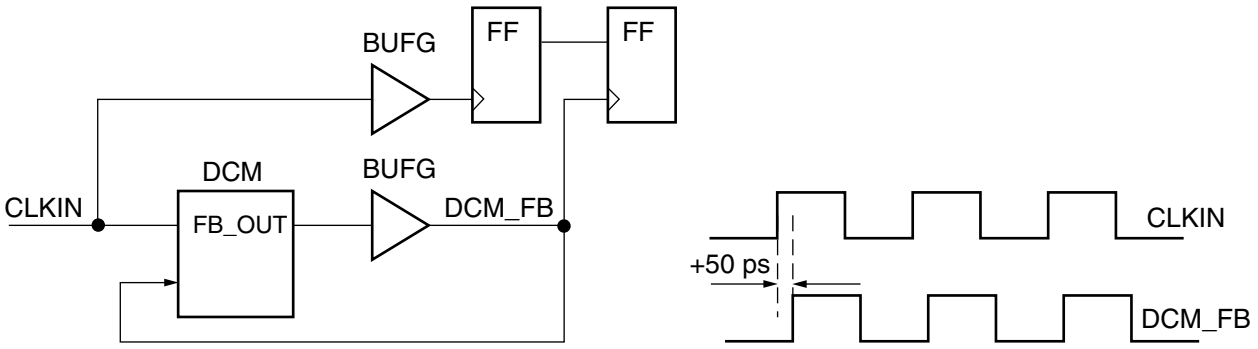


OUT1 or OUT2 can either be CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180
If CLKFB is not connected in DCM2,
then the phase relationship between CLKFX/CLKFX180 and CLKIN is not guaranteed

x259_06_033103

Figure 22: **DCM1/OUT1 and DCM2/OUT2**

In Figure 23, the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit one DCM and one BUFG with the same source clock are used. This is a special case where the CLKIN_CLKFB_PHASE parameter must be used with a single DCM. Consider the feedback output of the DCM, DCM_FB to be 50 ps ahead of CLKIN. Only the feedback output is used to clock the flip-flop with the DCM, therefore the CLKOUT_PHASE parameter must not be considered. This results in a total phase error between the flip-flop clock inputs of 50 ps. DCM_FB can be 50 ps ahead of or behind CLKIN. For a worst-case timing analysis, consider the situation that provides the worst available margin in a system. The additional IBUFG delay in the non-DCM clock path and the clock-tree skew are factored into the software timing analysis.



FB_OUT can either be CLK0 or CLK2X

x259_07_033103

Figure 23: **BUFG and DCM/FB_OUT**

In Figure 24, the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit one DCM and one BUFG with the same source clock are used. Therefore, the CLKIN_CLKFB_PHASE parameter must be used for the DCM. Consider the feedback output of the DCM, DCM_FB to be 50 ps behind CLKIN. The non-feedback output, OUT is used to clock the flip-flop with the DCM therefore the CLKOUT_PHASE parameter is used. For a worst-case analysis, consider OUT_BUFG to be 140 ps behind its feedback output, DCM_FB. This results in a total phase error between the flip-flop clock inputs of 190 ps. The additional IBUFG delay in the non-DCM clock path and the clock-tree skew are factored into the software timing analysis.

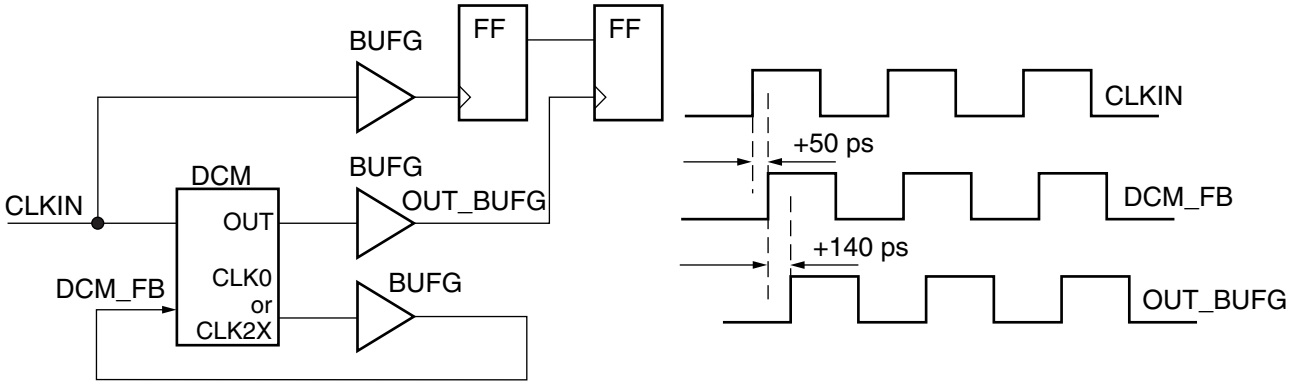
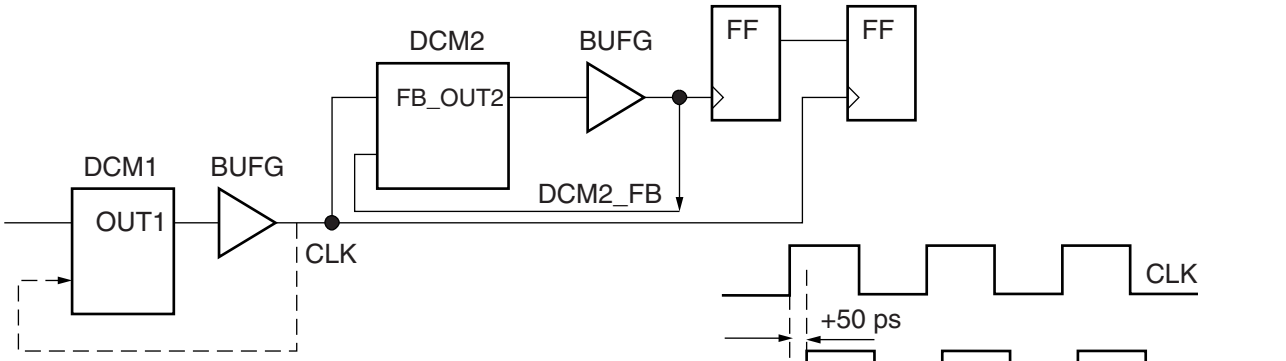


Figure 24: **BUFG and DCM/OUT**

In Figure 25, the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit two DCMs are cascaded with the output of DCM1 being input to DCM2 clock input. One of the flip-flops is clocked by the output of DCM1 and the other flip-flop is clocked by the output of DCM2 that gets its clock input from DCM1. Therefore the phase error introduced by DCM1 applies equally to both the flip-flop clock inputs and cancel out. Consider the output of DCM1, CLK as the clock source. The phase error between the clock inputs to the flip-flops is only by DCM2 because one flip-flop receives the clock source directly. The CLKIN_CLKFB_PHASE parameter must be used for the DCM2. Consider the feedback output of the DCM2, DCM2_FB to be 50 ps behind CLK. Only the feedback output is used to clock the flip-flop with the DCM, therefore the CLKOUT_PHASE parameter must not be considered. This results in a total phase error between the flip-flop clock inputs of 50 ps. DCM2_FB can be 50 ps ahead of or behind CLK. For a worst-case timing analysis, consider the situation that provides the worst available margin in a system.



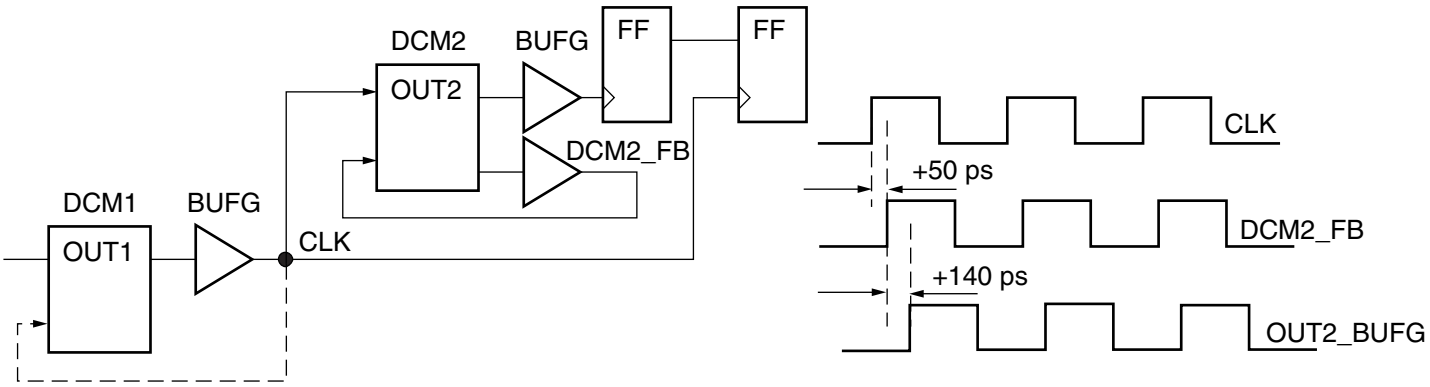
OUT1 can either be CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180
If CLKFB is not connected in DCM2,
then the phase relationship between CLKFX/CLKFX180 and CLKIN is not guaranteed

FB_OUT2 can be either CLK0 or CLK2X

x259_09_033103

Figure 25: **Cascaded DCMs with DCM2/FB_OUT2**

In Figure 26, the goal is to determine the phase error between the clock inputs to the flip-flops. In this circuit two DCMs are cascaded with the output of DCM1 being input to DCM2 clock input. One of the flip-flops is clocked by the output of DCM1 and the other flip-flop is clocked by the output of DCM2 that gets its clock input from DCM1. Therefore the phase error introduced by DCM1 applies equally to both the flip-flop clock inputs and cancel out. Consider the output of DCM1, CLK as the clock source. The phase error between the clock inputs to the flip-flops is only by DCM2 because one flip-flop receives the clock source directly. The CLKIN_CLKFB_PHASE parameter must be used for the DCM2. Consider the feedback output of the DCM2, DCM2_FB to be 50 ps behind CLK. The non-feedback output, OUT2 is used to clock the flip-flop with DCM2 therefore the CLKOUT_PHASE parameter is used. For a worst-case analysis, consider OUT2_BUFG to be 140 ps behind its feedback output, DCM2_FB. This results in a total phase error between the flip-flop clock inputs of 190 ps.



OUT1 can either be CLK0, CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180

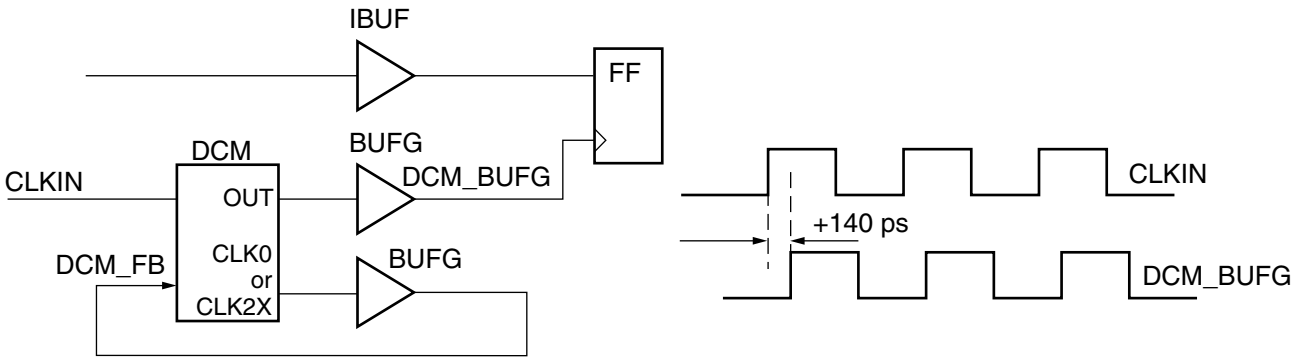
OUT2 can either be CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180

If CLKFB is not connected in DCM2,
then the phase relationship between CLKFX/CLKFX180 and CLKIN is not guaranteed

x259_10_033103

Figure 26: **Cascaded DCMs with DCM2/OUT2**

In Figure 27, the total phase error introduced by the DCM when using a non-feedback output to clock the flip-flop is 140 ps (CLKOUT_PHASE). The total phase error is zero when using the feedback output to clock the flip-flop. The pin-to-pin setup parameter relevant for this circuit includes CLKIN_CLKFB_PHASE. Therefore, it is not included to compute the phase error.



OUT can either be CLK90, CLK180, CLK270,
CLK2X (not feedback), CLKDV, CLKFX, or CLKFX180

x259_27_042203

Figure 27: **DCM and Data Input**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/28/03	1.0	Initial Xilinx release.