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Xilinx Power Tools: The Power Estimator

Summary

This application note is offered as complementary text to the Power Estimator tools. A completed FPGA design and a successful functional simulation should be performed before using these tools. The Power Estimator tools support the Virtex™, Virtex-E, Spartan™-IIE, Spartan-3, Virtex-II, and Virtex-II Pro™ devices. The tools are available on the Xilinx web site at: http://www.xilinx.com/ise/power_tools

This application note focuses on how to use the power estimator spreadsheet and/or the web tools to calculate estimated power consumption for the supported devices.

Introduction

Power Estimator tools estimate power consumption for a design before it is downloaded to the device. It considers the design resource usage, toggle rates, I/O power, and many other factors in the estimation. The formulas used for calculations in the program are based on digital circuit behavior. The characteristic data is based on measurements, simulation, or extrapolation.

Xilinx provides three power estimator tools. A Microsoft Excel version, a CGI version for use with web browsers, and XPower a detailed estimation tool included with the Xilinx ISE software. The spreadsheet and web tools are similar in terms of estimations and data entries. These are pre-implementation tools for use in the early stages of design. After implementation, the XPower tool is more accurate since it utilizes the logic and routing resources of the actual design. For more information on the XPower tool, please refer to XPower documentation on the Xilinx web site: http://www.xilinx.com/support/sw_manuals/xilinx5

The Power Estimator tools have up to nine sections. Table 1 indicates the sections applicable for each device family.

Table 1: **Possible Selections by Device Family**

	Virtex	Virtex-E	Spartan-IIE	Spartan-3	Virtex-II	Virtex-II Pro
Quiescent Power	X	X	X	X	X	X
CLB Power	X	X	X	X	X	X
Block RAM Power	X	X	X	X	X	X
Block Multiplier Power				X	X	X
Processor Power						X
DLL/DCM	X	X	X	X	X	X
Multi-Gigabit Transceiver						X
I/O Power	X	X	X	X	X	X
Results Summary	X	X	X	X	X	X

Quiescent Power

The device quiescent power is automatically determined depending on the device selected. No input into the Power Estimator tools is required. The figures represent typical values using default conditions in moderate environments for the majority of devices.

Table 2: **Device Quiescent Power**

	V_{CCINT} Subtotal (mW)	V_{CCAUX} Subtotal (mW)
	300	**13**

CLB Logic Power

Table 3 shows the entries required for the CLB logic power section in the Power Estimator tools. This section estimates the power consumption of the CLBs for the design; partition designs into modules, specify the number of CLBs and the logic resources used, and specify toggle rates. The amount of routing must also be specified.

Table 3: **CLB Logic Power**

Name	Frequency (MHz)	Total Number of CLB Slice	Total Number of Flip/Flop or Latches	Total Number of Shift Register LUTs	Total Number of Select RAM LUTs	Average Toggle Rate %	Amount of Routing Used	V_{CCINT} Subtotal (mW)
CLB_MOD0	150	750	1000	450	101	7%	Low	**105**
CLB_MOD1	100	656	777	345	98	8%	Medium	**67**
User Module 3	0	0	0	0	0	0%	Low	**0**
User Module 4	0	0	0	0	0	0%	Low	**0**
User Module 5	0	0	0	0	0	0%	Low	**0**
User Module 6	0	0	0	0	0	0%	Low	**0**
User Module 7	0	0	0	0	0	0%	Low	**0**
User Module 8	0	0	0	0	0	0%	Low	**0**
User Module 9	0	0	0	0	0	0%	Low	**0**
User Module 10	0	0	0	0	0	0%	Low	**0**
User Module 11	0	0	0	0	0	0%	Low	**0**
User Module 12	0	0	0	0	0	0%	Low	**0**
							Total	**172**

Modules

Modules are portions of a design. A designer could treat the entire design as one module and calculate its toggle rate. However, estimating power this way is not as accurate as when the design is divided into multiple modules.

This Power Estimator tools allow designs to be partitioned into a maximum of eight modules. Determining how to partition the design into modules depends on user preference. Three partitioning approaches are presented as guidelines.

Grouping by Hierarchy

If a design contains hierarchical components at the top level, these components may be separated or grouped together to represent modules.

Grouping by Clocks

If a design has several different clocks, the logic associated with each clock should be treated as a module. For accuracy, each module should contain only one clock.

Grouping by Functionality

When a design has sub-components performing different functions, each sub-component can be considered as a module. For example, a microprocessor is thought of as three main modules: an ALU, a register file, and a control system.

Frequency (MHz)

Frequency is the clock frequency in MHz. Each module should contain only one clock.

CLB Slices

The number of CLBs used in a module is entered in this area. This number is available from the synthesis report in a specific synthesis tool. For a more accurate result, run only this module through the Xilinx ISE software as far as MAP. Take the numbers from the map report file (`.mrp`). The `.mrp` file is the output resource usage file produced by running the MAP program in the Xilinx ISE software.

For schematic-based designs, obtaining this number is slightly more difficult. Designers can either estimate CLB usage based on the design structure or MAP the module and read the numbers from the `.mrp` file.

Flip-Flops or Latches

The total number of flip-flop and latch elements used for each module are obtained from the synthesis report, the `.mrp` file, or by adding up the registers from the schematics.

Shift Register LUTs

This is the total number of SRL16 elements used in each module.

Total Number of SelectRAM LUTs

This is the total number of LUTs used as distributed SelectRAM components. For all devices supported by the Power Estimator tools, one 16 x 1 synchronous RAM is equivalent to one LUT, and one 16 x 1 dual-port RAM is equivalent to two LUTs.

Average Toggle Rate (%)

The toggle rate describes how often the output changes with respect to the input clock, usually between 6% and 12% for a typical module. Functional simulation is required to accurately calculate the toggle rate. Designers need to simulate all the flip-flop outputs in each module with regard to the clock, and calculate how often the flip-flop outputs change in relation to the clock.

Measuring the toggle rate becomes a more complex and a time-consuming process as module size increases. A toggle flip-flop has a 100% toggle rate, an 8-bit counter has 28%, and 16-bit counter has 14%. Figure 1 is an example of how to calculate the toggle rate for a 4-bit counter.

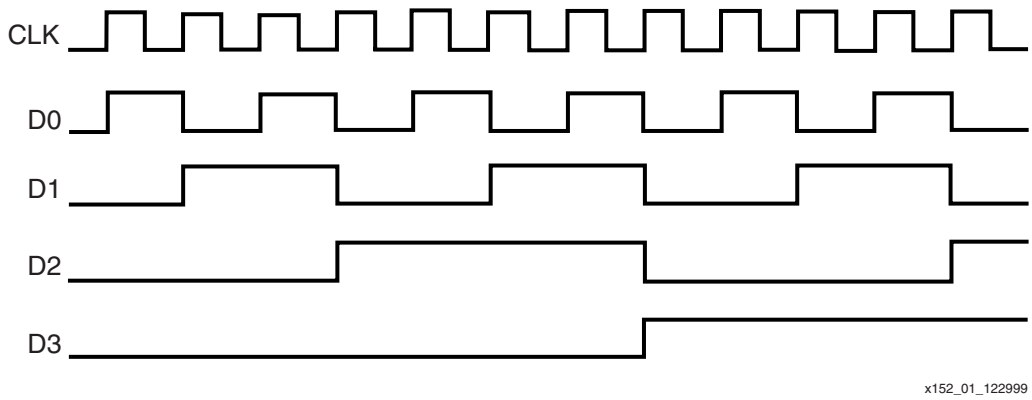

Figure 1: **Output Waveform of a 4-bit Counter**

Figure 1 shows the simulation wave form of a 4-bit counter. D0 is the LSB of the count, and D3 is the MSB. The toggle rate of D0 is 100% because D0 changes after every clock cycle. The toggle rate of D1 is 50% because D1 changes after every two clock cycles. The toggle rate of D2 is 25% because D2 changes after every four clock cycles. The toggle rate of D3 is 12.5% because D3 changes after every eight clock cycles. The derivation of an average toggle rate of a 4-bit counter is:

(100% + 50% + 25% + 12.5%)/4 = 46.875%

Routing Amount

There are three levels concerning the amount of routing to be used: low, medium, and high. The routing level is determined by the primary logic type of the module. Data-path logic uses combinatorial logic (multiplexers, adders, AND gates, and OR gates).This also applies to any other signals that have one or two fanouts between structures. Random logic includes decoders, encoders, or any logic with three to five fanouts. Control logic has high fanout signals (excluding clocks) such as clock enables or reset signals. Control logic used in state machines also belongs to this category. Each designer needs to determine the routing that is most appropriate for each module. Typical data-path logic normally requires a low routing usage, random logic calls for a medium level, and control logic needs a high level.

Block RAM Power

Table 4 shows the data entries required for the block RAM power section. This section is used to specify how many block RAMs are used and to determine their estimated power consumption. Before entering the data, designers can either treat all the block RAM primitives as one module or break them down into smaller modules. The Virtex, Virtex-E, and Spartan-IIE families use RAMB4 as a primitive name for the block RAM component. RAMB16 is the primitive name for the block RAM component in the Spartan-3, Virtex-II, and Virtex-II Pro families.

Table 4: **Block SelectRAM Power**

Name	Total Number of Block RAM Cells	Port A Frequency (MHz)	Port A Width	Port A Read Rate (%)	Port A Write Rate (%)	Port B Frequency (MHz)	Port B Width	Port B Read Rate (%)	Port B Write Rate (%)	V_{CCINT} Subtotal (mW)
DPRAM_A	20	45	18	50%	50%	50	18	75%	25%	**139**
DPRAM_B	15	56	4	50%	50%	25	9	80	20	**75**
User Module 3	0	0	0	0	0	0	0	0	0	**0**
User Module 4	0	0	0	0	0	0	0	0	0	**0**
User Module 5	0	0	0	0	0	0	0	0	0	**0**
User Module 6	0	0	0	0	0	0	0	0	0	**0**
User Module 7	0	0	0	0	0	0	0	0	0	**0**
User Module 8	0	0	0	0	0	0	0	0	0	**0**
User Module 9	0	0	0	0	0	0	0	0	0	**0**
User Module 10	0	0	0	0	0	0	0	0	0	**0**
User Module 11	0	0	0	0	0	0	0	0	0	**0**
User Module 12	0	0	0	0	0	0	0	0	0	**0**
									Total	**214**

Block RAM

This is total number of block RAMs (RAMB4 or RAMB16 primitives) used in each module.

Port A/B Frequency (MHz)

This is the frequency on the CLKA and CLKB pins.

Port A/B Width

This is data width of DIA, DOA, DIB, and DOB busses.

Port A/B Read/Write Rate (%)

This specifies the percentage of time when the block RAM ports are enabled for reading and writing.

Block Multiplier Power

Table 5 shows the data entries required for the block multiplier section. This section is used to estimate how much power each module consumes. Block multipliers are available in the Spartan-3, Virtex-II, and Virtex-II Pro architectures.

Table 5: **Block Multiplier Power**

Name	Total Number of Multipliers	Data Frequency (MHz)	Data Toggle Rate %		V_{CCINT} Subtotal (mW)
MULT_A	18	45	Low		**36**
MULT_B	9	50	Low		**20**
User Module 3	0	0	Low		**0**
User Module 4	0	0	Low		**0**
User Module 5	0	0	Low		**0**
User Module 6	0	0	Low		**0**
User Module 7	0	0	Low		**0**
User Module 8	0	0	Low		**0**
				Total	**56**

Total Number of Multipliers

This is the number of block multipliers in each user module.

Data Frequency

The data frequency (multiplication frequency) is the clock frequency on the clock pin of the block multiplier. When the multiplier is set to asynchronous mode, the data frequency is the input signal frequency.

Data Toggle Rate

This number is obtained in the same way as the average toggle rate in the "CLB Logic Power" section.

Processor Power

Table 6 shows the data entries required for the embedded PowerPC section. This section is used to estimate how much power the processors consume. Processors are only available in the Virtex-II Pro architecture. The number of PowerPC processors available in a single Virtex-II Pro device vary by device size, ranging from 0 to 4.

Table 6: **Processor Power**

Name	Processor Frequency (MHz)	PLB Frequency (MHz	DCR Bus Frequency (MHz)	OCM Bus Frequency (MHz)		V_{CCINT} Subtotal (mW)
FFTPPC	46	24	20	38		**48**
User PPC 2	0	0	0	0		**0**
User PPC 3	0	0	0	0		**0**
User PPC 4	0	0	0	0		**0**
					Total	**48**

Processor Frequency

This is the clock speed of the PowerPC processor.

Processor Local Bus (PLB) Frequency

This is the frequency of the PLB. This is the primary bus that connects the PowerPC processor to the high speed peripherals in the FPGA logic.

Device Control Register (DCR) Bus Frequency

This is the frequency of the DCR bus. The DCR bus interface connects to DCR slaves containing a set of registers. The PowerPC processor reads and writes to these registers to initialize and control peripherals. The clocks to the DCR slaves are in phase with the PowerPC clock. The frequency of the DCR slaves must be an integer ratio of the processor clock frequency. However, each slave can run at a frequency with a different integer ratio.

On-Chip Memory (OCM) Bus Frequency

This is the frequency of the OCM bus. The OCM bus is a bus dedicated to interfacing between the PowerPC processor and on-chip memory.

Clock DLL or DCM Power

Delay Locked Loop (DLL) or Digital Clock Manager (DCM)

Table 7 shows the data entries required for the DLL/DCM power section. This section is used to estimate how much power the DLL/DCMs consume. Only the clock input frequencies and the configuration of the DLL/DCM need to be entered.

Table 7: **Digital Clock Manager Power**

Module	Clock Input Frequency (MHz)	DCM Frequency Mode		V_{CCINT} Subtotal (mW)
RXCLK	100	Low		**3**
TXCLK	75	Low		**2**
VXCLK	150	High		**5**
User DCM 4	0	Low		**0**
User DCM 5	0	Low		**0**
User DCM 6	0	Low		**0**
User DCM 7	0	Low		**0**
User DCM 8	0	Low		**0**
User DCM 9	0	Low		**0**
User DCM 10	0	Low		**0**
User DCM 11	0	Low		**0**
User DCM 12	0	Low		**0**
			Total	**10**

MGT Power

Table 8 shows the data entries required for the Multi-Gigabit Transceiver (MGT) power section. This section is used to estimate how much power the MGTs consume. The MGTs are available in the Virtex-II Pro architecture only. The number of MGTs in a device vary by device size, ranging from 0 to 24.

Table 8: **Multi-Gigabit Transceiver Power**

Name	Total Number of MGTs	Reference Clock Frequency (MHz)	Amplitude Setting (mV)		V_{CCINT} Subtotal (mW)	V_{CCAUX} Subtotal (mW)	$V_{CCAUXRX}$ Subtotal (mW)	$V_{CCAUXTX}$ Subtotal (mW)	V_{TRX} Subtotal (mW)	V_{TTX} Subtotal (mW)
XAUIMGT	2	100	800		35	60	126	231	54	54
User Module 2	0	0	800		0	0	0	0	0	0
User Module 3	0	0	800		0	0	0	0	0	0
User Module 4	0	0	800		0	0	0	0	0	0
User Module 5	0	0	800		0	0	0	0	0	0
User Module 6	0	0	800		0	0	0	0	0	0
User Module 7	0	0	800		0	0	0	0	0	0
User Module 8	0	0	800		0	0	0	0	0	0
User Module 9	0	0	800		0	0	0	0	0	0
User Module 10	0	0	800		0	0	0	0	0	0
User Module 11	0	0	800		0	0	0	0	0	0
User Module 12	0	0	800		0	0	0	0	0	0
				Total	35	60	126	231	54	54

Total Number of MGTs

The total number of MGTs in use in each user module.

Reference Clock Frequency

The clock frequency being applied to the MGT's reference clock (REFCLK) pin.

Amplitude Setting

Amplitude setting determines the pre-emphasis given to the MGT output. This defaults to 800 mV in the spreadsheet although there are five permissible values of 400, 500, 600, 700 and 800 mV.

Input/Output Power

Table 9 shows the data entries for the input/output power section. This section is used to estimate the power dissipation of the inputs and outputs. Users should try to group the I/Os into modules based on their I/O standard type. If the entire design has only one I/O standard type, all the I/Os can be treated as one module. However, separating the I/Os into smaller modules makes it easier to obtain better accuracy.

Table 9: **Input/Output Power**

Name	Frequency (MHz)	I/O Standard Type	Total Number of Inputs	Total Number of Outputs	Average IOB Toggle Rate (%)	Average Output Enable Rate (%)	Average Output Load (pF)	IOB Registers	V_{CCINT} Subtotal (mW)	V_{CCO} Subtotal (mW)
dbs_lvcmos	100	LVCMOS25_12	12	12	6%	100%	35	SDR	**1**	**10**
dbs_sstl	140	SSTL2_II	26	20	6%	100%	35	SDR	**47**	**110**
dbs_lvttl	75	LVTTL_8	16	16	13%	80%	35	SDR	**2**	**39**
User Module 4	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 5	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 6	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 7	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 8	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 9	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 10	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 11	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 12	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 13	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 14	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 15	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
User Module 16	0	LVCMOS25_12	0	0	0%	100%	35	SDR	**0**	**0**
								Total	**50**	**160**

Frequency (MHz)

This is the frequency of the module.

I/O Standard Type

This is the I/O standard used in the module. Each module may have only one I/O standard type. I/O power is strongly influenced by the I/O standard used. The permissible I/O standards vary between device families. Consult the device specific data sheet for supported standards.

Inputs

This is the total number of the inputs in each module.

Outputs

This is the total number of the outputs from each module.

Average I/O Block (IOB) Toggle Rate (%)

This number can be obtained in the same way as obtaining the Average Toggle Rate (%) in the CLB Logic Power section.

Average Output Enable Toggle Rate (%)

This number can be obtained in the same way as obtaining the Average Toggle Rate (%) in the CLB Logic Power section.

Average Output Load (pF)

This specifies the average capacitive load on the outputs.

IOB Registers

This defines the configuration of the IOB registers, either single data rate (SDR) or double-data rate (DDR). This selection is only available for devices in the Spartan-3, Virtex-II, or Virtex-II Pro families.

Results

The results section of the Power Estimator tools is shown in Table 10. Each section of the Power Estimator tool independently estimates power consumption, and displays the results at the end of the section. The total design power consumption is the summation of those, and is displayed at the very top of the program.

Table 10: **Results**

Target Device	Target Package	Total Estimated Design Power (mW)	Estimated Design										
			V_{CCINT} 1.5V Power (mW)	V_{CCAUX} 2.5V Power (mW)	V_{CCO} 3.3V Power (mW)	V_{CCO} 2.5V Power (mW)	V_{CCO} 1.8V Power (mW)	V_{CCO} 1.5V Power (mW)	V_{CCO} 1.2V Power (mW)	$V_{CCAUXRX}$ 2.5V Power (mW)	$V_{CCAUXTX}$ 2.5V Power (mW)	V_{TRX} 2.5V Power (mW)	V_{TTX} 2.5V Power (mW)
XC2VP7	FG456	1,582	885	73	39	120	0	0	0	126	231	54	54
Ambient Temperature (ºC)	**Air Flow (LFM)**	**Junction Temperature (ºC)**											
26	500	**47**											

Target Device

The target device allows user selection of the FPGA. No verification is performed to determine whether the module entries fit into the amount of resources available in the selected devices.

Target Package

The target package allows user selection of the targeted package. No verification is performed to determine whether the selected device-package combination is valid for Virtex and Virtex-E devices. The Virtex-II, Spartan-IIE, Spartan-3, and Virtex-II Pro tools link the two fields. Only valid combinations of device/package can be selected.

Estimated Total Power

This section displays the total power consumption of the design. It is the summation of all of the following power sections.

Estimated V_{CCINT} Power

This section displays the total power consumption from the core supply voltage (V_{CCINT}). It does not include the power consumption from the output source voltage (V_{CCO}).

Estimated V_{CCAUX} Power

This section displays power consumption for the auxiliary power source (V_{CCAUX}).

Estimated V_{CCO} 3.3V Power

This section displays the V_{CCO} power consumption for 3.3 V applications. The supported I/O standards using 3.3V V_{CCO} are LVCMOS33, LVTTL, LVPECL, PCI and PCI-X, SSTL3 Class I and II, CTT, and AGP.

Estimated V_{CCO} 2.5V Power

This section displays the V_{CCO} power consumption for 2.5 V applications. The supported I/O standards are LVDS, BLVDS, LVCMOS25, and SSTL2 Class I and II.

Estimated V_{CCO} 1.8V Power

This section displays the V_{CCO} power consumption for 1.8 V applications. The supported I/O standards are LVCMOS18, HSTL Class I_18, II_18, III_18, IV_18, and SSTL18 Class I and II.

Estimated V_{CCO} 1.5V Power

This section displays the V_{CCO} power consumption for 1.5 V applications. The supported I/O standards are LVCMOS15 and HSTL Class I, II, III, and IV.

Estimated V_{CCO} 1.2V Power

This section displays the V_{CCO} power consumption for 1.2 V applications. This is only applicable to the Spartan-3, Virtex-II, and Virtex-II Pro architectures.

Estimated $V_{CCAUXRX}$ 2.5V Power

This section displays the $V_{CCAUXRX}$ power consumption of the MGT receiver. This is only applicable to the Virtex-II Pro architecture.

Estimated $V_{CCAUXTX}$ 2.5V Power

This section displays the $V_{CCAUXTX}$ power consumption of the MGT transmitter. This is only applicable to the Virtex-II Pro architecture.

Estimated V_{TRX} 2.5V Power

This section displays the power consumption of V_{TRX} the input termination supply voltage of the MGT. This is only applicable to the Virtex-II Pro architecture.

Estimated V_{TTX} 2.5V Power

This section displays the power consumption of V_{TTX}, the output termination supply voltage of the MGT. This is only applicable to the Virtex-II Pro architecture.

Estimated Output Sink Power

This section displays the power consumption when sinking current to ground. It is applicable to Virtex, Virtex-E and Spartan-IIE designs only. The supported I/O standards (GTL and GTL+) require an open drain output buffer.

Ambient Temperature

This section is for the ambient temperature in degrees Celsius. This information is used in conjunction with the estimated power, air flow, and the thermal characteristics of the selected package to determine the junction temperature.

Air Flow

This section is for the linear feet-per-minute (LFM) airflow characteristics. The air flow has an impact on the junction temperature.

Conclusion

The ability to estimate power consumption in a design is imperative. After a successful functional simulation, check the power utilization using these tools for the following devices: Virtex, Virtex-E, Spartan-IIE, Spartan-3, Virtex-II, and Virtex-II Pro devices. The tools are available on the Xilinx web site at: http://www.xilinx.com/ise/power_tools.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/28/99	1.0	Initial release.
02/18/00	1.1	Reformatted text
06/03/03	2.0	Updated to include Virtex-E, Spartan-IIE, Virtex-II, and Virtex-II Pro devices.
09/19/03	2.1	Added Spartan-3 device support.