WM8728

24-bit, 192kHz Stereo DAC with Volume Control

DESCRIPTION

The WM8728 is a high performance stereo DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8728 supports PCM data input word lengths from 16 to 32-bits and sampling rates up to 192kHz. The WM8728 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a small 20-lead SSOP package. The WM8728 also includes a digitally controllable mute and attenuate function for each channel.

The WM8728 supports a variety of connection schemes for audio DAC control. The 2 or 3-wire MPU serial port provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available

The WM8728 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in DVD players supporting DVD-A.

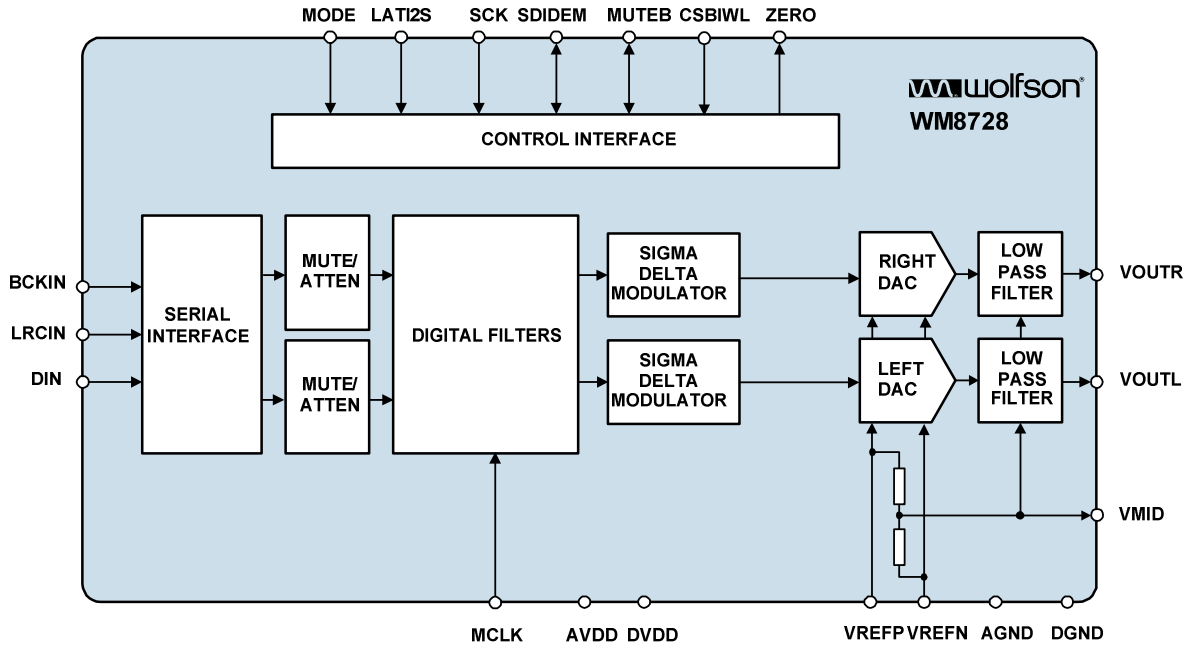
FEATURES

- Stereo DAC with 24 bit PCM
- Audio Performance
  - 106dB SNR ('A' weighted @ 48kHz) DAC
  - -97dB THD
- DAC Sampling Frequency: 8kHz - 192kHz
- 2 or 3-Wire Serial Control Interface or Hardware Control
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified, DSP
  - 16/20/24/32 bit Word Lengths
- Independent Digital Volume Control on Each Channel with 127.5dB Range in 0.5dB Steps
- 3.0V - 5.5V Supply Operation
- 20-lead SSOP Package
- Exceeds Dolby Class A Performance Requirements

APPLICATIONS

- DVD-Audio and DVD 'Universal' Players
- Home theatre systems
- Digital TV
- Digital broadcast receivers

BLOCK DIAGRAM



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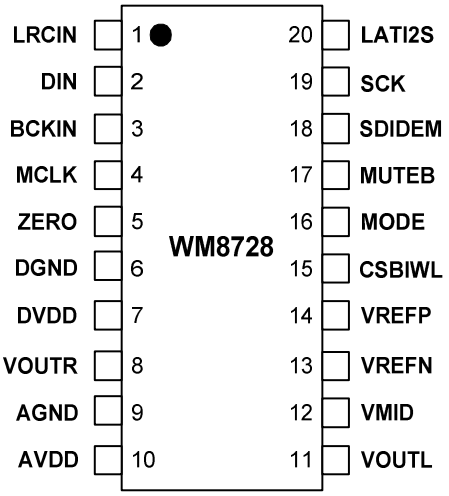
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMP
WM8728SEDS/V	-40 to +85°C	20-lead SSOP (Pb-free)	MSL2	260°C
WM8728SEDS/RV	-40 to +85°C	20-lead SSOP (Pb-free, tape and reel)	MSL2	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital Input	DAC Sample Rate Clock Input: PCM Input Mode
2	DIN	Digital Input	Serial Audio Data Input: PCM Input Mode
3	BCKIN	Digital Input	Audio Data Bit Clock Input
4	MCLK	Digital Input	Master Clock Input
5	ZERO	Digital Output (Open drain)	Infinite ZERO Detect Flag (L = IZD detected, H = IZD not detected).
6	DGND	Supply	Digital Ground Supply
7	DVDD	Supply	Digital Positive Supply
8	VOUTR	Analogue Output	Right Channel DAC Output
9	AGND	Supply	Analogue Ground Supply
10	AVDD	Supply	Analogue Positive Supply
11	VOUTL	Analogue Output	Left Channel DAC Output
12	VMID	Analogue Output	Mid Rail Decoupling Point
13	VREFN	Supply	DAC Negative Reference – normally AGND, must not be below AGND
14	VREFP	Supply	DAC Positive Reference – normally AVDD, must not be above AVDD
15	CSBIWL	Digital Input (pull-up)	Software Mode: 3-Wire Serial Control Chip Select Hardware Mode: Input Word Length
16	MODE	Digital Input (pull-down)	Control Mode Selection (L = Hardware, H = Software)
17	MUTEB	Digital Bi-directional	Mute Control (L = Mute on, H = Mute off, Z = Automute Enabled)
18	SDIDEM	Digital Bi-directional	Software Mode: 3 or 2-Wire Serial Control Data Input: Hardware Mode: De-Emphasis Select
19	SCK	Digital Input (pull-down)	Software Mode: 3 or 2-Wire Serial Control Clock Input
20	LATI2S	Digital Input (pull-up)	Software Mode 3-Wire Serial Control Load Input Hardware Mode: Input Data Format Selection

Note:

Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		50MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Note:
Analogue and digital grounds must always be within 0.3V of each other.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.0		5.5	V
Analogue supply range	AVDD		3.0		5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current		AVDD = 5V		19		mA
Digital supply current		DVDD = 5V		8		mA
Analogue supply current		AVDD = 3.3V		18		mA
Digital supply current		DVDD = 3.3V		4		mA

Note:

DVDD supply needs to be active before AVDD supply for correct device power on reset. See Power Supply Timing section.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL} = 1mA			DGND + 0.3V	V
Output HIGH	V_{OH}	I_{OH} = 1mA	DVDD – 0.3V			V
Analogue Reference Levels						
Reference voltage		VMID	(VREFP - VREFN)/2 - 50mV	(VREFP - VREFN)/2	(VREFP - VREFN)/2 + 50mV	V
Potential divider resistance	R_{VMID}			10k		Ω
DAC Output (Load = 10kΩ 50pF)						
0dBFs Full scale output voltage		At DAC outputs		1.1 x AVDD/5		Vrms
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz	100	106		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz		106		dB
SNR (Note 1,2,3)		A-weighted @ fs = 192kHz		106		dB
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz AVDD, DVDD = 3.3V		102		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz AVDD, DVDD = 3.3V		102		dB
SNR (Note 1,2,3)		Non 'A' weighted @ fs = 48kHz		103		dB
THD (Note 1,2,3)		1kHz, 0dBFs		-97		dB
THD+N (Dynamic range, Note 2)		1kHz, -60dBFs	100	106		dB
DAC channel separation				100		dB

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output level		Load = 10kΩ, 0dBFS		1.1		V_{RMS}
		Load = 10kΩ, 0dBFS, (AVDD = 3.3V)		0.726		V_{RMS}
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		1		kΩ
		To midrail or a.c. coupled (AVDD = 3.3V)		600		ohms
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				(VREFP - VREFN)/2		V
Power On Reset (POR)						
POR threshold				2.4		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all ZEROS into the digital input, over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full-scale output and the output with a ZERO signal applied. (No Auto-ZERO or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full-scale signal down one channel and measuring the other.

MASTER CLOCK TIMING

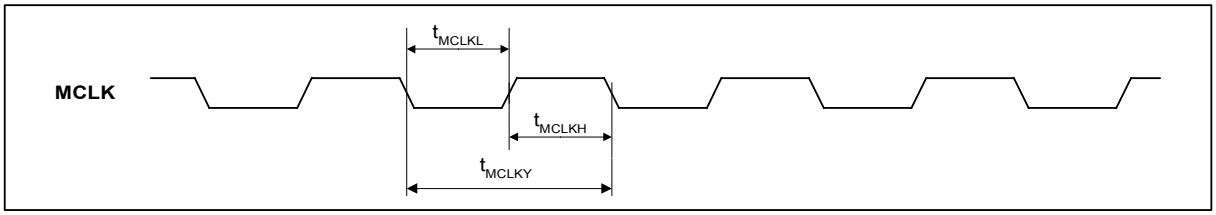


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		13			ns
MCLK Master clock pulse width low	t_{MCLKL}		13			ns
MCLK Master clock cycle time	t_{MCLKY}		26			ns
MCLK Duty cycle			40:60		60:40	

DIGITAL AUDIO INTERFACE

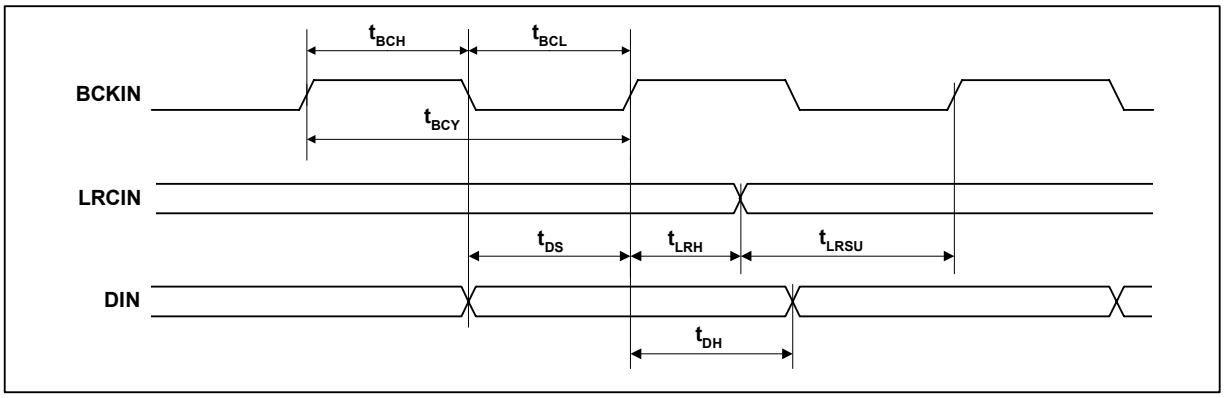


Figure 2 Digital Audio Data Timing

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from BCKIN rising edge	t_{LRH}		8			ns
DIN set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN hold time from BCKIN rising edge	t_{DH}		8			ns

POWER SUPPLY TIMING

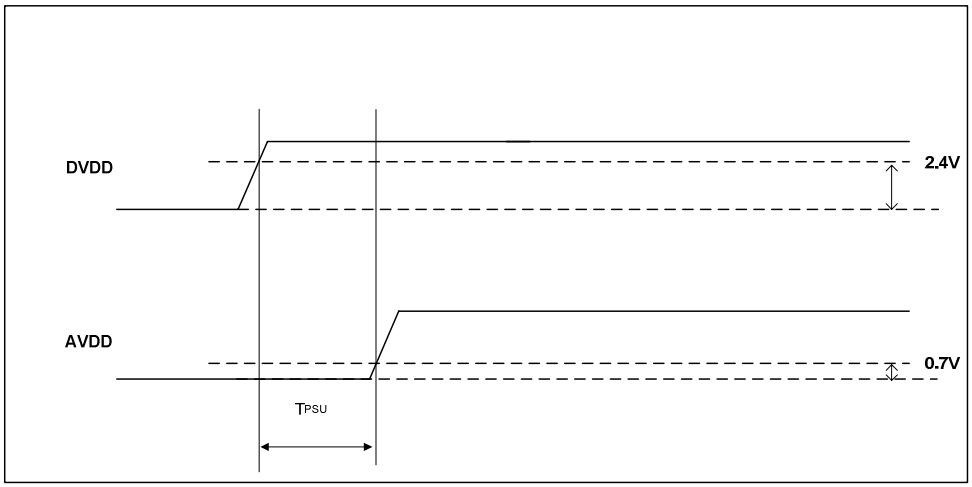


Figure 3 Power Supply Timing Requirements

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
DVDD set up time to AVDD rising edge	T_{PSU}	Measured from DVDD=+2.4V to AVDD=+0.7V	100			µs

POWER ON RESET (POR)

The WM8728 has an internal power-on-reset (POR) circuit which is used to reset the digital logic into a default state after power up. A block diagram of the reset circuit is shown in Figure 4

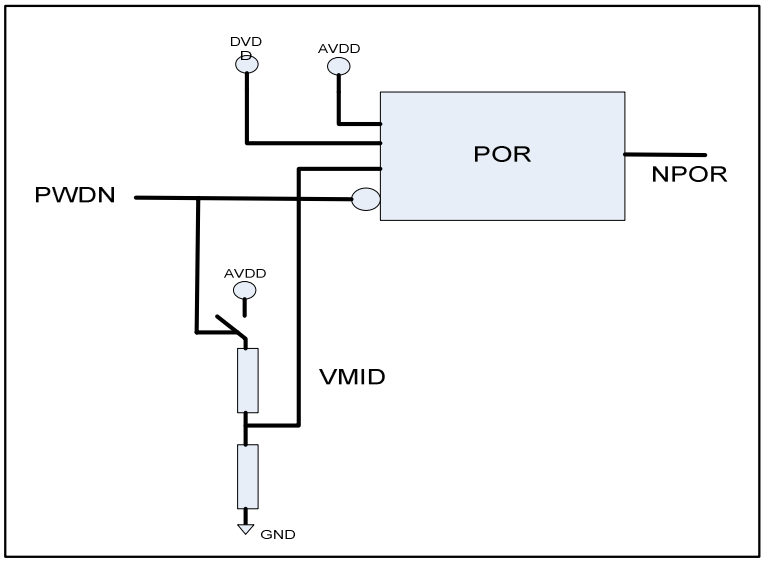


Figure 4 Block Diagram of Power-On-Reset Circuit

The POR circuit requires that the DVDD is applied before the AVDD. The active low reset signal NPOR will be asserted low until VMID rises to 1.2V. When this threshold has been reached, then the NPOR is released and the digital interface has been reset. This is illustrated in the diagram shown in Figure 5.

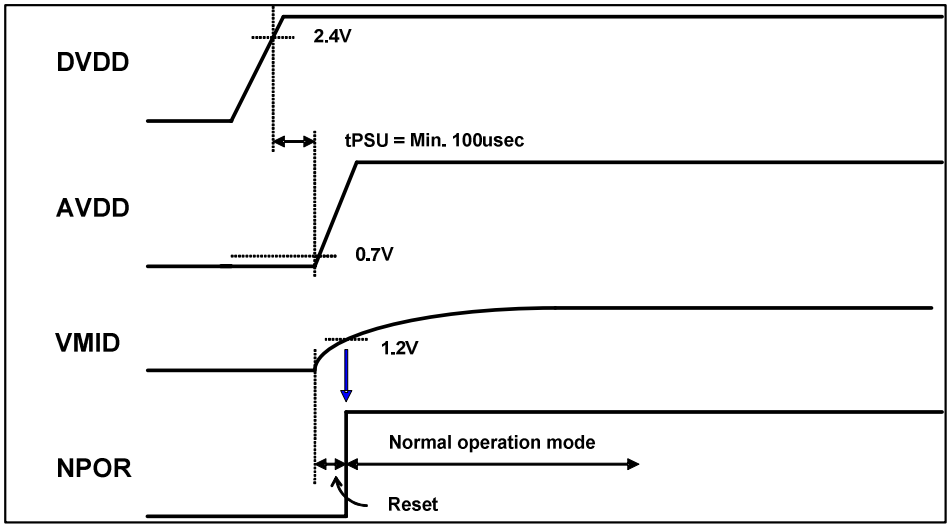


Figure 5 NPOR Generation At Power On Reset

Figure 6 and Figure 7 illustrate the NPOR generation when the AVDD and DVDD power are removed. Figure 6 illustrates the removal of DVDD before AVDD. Figure 7 illustrates the removal of AVDD before AVDD.

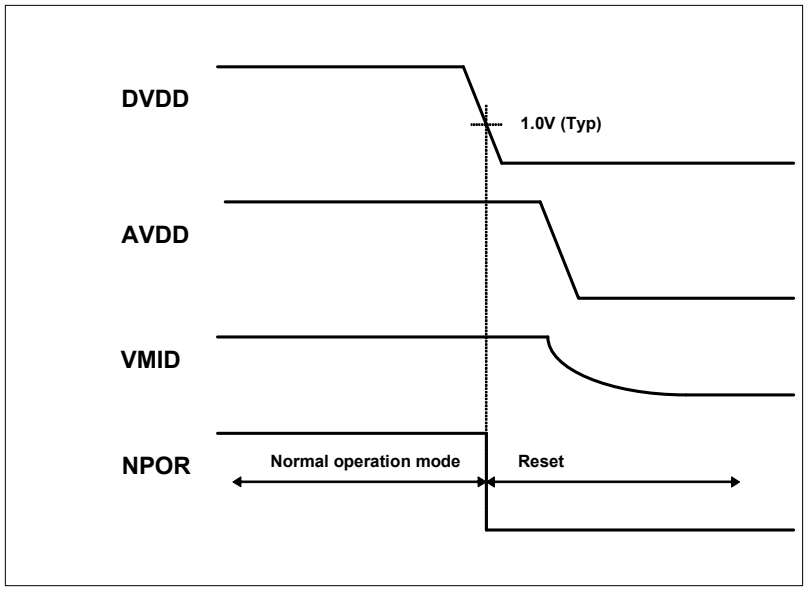


Figure 6 NPOR Generation at Power-off Reset (DVDD falls before AVDD)

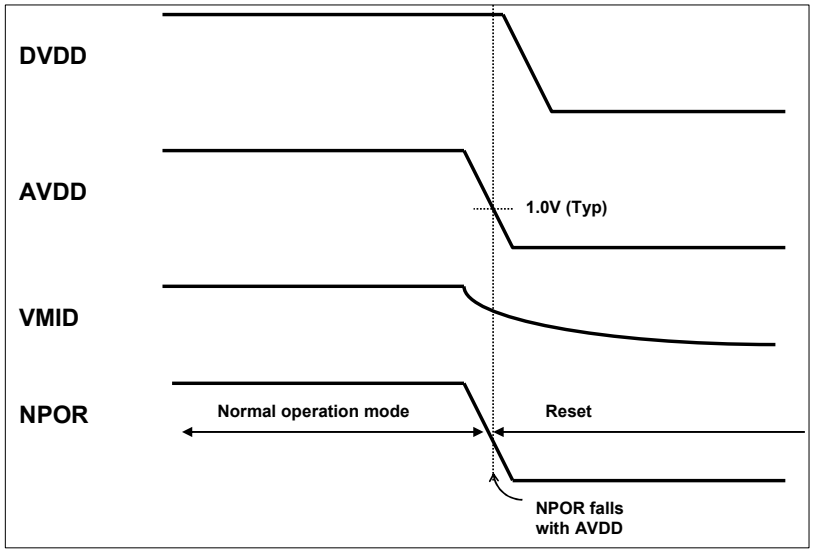


Figure 7 NPOR Generation at Power-off Reset (AVDD falls before DVDD)

MPU 3-WIRE INTERFACE TIMING

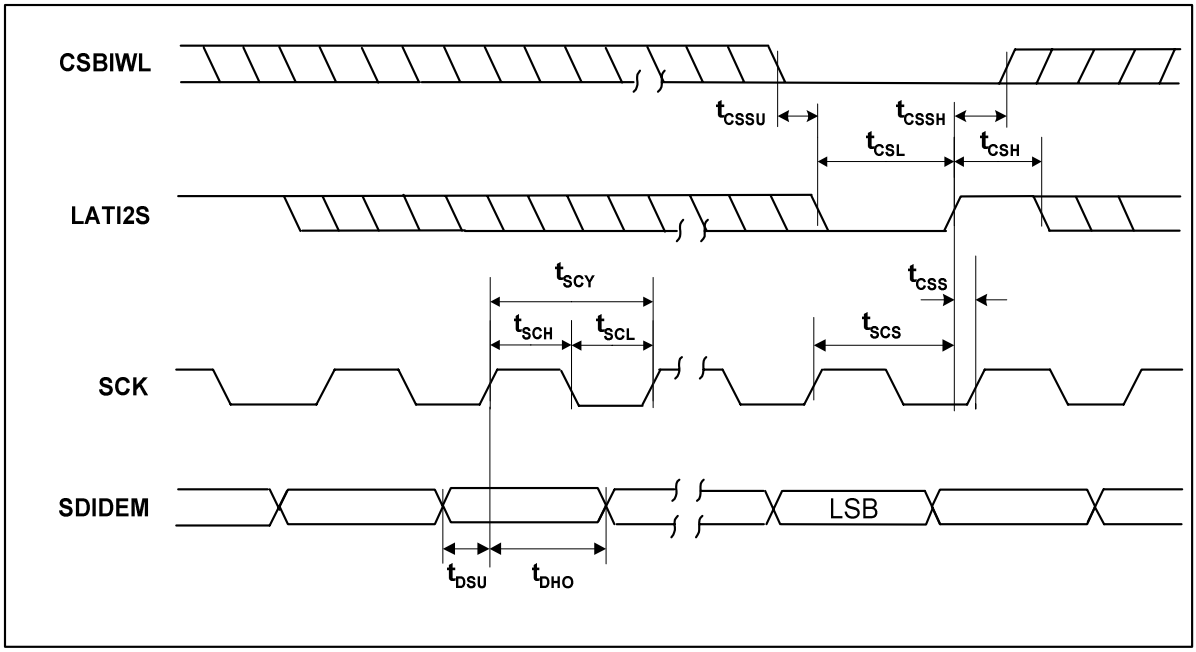


Figure 8 Program Register Input Timing - 3-Wire Serial Control Mode

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCK rising edge to LATI2S rising edge	t_{SCS}		40			ns
SCK pulse cycle time	t_{SCY}		80			ns
SCK pulse width low	t_{SCL}		20			ns
SCK pulse width high	t_{SCH}		20			ns
SDIDEM to SCK set-up time	t_{DSU}		20			ns
SCK to SDIDEM hold time	t_{DHO}		20			ns
LATI2S pulse width low	t_{CSL}		20			ns
LATI2S pulse width high	t_{CSH}		20			ns
LATI2S rising to SCK rising	t_{CSS}		20			ns
CSBIWL to LATI2S set-up time	t_{CSSU}		20			ns
LATI2S to CSBIWL hold time	t_{CSSH}		20			ns

MPU 2-WIRE INTERFACE TIMING

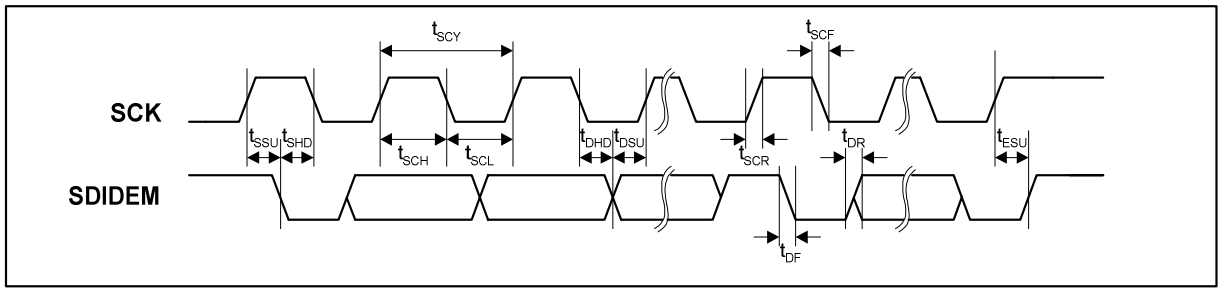


Figure 9 Program Register Input Timing - 2-Wire Serial Control Mode

Test Conditions

AVDD, DVDD = 5V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCK pulse cycle time	t_{SCY}		80			ns
SCK pulse width low	t_{SCL}		20			ns
SCK pulse width high	t_{SCH}		20			ns
SDIDEM to SCK data set-up time for start signal	t_{SSU}		10			ns
SDIDEM from SCK data hold time for start signal	t_{SHD}		10			ns
SDIDEM to SCK data set-up time	t_{DSU}		20			ns
SCK to SDIDEM data hold time	t_{DHD}		20			ns
SCK rise time	t_{SCR}		5			ns
SCK fall time	t_{SCF}		5			ns
SDIDEM rise time	t_{DR}		5			ns
SDIDEM fall time	t_{DF}		5			ns
SDIDEM to SCK data set-up time for stop signal	t_{ESU}		10			ns

Notes:

1. The address for the device in the 2-wire mode is 001101X (binary) with the last bit selectable.
2. In the two-wire interface mode, the CSBIWL pin indicates the final bit of the chip address.
3. In 2-wire mode the LATI2S pin should be tied to either DGND or DVSS to avoid noise toggling the interface into 3-wire mode.

DEVICE DESCRIPTION

INTRODUCTION

The WM8728 is a high performance DAC designed for digital consumer audio applications. Its range of features makes it ideally suited for use in DVD players, AV receivers and other high-end consumer audio equipment.

WM8728 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, switched capacitor multi-bit stereo DAC and output smoothing filters. The WM8728 includes an on-chip digital volume control, configurable digital audio interface and a 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

Control of internal functionality of the device is by either hardware control (pin programmed) or software control (2 or 3-wire serial control interface). The MODE pin selects between hardware and software control. The software control interface may be asynchronous to the audio data interface. In which case control data will be re-synchronised to the audio processing internally.

Operation using a master clock of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled in hardware mode, or serial controlled when in software mode. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate master clock is input. Support is also provided for up to 192ks/s using a master clock of 128fs or 192fs.

The audio data interface supports right justified, left justified and I^2S (Philips left justified, one bit delayed) interface formats along with a highly flexible DSP serial port interface. When in hardware mode, the three serial interface pins become control pins to allow selection of, input data format type (I^2S or right justified), input word length (20 or 24 bit) and de-emphasis functions.

The device is packaged in a small 20-pin SSOP.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary for sample rate selection.

Note that on the WM8728, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

WM8728 always acts as a slave and requires clocks to be inputs.

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP mode A
- DSP mode B

All five formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits with the exception that 32 bit data is not supported in right justified mode. DIN and LRCIN maybe configured to be sampled on the rising or falling edge of BCKIN.

In left justified, right justified and I^2S modes, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words. The minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met

The WM8728 will automatically detect when data with a LRCIN period of exactly 32 BCKINs is sent, and select 16-bit mode - overriding any previously programmed word length. Word length will revert to a programmed value only if a LRCIN period other than 32 BCKINs is detected.

In DSP mode A or B, the data is time multiplexed onto DIN. LRCIN is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCKINs per LRCIN period is 2 times the selected word length. Any mark to space ratio is acceptable on LRCIN provided the rising edge is correctly positioned. (See Figure 13 and Figure 14)

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCKIN following a LRCIN transition. LRCIN is high during the left data word and low during the right data word.

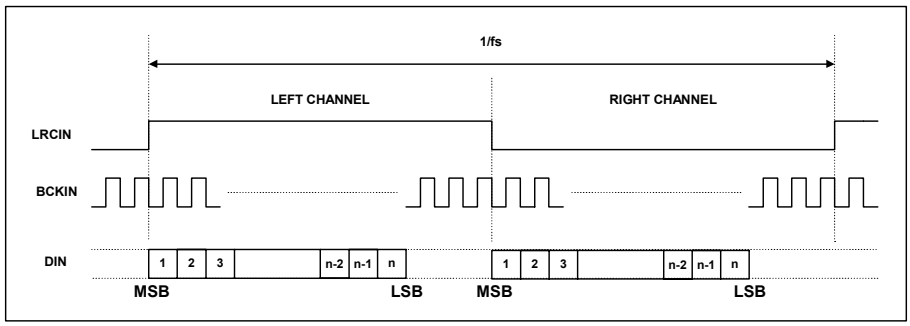


Figure 10 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left data word and low during the right data word.

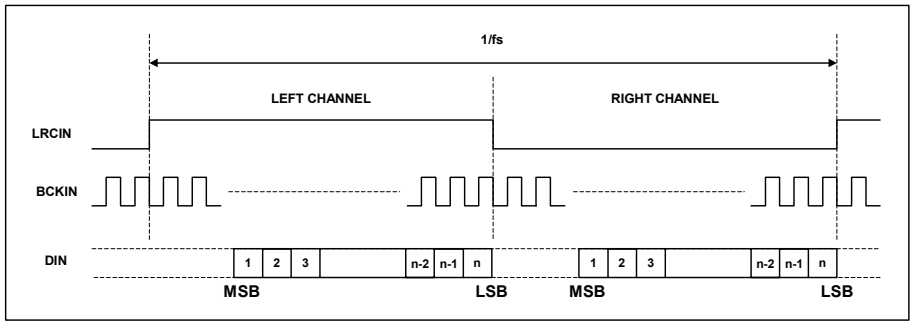


Figure 11 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left data word and high during the right data word.

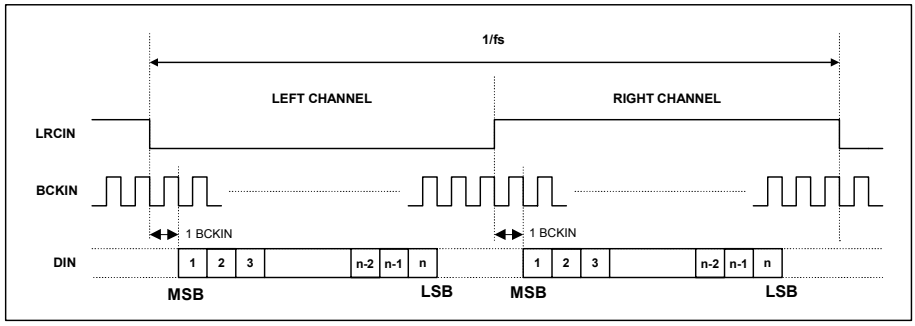


Figure 12 I²S Mode Timing Diagram

DSP MODE A

In DSP mode A, the first bit is sampled on the BCKIN rising edge following the one that detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

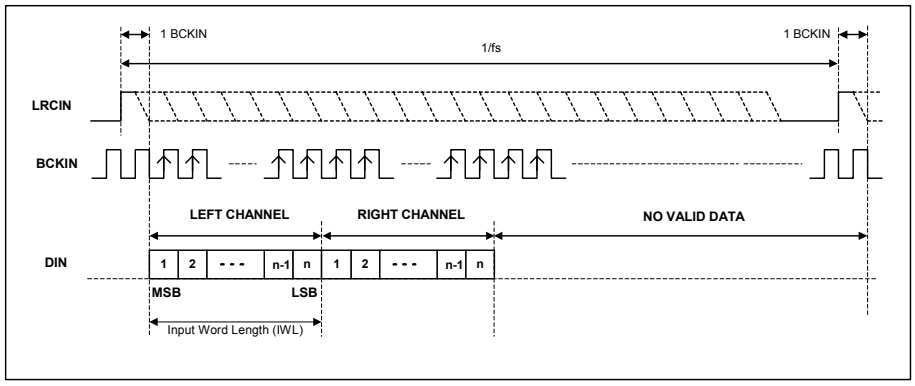


Figure 13 DSP Mode A Timing Diagram

DSP MODE B

In DSP mode B, the first bit is sampled on the BCKIN rising edge, which detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

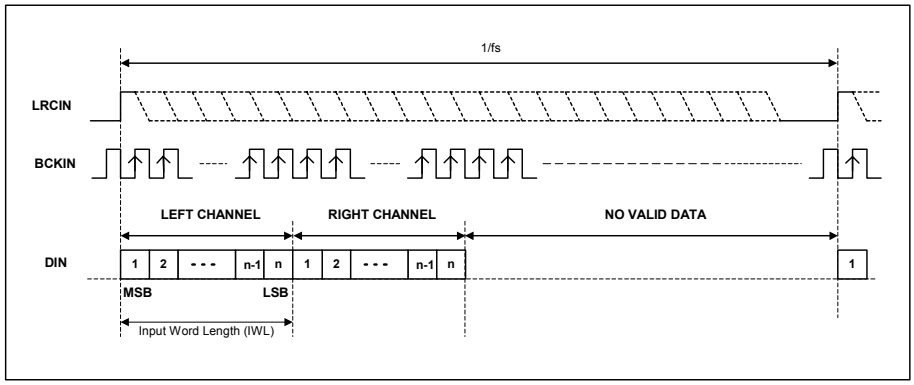


Figure 14 DSP Mode B Timing Diagram

AUDIO DATA SAMPLING RATES

The master clock for WM8728 can range from 128fs to 768fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8728 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error, the interface shuts down the DAC and mutes the output. The master clock should be synchronised with LRCIN, although the WM8728 is tolerant of phase differences or jitter on this clock. See Table 1

SAMPLING RATE (LRCIN)	MASTER CLOCK FREQUENCY (MHZ) (MCLK)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.114	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 Typical Relationships Between Master Clock Frequency and Sampling Rate

HARDWARE CONTROL MODES

When the MODE pin is held low, the following hardware modes of operation are available.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes, pin 17 (MUTEB) controls the selection of MUTE directly, and can be used to enable and disable the automute function. Automute is enabled by leaving MUTEB pin floating, it is disabled by applying a signal to the pin. When left floating this pin becomes an output and indicates infinite ZERO detect (IZD), see also pin 5 (ZERO). The status of IZD controls the selection of MUTE when automute is enabled. When IZD is detected MUTE is enabled and when IZD is not detected MUTE is disabled.

MUTEB PIN	DESCRIPTION
0	Mute DAC channels
1	Normal Operation
Floating	MUTEB becomes an output to indicate when IZD occurs. L=IZD detected (MUTE enabled), H=IZD not detected (MUTE disabled).

Table 2 Mute and Automute Control

ZERO PIN	DESCRIPTION
0	Indicates Infinite Zero detected from the digital input.
1	Indicates Infinite Zero not detected from the digital input.

Table 3 Zero Pin Output

Figure 15 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. When MUTE is de-asserted, the output will restart almost immediately from the current input sample.

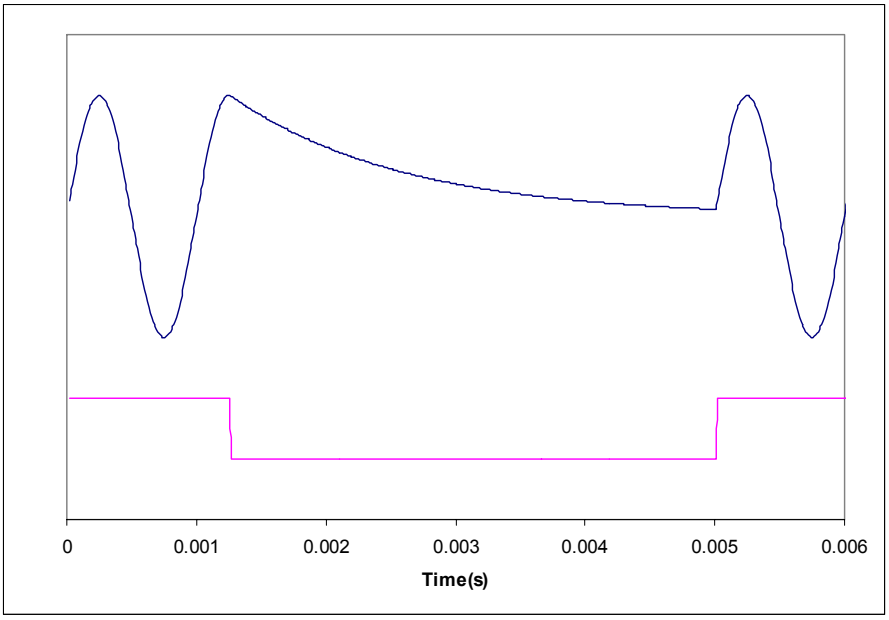


Figure 15 Application and Release of Soft Mute

The MUTEB pin is an input to select mute or not mute. MUTEB is active low; taking the pin low causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTEB high again allows data into the filter.

The automute function detects a series of ZERO value audio samples of 1024 samples long being applied to both channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a 10kohm resistor to the MUTEB pin. Thus if the MUTEB pin is not being driven, the automute function will assert mute.

If MUTEB is tied high, AUTOMUTED is overridden and will not mute unless the IZD register bit is set. If MUTEB is driven from a bi-directional source, then both MUTE and automute functions are available. If MUTEB is not driven, AUTOMUTED appears as a weak output (10kOhm-source impedance) so can be used to drive external mute circuits. AUTOMUTED will be removed as soon as any channel receives a non-ZERO input.

A diagram showing how the various Mute modes interact is shown below Figure 16.

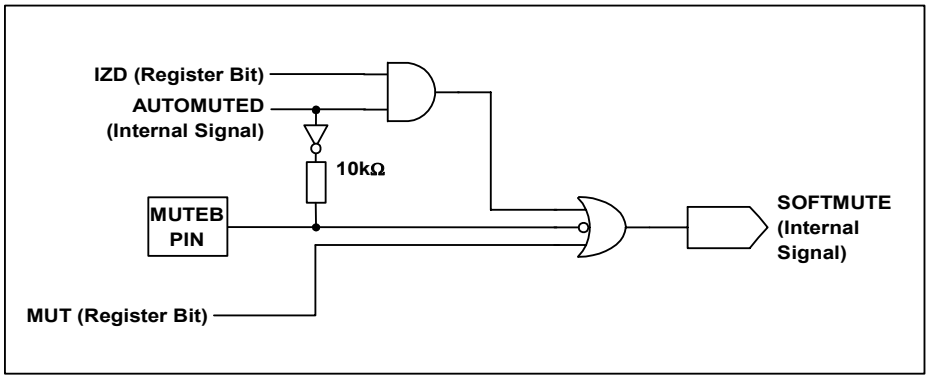


Figure 16 Selection Logic for MUTE Modes

INPUT FORMAT SELECTION

In hardware mode, LATI2S (pin 20) and CSBIWL (pin 15) become input controls for selection of input data format type and input data word length.

LATI2S	CSBIWL	INPUT DATA MODE
0	0	24-bit right justified
0	1	20-bit right justified
1	0	16-bit I^2S
1	1	24-bit I^2S

Table 4 Input Format Selection

Note:

In 24 bit I^2S mode, any width of 24 bits or less is supported provided that LRCIN is high for a minimum of 24 BCKINs and low for a minimum of 24 BCKINs. If exactly 32 BCKINs occur in one LRCIN (16 high, 16 low) the chip will auto detect and run a 16 bit data mode.

DE-EMPHASIS CONTROL

In hardware mode, SDIDEM (pin 18) becomes an input control for selection of de-emphasis filtering to be applied.

SDIDEM	DE-EMPHASIS
0	Off
1	On

Table 5 De-emphasis Control

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using a 2-wire interface compatible or 3-wire (SPI-compatible) interface.

SELECTION OF CONTROL MODE

The WM8728 may be programmed to operate in hardware or software control modes. This is achieved by setting the state of the MODE pin.

MODE	INTERFACE FORMAT
0	Hardware Control Mode
1	Software Control Mode

Table 6 Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

In this mode, SDIDEM is used for the program data, SCK is used to clock in the program data and LATI2S is used to latch in the program data. The 3-wire interface protocol is shown in Figure 17.

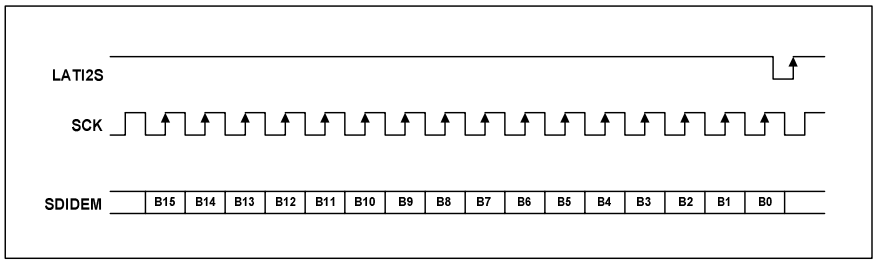


Figure 17 3-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CSBIWL needs to be low during writes – see **Figure 8**

2-WIRE SERIAL CONTROL MODE

In 2-wire mode, which is the default, SDIDEM is used for the program data and SCK is used to clock in the program data see Figure 18.

WM8728 has an address of 001101X (binary) which represents an audio device. The final address digit is dependent on pin CSBIWL, which should be tied to either DVDD or DGND. This allows the device to have a choice of two identification header addresses used in the 2 wire interface word. This feature allows more than one WM8728 device to be present on the interface bus.

LATI2S should be tied to either DVDD or DGND, as it is unused. This pin if toggled from low to high and high to low, will cause the device to enter the 3-wire interface mode and cannot be placed back into 2-wire mode except by toggling the MODE pin, or powering off the device.

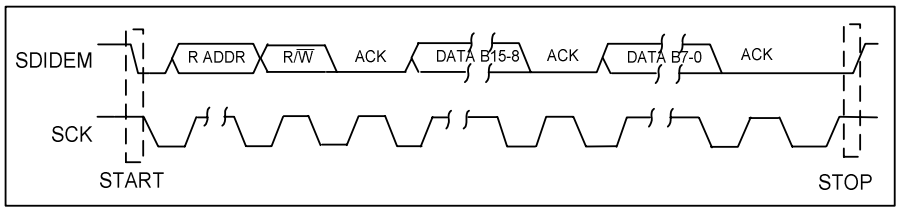


Figure 18 2-Wire Serial Interface

REGISTER MAP

WM8728 uses a total of 4 program registers, which are 16-bits long. These registers are all loaded through input pin SDIDEM. Using either 2-wire or 3-wire serial control mode as shown Figure 8 and Figure 9

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
M0	0	0	0	0	0	0	0	UPDATEL	LAT7	LAT6	LAT5	LAT4	LAT3	LAT2	LAT1	LAT0
M1	0	0	0	0	0	0	1	UPDATER	RAT7	RAT6	RAT5	RAT4	RAT3	RAT2	RAT1	RAT0
M2	0	0	0	0	0	1	0	0	0	0	IW2	IW1	IW0	PWDN	DEEMPH	MUT
M3	0	0	0	0	0	1	1	IZD	0	0	BCP	REV	0	ATC	LRP	I^2S
	ADDRESS							**DATA**								

Table 7 Mapping of Program Registers

REGISTER ADDRESS (A3,A2,A1,A0)	BITS	NAME	DEFAULT	DESCRIPTION
0000 DACL Attenuation	[7:0]	LAT[7:0]	11111111 (0dB)	Attenuation data for left channel in 0.5dB steps, see Table 10
	8	UPDATEL	0	Attenuation data load control for left channel. 0: Store DACL in intermediate latch (no change to output) 1: Store DACL and update attenuation on both channels.
0001 DACR Attenuation	[7:0]	RAT[7:0]	11111111 (0dB)	Attenuation data for right channel in 0.5dB steps, see Table 10
	8	UPDATER	0	Attenuation data load control for right channel. 0: Store DACR in intermediate latch (no change to output) 1: Store DACR and update attenuation on both channels.
0010 DAC Control	0	MUT	0	Left and right DACs soft mute control. 0: No mute 1: Mute
	1	DEEMPH	0	De-emphasis control. 0: De-emphasis off 1: De-emphasis on
	2	PWDN	0	Left and Right DACs Power-down Control 0: All DACs running, output is active 1: All DACs in power saving mode, output muted
	[5:3]	IW[2:0]	0	Audio data format select, see Table 15
0011 Interface Control	0	I^2S	0	Audio data format select, see Table 15
	1	LRP	0	Polarity select for LRCIN/DSP mode select. 0: normal LRCIN polarity/DSP late mode 1: inverted LRCIN polarity/DSP early mode
	2	ATC	0	Attenuator Control. 0: All DACs use attenuation as programmed. 1: Right channel DACs use corresponding left DAC attenuation
	4	REV	0	Output phase reverse.
	5	BCP	0	BCKIN Polarity 0 : normal BCKIN polarity 1: inverted BCKIN polarity
	8	IZD	0	Infinite ZERO detection circuit control and automute control 0: Infinite ZERO detect disabled 1: Infinite ZERO detect enabled

Table 8 Register Bit Descriptions

ATTENUATION CONTROL

Each DAC channel can be attenuated digitally before being applied to the digital filter. Attenuation is 0dB by default but can be set between 0 and 127.5dB in 0.5dB steps using the 8 Attenuation control bits. All attenuation registers are double latched allowing new values to be pre-latched to both channels before being updated synchronously. Setting the UPDATE bit on any attenuation write will cause all pre-latched values to be **immediately** applied to the DAC channels.

REGISTER ADDRESS	BITS	LABEL	DEFAULT	DESCRIPTION
0000 Attenuation DACL	[7:0]	LAT[7:0]	11111111 (0dB)	Attenuation data for Left channel DACL in 0.5dB steps.
	8	UPDATEL	0	Controls simultaneous update of all Attenuation Latches 0: Store DACL in intermediate latch (no change to output) 1: Store DACL and update attenuation on all channels.
0001 Attenuation DACR	[7:0]	RAT[7:0]	11111111 (0dB)	Attenuation data for Right channel DACR in 0.5dB steps.
	8	UPDATER	0	Controls simultaneous update of all Attenuation Latches 0: Store DACR in intermediate latch (no change to output) 1: Store DACR and update attenuation on all channels.

Table 9 Attenuation Register Map

Note:

1. The UPDATE bit is not latched. If UPDATE=0, the Attenuation value will be written to the pre-latch but not applied to the relevant DAC. If UPDATE=1, all pre-latched values and the current value being written will be applied on the next input sample.

2. Care should be used in reducing the attenuation as rapid large volume changes can introduce zipper noise.

DAC OUTPUT ATTENUATION

Registers LAT and RAT control the left and right channel attenuation. Table 9 shows how the attenuation levels are selected from the 8-bit words.

XAT[7:0]	ATTENUATION LEVEL
00(hex)	∞dB (mute)
01(hex)	127dB
:	126.5 dB
:	:
:	:
FE(hex)	0.5dB
FF(hex)	0dB

Table 10 Attenuation Control Levels

MUTE MODES

Setting the MUT register bit will apply a 'soft' mute to the input of the digital filters:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 DAC Control	0	MUT	0	Soft Mute select 0 : Normal Operation 1: Soft mute all channels

Table 11 Mute control

DE-EMPHASIS MODE

Setting the DEEMPH register bit puts the digital filters into de-emphasis mode:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 DAC Control	1	DEEMPH	0	De-emphasis mode select: 0 : De-emphasis Off 1: De-emphasis On

Table 12 De-emphasis Control

POWERDOWN MODE

Setting the PWDN register bit immediately connects all outputs to V_{MID} and selects a low power mode. All trace of the previous input samples is removed, and all control register settings are cleared. When PWDN is cleared again the first 16 input samples will be ignored, as the FIR will repeat it's power-on initialisation sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 DAC Control	2	PWDN	0	Power Down Mode Select: 0 : Normal Mode 1: Power Down Mode

Table 13 Powerdown control

DIGITAL AUDIO INTERFACE CONTROL REGISTERS

The WM8728 has a fully featured digital audio interface that is a superset of that contained in the WM8716. Interface format is selected via the IWL[2:0] register bits in register M2 and the I^2S register bit in M3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 DAC Control	5:3	IWL[2:0]	000000	Interface format Select
0011 Interface Control	0	I^2S	0	Interface format Select

Table 14 Interface Format Controls

IW2	I^2S	IW1	IW0	AUDIO INTERFACE DESCRIPTION (NOTE 1)
0	0	0	0	16 bit right justified mode
0	0	0	1	20 bit right justified mode
0	0	1	0	24 bit right justified mode
0	0	1	1	24 bit left justified mode
0	1	0	0	16 bit I^2S mode
0	1	0	1	24 bit I^2S mode
0	1	1	0	20 bit I^2S mode
0	1	1	1	20 bit left justified mode
1	0	0	0	16 bit DSP mode
1	0	0	1	20 bit DSP mode
1	0	1	0	24 bit DSP mode
1	0	1	1	32 bit DSP mode
1	1	0	0	16 bit left justified mode

Table 15 Audio Data Input Format

Note:

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8728 pads the unused LSBs with ZEROS. If the DAC is programmed into 32-bit mode, the 8 LSBs are treated as zero.

SELECTION OF LRCIN POLARITY

In left justified, right justified or I^2S modes, the LRP register bit controls the polarity of LRCIN. If this bit is set high, the expected polarity of LRCIN will be the opposite of that shown in Figure 10, Figure 11 and Figure 12. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	1	LRP	0	LRCIN Polarity (normal) 0 : normal LRCIN polarity 1: inverted LRCIN polarity

Table 16 LRCIN Polarity Control

In DSP modes, the LRCIN register bit is used to select between early and late modes (see Figure 13 and Figure 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	1	LRP	0	DSP Format (DSP modes) 0 : Late DSP mode 1: Early DSP mode

Table 17 DSP Format Control

In DSP early mode, the first bit is sampled on the BCKIN rising edge following the one that detects a low to high transition on LRCIN. In DSP late mode, the first bit is sampled on the BCKIN rising edge, which detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	2	ATC	0	Attenuator Control Mode: 0 : Right channels use Right attenuation 1: Right Channels use Left Attenuation

Table 18 Attenuation Control Select

OUTPUT PHASE REVERSAL

The REV register bit controls the phase of the output signal. Setting the REV bit causes the phase of the output signal to be inverted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	4	REV	0	Analogue Output Phase 0: Normal 1: Inverted

Table 19 Output Phase Control

BCKIN POLARITY

By default, LRCIN and DIN are sampled on the rising edge of BCKIN and should ideally change on the falling edge. Data sources which change LRCIN and DIN on the rising edge of BCKIN can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCKIN to the inverse of that shown in Figure 10, Figure 11, Figure 12, Figure 13 and Figure 14.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	5	BCP	0	BCKIN Polarity 0 : normal BCKIN polarity 1: inverted BCKIN polarity

Table 20 BCKIN Polarity Control

INFINITE ZERO DETECTION

Setting the IZD register bit determines whether the device is automuted when a sequence of more than 1024 ZEROS is detected.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Interface Control	8	IZD	0	Infinite ZERO detection circuit control and automute control 0: Infinite ZERO detect disabled 1: Infinite ZERO detect enabled

Table 21 IZD Control

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.05	dB
Stopband Attenuation		f > 0.555fs	-60			dB

Table 22 Digital Filter Characteristics

DAC FILTER RESPONSES

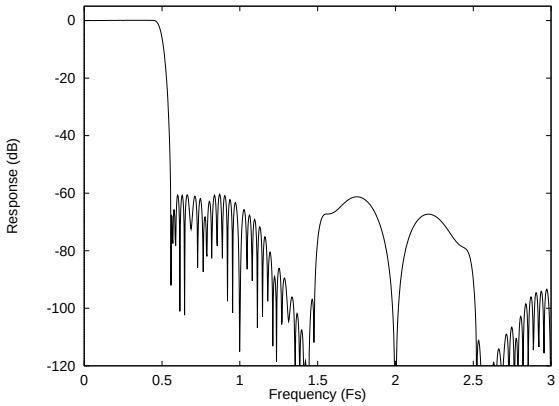


Figure 19 DAC Digital Filter Frequency Response -44.1, 48 and 96kHz

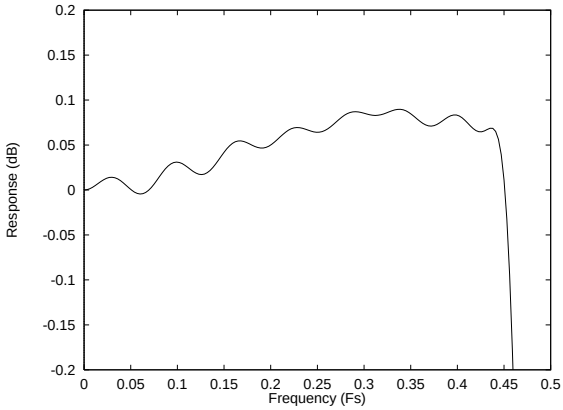


Figure 20 DAC Digital Filter Ripple -44.1, 48 and 96kHz

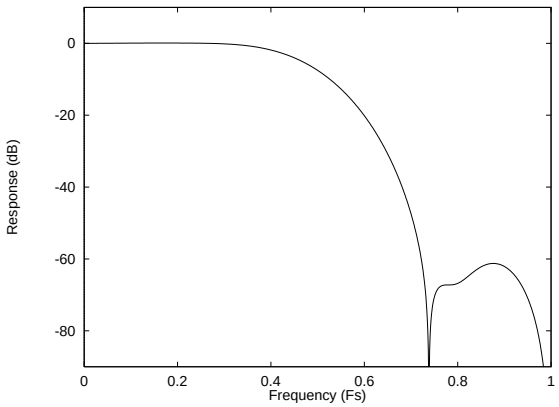


Figure 21 DAC Digital Filter Frequency Response -192kHz

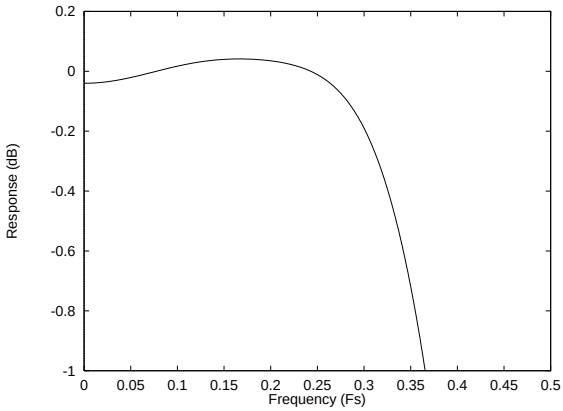


Figure 22 DAC Digital Filter Ripple -192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

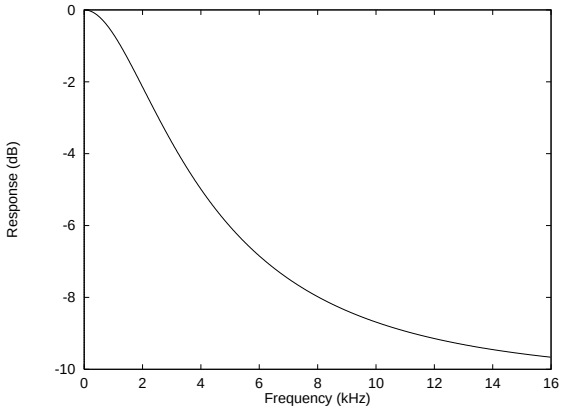


Figure 23 De-Emphasis Frequency Response (32kHz)

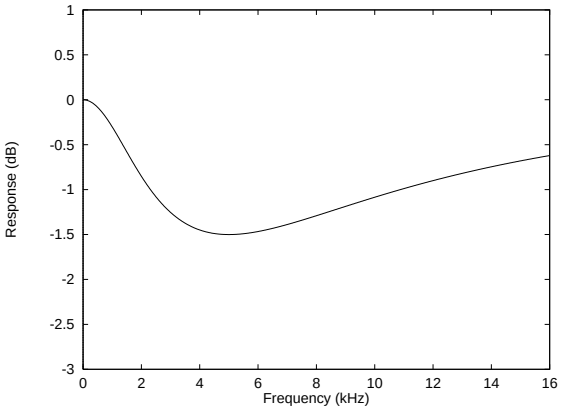


Figure 24 De-Emphasis Error (32kHz)

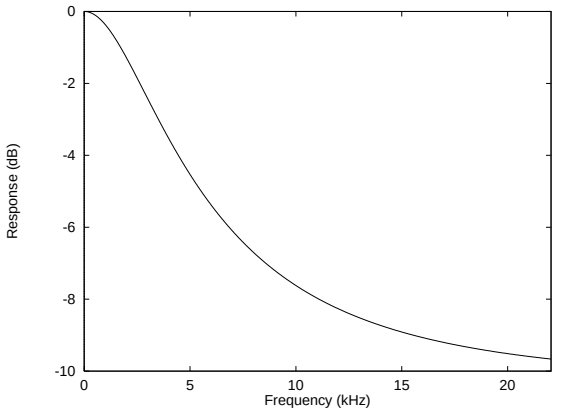


Figure 25 De-Emphasis Frequency Response (44.1kHz)

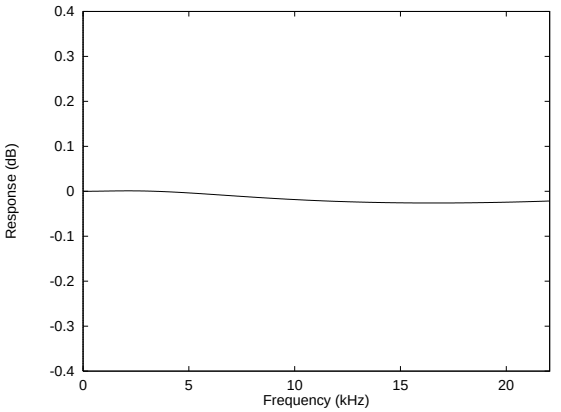


Figure 26 De-Emphasis Error (44.1kHz)

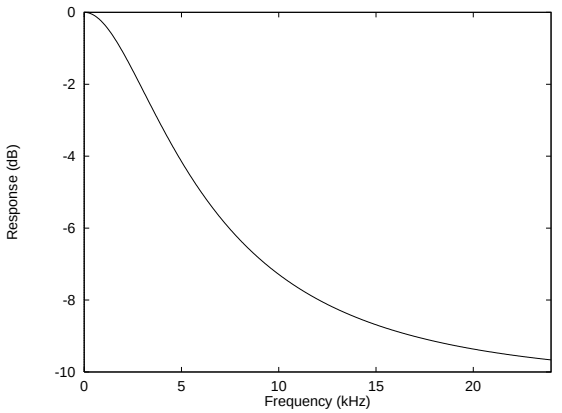


Figure 27 De-Emphasis Frequency Response (48kHz)

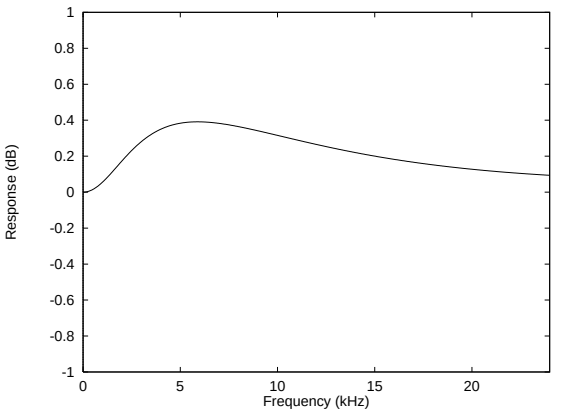
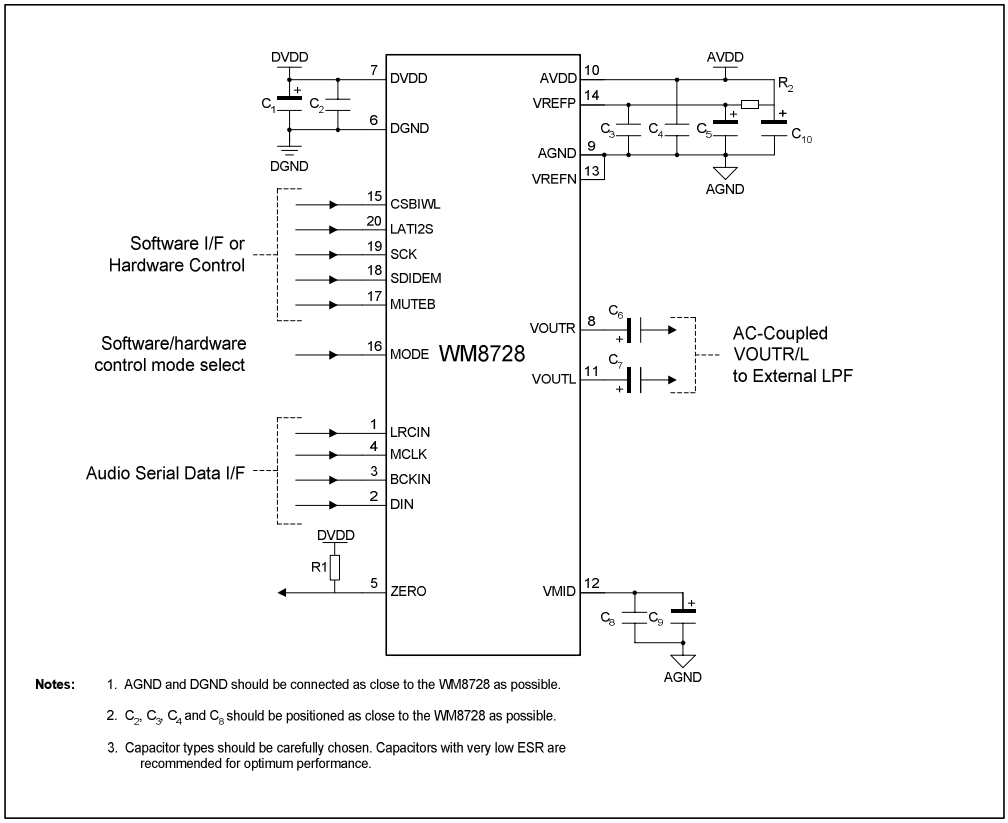


Figure 28 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS (PCM AUDIO)



Notes:
1. AGND and DGND should be connected as close to the WM8728 as possible.
2. C_2, C_3, C_4 and C_8 should be positioned as close to the WM8728 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

Figure 29 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C5	10µF	De-coupling for DVDD and AVDD/VREFP
C2 to C4	0.1µF	De-coupling for DVDD and AVDD/VREFP
C6 and C7	10µF	Output AC coupling caps to remove midrail DC level from outputs.
C8	0.1µF	Reference de-coupling capacitors for VMID pin.
C9	10µF	
C10	10µF	Filtering for VREFP. Omit if AVDD low noise.
R1	10kΩ	10k pull-up to DVDD
R2	33Ω	Filtering for VREP. Use 0Ω if AVDD low noise.

Table 23 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER FOR PCM DATA FORMAT (OPTIONAL)

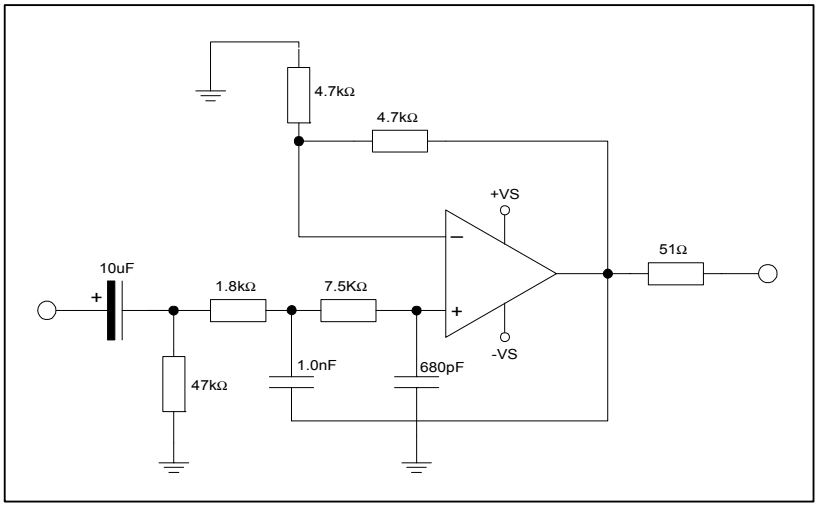
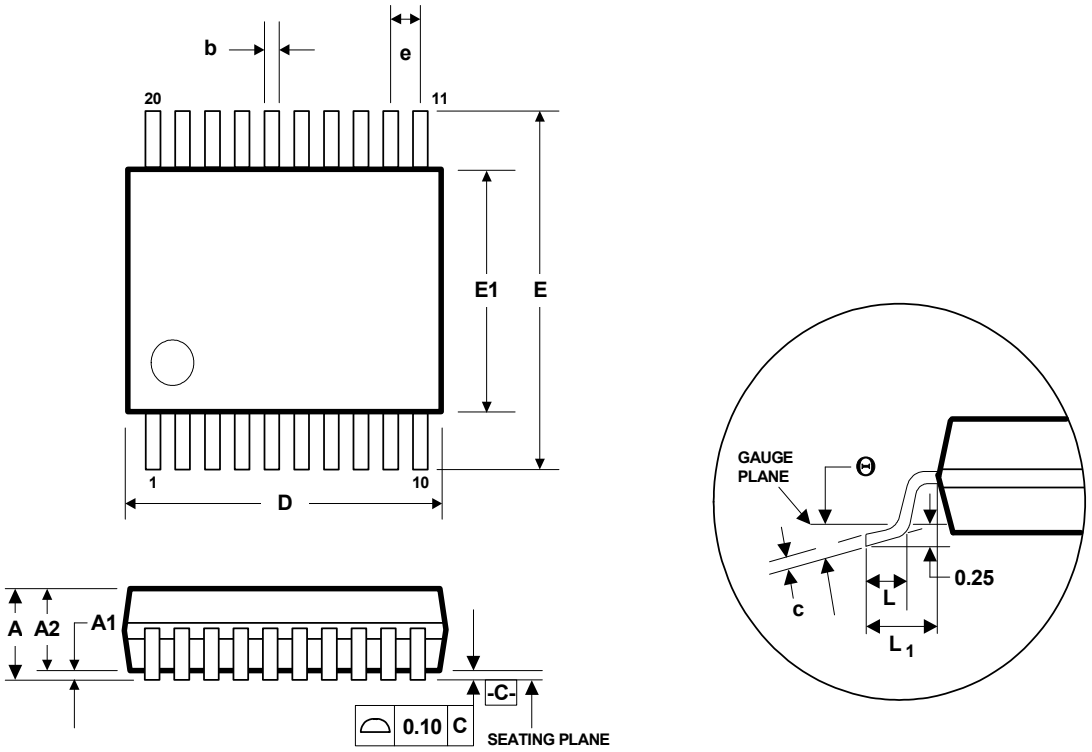


Figure 30 Recommended Low Pass Filter (Optional)

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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