64-NOTE POLYPHONIC RINGTONE CHIP

1. GENERAL DESCRIPTION

The W56964 is designed for the ringtone application of cell phones with 64-note MIDI plus ADPCM/PCM synthesis. This single chip consists of a CPU interface, FIFO buffering, a wavetable sound set, a MIDI sequencer, a wavetable synthesizer, DAC, and a power amplifier to drive an 8-ohm speaker directly.

With an on-chip, high-quality, GM-compliant sound set, the W56964 supports up to 128 instruments and 47 drums for playback of any MIDI songs with up to 64 notes simultaneously. MIDI songs in various formats can be downloaded and played back via the CPU interface between the baseband CPU and W56964.

The ADPCM/PCM synthesizer is designed to allow for customized SFX (sound effects), in addition to ordinary MIDI songs. The sound effects can be played along with the MIDI tunes for more fantastic sound experiences.

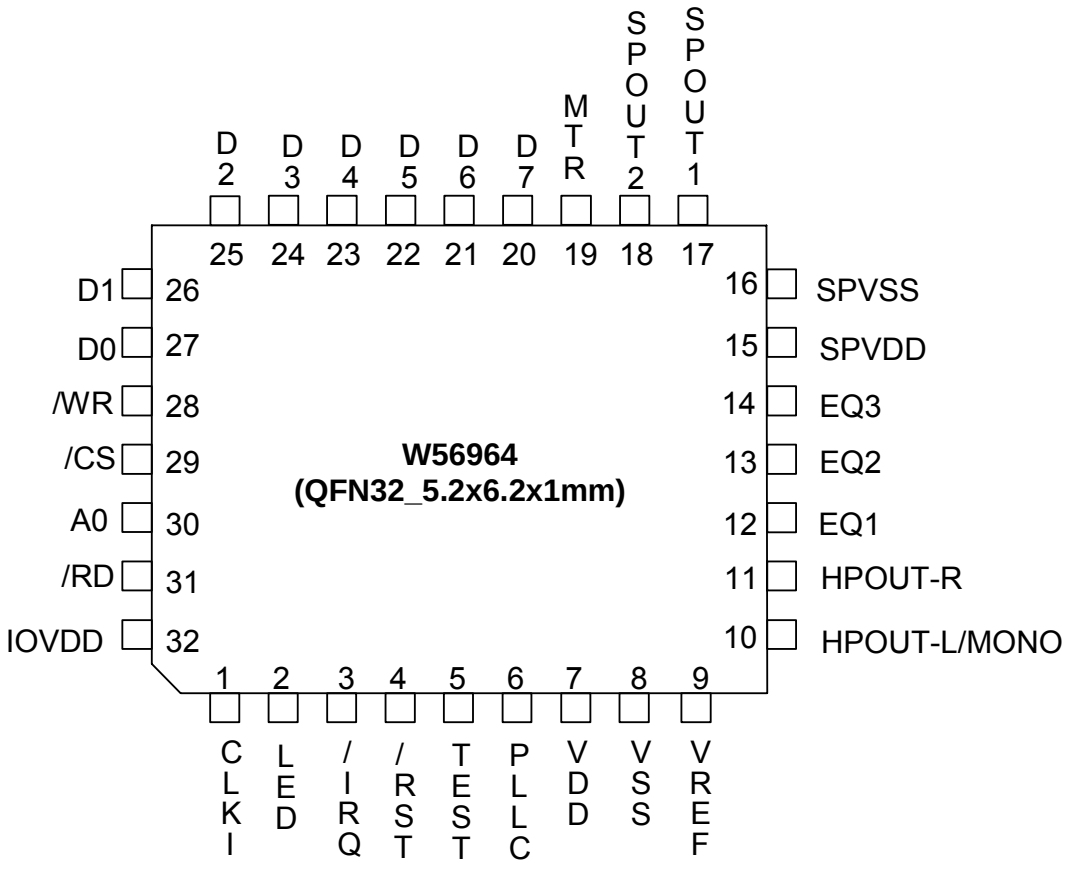
Synchronization among MIDI, SFX, LED, and MTR is done using embedded events in the MIDI file, which the W56964 would decode and process accordingly. The LED and MTR output pins with 256-level control output can be used for brightness and speed control, respectively.

In addition, API (Application Program Interface) source code is provided for the CPU to control the W56964 easily via the memory bus interface.

2. FEATURES

- General MIDI compliant sound set: 128 instruments + 47 drums
- 64-note, 100% wavetable MIDI synthesizer with ADPCM/PCM synthesis
- High quality sound
- Simultaneous playback of
  - Two MIDI song files,
  - Two ADPCM files, or
  - ADPCM + MIDI
- Karaoke feature support
- MIP support for SP-MIDI format
- Middleware API source code provided for function control and CPU interface
- Multiple Format Parser that supports
  - MIDI: SMF, SP-MIDI, i-Melody, RTTTL, etc.
  - Audio: stereo WAV @ 48 KHz
- Stereophonic DAC with 12-bit resolution per channel
- On-chip power amplifier to drive 8Ω speaker directly
- Equalizer embedded to meet speaker response
- Stereophonic headphone outputs available
- Line-In to receive external analog signals
- LED output with 256 levels of brightness
- MTR output with 256 levels of speed
- Harmonized synchronization between MIDI, SFX, LED, and MTR
- Embedded PLL operates on 1.7 ~ 36 MHz clock input
- Power supply
  - VDD: 2.7 ~ 3.3 volt
  - SPVDD: 2.7 ~ 4.5 volt
  - IOVDD: 1.65 ~ VDD
- Operating current: 20 mA (25°C at no load)
- Standby current: 1 uA @ 25°C
- Operating temperature: -20°C ~ 85°C
- Package
  - 32-pin plastic QFN (5.2mmx6.2mmx1mm)

3. PIN CONFIGURATION



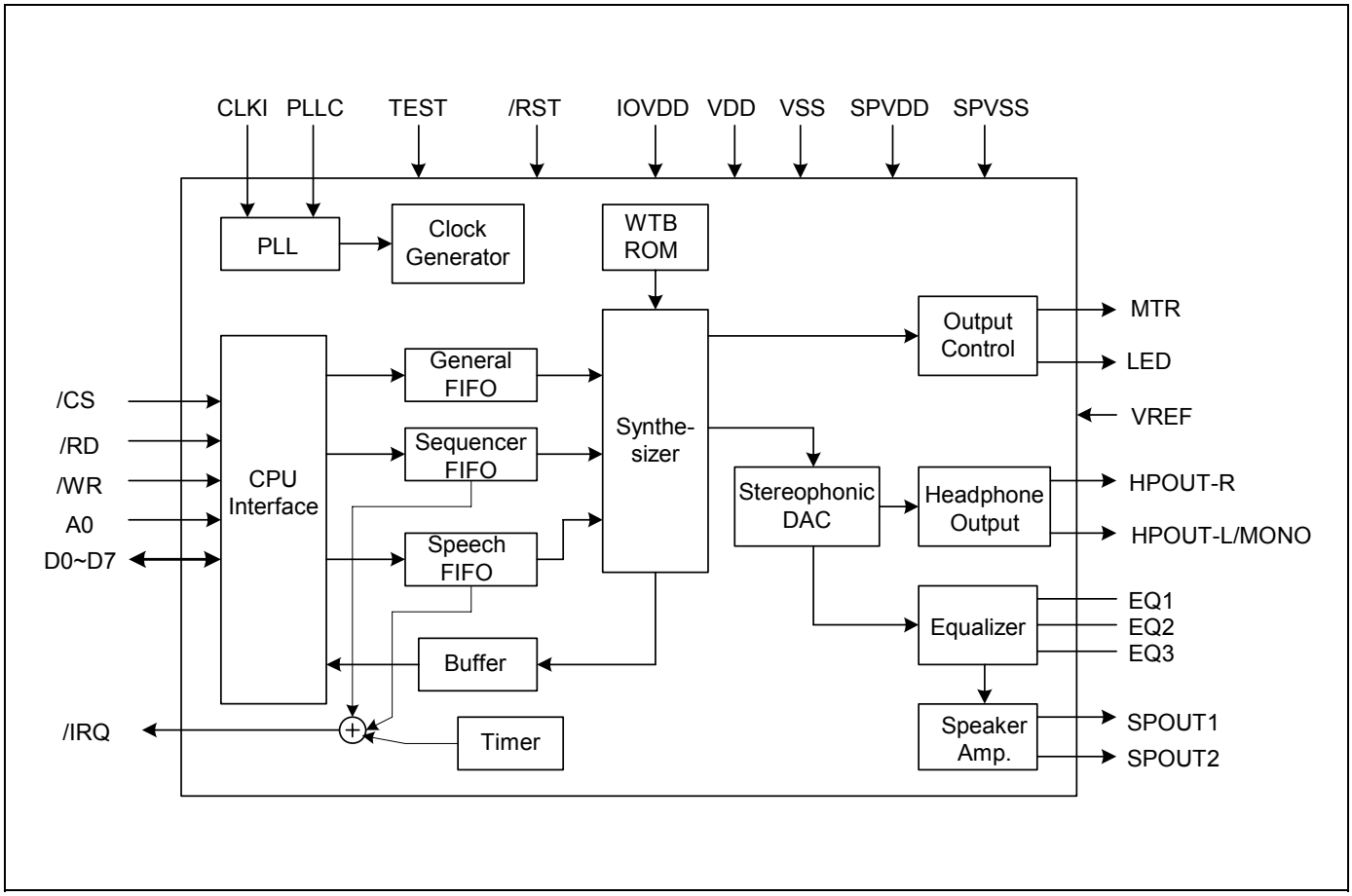
4. PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	FUNCTION
1	CLKI	Ish	Clock input (1.7 ~ 36 MHz)
2	LED	O	LED output (Drive capability: 4 mA)
3	/IRQ	O	Interrupt request (Drive capability: 1 mA)
4	/RST	Ish	Hardware reset with Schmidt trigger
5	TEST	I	Test pin
6	PLLC	A	Connection to internal PLL capacitor. Connect a 1000 pF capacitor and a 3.3 KΩ resistor in series between PLLC and VSS. Minimize the length of this route .
7	VDD	-	Power supply, typically 3.0 . Connect 0.1 uF and 4.7 uF capacitors between VDD and VSS.
8	VSS	-	Ground
9	VREF	A	Analog reference voltage. Connect a 0.1 uF capacitor between VREF and VSS.
10	HPOUT-L/MONO	A	Headphone output (left channel) or mono output
11	HPOUT-R	A	Headphone output (right channel)
12	EQ1	A	Equalizer pin 1
13	EQ2	A	Equalizer pin 2
14	EQ3	A	Equalizer pin 3
15	SPVDD	-	Speaker amplifier analog power supply, typically 3.6. Connect 0.1 uF and 4.7 uF capacitors between SPVDD and SPVSS.
16	SPVSS	-	Speaker amplifier analog ground
17	SPOUT1	A	Speaker connection pin 1
18	SPOUT2	A	Speaker connection pin 2
19	MTR	O	Motor output (Drive capability: 4 mA)
20	D7	I/O	CPU interface data bus, bit 7 (Drive capability: 1 mA)
21	D6	I/O	CPU interface data bus, bit 6 (Drive capability: 1 mA)
22	D5	I/O	CPU interface data bus, bit 5 (Drive capability: 1 mA)
23	D4	I/O	CPU interface data bus, bit 4 (Drive capability: 1 mA)
24	D3	I/O	CPU interface data bus, bit 3 (Drive capability: 1 mA)
25	D2	I/O	CPU interface data bus, bit 2 (Drive capability: 1 mA)

26	D1	I/O	CPU interface data bus, bit 1 (Drive capability: 1 mA)
27	D0	I/O	CPU interface data bus, bit 0 (Drive capability: 1 mA)
28	/WR	I	CPU interface, write enable
29	/CS	I	CPU interface, chip select
30	A0	I	CPU interface, address 0
31	/RD	I	CPU interface, read enable
32	IOVDD	-	IO peripheral power supply for 1.8 or 3.0 CPU interface.

A: Analog pin, I: Input, O: Output, I/O: Bidirectional, Ish: Input with Schmidt trigger

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

CPU interface

The 8-bit memory bus and A0 are used as the CPU interface for the streaming playback of MIDI & ADPCM/PCM synthesizers. /CS and /IRQ are required to address the peripheral (W56964) and to send interrupt requests to the baseband CPU.

Depending on the data type, the interface transfers data both ways between the W56964 and baseband CPU to construct the signal path for MIDI & ADPCM/PCM playback.

The W56964 supports a 1.8 or 3 Volt CPU interface via the connection of IOVDD.

MIDI sequencer & FIFO

The built-in sequencer works with the FIFO to handle MIDI events based on the delta times stamped in the MIDI file. The FIFO operates this way to alleviate the loading on the baseband CPU.

Wavetable & ADPCM synthesizers

In contrast to FM synthesis, the W56964 is equipped with a 100% wavetable synthesizer to generate 64-note melody tunes with more realistic and natural instrument sounds.

Speech synthesis is also available for the playback of 4-bit ADPCM or 8-bit PCM at a sample rate of up to 48 KHz.

Timbre ROM

With the built-in timbre ROM, the W56964 provides a GM-compatible sound set that supports up to 128 instruments plus 47 drum voices.

Any GM-compliant MIDI songs can be played back by the W56964.

DAC

The stereophonic DAC converts internal PCM data into left-channel and right-channel analog signals with 12-bit resolution each.

/IRQ and Timer

The W56964 supports the /IRQ generation for FIFO, two timers, and the sequencer in order to interface with baseband CPU for ringtone generation.

EQ amplifier

The gain and frequency response of the equalizer can be changed by adjusting values of external components, like capacitors and resistors. See typical application circuit for recommended values.

Up to 32 levels of volume control, in steps of 1 dB, is available in the EQ amplifier to directly adjust the volume from the analog section.

Speaker amplifier

To save PCB space and additional power amplifier cost, the PA (power amplifier) is built in the W56964. It can deliver up to 550 mW at SPVDD = 3.6 volt.

Up to 32 levels of volume control, in steps of 1 dB, is available in the power amplifier to directly adjust the volume from the analog section beside EQ amplifier.

LED & MTR control

To give customers more freedom in synchronizing LED and vibrator control with MIDI and ADPCM/PCM playback, the W56964 provides 256-level control of brightness (LED) and speed (MTR).

The LED can flash with different brightnesses, while the MTR can be used to give soft or rock vibration. Synchronized control is easily done through the API provided on the CPU side.

Clock Generation

Clock input from the board can range from 1.7 to 36 MHz. Power down mode is available to help conserve standby current, which is under 1 uA.

The PLL circuitry is then configured by the CPU to get the fixed internal frequency for the W56964 to work.

TIMING WAVEFORMS

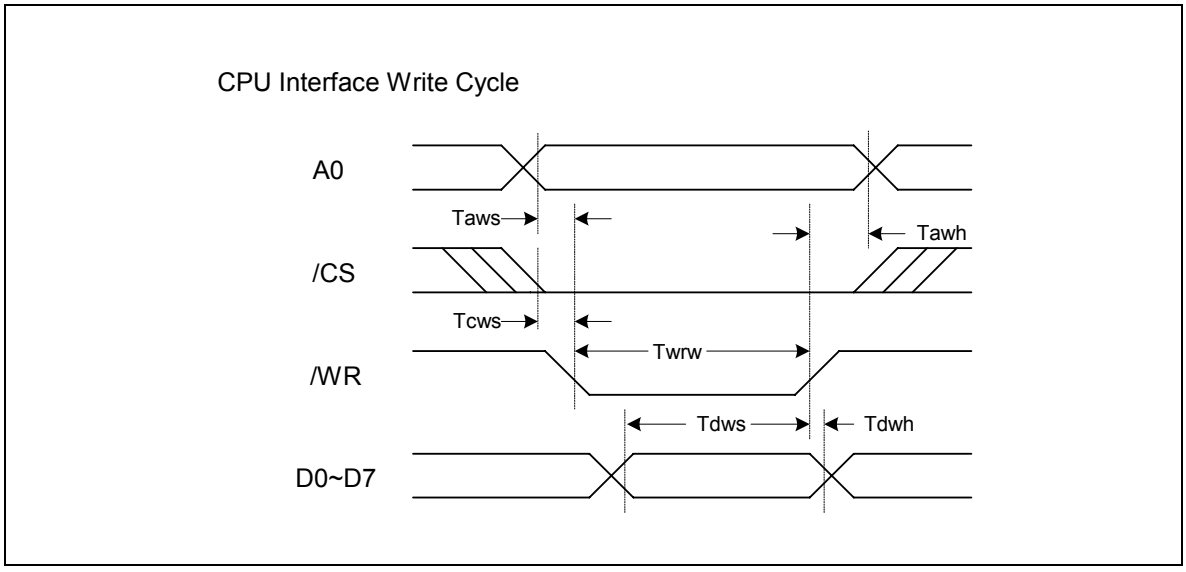


Figure 1. CPU Interface Write Cycle

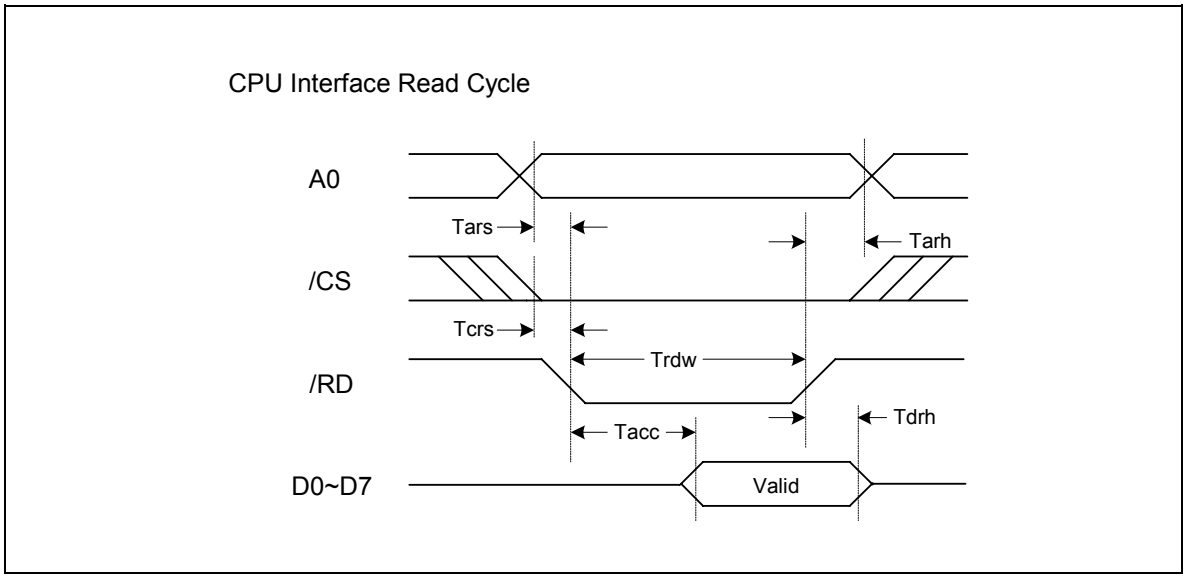


Figure 2. CPU Interface Read Cycle

7. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITIONS	RATED VALUE	UNIT
Power Supply	$V_{DD} - V_{SS}$	-	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	All Inputs	V_{SS}-0.3 ~ V_{DD}+0.3	V
Storage Temp.	T_{STG}	-	-55 ~ +150	°C
Operating Temp.	T_{OPR}	-	-20 ~ 85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

8. ELECTRICAL CHARACTERISTICS

8.1 DC parameters

(VDD–VSS = 3.0V, SPVDD-SPVSS=3.6V, TA = 25° C; unless otherwise specified.)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
Operating voltage	VDD		2.7	3.0	3.3	V
CPU interface voltage	IOVDD		1.65	-	VDD	V
Speaker amplifier operating voltage	SPVDD		2.7	3.6	4.5	V
Input low voltage	V_{IL}		VSS		0.3VDD	V
Input high voltage	V_{IH}		0.7VDD		VDD	V
Input voltage amplitude	V_{CK}	CLKI@TCXO mode	0.5		0.7VDD	V
Output low current (MTR, LED)	I_{OL1}	V_{OUT} = 0.4V	8			mA
Output high current (MTR, LED)	I_{OH1}	V_{OUT} = 2.6V	-4			mA
Output low current (D0 ~ D7, /IRQ)	I_{OL2}	V_{OUT} = 0.4V	1			mA
Output high current (D0 ~ D7, /IRQ)	I_{OH2}	V_{OUT} = 2.6V	-1			mA
Operating current (VDD+IOVDD)	I_{OP}	Synthesizer works, no load		15		mA
Operating current (SPVDD)	I_{OPA}	Amplifier works, no load		5		mA
Operating current (SPVDD)	I_{OPB}	8 Ω load, 400mW output		210		mA
Standby current[1] (VDD+IOVDD+SPVDD)	I_{SB}	Power down mode		3	TBD	μA
SP amplifier						
Speaker volume setting			-30		0	dB
Speaker volume step				1		dB

[1] /CS input is fixed to VIH=IOVDD, the other input pins are VIL=VSS and VIH=(IO)VDD.

Minimum load resistance (R_L)			8		Ω
Maximum output voltage amplitude	R_L=8Ω		5.8		Vp-p
Total harmonic distortion plus noise (THD+N)	R_L=8Ω, f=1KHz, 400mW output		0.1		%
Differential output voltage			10	50	mV
Maximum output power	R_L=8Ω, THD+N<1%		550		mW
EQ amplifier					
Equalizer volume setting		-30		0	dB
Equalizer volume step			1		dB
Max. output current		120			uA
Max. output voltage amplitude			1.5		Vp-p
Total harmonic distortion plus noise (THD+N)	f=1 KHz			0.3	%
HP Volume					
HP volume setting		-30		0	dB
HP volume step			1		dB
Max. output current		120			uA
Max. output voltage amplitude			1.5		Vp-p
DAC					
Resolution per channel			12		Bits
Full scale output voltage			1.5		Vp-p
Total harmonic distortion plus noise (THD+N)	f = 1 KHz			0.5	%

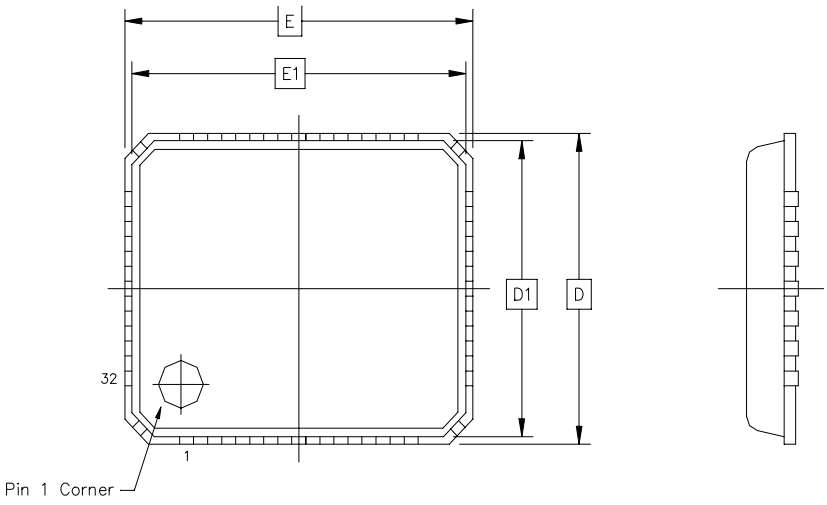
8.2 AC parameters

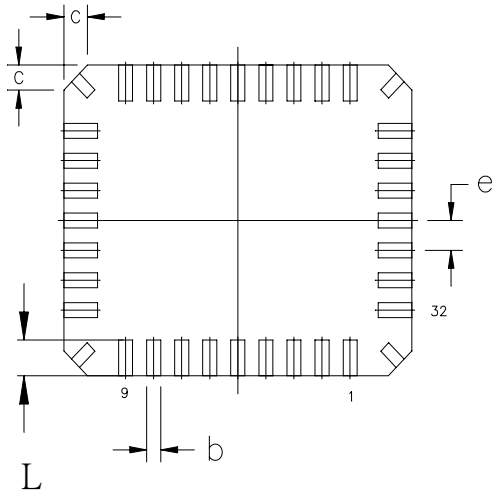
(VDD–VSS = 3.0V, TA = 25° C; unless otherwise specified.)

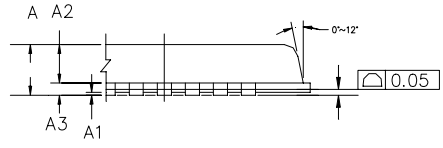
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clock						
CLKI frequency	FCLK		1.7		36	MHz
CLKI duty			40	50	60	%
RESETB Active Width	T_{RES}		500	-	-	nS
CPU Write						
Chip select setup time	TCWS		0			nS
Address setup time	TAWS		0			nS
Write enable pulse width	TWRW		50			nS
Write data setup time	TDWS		30			nS
Write data hold time	TDWH		0			nS
Address hold time	TAWH		0			nS
CPU Read						
Chip select setup time	TCRS		0			nS
Address setup time	TARS		0			nS
Read enable pulse width	TRDW		80			nS
Read data access time	TACC				70	nS
Read data hold time	TDRH		10			nS
Address hold time	TARH		0			nS

9. PACKAGE DIMENSIONS

- **W56964 DYX**



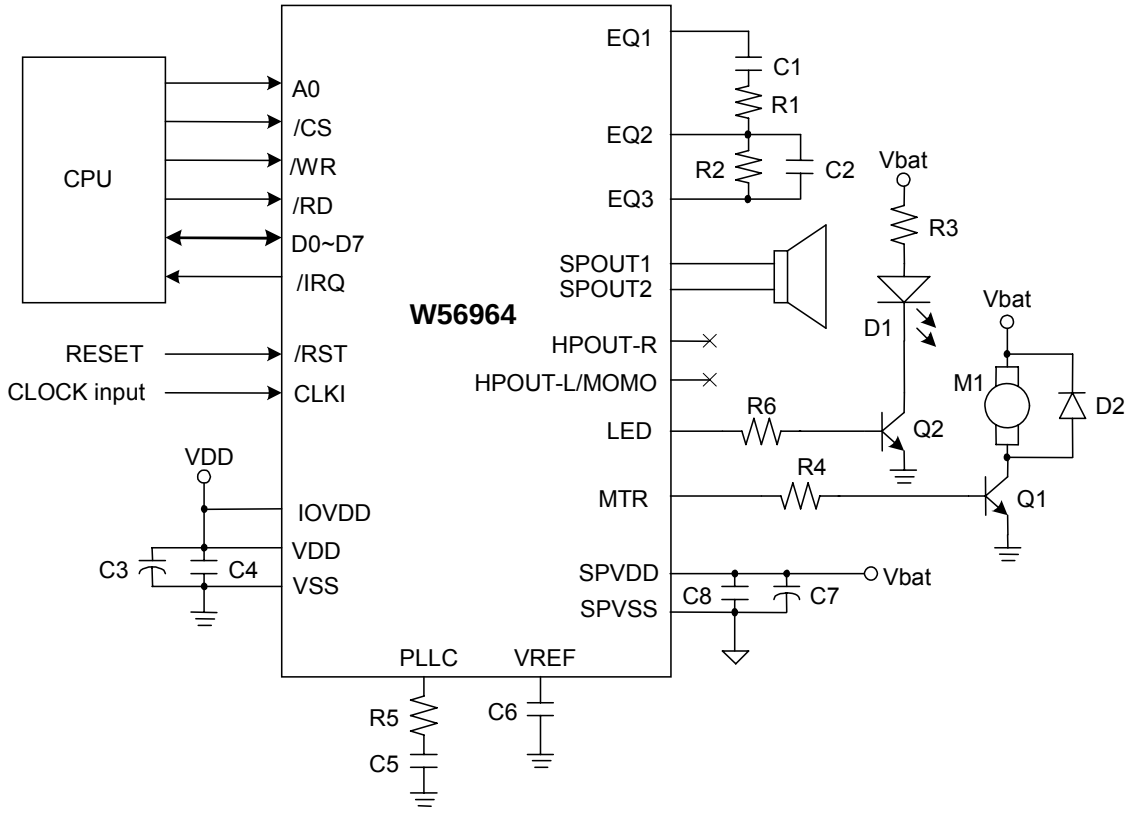




Cotrol Dimensions :Millmeters

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	---	1.00	0.0314	---	0.0394
A1	0.00	0.02	0.05	0.0000	0.0007	0.0019
A2	0.65	---	0.69	0.0255	---	0.0271
A3	0.203 REF.			0.0079 REF.		
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
C	0.24	0.42	0.60	0.0094	0.0165	0.0236
D	5.20 BSC			0.2047 BSC		
D1	4.95 BSC			0.1948 BSC		
E	6.20 BSC			0.2440 BSC		
E1	5.95 BSC			0.2342 BSC		
e	0.50 BSC			0.0196 BSC		
L	0.50	0.60	0.70	0.0196	0.0236	0.0275

10. TYPICAL APPLICATION CIRCUIT



Recommended component values:

C1=2200pF	C2=220pF	C3=4.7μF	C4=0.1μF	C5=1000pF
C6=0.1μF	C7=4.7μF	C8=0.1μF		
R1=51KΩ	R2=91KΩ	R3=330Ω	R4=4.7KΩ	R5=3.3KΩ
R6=4.7KΩ				

Note: IOVDD should be connected to another power supply if the CPU interface voltage is different than VDD.

11. ORDERING INFORMATION

PART NUMBER	PACKAGE	UNDER EXPOSED PAD	PB FREE + HALOGEN FREE	RELEASE DATE
W56964DYX	QFN32_6.2x5.2x1mm	Without	Yes	Available

12. HOW TO READ THE TOP MARKING

W56964DYX

14498005992

450LDBA

1st line: Winbond logo

2nd line: the type number: W56964DYX

3rd line: wafer production series lot number: 14498005992

4th line: the tracking code: 450 L D BA

450: package made in 2004, week 50

L: assembly house ID.

D: IC version.

BA: Winbond internal use.

13. REVISION HISTORY

Revision	Date	Modifications
A0	August 2004	• Initial release.
A1	September 2004	• Update standby current on DC parameters. • Update package dimensions.
A2	October 2004	• Add the spec of RESETB Active Width in AC Characteristic. • Add the spec of input voltage amplitude @ TCXO mode in DC Characteristic.
A3	January 2005	• Revised grammar • Add Section 12 “How to read the top marking”
A4	March 2005	• Add W56964 BY,BYX package dimension
A5	March 2005	• Add Disclaimer
A6	August 2005	• Release W56964CY • Remove W56964AY package dimension
A7	June 2006	• Release W56964DYX