VS10XX AppNote: PCB Layout Considerations

Description

This document describes how to make a succesful PCB layout for the VS10xx family devices. It shows an example layout on how to connect grounds and bypass capacitors.

This document applies to entire VS10xx family.

For detailed info on VS10XX registers see datasheets at http://www.vlsi.fi/

Revision History			
Rev	**Date**	**Author**	**Description**
1.0	2008-03-25	PLe	Initial revision.

Table of Contents

List of Figures

1 General Info on Layout Design

VS10xx family devices have separate analog and digital power net and grounds. Most of the devices also have separate power net for the DSP core. Devices have several power and ground pins. To obtain best performance the layout designer must know to connect these pins properly. The purpose of this document is to suggest good design practices.

Each chapter in the application note has a picture describing the part of the layout that the chapter covers. Top layer is red and bottom layer is blue. For sake of clarity silk screen is not included in the detailed pictures. A schematic of the example (figure 1) and picture of the complete layout (figure 6) are also provided. Notice that this is not a working application but an example of good layout design.

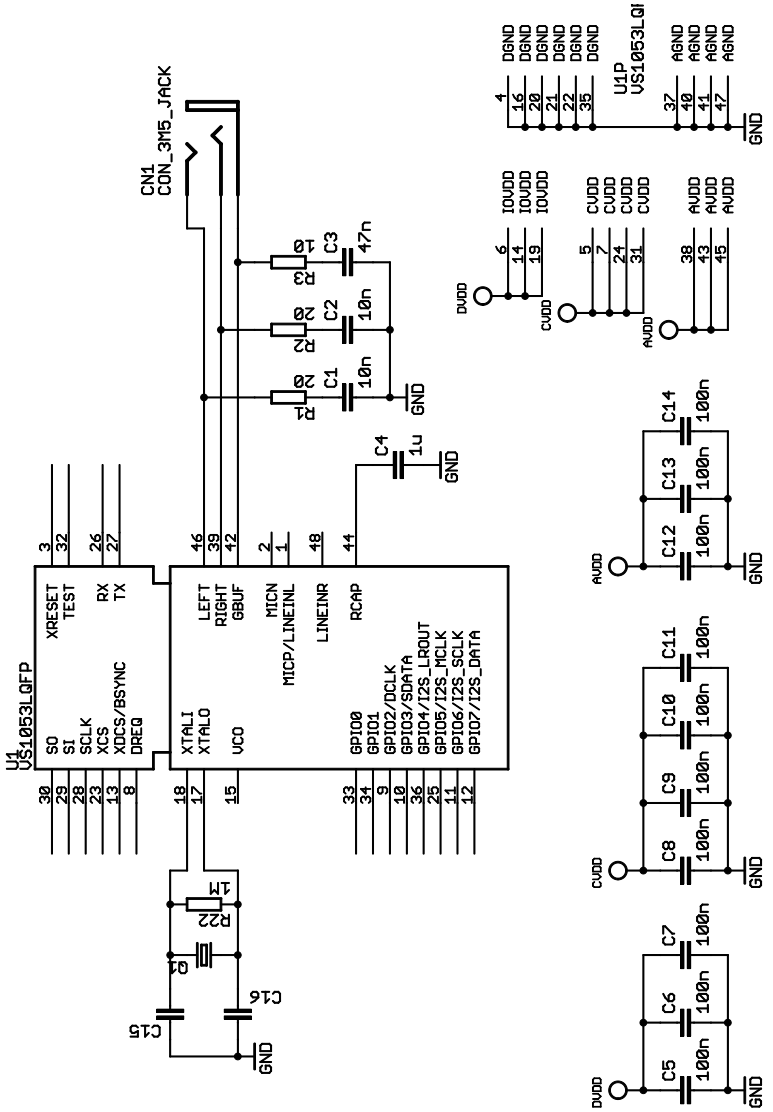

Figure 1: Schematic of the layout example. Notice multiple vias that connect top and bottom layer ground planes.

2 4-layer board

The easiest way to get good performance is to use a four layer board with separate ground and power layers. Top and bottom layer should be used to route all signals, 2nd layer as ground and 3rd layer as power. Power and ground layer can be divided into several sections to provide different operating voltages and separate grounds for analog and digital.

3 2-layer board

It is also possible but more difficult to get good performance with a two layer board. In this case the designer must be very careful when routing power, ground and signal lines.

We have found that the best solution for two layer boads is to fill both the top and bottom layer of the board with a copper pour that acts as ground. These planes should be connected together from several points around the board. Most signals should be routed on the top layer so the bottom layer stays as uniform as possible.

4 Grounds

VS10xx devices have separate grounds for digital (DGND) and analog (AGND) sections. In PCB designs these can be treated as the same ground. These are also internally connected together.

It is recommended to use the bottom layer of a two layer board as a ground plane. The plane must be as uniform as possible. The VS10xx device ground pins are connected to the ground plane under the device with multiple vias. If there is a ground plane also on the top layer under the chip, grounds should be connected to this and the plane connected to the bottom plane with separate vias. See figure 2 for an example how to connect VS10xx ground pins.

Analog and digital ground pins must be connected together under the device.

5 Power Pins

A 100nF ceramic capacitor shall be placed near every xVDD pin of the VS10xx device. The capacitors should be placed as close as possible to the device. Power should be routed so that it is first taken to the cap and then to the VS10xx power pin. Ideally each cap has a separate via to the ground plane.

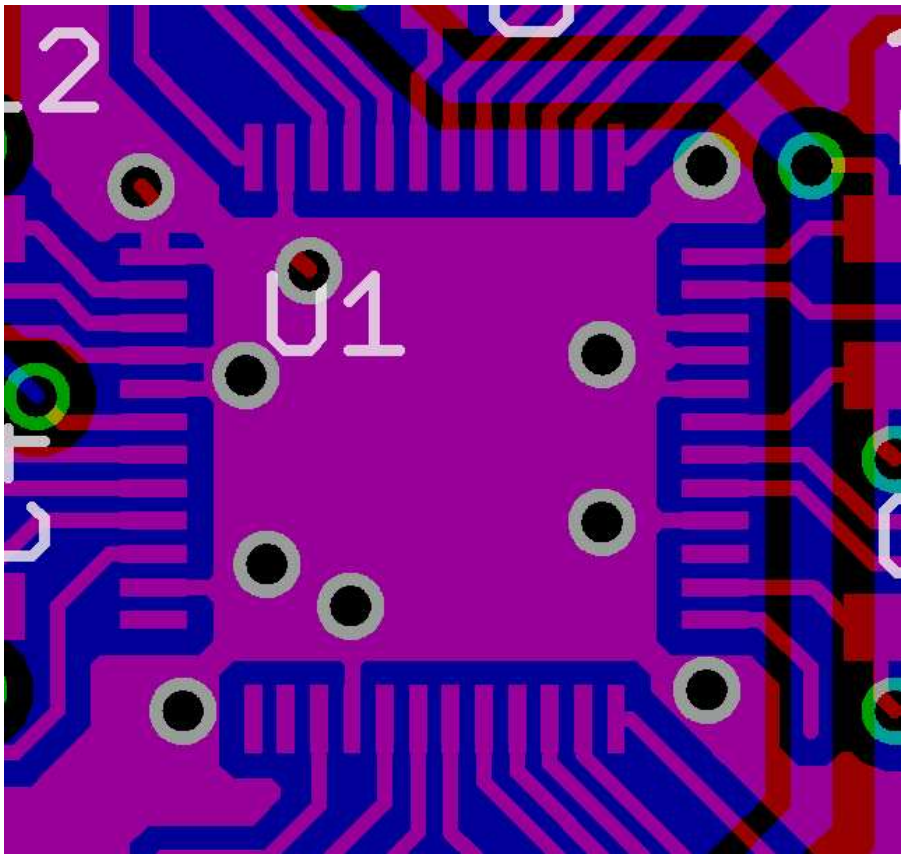

Figure 2: Example on how to connect grounds.

Since VS10xx devices use up to three different oparating voltages several power supply nets are also needed. Often the AVDD and DVDD can be povered from the same supply. The CVCC usually needs a separate supply due to its low voltage requirement. With VS1053 a separate AVDD supply might be needed if one wishes to use 3.6V AVDD for highest analog performance.

The power supplies should be located near the VS10xx device so that traces from the regulator outputs to the VDD inputs are short. See figures 3 and 4 for detailed examples.

It is not recommended to use inductor to isolate AVDD from DVDD net. A small resistor or a short usually works better.

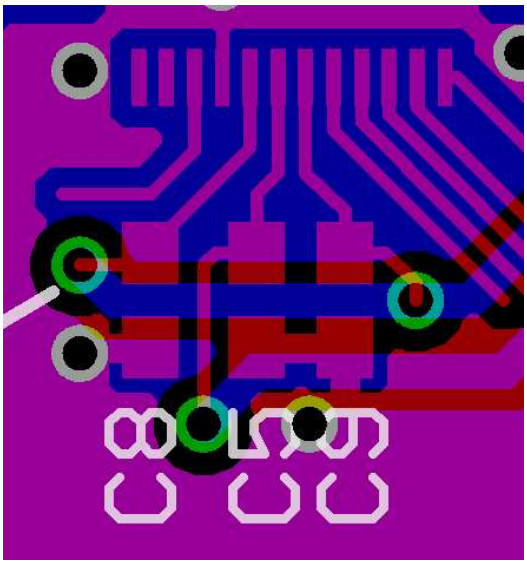

Figure 3: Example on how to place and route power filter capacitors.

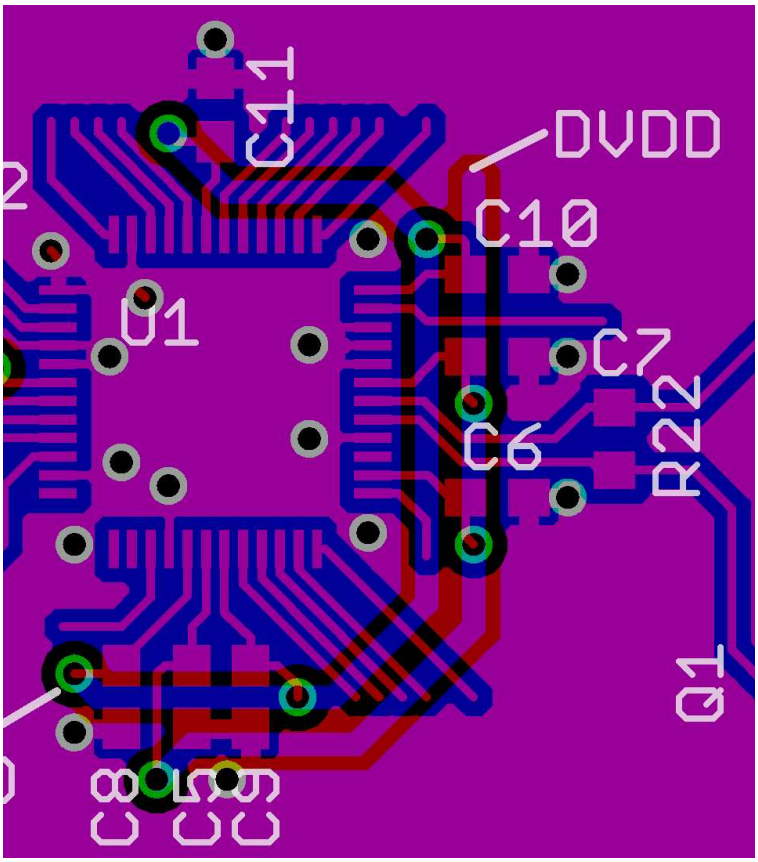

Figure 4: Example on how to route DVDD and CVDD traces (on the blue bottom layer). Notice the vias connecting top and bottom ground plane together.

6 Analog pins

The analog sections of VS10xx devices are most sensitive to mistakes in the layout. Special care must be taken when routing these signals and specially the ground of the RCAP capacitor.

As mentioned in chapter 4 also the analog grounds (AGND) are connected to a ground plane. Also the ground of the passive components at the analog outputs (LEFT, RIGHT, GBUF) must have a good ground path to the AGND pins of the VS10xx device. Figure 5 shows an example layout.

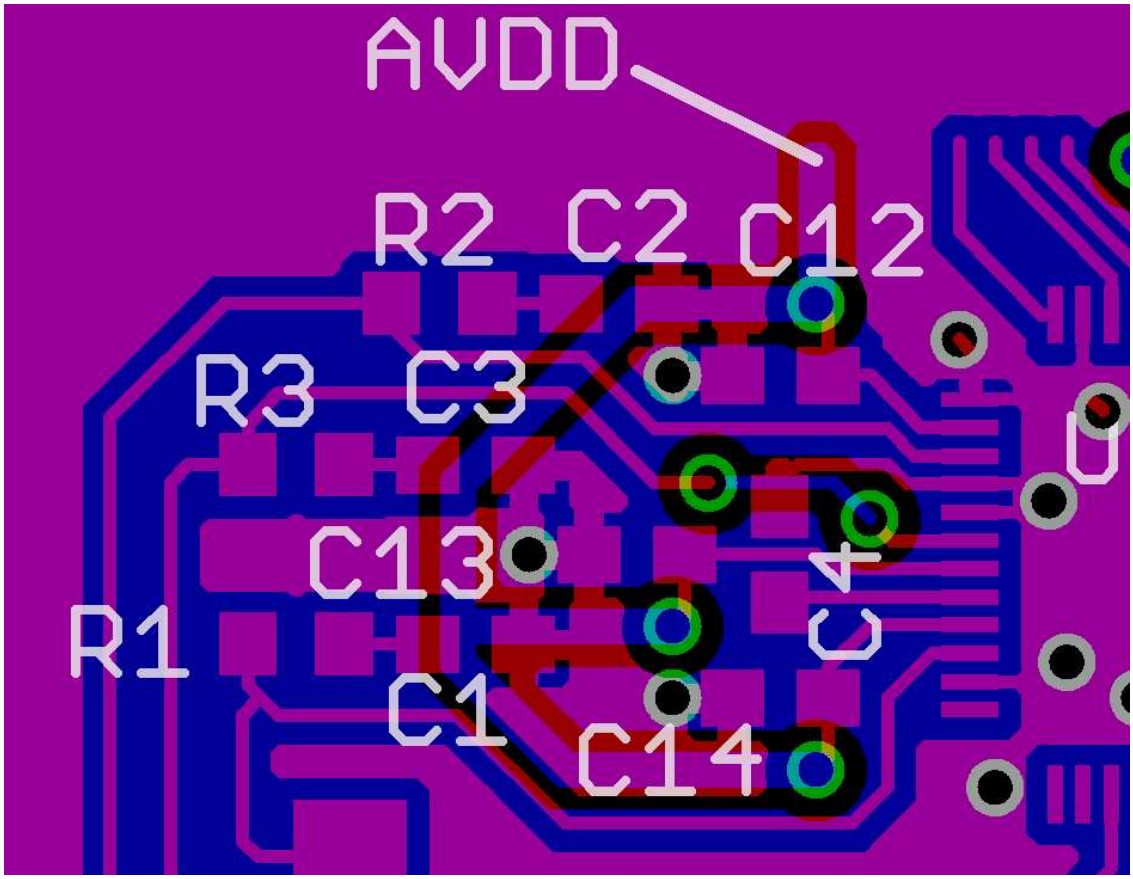

Figure 5: Example on how to place and route components at the analog outputs. Notice the connection of the RCAP capacitor (C4). Notice how the ground vias of the filter capacitors an the output RC-pairs are connected inside the AVDD trace (bottom of the board).

6.1 The RCAP pin

The RCAP pin is the most sensitive pin in the entire VS10xx family of devices. Any noise at this pin is transferred also to the analog outputs. This is why special

care must be taken when routing it.

The RCAP capacitor (C4 in the example) must be placed very close to the RCAP pin. The ground side of the RCAP capacitor must have a separate trace to the pins 40 and 41 of the VS10xx device. These pins must be connected to the ground plane. This means that the ground of the RCAP capacitor is separate from the plane and no noise from the plane can enter the RCAP pin. See figure 5 for details.

7 Example Layout

Figure 6 shows a general view of the example layout for a two layer board. This layout is expected to provide good results. This is not the only way to route the board but it is relatively simple and it demonstrates the important aspects of layout design. Use this figure to see how the two layers align.

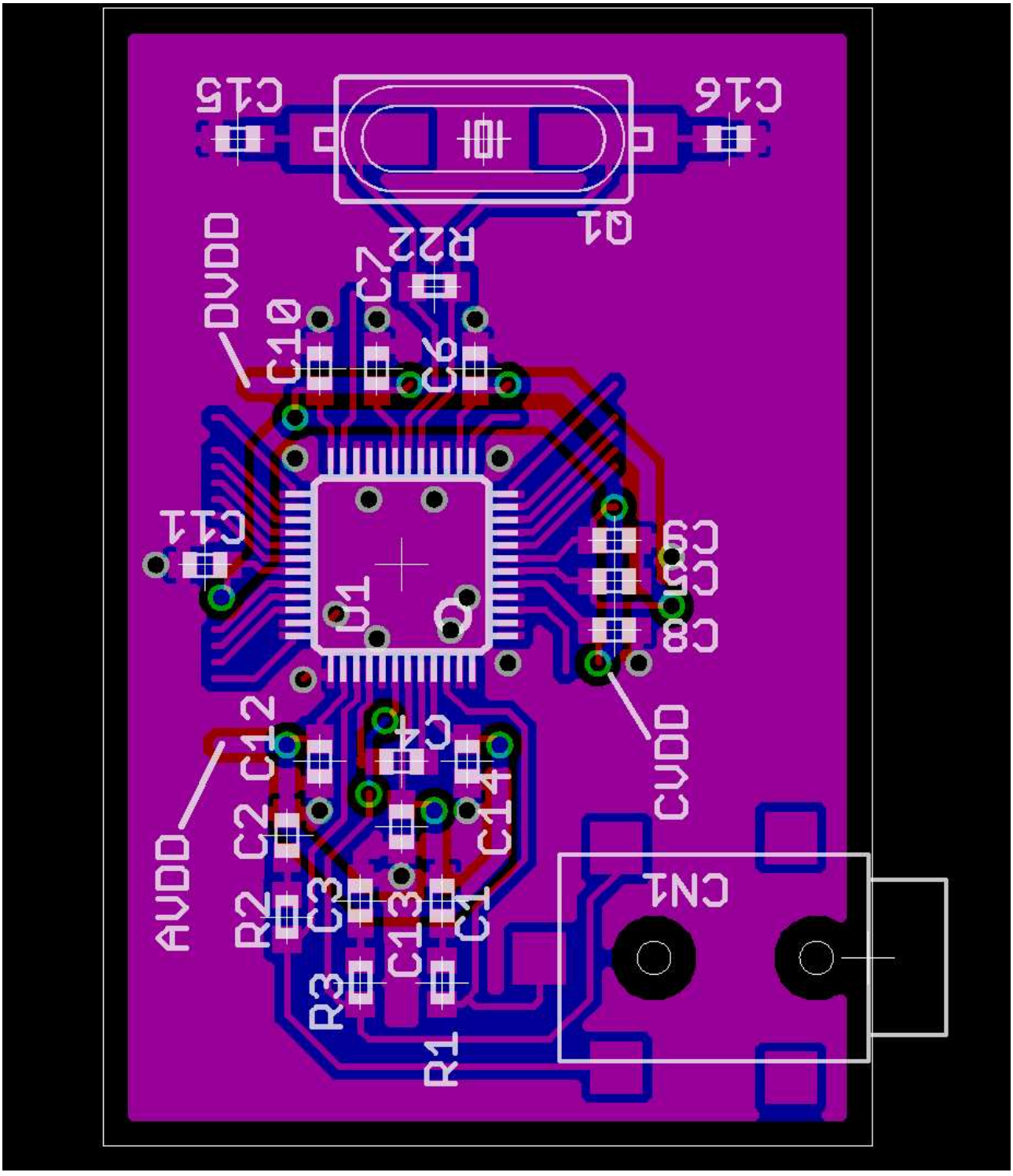

Figure 6: Example layout, general view. Notice the alignment of layers and via locations for ground and VDD signals.

8 Document Version Changes

This chapter describes the most important changes to this document.

Version 1.0, 2008-03-25

- Initial version.

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