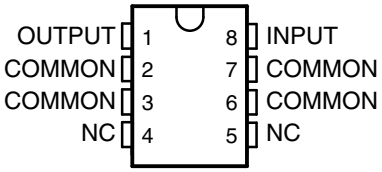
# LOW-DROPOUT VOLTAGE REGULATORS

## FEATURES

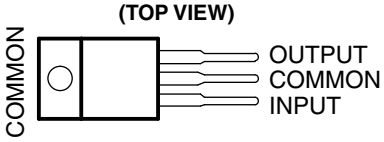
- Very Low Dropout Voltage, Less Than 0.6 V at 150 mA
- Very Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751L Series
- 60-V Load-Dump Protection
- Reverse Transient Protection Down to –50 V
- Internal Thermal-Overload Protection
- Overvoltage Protection
- Internal Overcurrent-Limiting Circuitry
- Less Than 500-µA Disable (TL751L Series)

**TL750L . . . D PACKAGE**
**(TOP VIEW)**

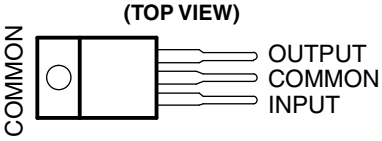



NC – No internal connection

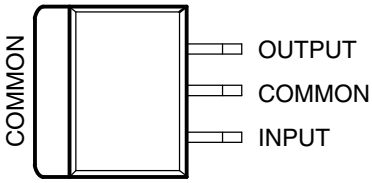
**TL750L . . . KC PACKAGE**
**(TOP VIEW)**



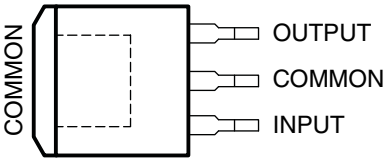

**TL750L . . . KCS PACKAGE**
**(TOP VIEW)**



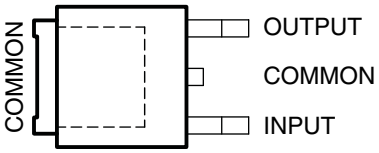

**TL750L . . . KTE PACKAGE**
**(TOP VIEW)**



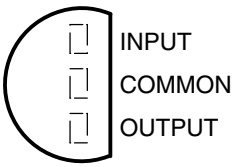

**TL750L . . . KTT PACKAGE**
**(TOP VIEW)**



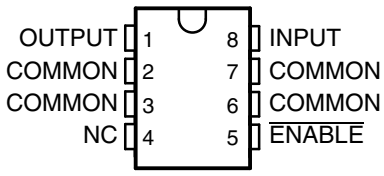

**TL750L . . . KVU PACKAGE**
**(TOP VIEW)**




**TL750L . . . LP PACKAGE**
**(TO-92, TO-226AA)**
**(TOP VIEW)**

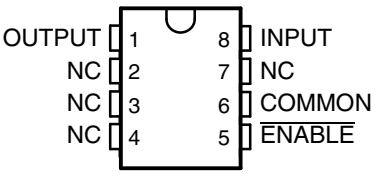



**TL751L . . . D PACKAGE**
**(TOP VIEW)**




NC – No internal connection

**TL751L . . .P PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable (ENABLE) input. When ENABLE is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

## ORDERING INFORMATION(1)

| $T_J$ | $V_O$ TYP AT 25°C | PACKAGE (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| 0°C to 125°C | 5 V | PowerFLEX™ – KTE | Reel of 2000 | TL750L05CKTER | TL750L05C |
| | | SOIC – D | Tube of 75 | TL750L05CD | 50L05C |
| | | | Reel of 2500 | TL750L05CDR | |
| | | | Tube of 75 | TL751L05CD | 51L05C |
| | | | Reel of 2500 | TL751L05CDR | |
| | | TO-226/TO-92 – LP | Bulk of 1000 | TL750L05CLP | 750L05C |
| | | | Reel of 2000 | TL750L05CLPR | |
| | | TO-220 – KC | Tube of 50 | TL750L05CKC | TL750L05C |
| | | TO-220 – KCS | Tube of 50 | TL750L05CKCS | TL750L05C |
| | | TO-252 – KVU | Reel of 2500 | TL750L05CKVUR | 750L05C |
| | | TO-263 – KTT | Reel of 500 | TL750L05CKTTR | 750L05C |
| | 8 V | SOIC – D | Tube of 75 | TL750L08CD | 50L08C |
| | | | Reel of 2500 | TL750L08CDR | |
| | | TO-226/TO-92 – LP | Bulk of 1000 | TL750L08CLP | 750L08C |
| | 10 V | PDIP – P | Tube of 50 | TL751L10CP | TL751L10C |
| | | SOIC – D | Tube of 75 | TL750L10CD | 50L10C |
| | | | Reel of 2500 | TL750L10CDR | |
| | | | Tube of 75 | TL751L10CD | 51L10C |
| | | | Reel of 2500 | TL751L10CDR | |
| | | TO-226/TO-92 – LP | Bulk of 1000 | TL750L10CLP | 750L10C |
| | | | Reel of 2000 | TL750L10CLPR | |
| | 12 V | SOIC – D | Tube of 75 | TL750L12CD | 50L12C |
| | | | Reel of 2500 | TL750L12CDR | |
| | | | Tube of 75 | TL751L12CD | 51L12C |
| | | | Reel of 2500 | TL751L12CDR | |
| | | TO-226/TO-92 – LP | Bulk of 1000 | TL750L12CLP | 750L12C |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

| DEVICE COMPONENT COUNT | |
|---|---|
| Transistors | 20 |
| JFETs | 2 |
| Diodes | 5 |
| Resistors | 16 |

## Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | Continuous input voltage | | | 26 | V |
| | Transient input voltage(2) | $T_A$ = 25°C | | 60 | V |
| | Continuous reverse input voltage | | | –15 | V |
| | Transient reverse input voltage | t ≤ 100 ms | | –50 | V |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| | Lead temperature | 1,6 mm (1/16 in) for 10 s | | 260 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The transient input voltage rating applies to the waveform shown in Figure 1.

## Package Thermal Data(1)

| PACKAGE | BOARD | $\theta_{JC}$ | $\theta_{JA}$ |
|---|---|---|---|
| PDIP (P) | High K, JESD 51-7 | 57°C/W | 85°C/W |
| PowerFLEX™ (KTE) | High K, JESD 51-5 | 3°C/W | 23°C/W |
| SOIC (D) | High K, JESD 51-7 | 39°C/W | 97°C/W |
| TO-226/TO-92 (LP) | High K, JESD 51-7 | 55°C/W | 140°C/W |
| TO-220 (KC) | High K, JESD 51-5 | 3°C/W | 19°C/W |
| TO-220 (KCS) | High K, JESD 51-5 | 3°C/W | 19°C/W |
| TO-252 (KVU) | High K, JESD 51-5 | – | 30.3°C/W |
| TO-263 (KTT) | High K, JESD 51-5 | 18°C/W | 25.3°C/W |

(1) Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.

## Recommended Operating Conditions

over recommended operating junction temperature range (unless otherwise noted)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_I$ | Input voltage | | TL75xL05 | 6 | 26 | V |
| | | | TL75xL08 | 9 | 26 | |
| | | | TL75xL10 | 11 | 26 | |
| | | | TL75xL12 | 13 | 26 | |
| $V_{IH}$ | High-level $\overline{\text{ENABLE}}$ input voltage | | TL75xLxx | 2 | 15 | V |
| $V_{IL}$ (1) | Low-level $\overline{\text{ENABLE}}$ input voltage | $T_J$ = 25°C | TL75xLxx | –0.3 | 0.8 | V |
| | | $T_J$ = 0°C to 125°C | TL75xLxx | –0.15 | 0.8 | |
| $I_O$ | Output current | | TL75xLxx | 0 | 150 | mA |
| $T_J$ | Operating virtual junction temperature | | TL75xLxxC | 0 | 125 | °C |

(1) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

## TL75xL05 Electrical Characteristics[1]

$V_I$ = 14 V, $I_O$ = 10 mA, $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | TL750L05 TL751L05 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Output voltage | $V_I$ = 6 V to 26 V, $I_O$ = 0 to 150 mA | $T_J$ = 25°C | 4.8 | 5 | 5.2 | V |
| | | $T_J$ = 0°C to 125°C | 4.75 | | 5.25 | |
| Input regulation voltage | $V_I$ = 9 V to 16 V | | | 5 | 10 | mV |
| | $V_I$ = 6 V to 26 V | | | 6 | 30 | |
| Ripple rejection | $V_I$ = 8 V to 18 V, f = 120 Hz | | 60 | 65 | | dB |
| Output regulation voltage | $I_O$ = 5 mA to 150 mA | | | 20 | 50 | mV |
| Dropout voltage | $I_O$ = 10 mA | | | | 0.2 | V |
| | $I_O$ = 150 mA | | | | 0.6 | |
| Output noise voltage | f = 10 Hz to 100 kHz | | | 500 | | µV |
| Quiescent current | $I_O$ = 150 mA | | | 10 | 12 | mA |
| | $V_I$ = 6 V to 26 V, $I_O$ = 10 mA, $T_J$ = 0°C to 125°C | | | 1 | 2 | |
| | $\overline{\text{ENABLE}}$ ≥ 2 V | | | | 0.5 | |

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

## TL75xL08 Electrical Characteristics[1]

$V_I$ = 14 V, $I_O$ = 10 mA, $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | TL750L08 TL751L08 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Output voltage | $V_I$ = 9 V to 26 V, $I_O$ = 0 to 150 mA | $T_J$ = 25°C | 7.68 | 8 | 8.32 | V |
| | | $T_J$ = 0°C to 125°C | 7.6 | | 8.4 | |
| Input regulation voltage | $V_I$ = 10 V to 17 V | | | 10 | 20 | mV |
| | $V_I$ = 9 V to 26 V | | | 25 | 50 | |
| Ripple rejection | $V_I$ = 11 V to 21 V, f = 120 Hz | | 60 | 65 | | dB |
| Output regulation voltage | $I_O$ = 5 mA to 150 mA | | | 40 | 80 | mV |
| Dropout voltage | $I_O$ = 10 mA | | | | 0.2 | V |
| | $I_O$ = 150 mA | | | | 0.6 | |
| Output noise voltage | f = 10 Hz to 100 kHz | | | 500 | | µV |
| Quiescent current | $I_O$ = 150 mA | | | 10 | 12 | mA |
| | $V_I$ = 9 V to 26 V, $I_O$ = 10 mA, $T_J$ = 0°C to 125°C | | | 1 | 2 | |
| | $\overline{\text{ENABLE}}$ ≥ 2 V | | | | 0.5 | |

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

## TL75xL10 Electrical Characteristics[1]

$V_I$ = 14 V, $I_O$ = 10 mA, $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | TL750L10 TL751L10 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Output voltage | $V_I$ = 11 V to 26 V, $I_O$ = 0 to 150 mA | $T_J$ = 25°C | 9.6 | 10 | 10.4 | V |
| | | $T_J$ = 0°C to 125°C | 9.5 | | 10.5 | |
| Input regulation voltage | $V_I$ = 12 V to 19 V | | | 10 | 25 | mV |
| | $V_I$ = 11 V to 26 V | | | 30 | 60 | |
| Ripple rejection | $V_I$ = 12 V to 22 V, f = 120 Hz | | 60 | 65 | | dB |
| Output regulation voltage | $I_O$ = 5 mA to 150 mA | | | 50 | 100 | mV |
| Dropout voltage | $I_O$ = 10 mA | | | | 0.2 | V |
| | $I_O$ = 150 mA | | | | 0.6 | |
| Output noise voltage | f = 10 Hz to 100 kHz | | | 700 | | μV |
| Quiescent current | $I_O$ = 150 mA | | | 10 | 12 | mA |
| | $V_I$ = 11 V to 26 V, $I_O$ = 10 mA, $T_J$ = 0°C to 125°C | | | 1 | 2 | |
| | $\overline{\text{ENABLE}}$ ≥ 2 V | | | | 0.5 | |

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

## TL75xL12 Electrical Characteristics[1]

$V_I$ = 14 V, $I_O$ = 10 mA, $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | TL750L12 TL751L12 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Output voltage | $V_I$ = 13 V to 26 V, $I_O$ = 0 to 150 mA | $T_J$ = 25°C | 11.52 | 12 | 12.48 | V |
| | | $T_J$ = 0°C to 125°C | 11.4 | | 12.6 | |
| Input regulation voltage | $V_I$ = 14 V to 19 V | | | 15 | 30 | mV |
| | $V_I$ = 13 V to 26 V | | | 20 | 40 | |
| Ripple rejection | $V_I$ = 13 V to 23 V, f = 120 Hz | | 50 | 55 | | dB |
| Output regulation voltage | $I_O$ = 5 mA to 150 mA | | | 50 | 120 | mV |
| Dropout voltage | $I_O$ = 10 mA | | | | 0.2 | V |
| | $I_O$ = 150 mA | | | | 0.6 | |
| Output noise voltage | f = 10 Hz to 100 kHz | | | 700 | | μV |
| Quiescent current | $I_O$ = 150 mA | | | 10 | 12 | mA |
| | $V_I$ = 13 V to 26 V, $I_O$ = 10 mA, $T_J$ = 0°C to 125°C | | | 1 | 2 | |
| | $\overline{\text{ENABLE}}$ ≥ 2 V | | | | 0.5 | |

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

## PARAMETER MEASUREMENT INFORMATION

The TL750L, TL751L series are low-dropout regulators. This means that capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and its equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and temperature range. Figure 1 shows the recommended range of ESR for a given load with a 10-μF capacitor on the output.

## TYPICAL CHARACTERISTICS

**TL750L05**
**EQUIVALENT SERIES RESISTANCE**
**vs**
**LOAD CURRENT**

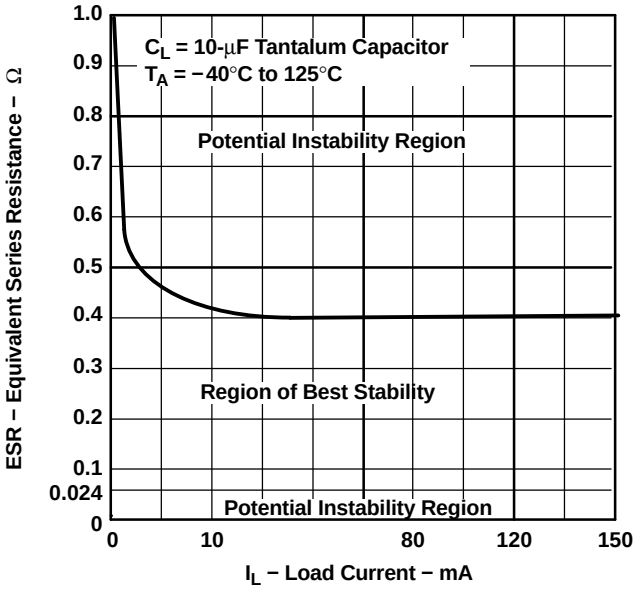



Figure 1.

**TRANSIENT INPUT VOLTAGE**
**vs**
**TIME**

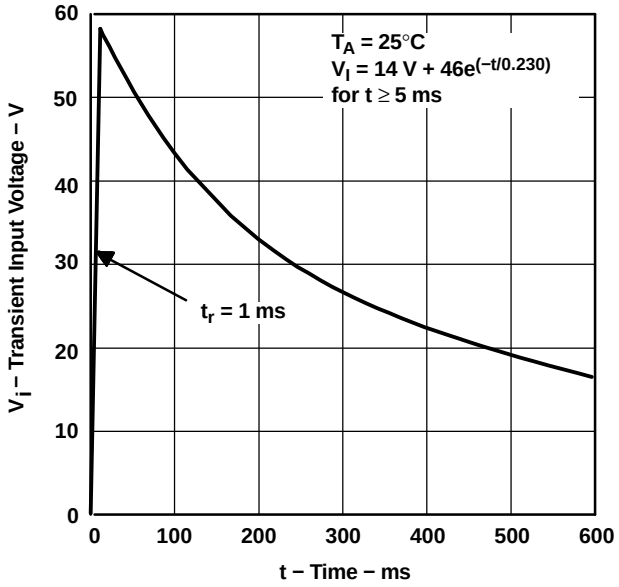



Figure 2.

**TL750L05**
**INPUT CURRENT**
**vs**
**INPUT VOLTAGE**

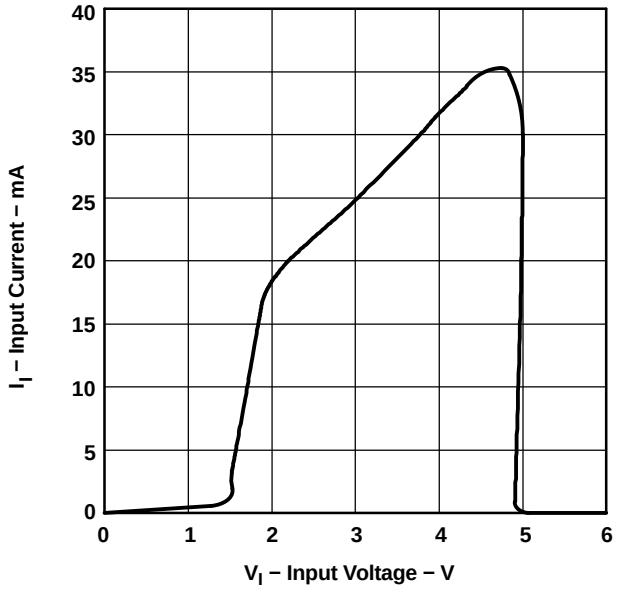



Figure 3.

**TL750L12**
**INPUT CURRENT**
**vs**
**INPUT VOLTAGE**

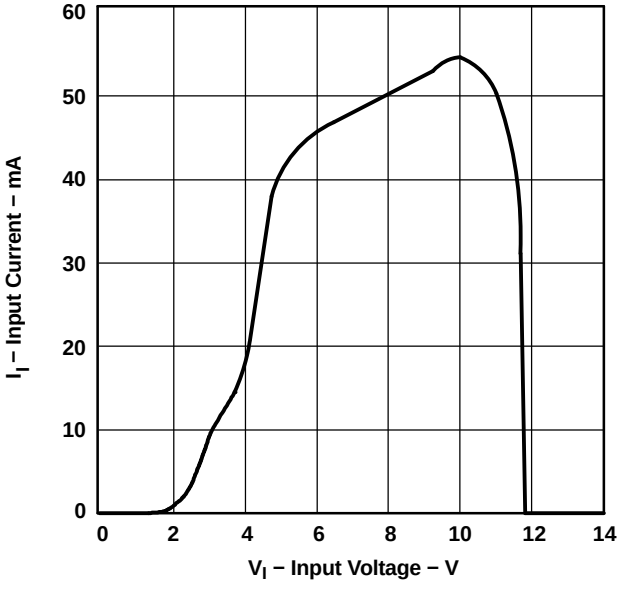
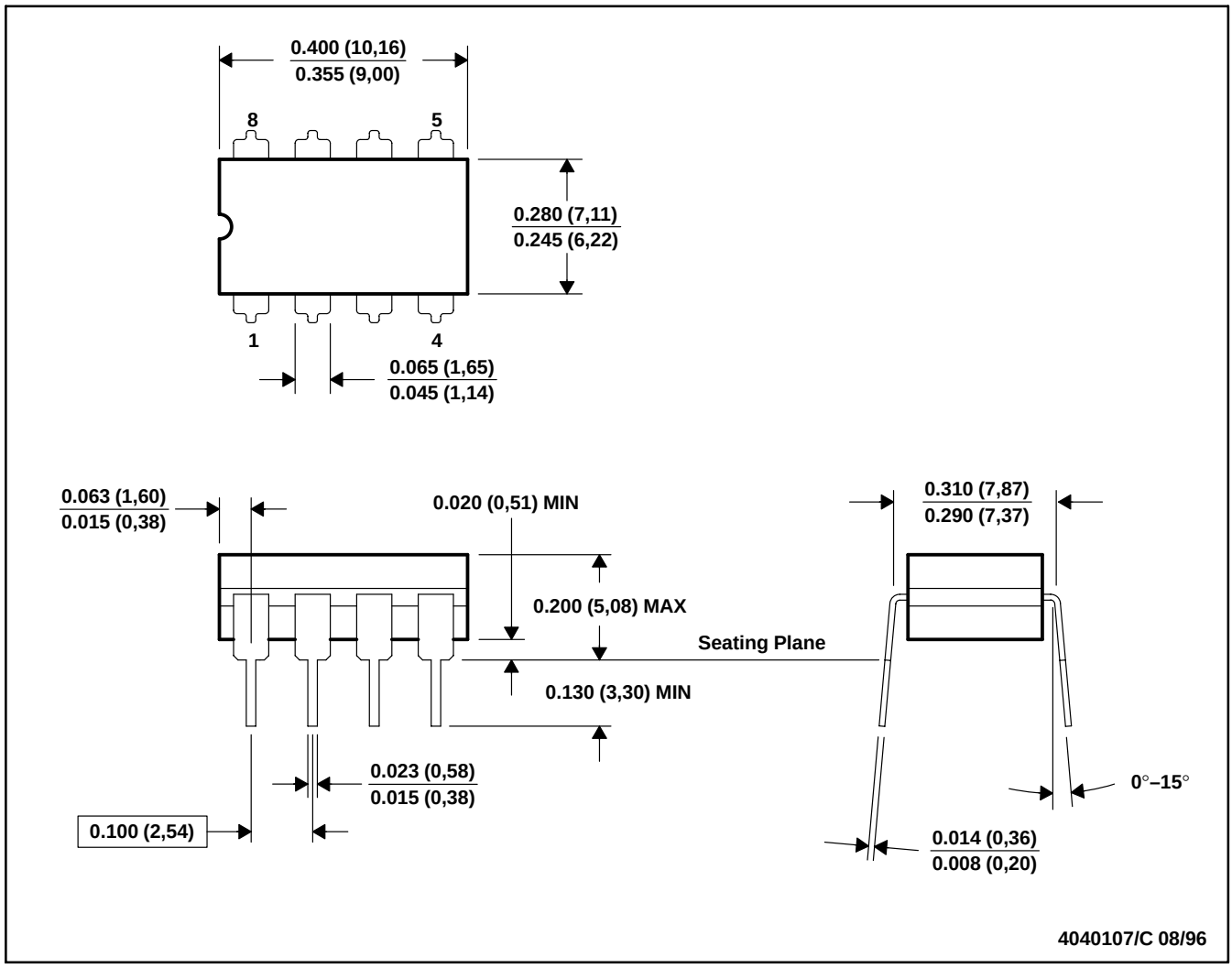



Figure 4.

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

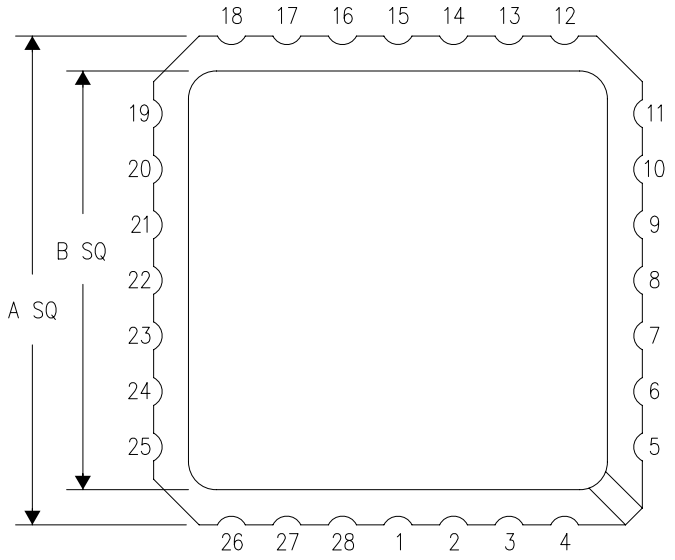
**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**



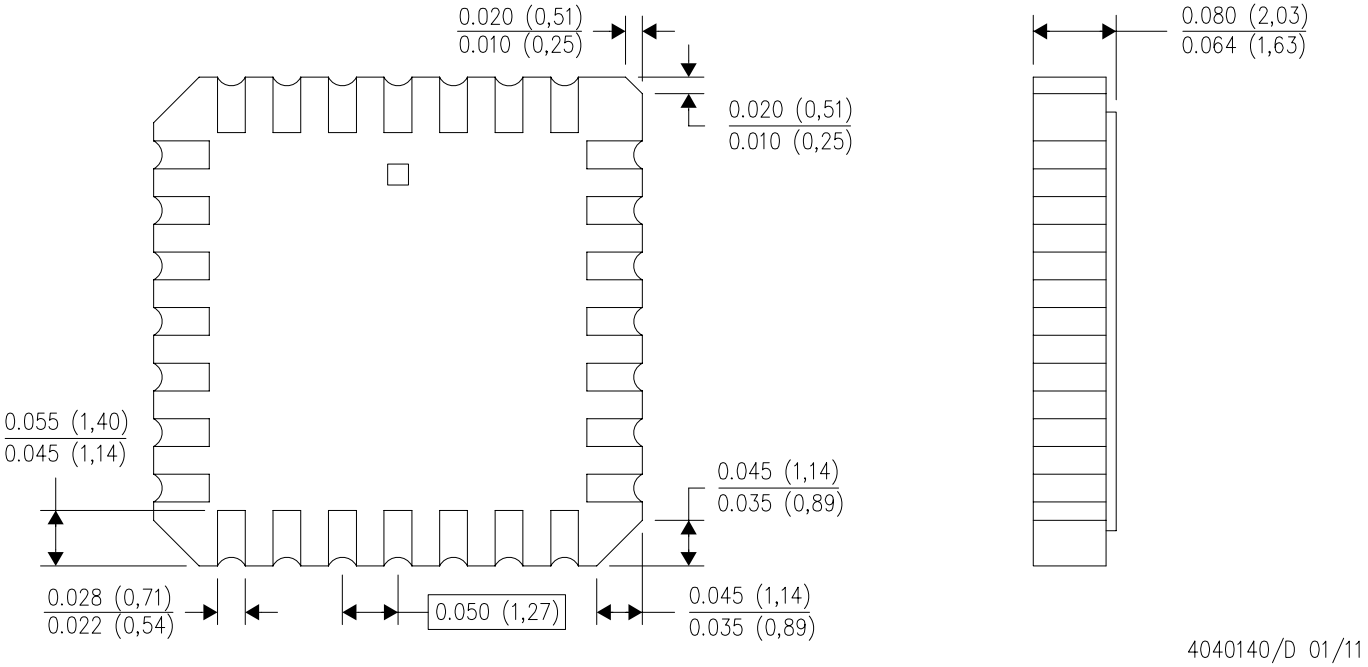

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

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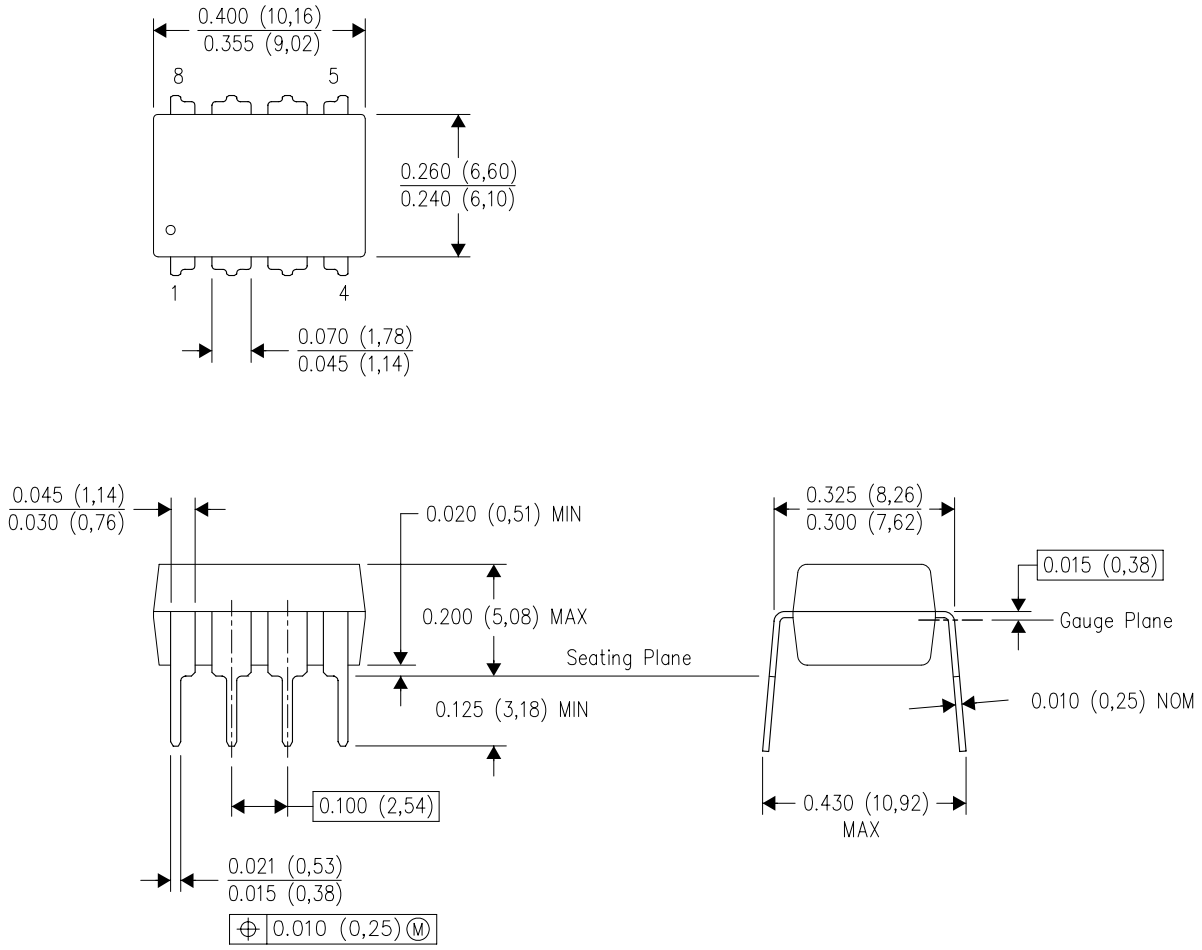
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

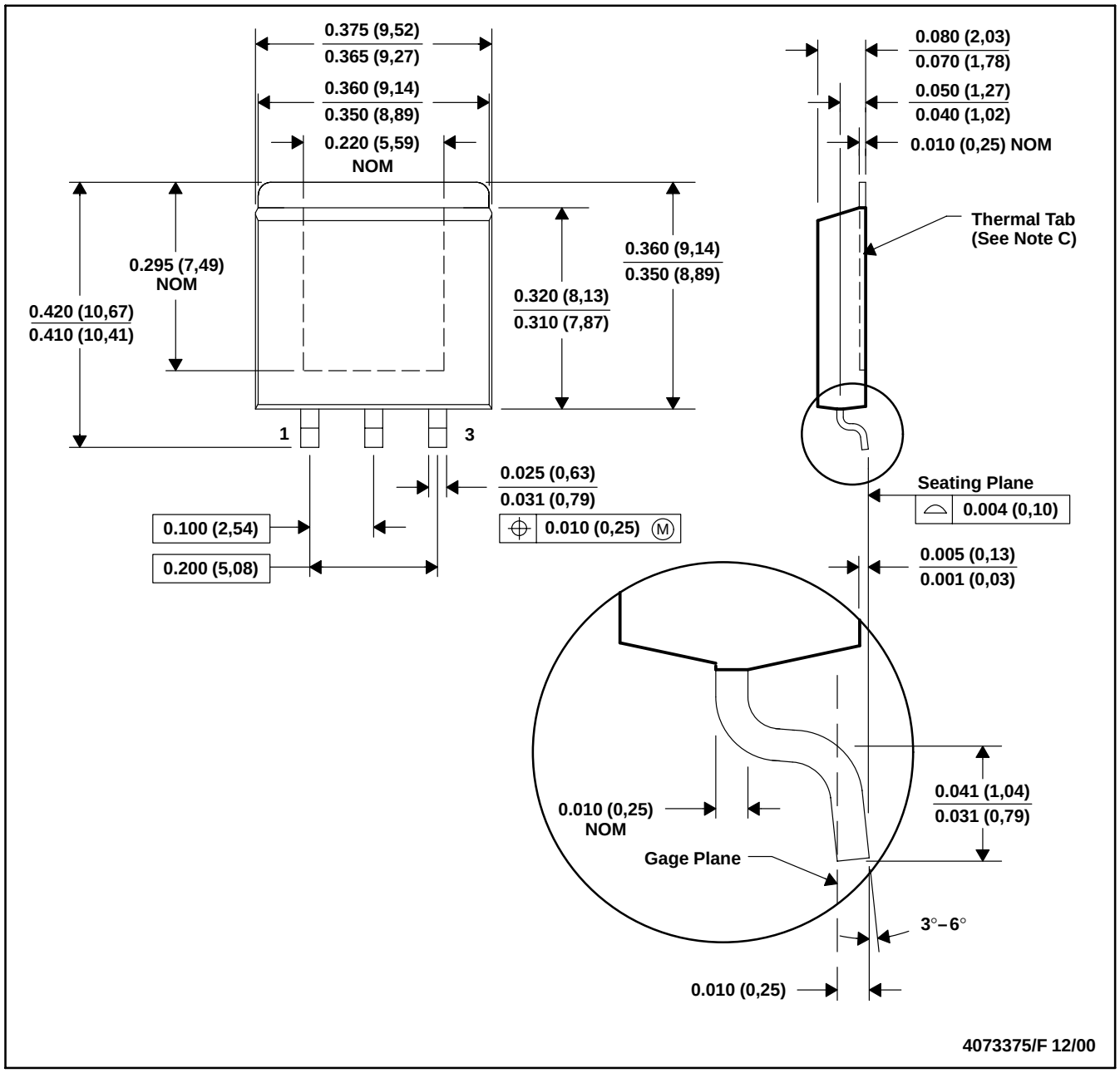
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

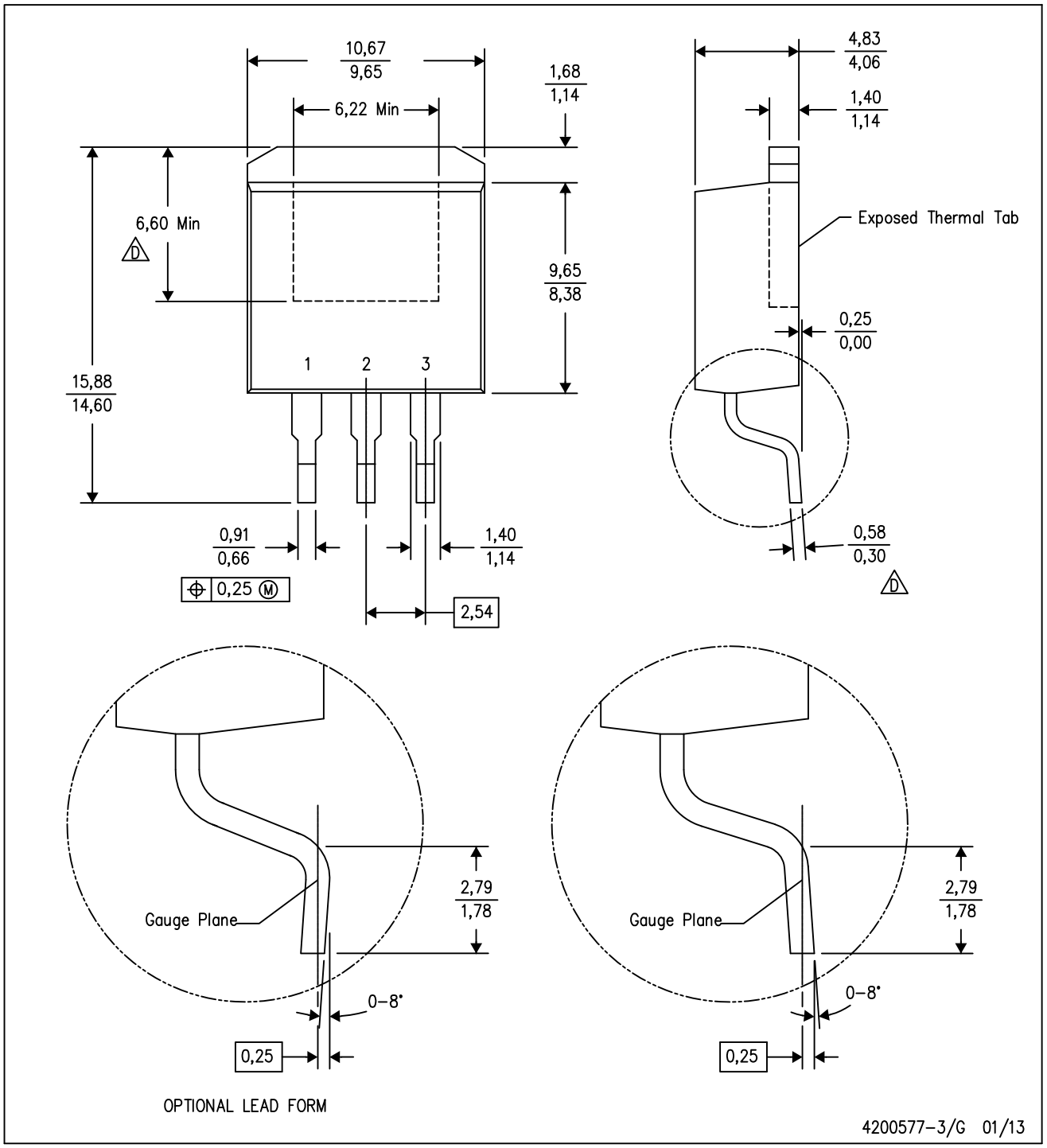
**KTE (R-PSFM-G3)** **PowerFLEX™ PLASTIC FLANGE-MOUNT**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC MO-169

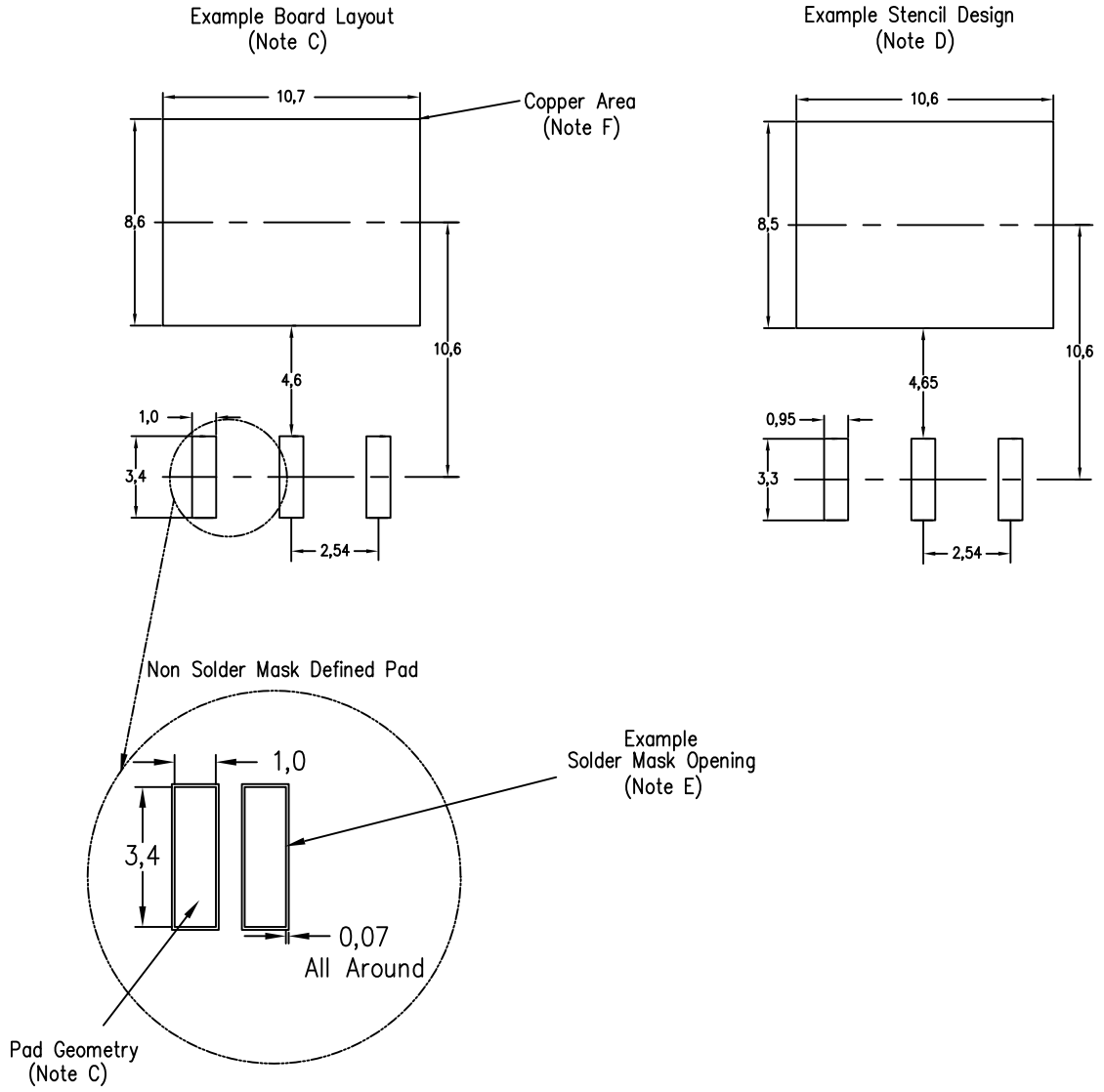
PowerFLEX is a trademark of Texas Instruments.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



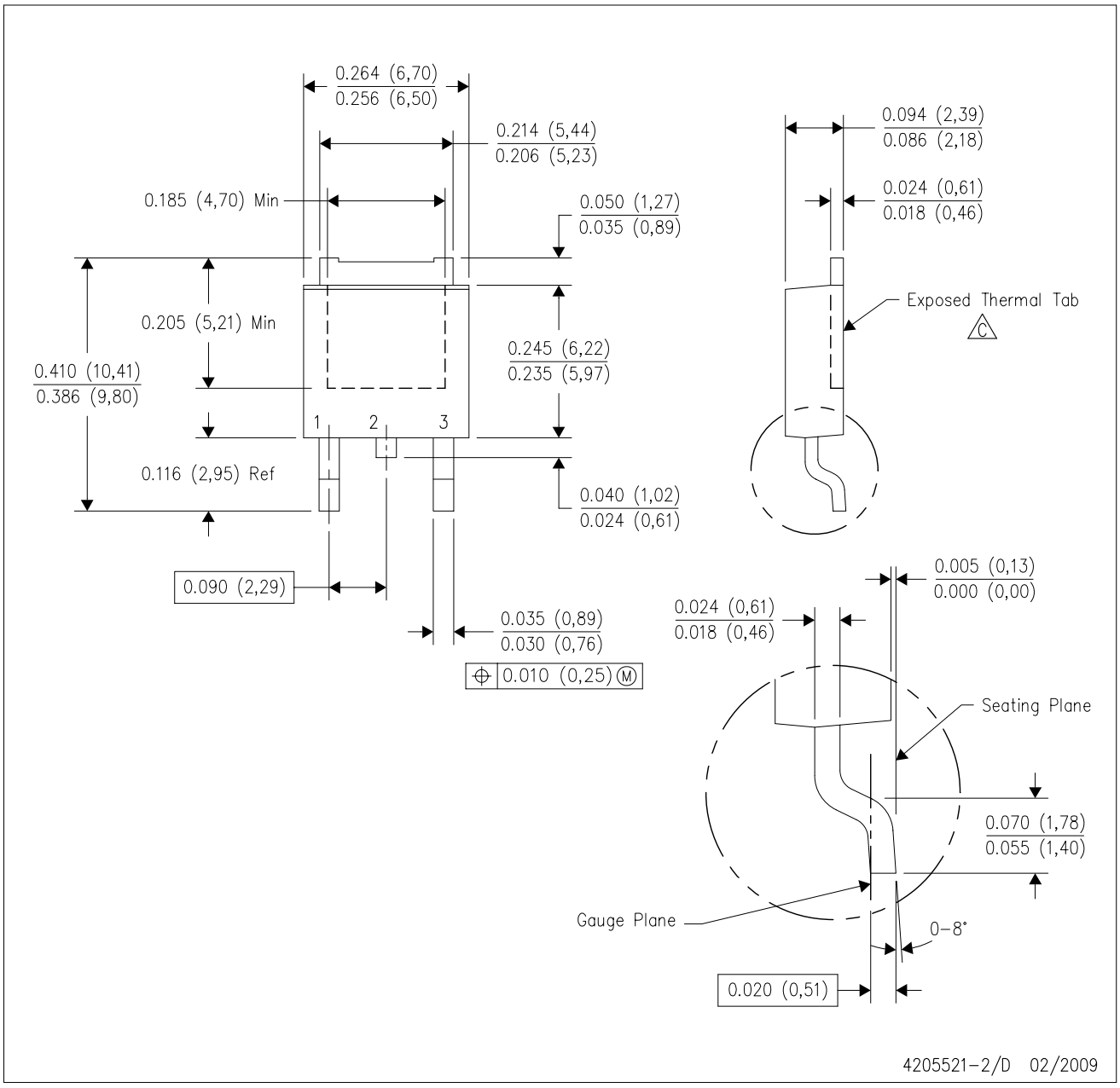

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



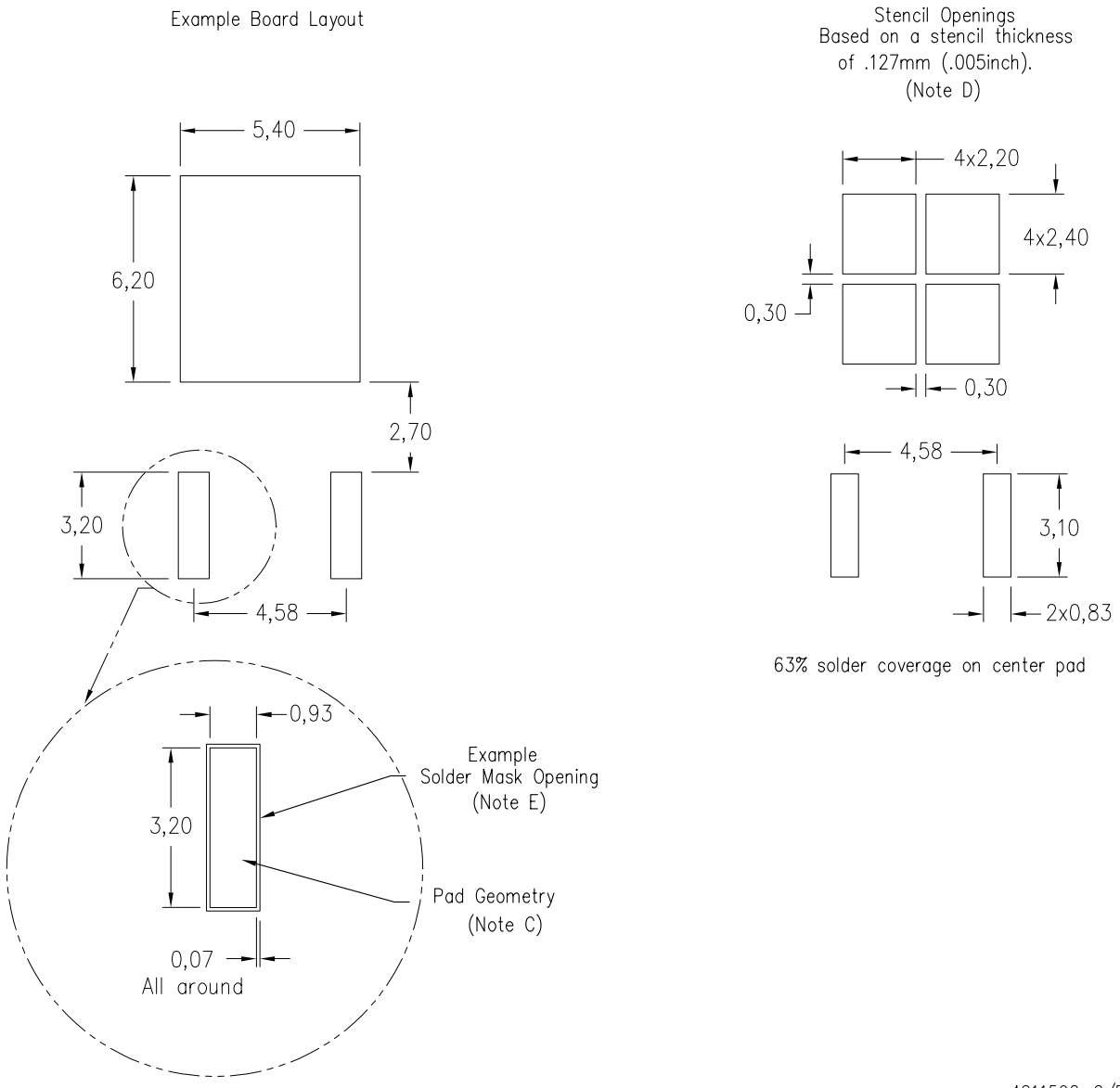

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

KVU (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE

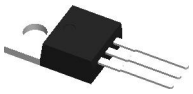



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AA.

# KVU (R–PSFM–G3) PLASTIC FLANGE MOUNT PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

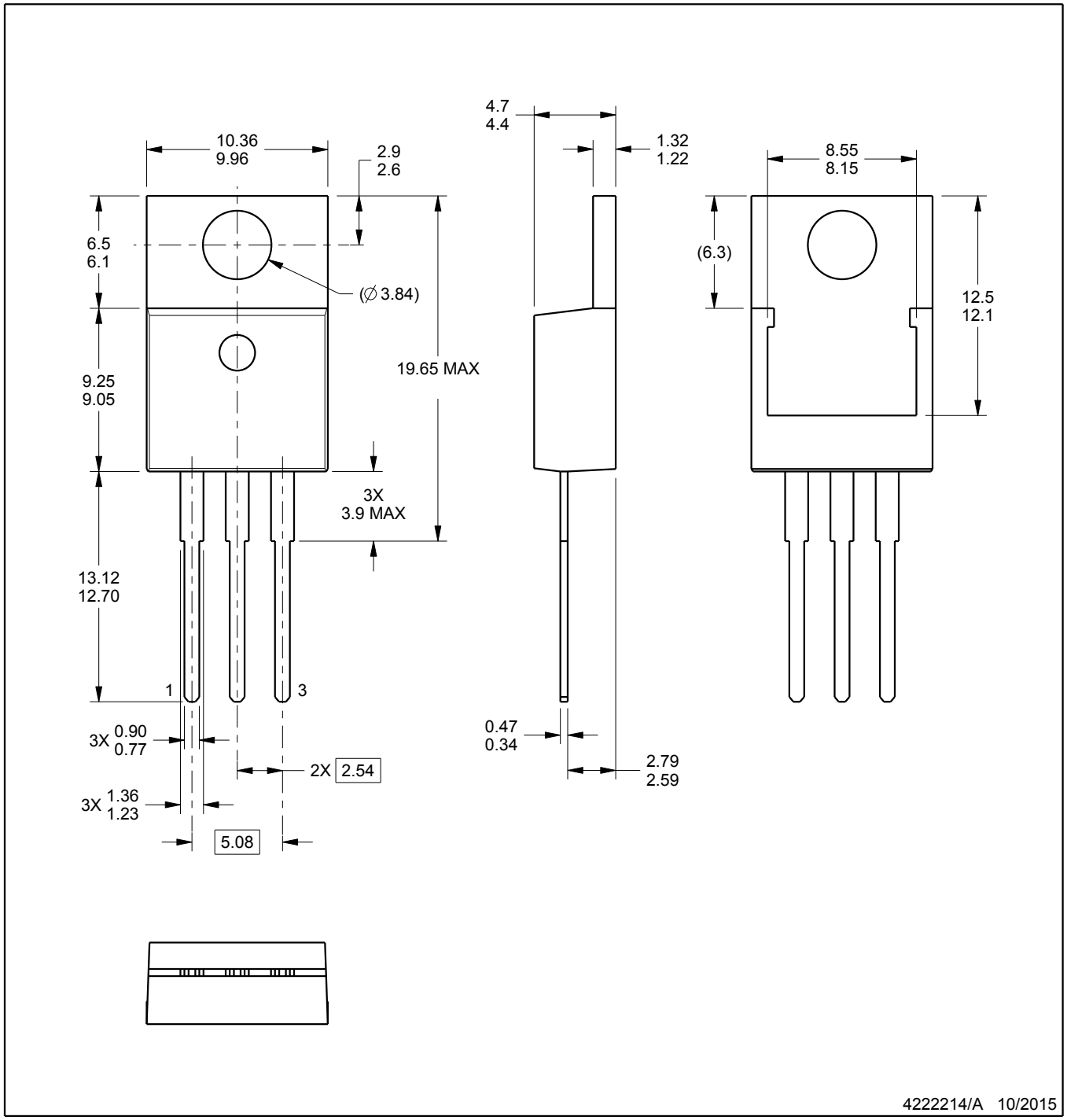


# PACKAGE OUTLINE

## KCS0003B

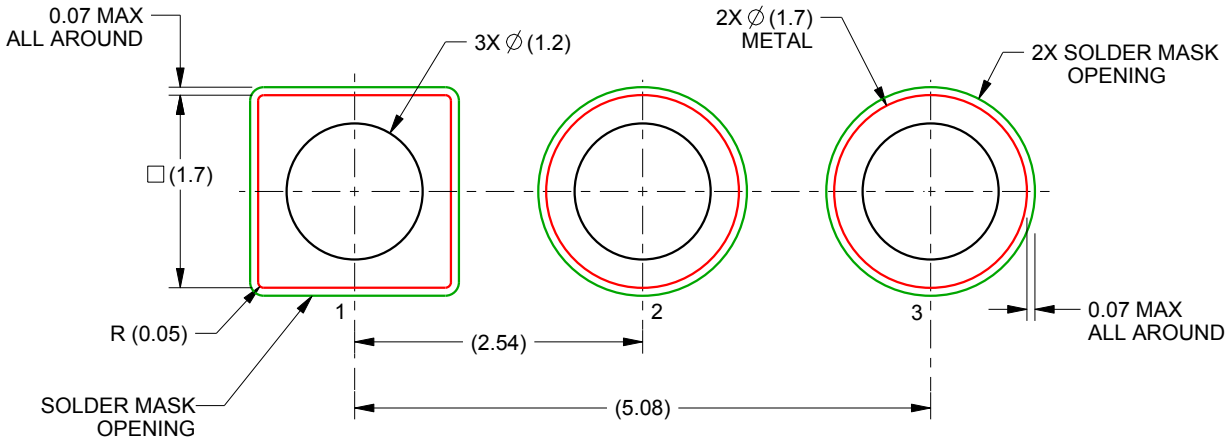
## TO-220 - 19.65 mm max height

TO-220




NOTES:

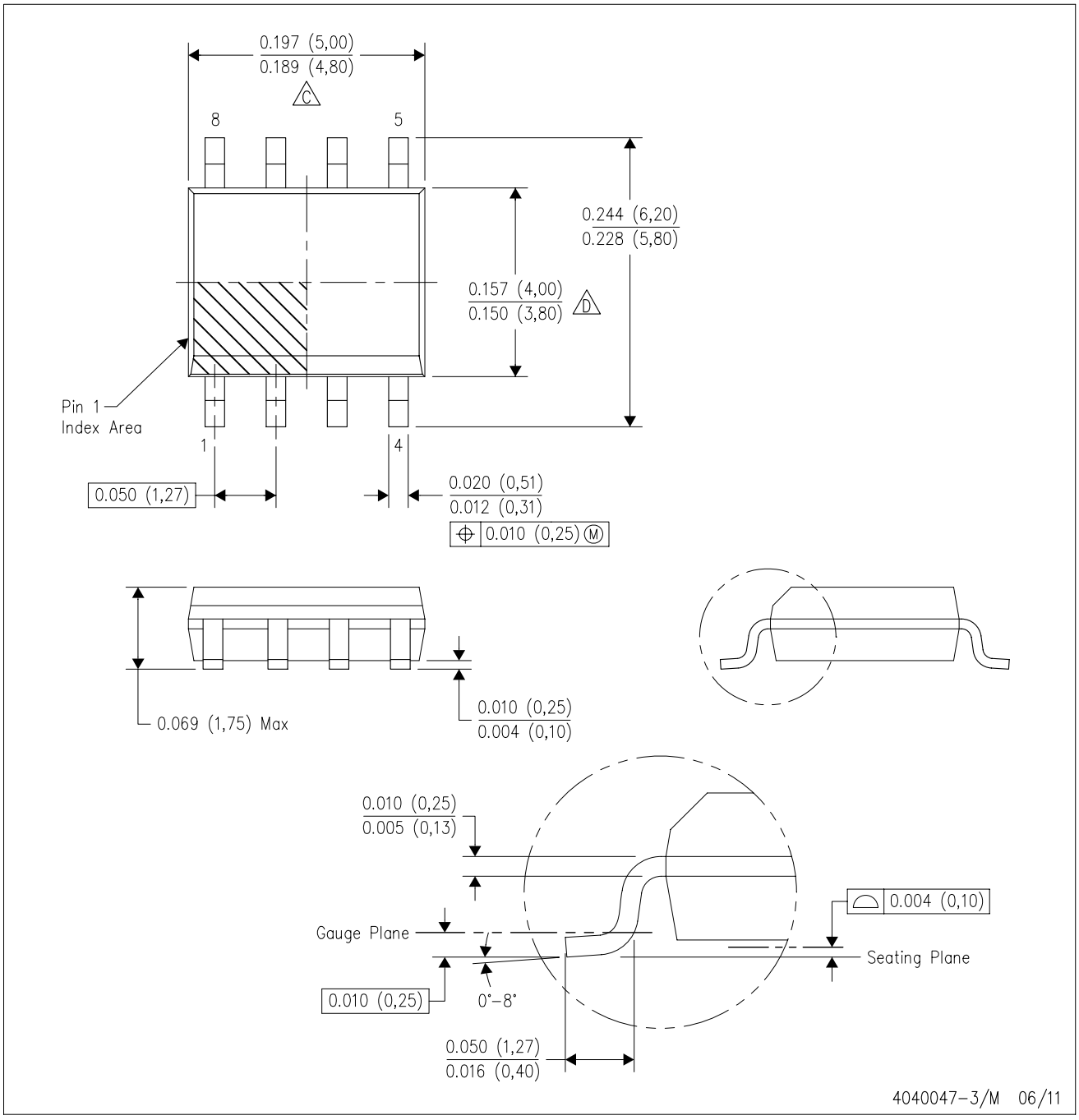
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

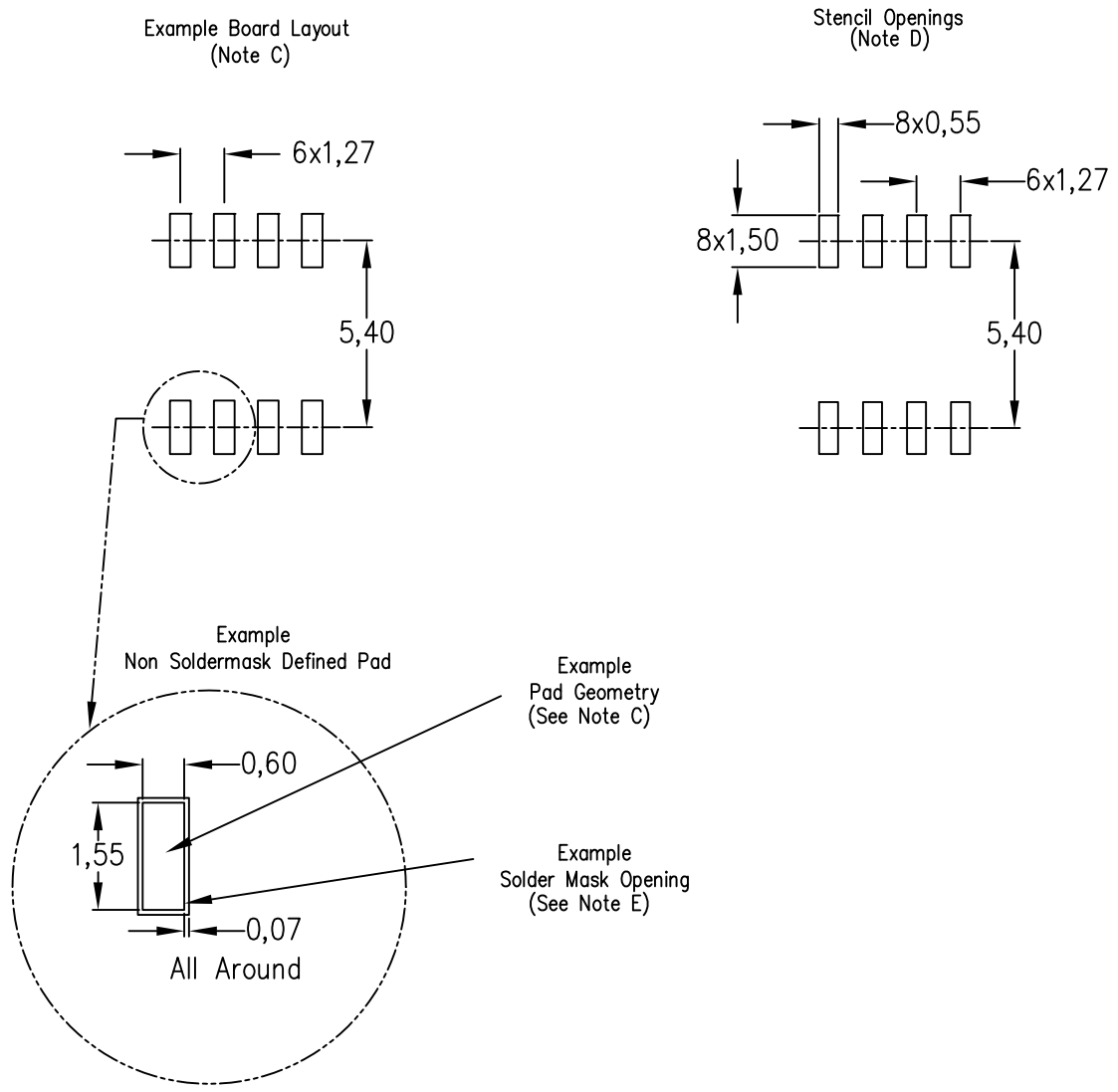
4222214/A 10/2015

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



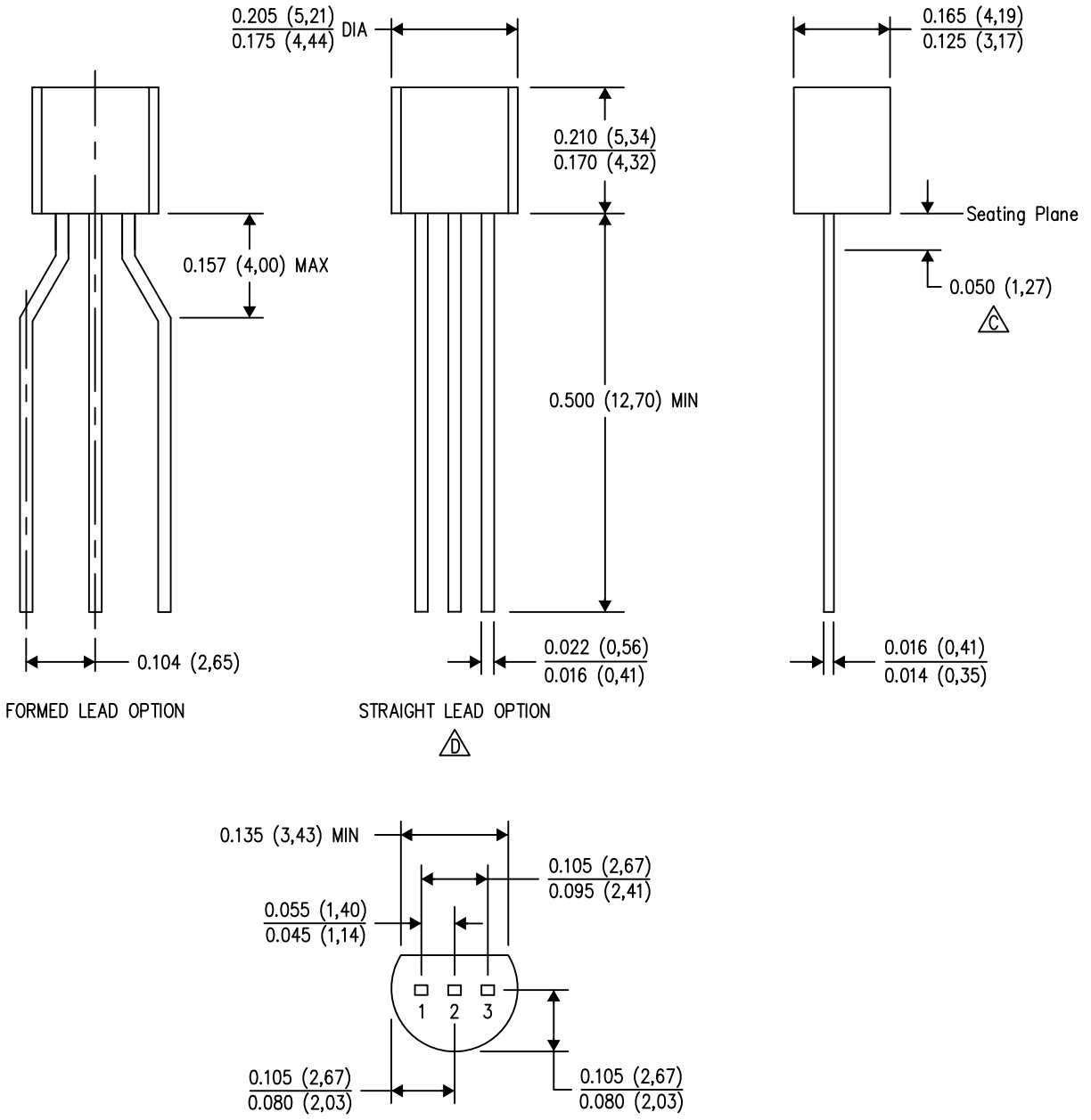

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



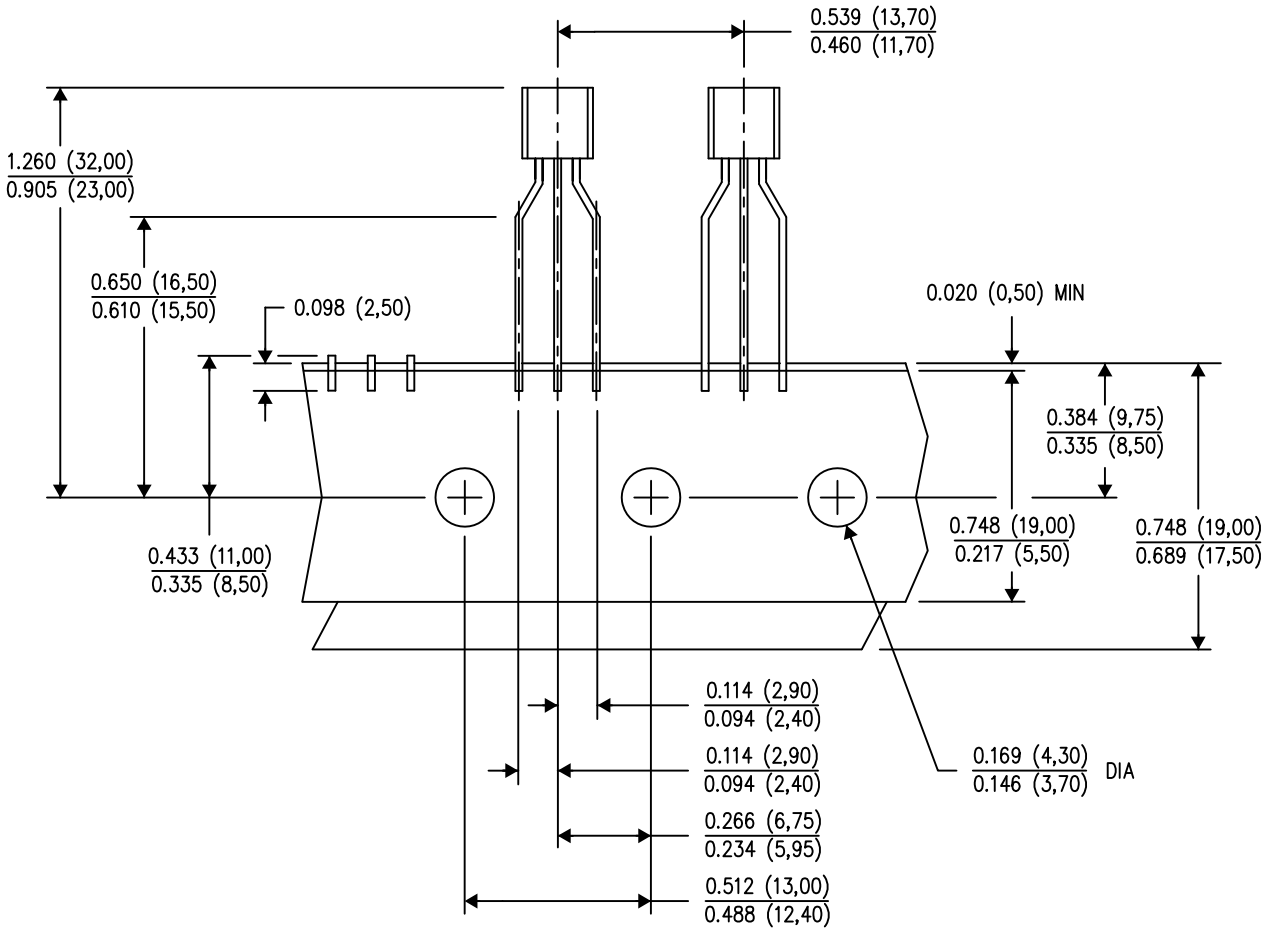

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO–226 Variation AA (TO–226 replaces TO–92).
E. Shipping Method:
Straight lead option available in bulk pack only.
Formed lead option available in tape & reel or ammo pack.
Specific products can be offered in limited combinations of shipping mediums and lead options.
Consult product folder for more information on available options.

LP (O–PBCY–W3) PLASTIC CYLINDRICAL PACKAGE

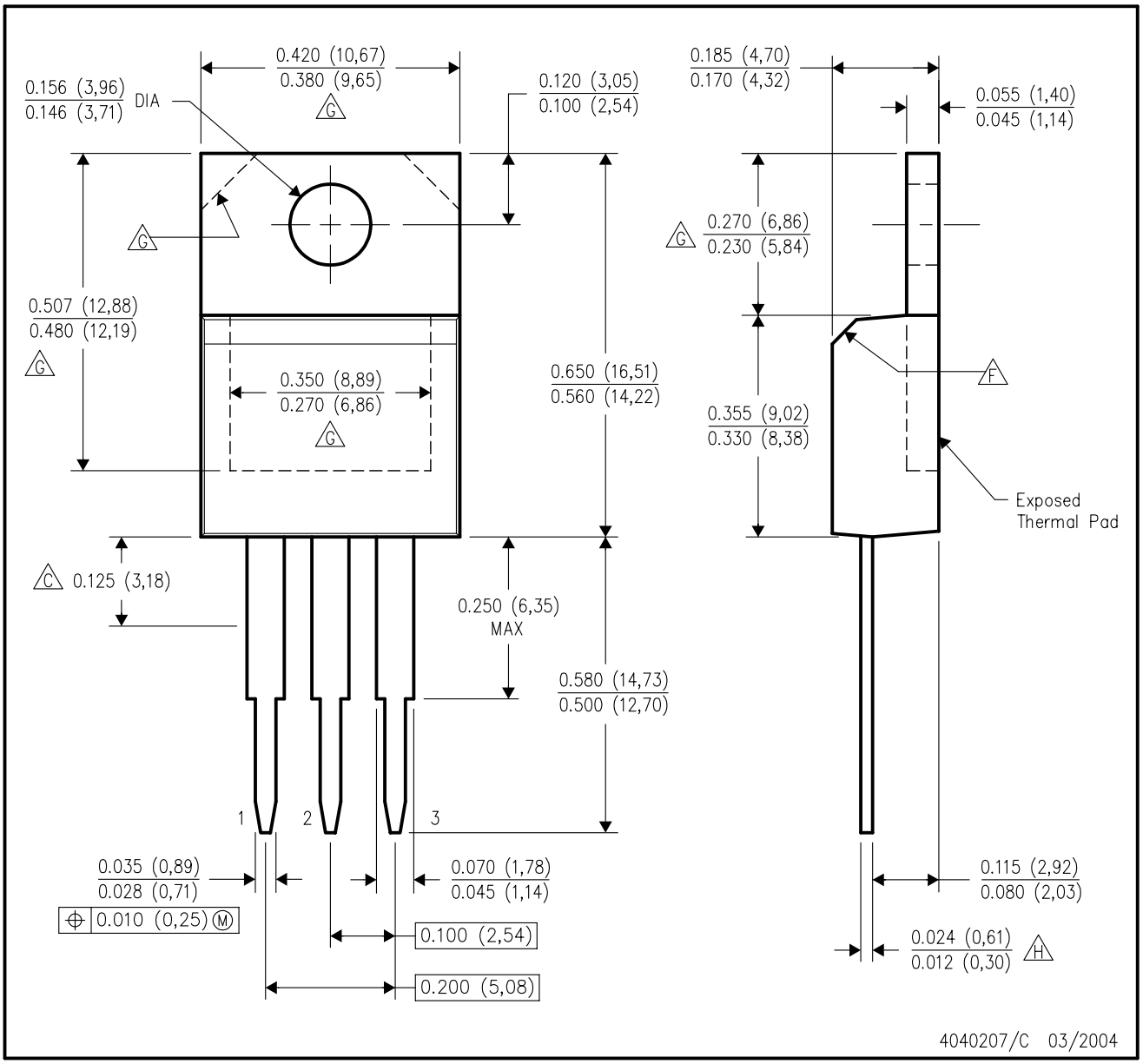



TAPE & REEL

4040001–3/E 08/13

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Formed Lead Option package.

## KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.