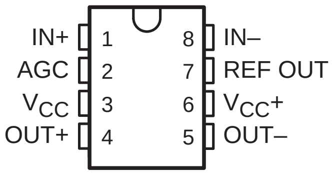
TL026C
DIFFERENTIAL HIGH-FREQUENCY AMPLIFIER WITH AGC

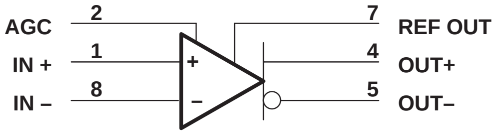
SLFS007A – JUNE 1985 – REVISED JULY 1990

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Peak Gain . . . 38 dB Typ**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D OR P PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage high-frequency amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pin. No external compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers where a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL026C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC+} (see Note 1)	8 V
Supply voltage, V_{CC-} (see Note 1)	– 8 V
Differential input voltage	±5 V
Common-mode input voltage	±6 V
Output current	±10 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	– 65°C to 150°C
Lead temperature range 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the midpoint of V_{CC+} and V_{CC-} except differential input and output voltages.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25$°C POWER RATING	OPERATING FACTOR ABOVE $T_A = 25$°C	$T_A = 70$°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	– 3	– 6	– 8	V
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics at 25°C operating free-air temperature, $V_{CC+} = \pm 6$ V, $V_{AGC} = 0$, REF OUT pin open (unless otherwise specified)

PARAMETER		FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)} = 3$ V, $R_L = 2$ kΩ	65	85	105	V/V
ΔA_{VD}	Change in voltage amplification	1	$V_{IPP} = 28.5$ mV, $R_L = 2$ kΩ, $V_{AGC} - V_{ref} = \pm 180$ mV		– 50		dB
V_{ref}	Voltage at REF OUT		$I_{ref} = -1$ mA to 100 µA	1.3		1.5	V
BW	Bandwidth (– 3 dB)	2	$V_{O(PP)} = 1$ V, $V_{AGC} - V_{ref} = \pm 180$ mV		50		MHz
I_{IO}	Input offset current				0.4	5	µA
I_{IB}	Input bias current				10	30	µA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OC}	Common-mode output voltage	1	$R_L = \infty$	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	$V_{AGC} = 0$ to 2 V, $R_L = \infty$			300	mV
V_{OO}	Output offset voltage	1	$V_{ID} = 0$, $R_L = \infty$			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	$R_L = 2$ kΩ	3	4		V
r_i	Input resistance at AGC, IN+, or IN –			10	30		kΩ
r_o	Output resistance				20		Ω
CMRR	Common-mode rejection ratio	3	$V_{IC} = \pm 1$ V, f = 100 kHz	60	86		dB
			$V_{IC} = \pm 1$ V, f = 5 mHz		60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	4	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz		12		µV
t_{pd}	Propagation delay time	2	$\Delta V_O = 1$ V		6	10	ns
t_r	Rise time	2	$\Delta V_O = 1$ V		4.5	12	ns
$I_{sink(max)}$	Maximum output sink current		$V_{ID} = 1$ V, $V_O = 3$ V	3	4		mA
I_{CC}	Supply current		No load, No signal		22	27	mA

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm6$ V, $V_{AGC} = 0$, REF OUT pin open (unless otherwise specified)

PARAMETER		FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)} = 3$ V,	$R_L = 2$ kΩ	55		115	V/V
I_{IO}	Input offset current						6	µA
I_{IB}	Input bias current						40	µA
V_{ICR}	Common-mode input voltage range	3			±1			V
V_{OO}	Output offset voltage	1	$V_{ID} = 0$,	$R_L = \infty$			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	$R_L = 2$ kΩ		2.8			V
r_i	Input resistance at AGC, IN+, or IN –				8			kΩ
CMRR	Common-mode rejection ratio	3	$V_{IC} = \pm1$ V,	f = 100 kHz	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC} / \Delta V_{IO}$)	4	$\Delta V_{CC+} = \pm 0.5$ V, $\Delta V_{CC-} = \pm 0.5$ V		50			dB
$I_{sink(max)}$	Maximum output sink current		$V_{ID} = 1$ V,	$V_O = 3$ V	2.8	4		mA
I_{CC}	Supply current	1	No load,	No signal			30	mA

PARAMETER MEASUREMENT INFORMATION

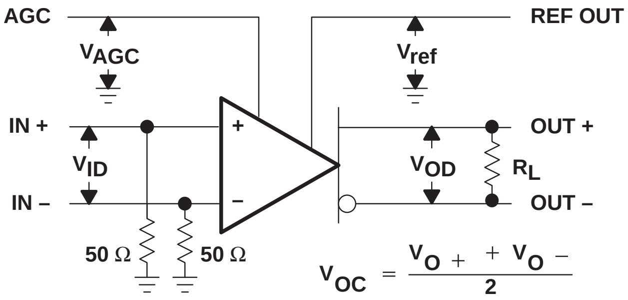


Figure 1. Test Circuit

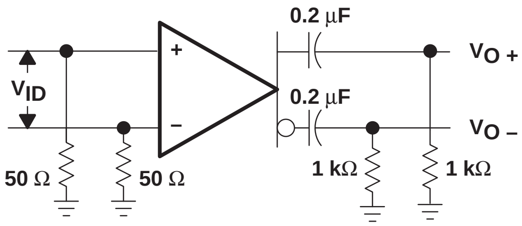


Figure 2. Test Circuit

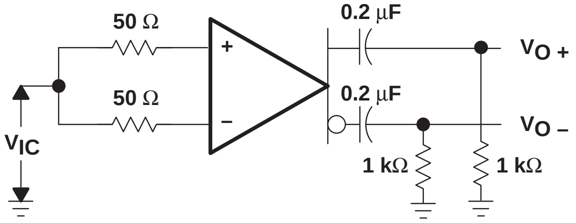


Figure 3. Test Circuit

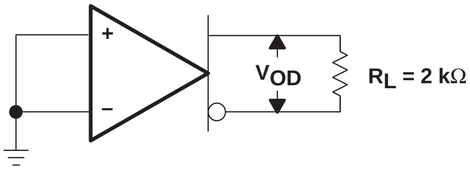


Figure 4. Test Circuit

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

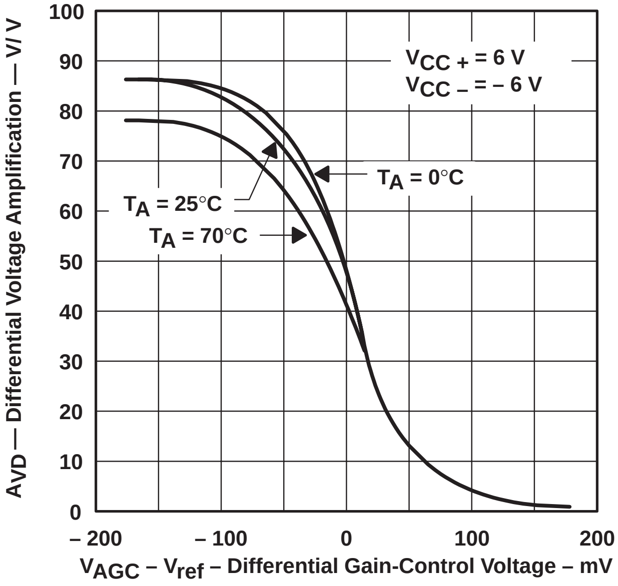


Figure 5

APPLICATION INFORMATION

gain characteristics

Figure 5 shows the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the A_{GC} input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL026C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\text{ mV} - (V_{ref} - 180\text{ mV}) \qquad (1)$$

$$\Delta V_{AGC} = 360\text{ mV}$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 6 and 7 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TL026C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 6 and 7) from the OUT output through the feedback amplifiers to the AGC input produces the following equations:

1. AC ouput to diode D1, assuming sinusoidal signals

$$V_O = V_{OP}\ (\sin\ (wt)) \qquad (2)$$

where:
V_{OP} = peak voltage of V_O

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \qquad (3)$$

where:
VF = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1}\ V_C \qquad (4)$$

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1}\ V_C + 2\frac{R6}{R5 + R6}\ V_{ref} \qquad (5)$$

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Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL026C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1}\ V_C \tag{6}$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC}(q) = 2\frac{R6}{R5 + R6}V_{ref} \tag{7}$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC}(q) = V_{ref} – 180$ mV). This voltage allows the TL026C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 6 and 7)

The output voltage level desired must fall within the following limits:

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. Aschottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_C = V_{OP} – V_d$), V_C is calculated as follows:

$V_C = 1\text{ V} – 0.7\text{ V}$

$V_C = 0.3\text{ V}$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL026C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_C} = \frac{\Delta V_{AGC}}{V_C} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 time R1 or 12 kΩ.

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 6 and 7 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

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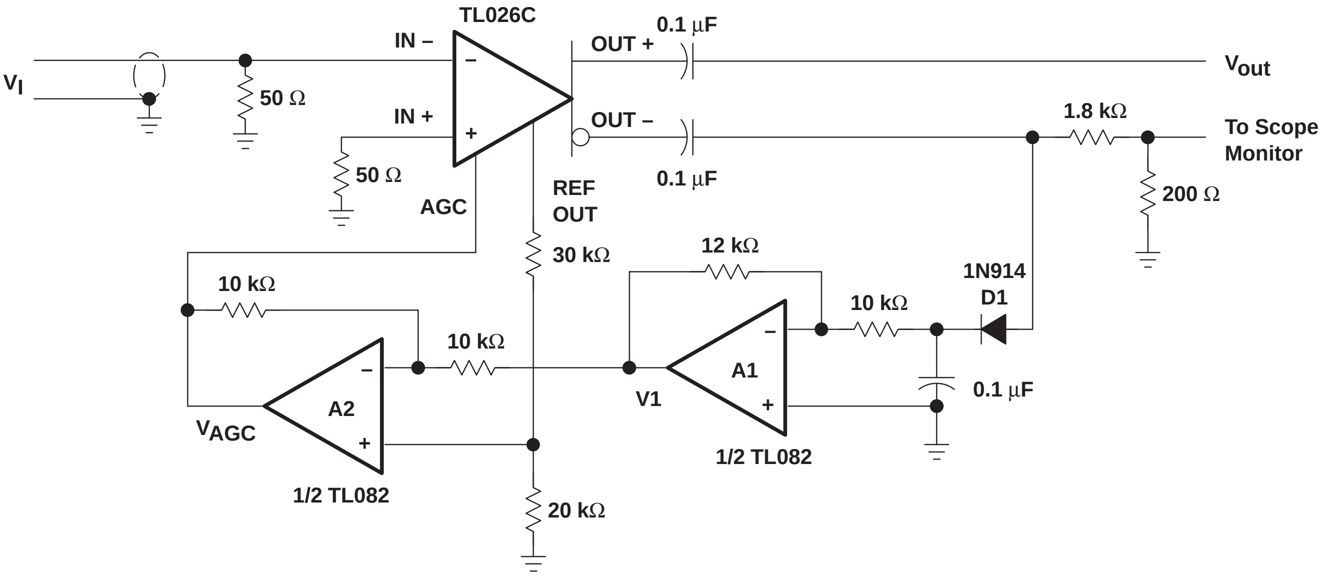
The circuit values in Figures 6 and 7 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 6 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 7 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL026C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL026C

To obtain the most reliable results, RF breadboarding techniques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL026C and, while the circuit is in the AGC mode, the output signal may become distorted.

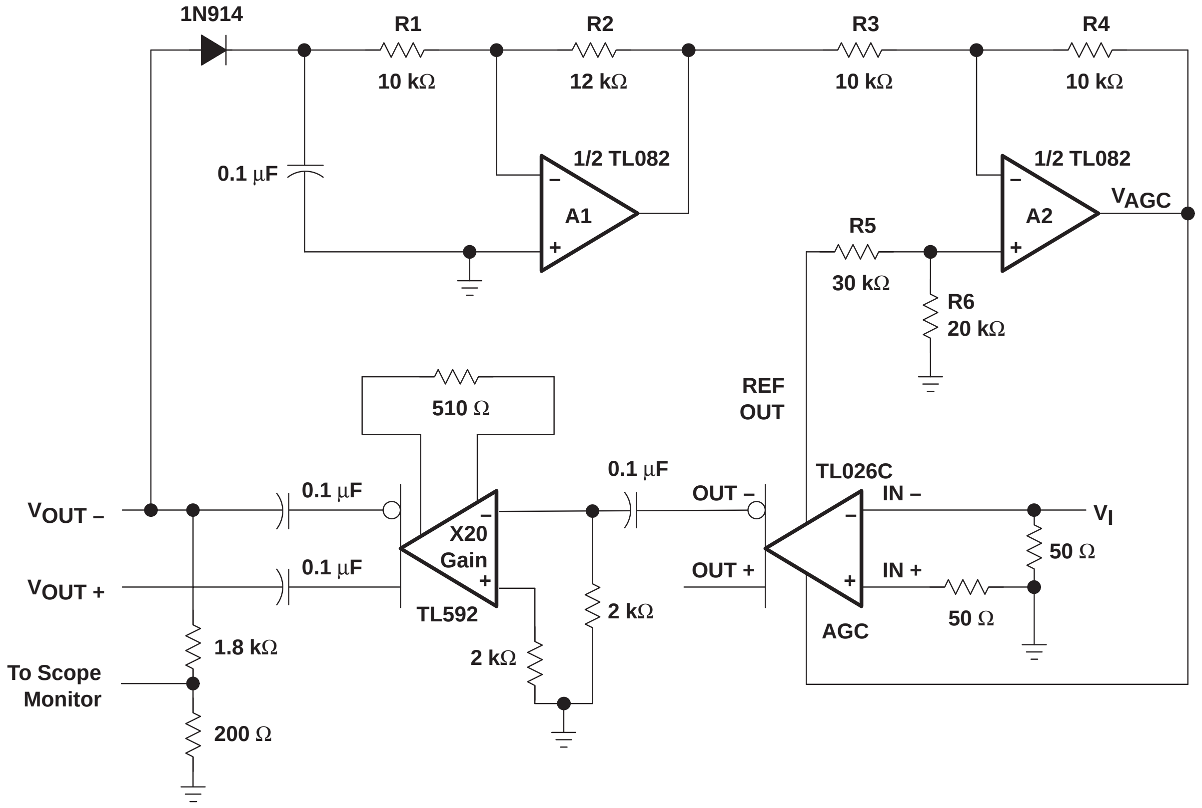
To observe the output signal of TL026C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 6 should be used.



NOTE: V_{CC+} = 6 V and V_{CC-} = – 6 V for TL026C and amplifiers A1 and A2.

Figure 6. Typical Application Circuit With No Attenuation

APPLICATION INFORMATION



NOTE: V_{CC+} = 6 V and V_{CC-} = – 6 V for TL026C and amplifiers A1 and A2.

Figure 7. Typical Application Circuit With Attenuation

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TL026CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TL026CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL026CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL026CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL026CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL026CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL026ID	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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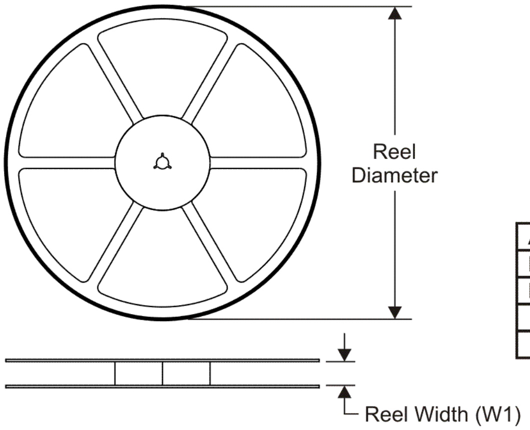
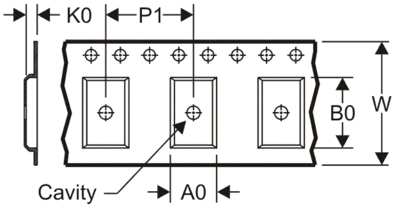
TAPE AND REEL INFORMATION

REEL DIMENSIONS

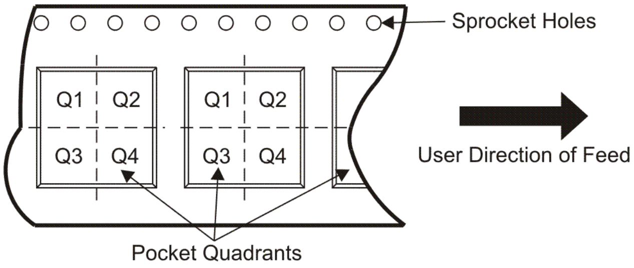


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

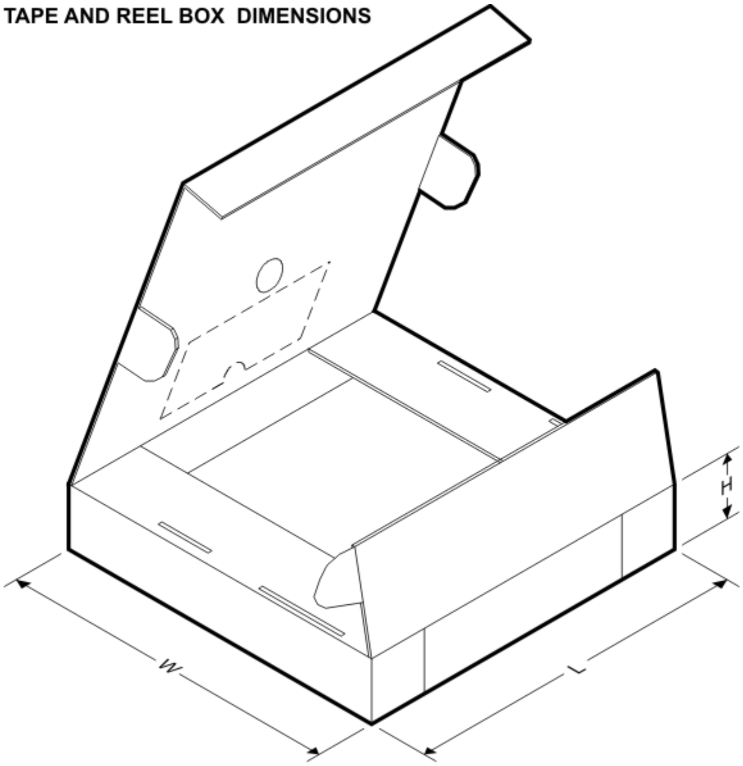
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL026CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL026CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

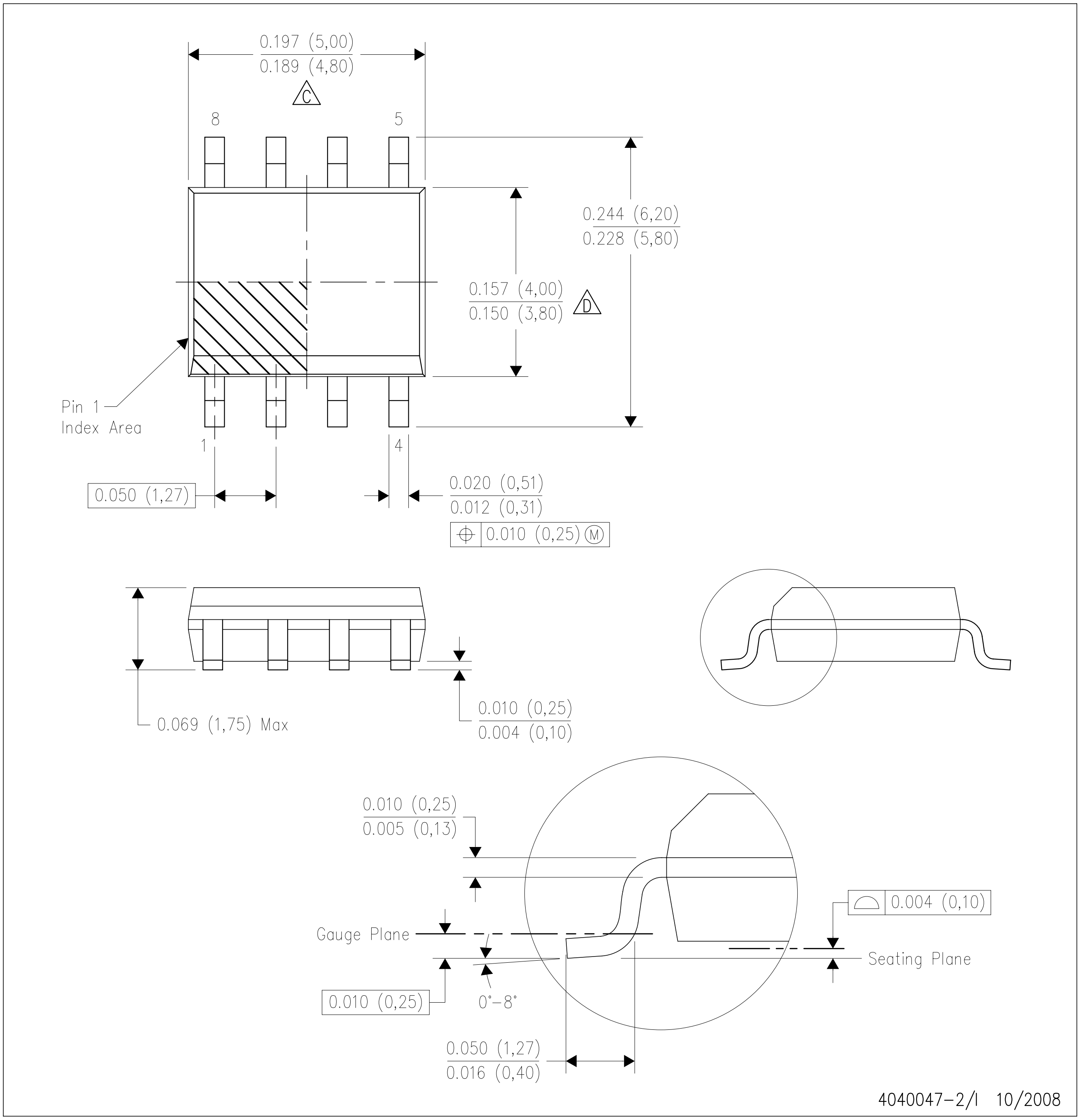
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

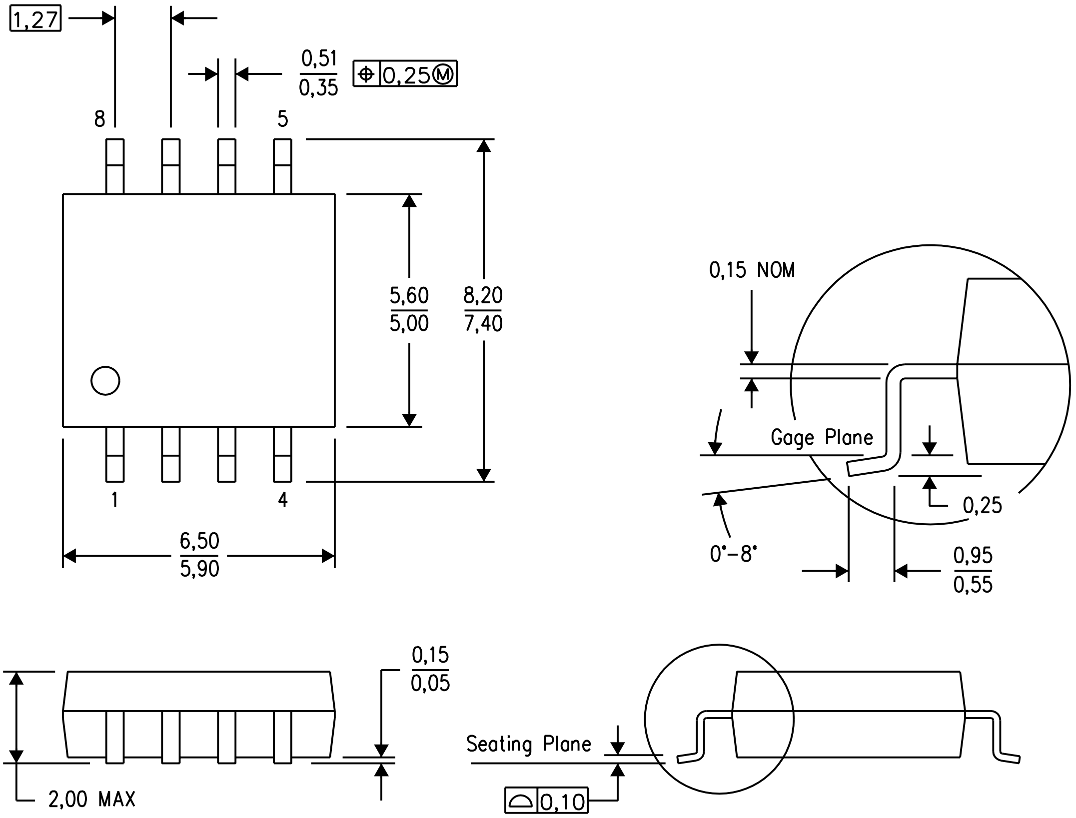
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL026CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL026CPSR	SO	PS	8	2000	346.0	346.0	33.0

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.



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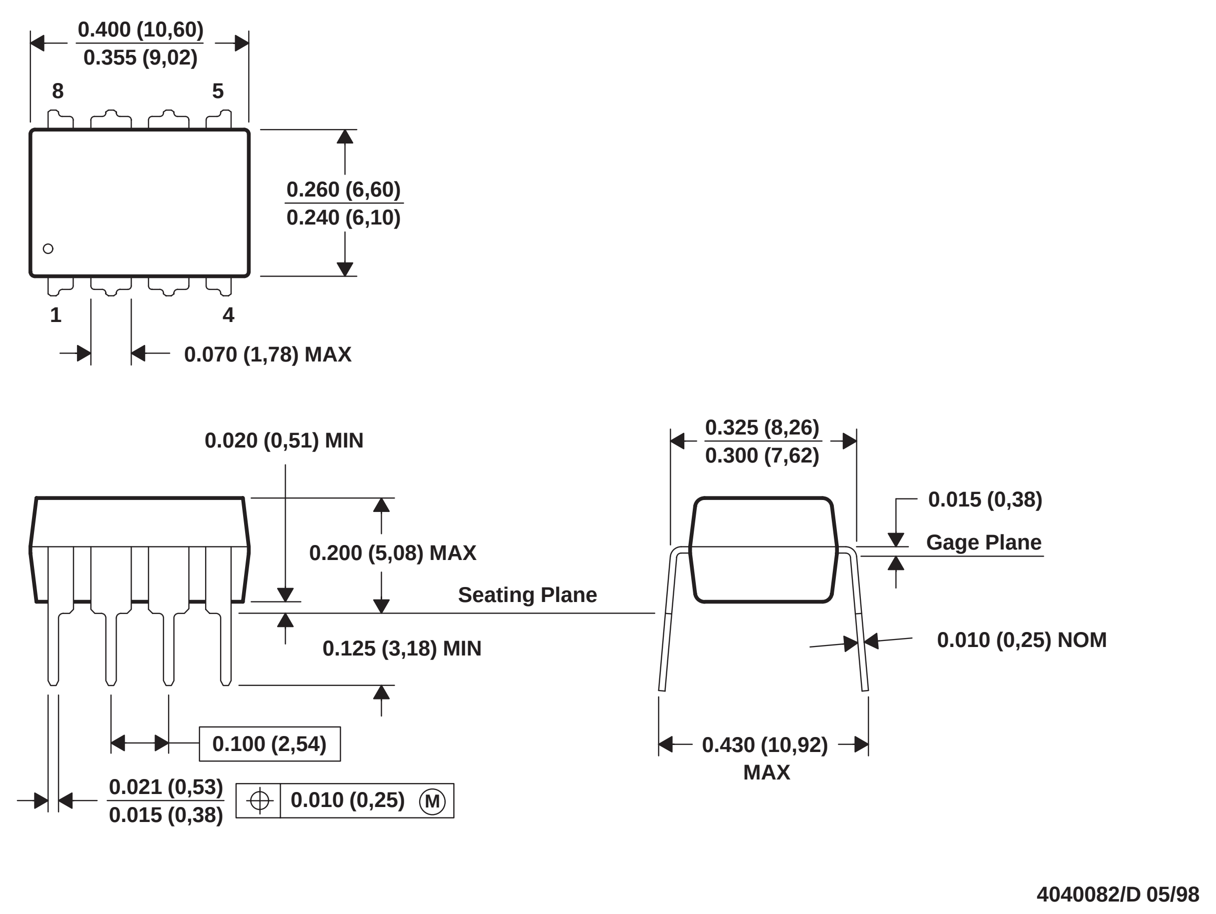
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

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