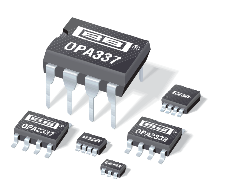


OPA337, OPA2337
OPA338, OPA2338

SBOS077B − JUNE 1997 − REVISED MARCH 2005

*Micro*SIZE, Single-Supply CMOS OPERATIONAL AMPLIFIERS *MicroAmplifier* ™ Series

FEATURES

- *Micro*SIZE PACKAGES:
  SOT23-5, SOT23-8
- SINGLE-SUPPLY OPERATION
- RAIL-TO-RAIL OUTPUT SWING
- FET-INPUT: I_B = 10pA max
- HIGH SPEED:
  OPA337: 3MHz, 1.2V/μs (G = 1)
  OPA338: 12.5MHz, 4.6V/μs (G = 5)
- OPERATION FROM 2.5V to 5.5V
- HIGH OPEN-LOOP GAIN: 120dB
- LOW QUIESCENT CURRENT: 525μA/amp
- SINGLE AND DUAL VERSIONS

APPLICATIONS

- BATTERY-POWERED INSTRUMENTS
- PHOTODIODE PRE-AMPS
- MEDICAL INSTRUMENTS
- TEST EQUIPMENT
- AUDIO SYSTEMS
- DRIVING ADCs
- CONSUMER PRODUCTS

SPICE model available at www.ti.com.

DESCRIPTION

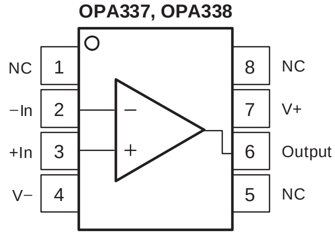
The OPA337 and OPA338 series rail-to-rail output CMOS operational amplifiers are designed for low cost and miniature applications. Packaged in the SOT23-8, the OPA2337EA and OPA2338EA are Texas Instruments' smallest dual op amps. At 1/4 the size of a conventional SO-8 surface-mount, they are ideal for space-sensitive applications.

Utilizing advanced CMOS technology, the OPA337 and OPA338 op amps provide low bias current, high-speed operation, high open-loop gain, and rail-to-rail output swing. They operate on a single supply with operation as low as 2.5V while drawing only 525μA quiescent current. In addition, the input common-mode voltage range includes ground—ideal for single-supply operation.

The OPA337 series is unity-gain stable. The OPA338 series is optimized for gains greater than or equal to 5. They are easy-to-use and free from phase inversion and overload problems found in some other op amps. Excellent performance is maintained as the amplifiers swing to their specified limits. The dual versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

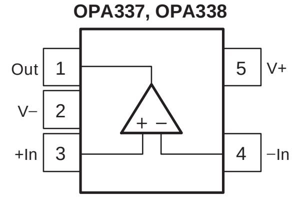
	G = 1 STABLE		G ≥ 5 STABLE	
PACKAGE	SINGLE OPA337	DUAL OPA2337	SINGLE OPA338	DUAL OPA2338
SOT23-5	✓		✓	
SOT23-8		✓		✓
MSOP-8	✓			
SO-8	✓	✓	✓	✓
DIP-8	✓	✓		

OPA337, OPA338



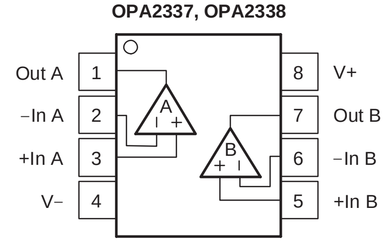
DIP−8(1), SO−8, MSOP−8(1)
NC = No Connection

OPA337, OPA338



SOT23−5

OPA2337, OPA2338



DIP−8(1), SO−8, SOT23−8

NOTE: (1) DIP AND MSOP-8 versions for OPA337, OPA2337 only.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	7.5V
Input Voltage(2)	(V−) − 0.5V to (V+) + 0.5V
Input Current(2)	10mA
Output Short Circuit(3)	Continuous
Operating Temperature	−55°C to +125°C
Storage Temperature	−55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

(3) Short-circuit to ground, one amplifier per package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA337 Series							
OPA337	Single, G = 1 Stable	SOT23-5	DBV	−40°C to +85°C	C37	OPA337NA/250	Tape and Reel, 250
						OPA337NA/3K	Tape and Reel, 3000
		MSOP-8	DGK		G37	OPA337EA/250	Tape and Reel, 250
						OPA337EA/2K5	Tape and Reel, 2500
		DIP-8	P		OPA337PA	OPA337PA	Rails
		SO-8 Surface-Mount	D		OPA337UA	OPA337UA	Rails
						OPA337UA/2K5	Tape and Reel, 2500
OPA2337	Dual, G = 1 Stable	SOT23-8	DCN	−40°C to +85°C	A7	OPA2337EA/250	Tape and Reel, 250
						OPA2337EA/3K	Tape and Reel, 3000
		DIP-8	P		OPA2337PA	OPA2337PA	Rails
		SO-8 Surface-Mount	D		OPA2337UA	OPA2337UA	Rails
						OPA2337UA/2K5	Tape and Reel, 2500
OPA338 Series							
OPA338	Single, G ≥ 5 Stable	SOT23-5	DBV	−40°C to +85°C	A38	OPA338NA/250	Tape and Reel, 250
						OPA338NA/3K	Tape and Reel, 3000
		SO-8 Surface-Mount	D		OPA338UA	OPA338UA	Rails
						OPA338UA/2K5	Tape and Reel, 2500
OPA2338	Dual, G ≥ 5 Stable	SOT23-8	DCN	−40°C to +85°C	A8	OPA2338EA/250	Tape and Reel, 250
						OPA2338EA/3K	Tape and Reel, 3000
		SO-8 Surface-Mount	D		OPA2338UA	OPA2338UA	Rails
						OPA2338UA/2K5	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V

Boldface limits apply over the specified temperature range, **−40°C to +85°C**, V_S = 5V.

At T_A = +25°C and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA337, OPA2337, OPA338, OPA2338 MIN	TYP(1)	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}			±0.5	±3	mV
T_A = −40°C to +85°C					**±3.5**	mV
vs Temperature	dV_{OS}/dT			±2		μV/°C
vs Power-Supply Rejection Ratio	PSRR	V_S = 2.7V to 5.5V		25	125	μV/V
T_A = −40°C to +85°C		**V_S = 2.7V to 5.5V**			**125**	μV/V
Channel Separation (dual versions)		dc		0.3		μV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±0.2	±10	pA
T_A = −40°C to +85°C				See Typical Curve		
Input Offset Current	I_{OS}			±0.2	±10	pA
NOISE						
Input Voltage Noise, f = 0.1Hz to 10Hz				6		μV_{PP}
Input Voltage Noise Density, f = 1kHz	e_n			26		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			0.6		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	**T_A = −40°C to +85°C**	**−0.2**		**(V+) − 1.2**	V
Common-Mode Rejection Ratio	CMRR	−0.2V < V_{CM} < (V+) − 1.2V	74	90		dB
T_A = −40°C to +85°C		**−0.2V < V_{CM} < (V+) − 1.2V**	**74**			dB
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 4		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 25kΩ, 125mV < V_O < (V+) − 125mV	100	120		dB
T_A = −40°C to +85°C		**R_L = 25kΩ, 125mV < V_O < (V+) − 125mV**	**100**			dB
		R_L = 5kΩ, 500mV < V_O < (V+) − 500mV	100	114		dB
T_A = −40°C to +85°C		**R_L = 5kΩ, 500mV < V_O < (V+) − 500mV**	**100**			dB
OPA337 FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	V_S = 5V, G = 1		3		MHz
Slew Rate	SR	V_S = 5V, G = 1		1.2		V/μs
Settling TIme: 0.1%		V_S = 5V, 2V Step, C_L = 100pF, G = 1		2		μs
0.01%		V_S = 5V, 2V Step, C_L = 100pF, G = 1		2.5		μs
Overload Recovery Time		V_{IN} × G = V_S		2		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, V_O = $3V_{PP}$, G = 1, f = 1kHz		0.001		%
OPA338 FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	V_S = 5V, G = 5		12.5		MHz
Slew Rate	SR	V_S = 5V, G = 5		4.6		V/μs
Settling TIme: 0.1%		V_S = 5V, 2V Step, C_L = 100pF, G = 5		1.4		μs
0.01%		V_S = 5V, 2V Step, C_L = 100pF, G = 5		1.9		μs
Overload Recovery Time		V_{IN} × G = V_S		0.5		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 5V, V_O = $3V_{PP}$, G = 5, f = 1kHz		0.0035		%

(1) V_S = 5V.
(2) Output voltage swings are measured between the output and negative and positive power-supply rails.

ELECTRICAL CHARACTERISTICS: V_S = 2.7V to 5.5V (continued)

Boldface limits apply over the specified temperature range, **−40°C to +85°C**, V_S = 5V.

At T_A = +25°C and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

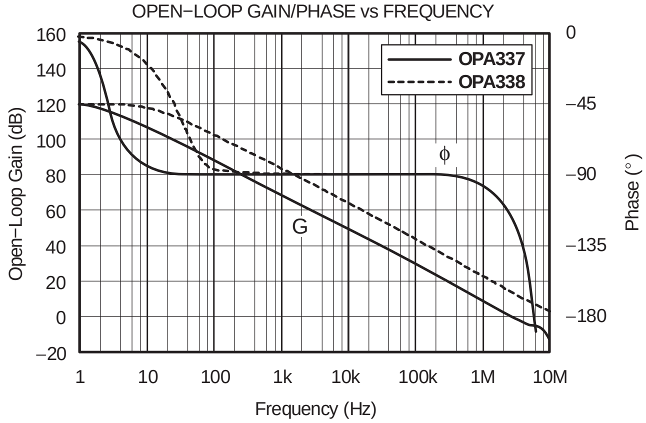
PARAMETER		CONDITION	OPA337, OPA2337, OPA338, OPA2338 MIN	TYP(1)	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail(2)		R_L = 25kΩ, A_{OL} ≥ 100dB		40	125	mV
T_A = −40°C to +85°C		**R_L = 25kΩ, A_{OL} ≥ 100dB**			**125**	mV
		R_L = 5kΩ, A_{OL} ≥ 100dB		150	500	mV
T_A = −40°C to +85°C		**R_L = 5kΩ, A_{OL} ≥ 100dB**			**500**	mV
Short-Circuit Current				±9		mA
Capacitive Load Drive				See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S	**T_A = −40°C to +85°C**	**2.7**		**5.5**	V
Minimum Operating Voltage				2.5		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		0.525	1	mA
T_A = −40°C to +85°C		**I_O = 0**			**1.2**	mA
TEMPERATURE RANGE						
Specified Range			−40		+85	°C
Operating Range			−55		+125	°C
Storage Range			−55		+125	°C
Thermal Resistance	θ_{JA}					
SOT23-5 Surface-Mount				200		°C/W
SOT23-8 Surface-Mount				200		°C/W
MSOP-8				150		°C/W
SO-8 Surface-Mount				150		°C/W
DIP-8				100		°C/W

(1) V_S = 5V.
(2) Output voltage swings are measured between the output and negative and positive power-supply rails.

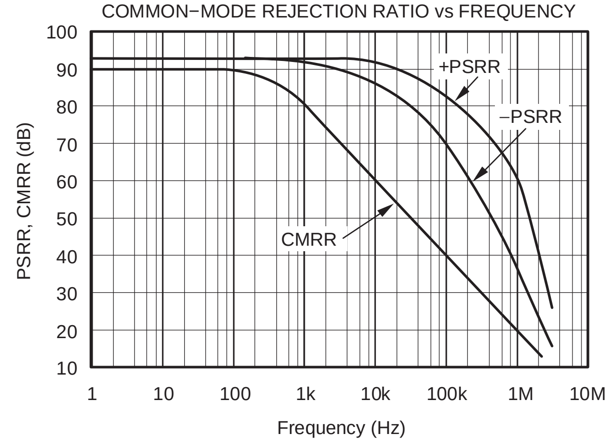
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

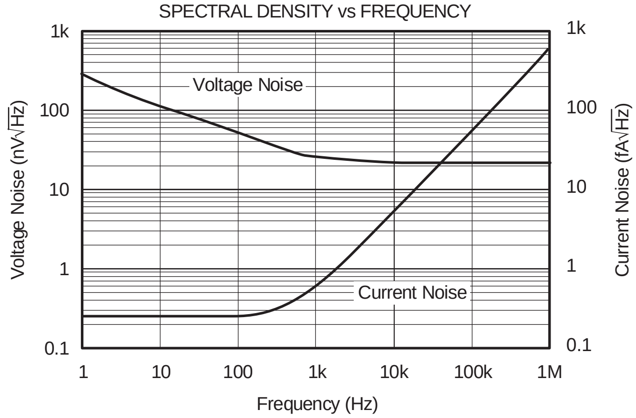
OPEN−LOOP GAIN/PHASE vs FREQUENCY



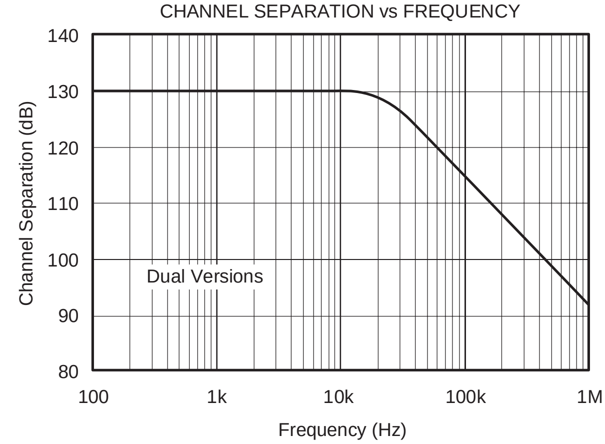
POWER−SUPPLY REJECTION RATIO AND COMMON−MODE REJECTION RATIO vs FREQUENCY



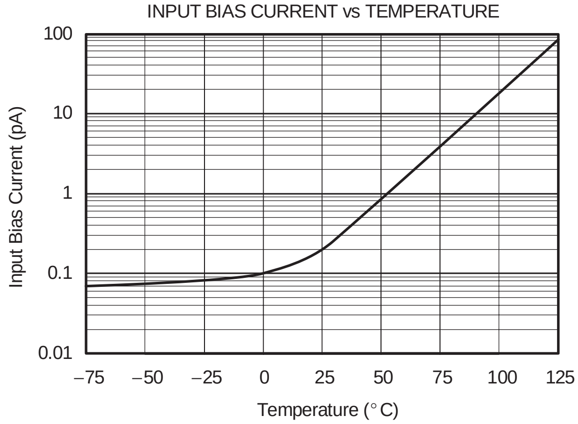
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



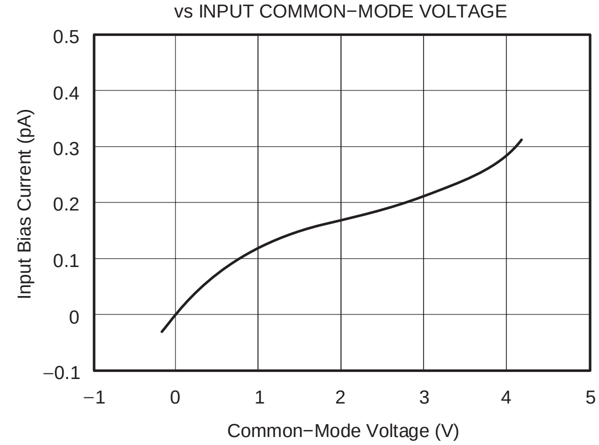
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS CURRENT vs TEMPERATURE



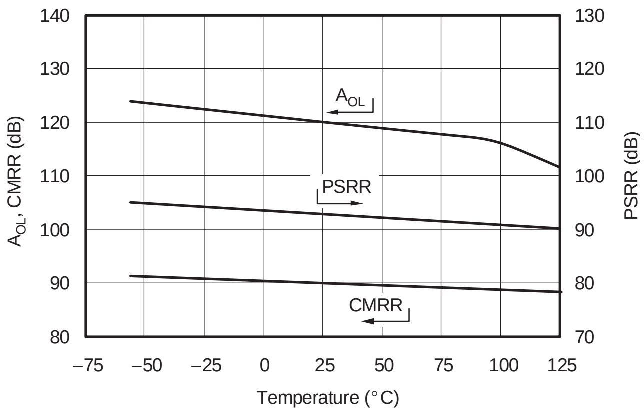
INPUT BIAS CURRENT vs INPUT COMMON−MODE VOLTAGE



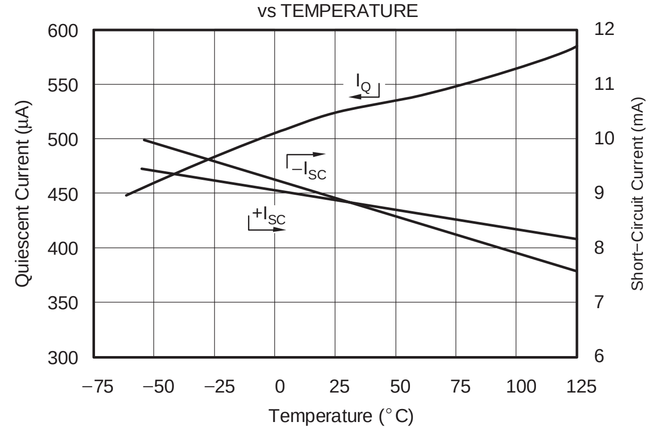
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

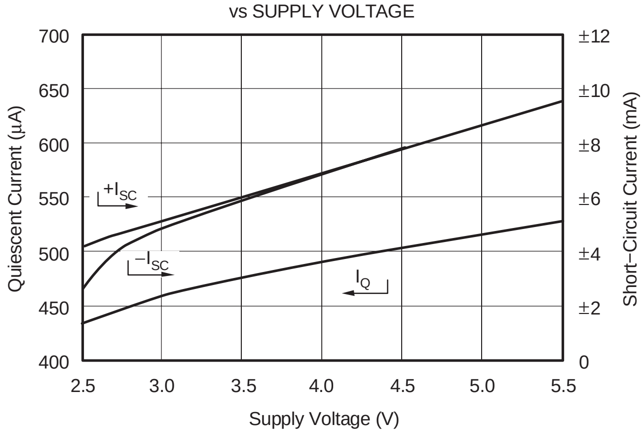
A_{OL}, CMRR, PSRR vs TEMPERATURE



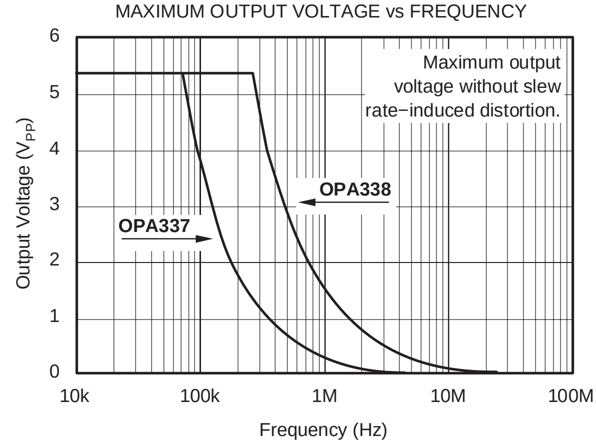
QUIESCENT CURRENT AND SHORT−CIRCUIT CURRENT vs TEMPERATURE



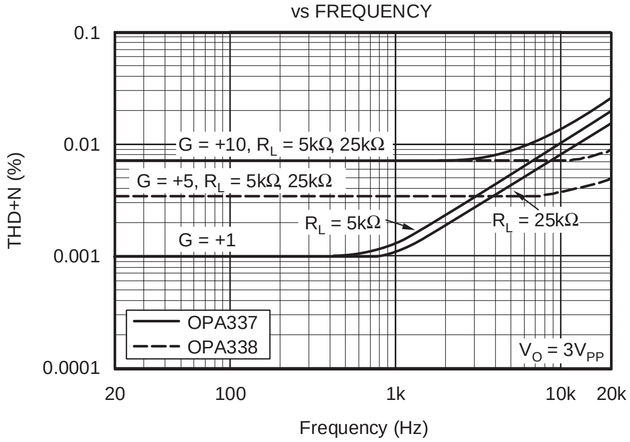
QUIESCENT AND SHORT−CIRCUIT CURRENT vs SUPPLY VOLTAGE



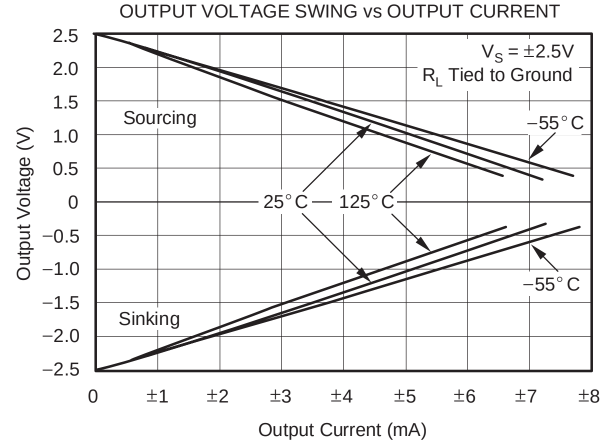
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



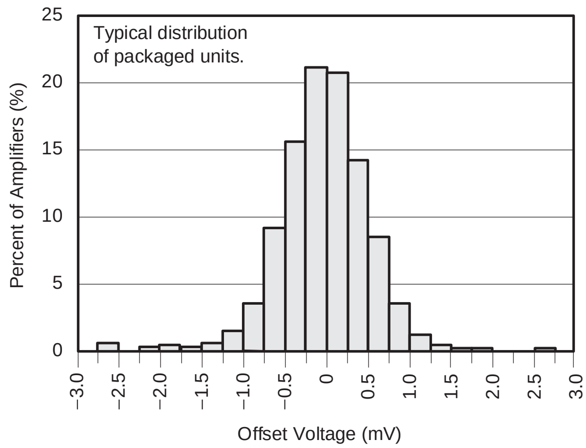
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



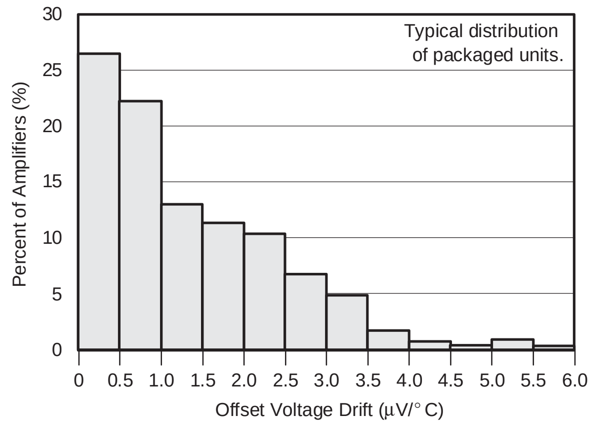
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5V, and R_L = 25kΩ connected to V_S/2, unless otherwise noted.

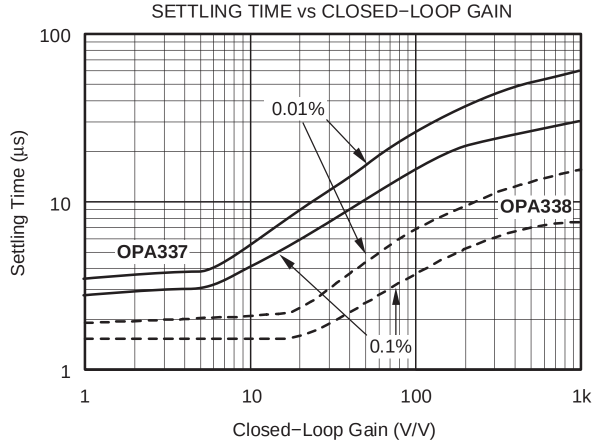
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



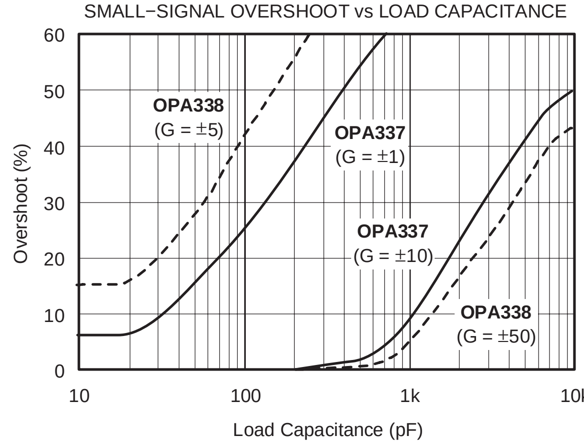
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



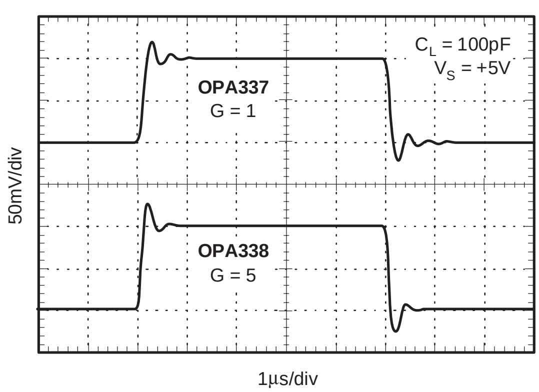
SETTLING TIME vs CLOSED−LOOP GAIN



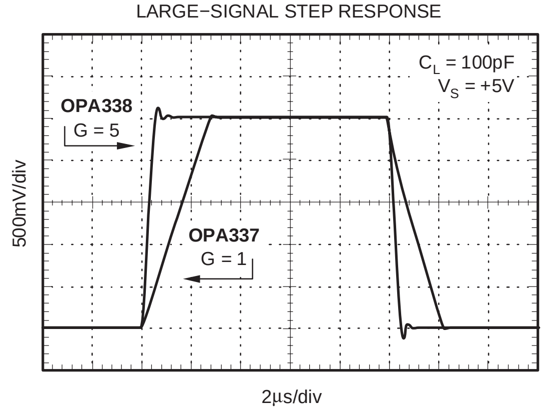
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



SMALL−SIGNAL STEP RESPONSE



LARGE−SIGNAL STEP RESPONSE



APPLICATIONS INFORMATION

The OPA337 and OPA338 series are fabricated on a state-of-the-art CMOS process. The OPA337 series is unity-gain stable. The OPA338 series is optimized for gains greater than or equal to 5. Both are suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA337 series and OPA338 series can operate from a +2.5V to +5.5V single supply with excellent performance. Unlike most op amps which are specified at only one supply voltage, these op amps are specified for real-world applications; a single limit applies throughout the +2.7V to +5.5V supply range. This allows a designer to have the same assured performance at any supply voltage within the specified voltage range. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristic curves.

INPUT VOLTAGE

The input common-mode range extends from (V−) − 0.2V to (V+) − 1.2V. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than maximum input voltage, while not valid, will not cause any damage to the op amp. Furthermore, if input current is limited the inputs may go beyond the power supplies without phase inversion (as shown in Figure 1) unlike some other op amps.

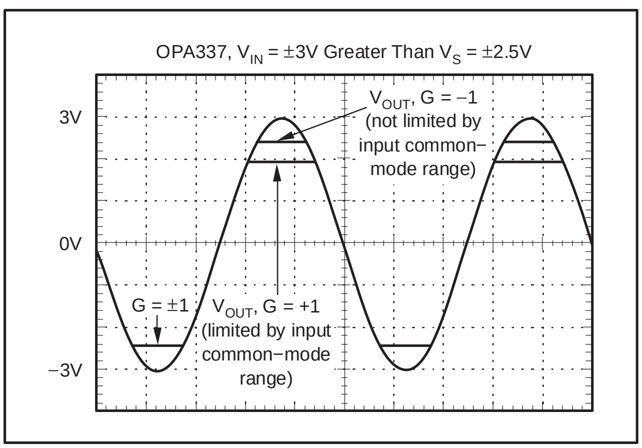


Figure 1. OPA337—No Phase Inversion with Inputs Greater than the Power-Supply Voltage

Normally, input currents are 0.2pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input resistor as shown in Figure 2.

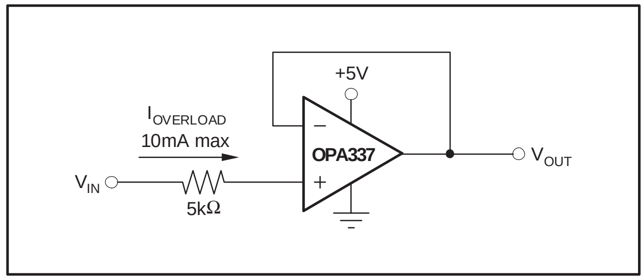


Figure 2. Input Current Protection for Voltages Exceeding the Supply Voltage

USING THE OPA338 IN LOW GAINS

The OPA338 series is optimized for gains greater than or equal to 5. It has significantly wider bandwidth (12.5MHz) and faster slew rate (4.6V/µs) when compared to the OPA337 series. The OPA338 series can be used in lower gain configurations at low frequencies while maintaining its high slew rate with the proper compensation.

Figure 3 shows the OPA338 in a unity-gain buffer configuration. At dc, the compensation capacitor C_1 is effectively *open* resulting in 100% feedback (closed-loop gain = 1). As frequency increases, C_1 becomes lower impedance and closed-loop gain increases, eventually becoming $1 + R_2/R_1$ (in this case 5, which is equal to the minimum gain required for stability).

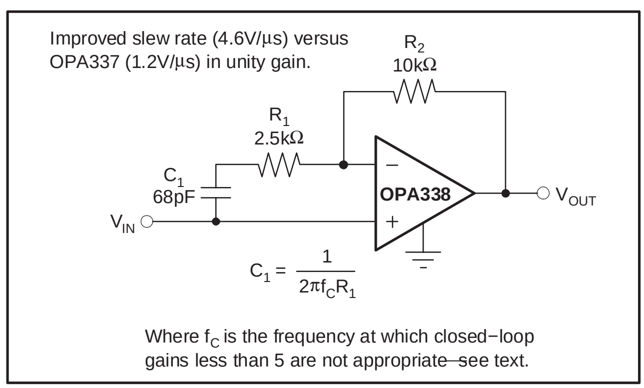


Figure 3. Compensation of the OPA338 for Unity-Gain Buffer

The required compensation capacitor value can be determined from the following equation:

$$C_1 = 1/(2\pi f_C R_1)$$

Since f_C may shift with process variations, it is recommended that a value less than f_C be used for determining C_1. With f_C = 1MHz and R_1 = 2.5kΩ, the compensation capacitor is about 68pF.

The selection of the compensation capacitor C_1 is important. A proper value ensures that the closed-loop circuit gain is greater than or equal to 5 at high frequencies. Referring to the *Open-Loop Gain vs Frequency* plot in the Typical Characteristics section, the OPA338 gain line (dashed in the curve) has a constant slope (−20dB/decade) up to approximately 3MHz. This frequency is referred to as f_C. Beyond f_C the slope of the curve increases, suggesting that closed-loop gains less than 5 are not appropriate.

Figure 4 shows a compensation technique using an inverting configuration. The low-frequency gain is set by the resistor ratio while the high-frequency gain is set by the capacitor ratio. As with the noninverting circuit, for frequencies above f_C the gain must be greater than the recommended minimum stable gain for the op amp.

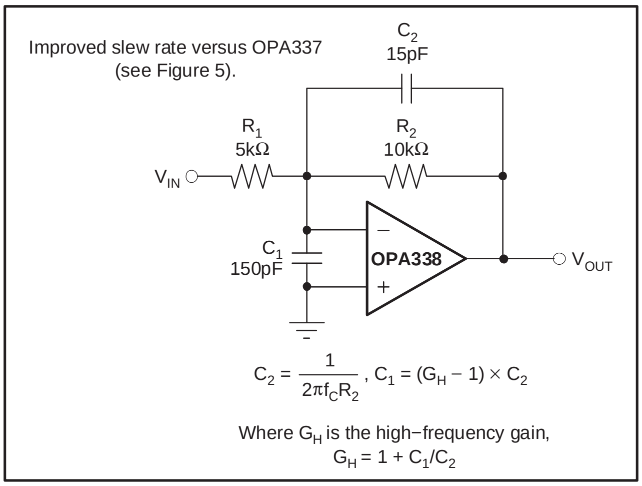


Figure 4. Inverting Compensation Circuit of the OPA338 for Low Gain

Resistors R_1 and R_2 are chosen to set the desired dc signal gain. Then the value for C_2 is determined as follows:

$$C_2 = 1/(2\pi f_C R_2)$$

C_1 is determined from the desired high-frequency gain (G_H):

$$C_1 = (G_H - 1) \times C_2$$

For a desired dc gain of 2 and high-frequency gain of 10, the following resistor and capacitor values result:

R_1 = 10kΩ C_1 = 150pF

R_2 = 5kΩ C_2 = 15pF

The capacitor values shown are the nearest standard values. Capacitor values may need to be adjusted slightly to optimize performance. For more detailed information, consult the section on *Low Gain Compensation* in the OPA846 data sheet (SBOS250) located at www.ti.com.

Figure 5 shows the large-signal transient response using the circuit given in Figure 4. As shown, the OPA338 is stable in low gain applications and provides improved slew rate performance when compared to the OPA337.

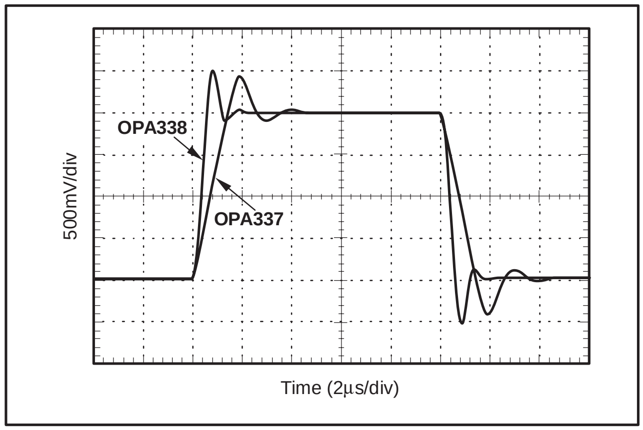


Figure 5. G = 2, Slew-Rate Comparison of the OPA338 and the OPA337

TYPICAL APPLICATION

See Figure 6 for the OPA2337 in a typical application. The ADS7822 is a 12-bit, micropower, sampling analog-to-digital converter available in the tiny MSOP-8 package. As with the OPA2337, it operates with a supply voltage as low as +2.7V. When used with the miniature SOT23-8 package of the OPA2337, the circuit is ideal for space-limited and low-power applications. In addition, the OPA2337's high input impedance allows large value resistors to be used which results in small physical capacitors, further reducing circuit size. For further information, consult the ADS7822 data sheet (SBAS062) located at www.ti.com.

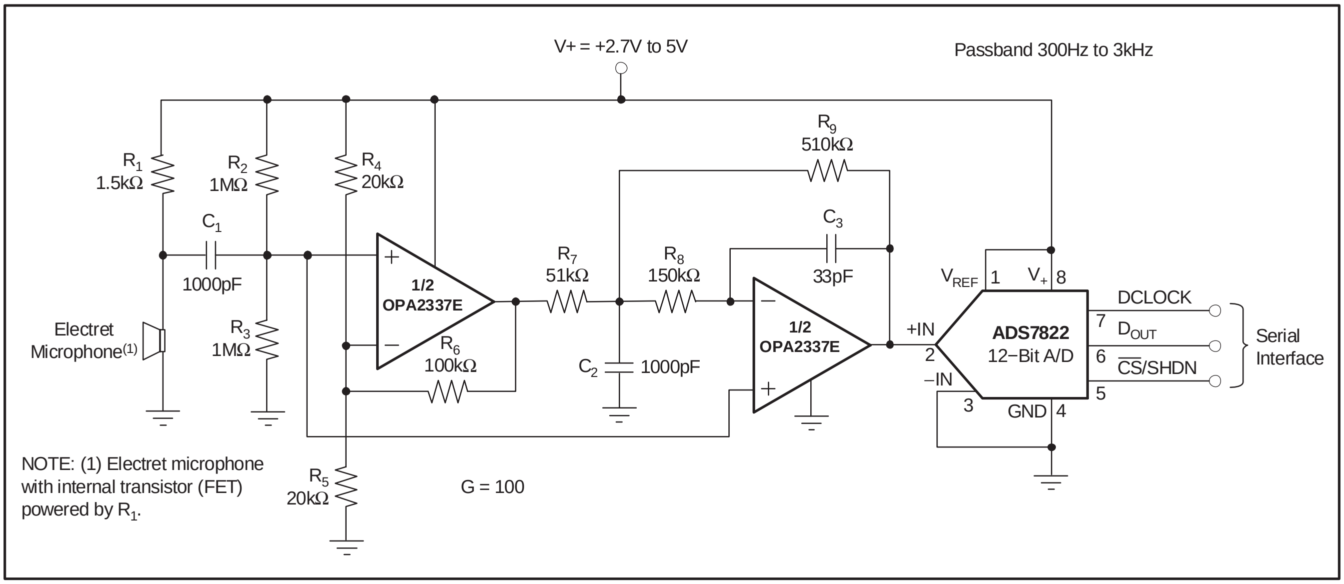


Figure 6. Low-Power, Single-Supply, Speech Bandpass Filtered Data Acquisition System

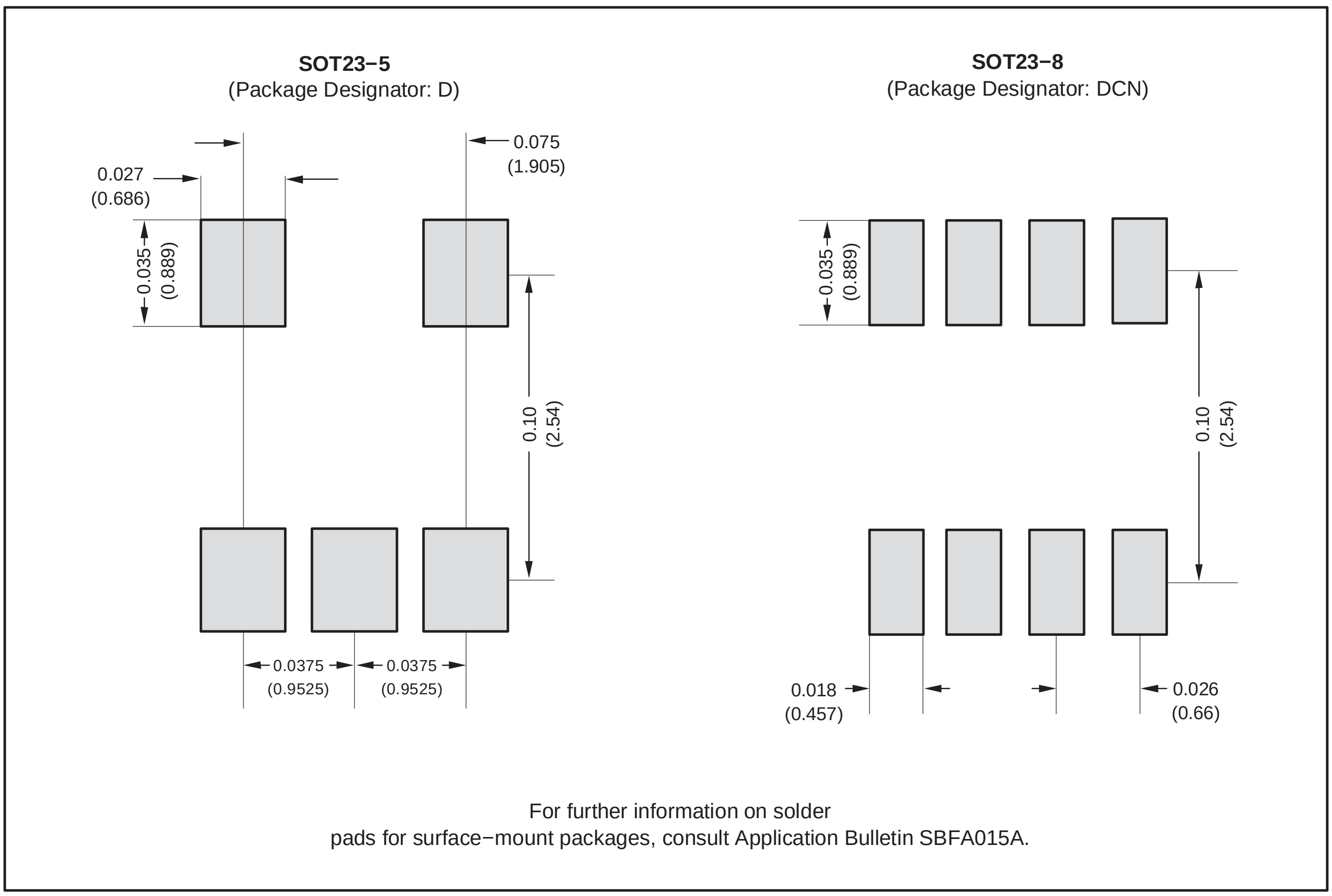
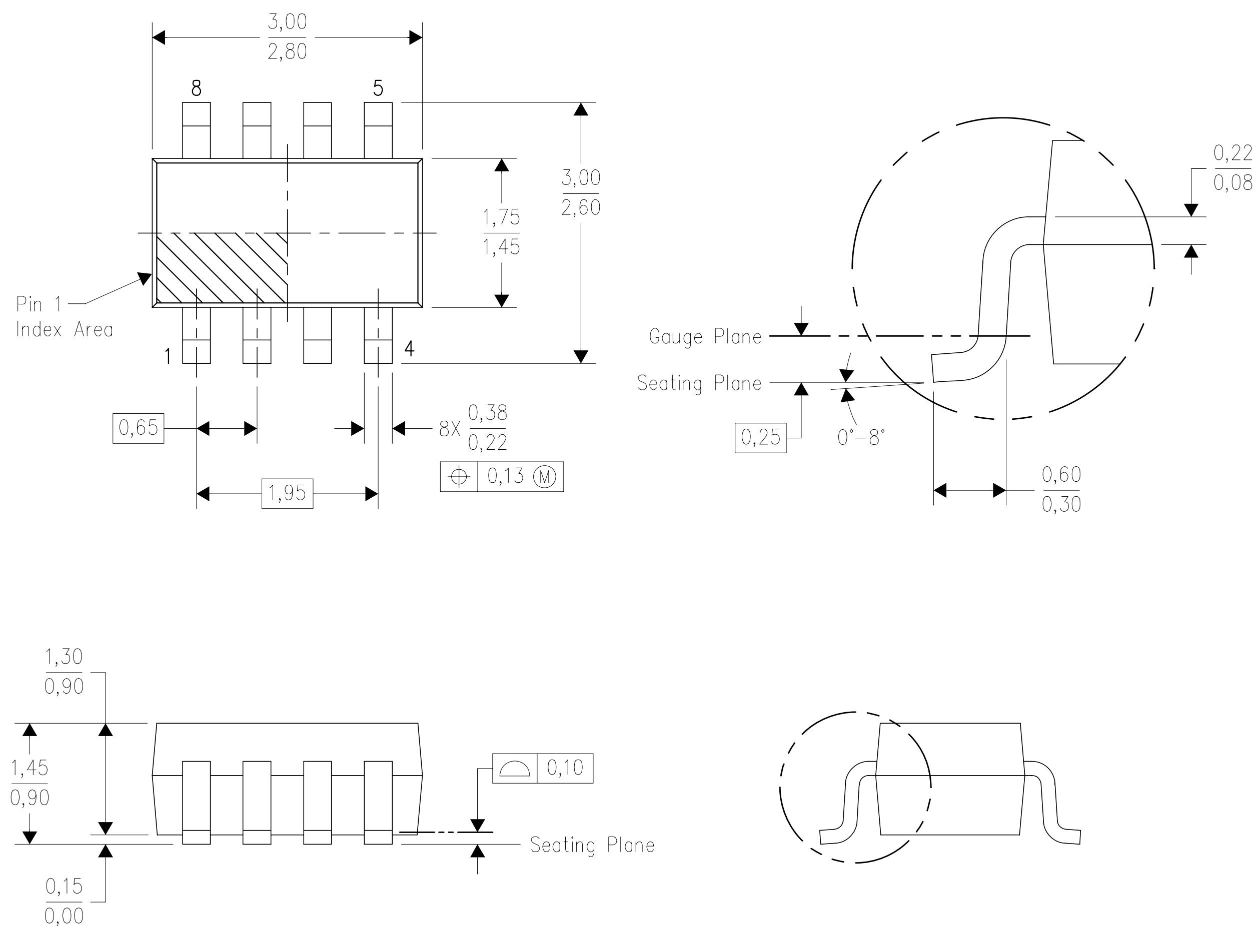


Figure 7. Recommended SOT23-5 and SOT23-8 Solder Footprints

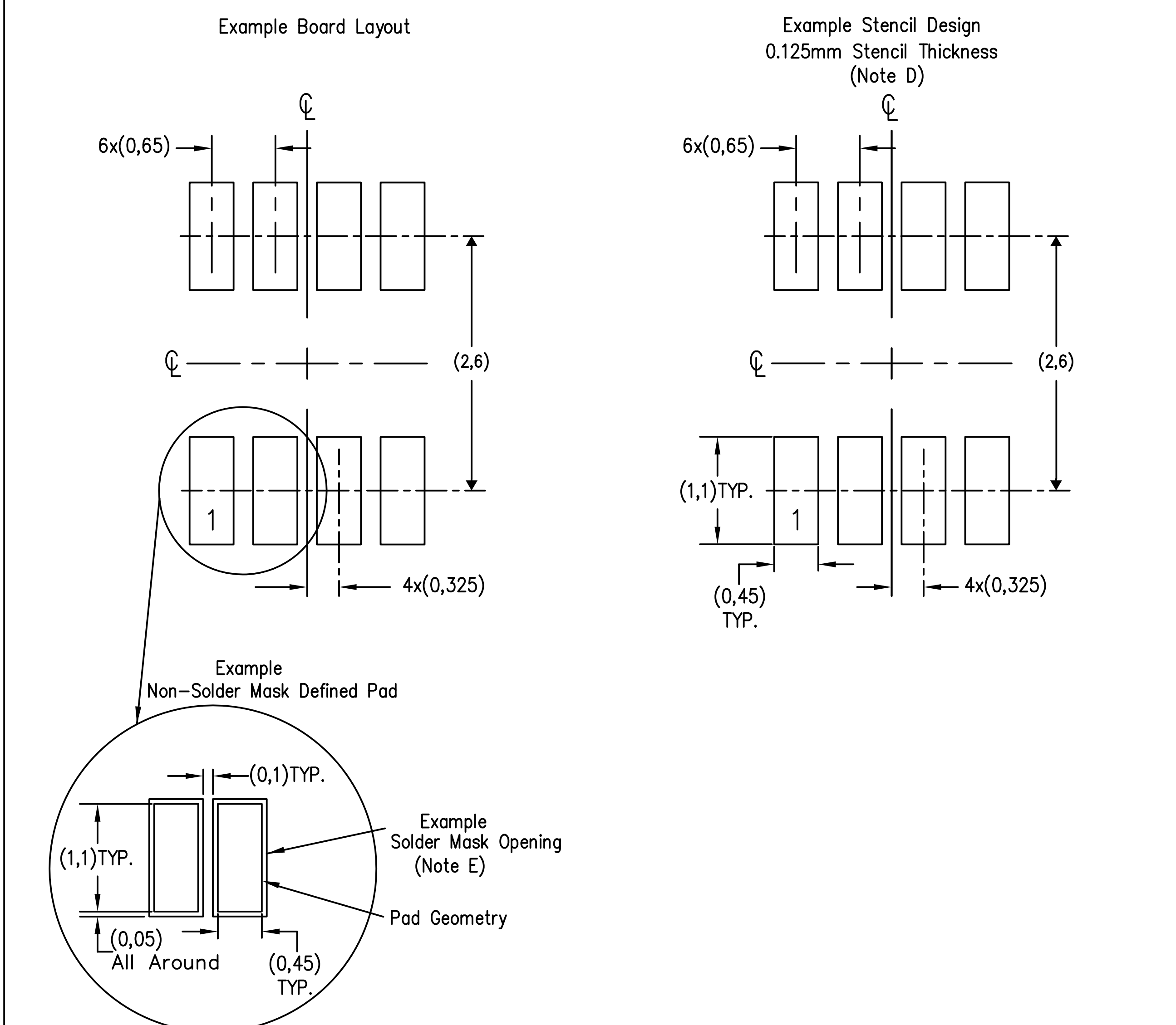
DCN (R–PDSO–G8)   PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4202106/D 11/2009

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

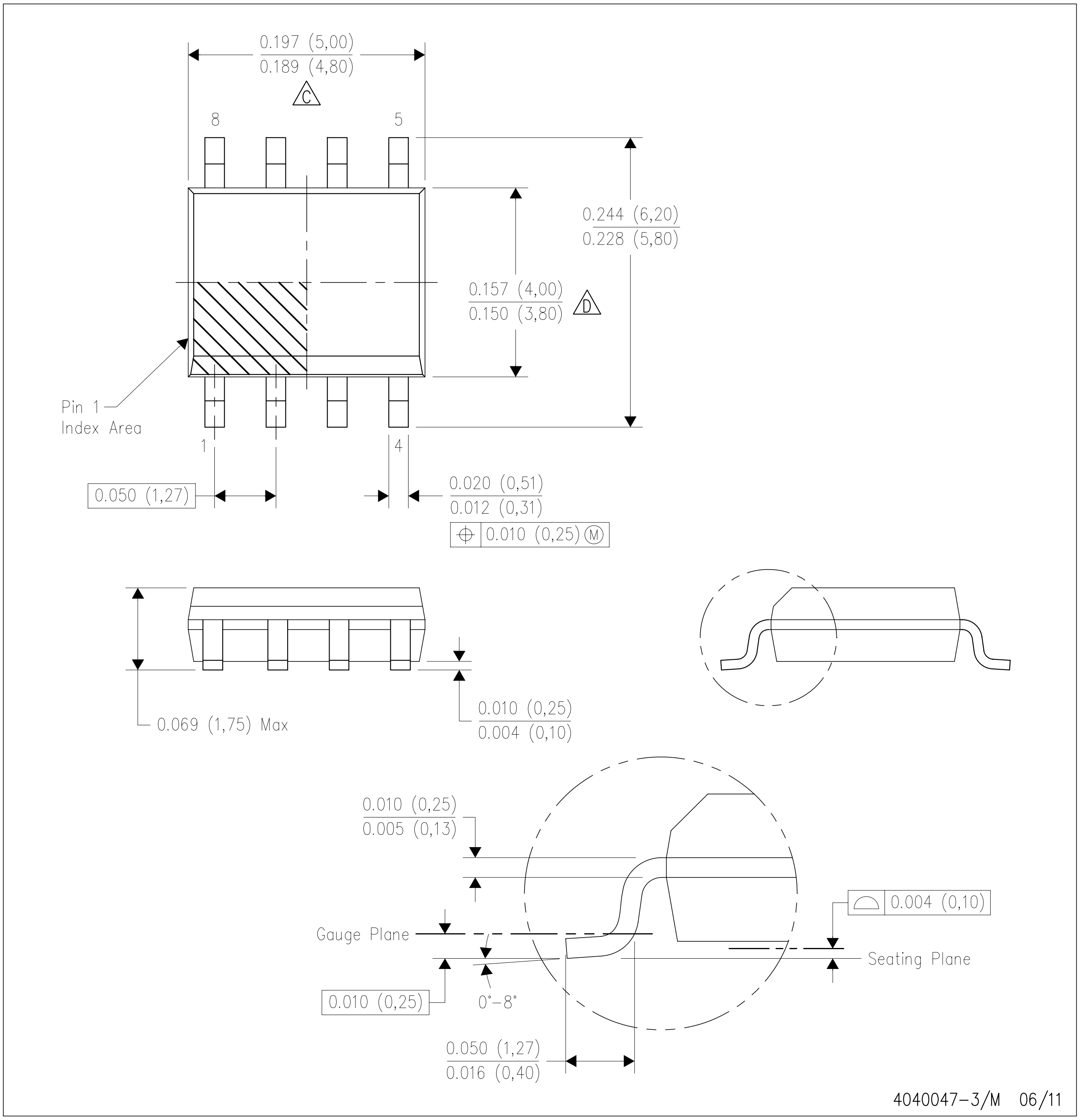
DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4211034/C 07/13

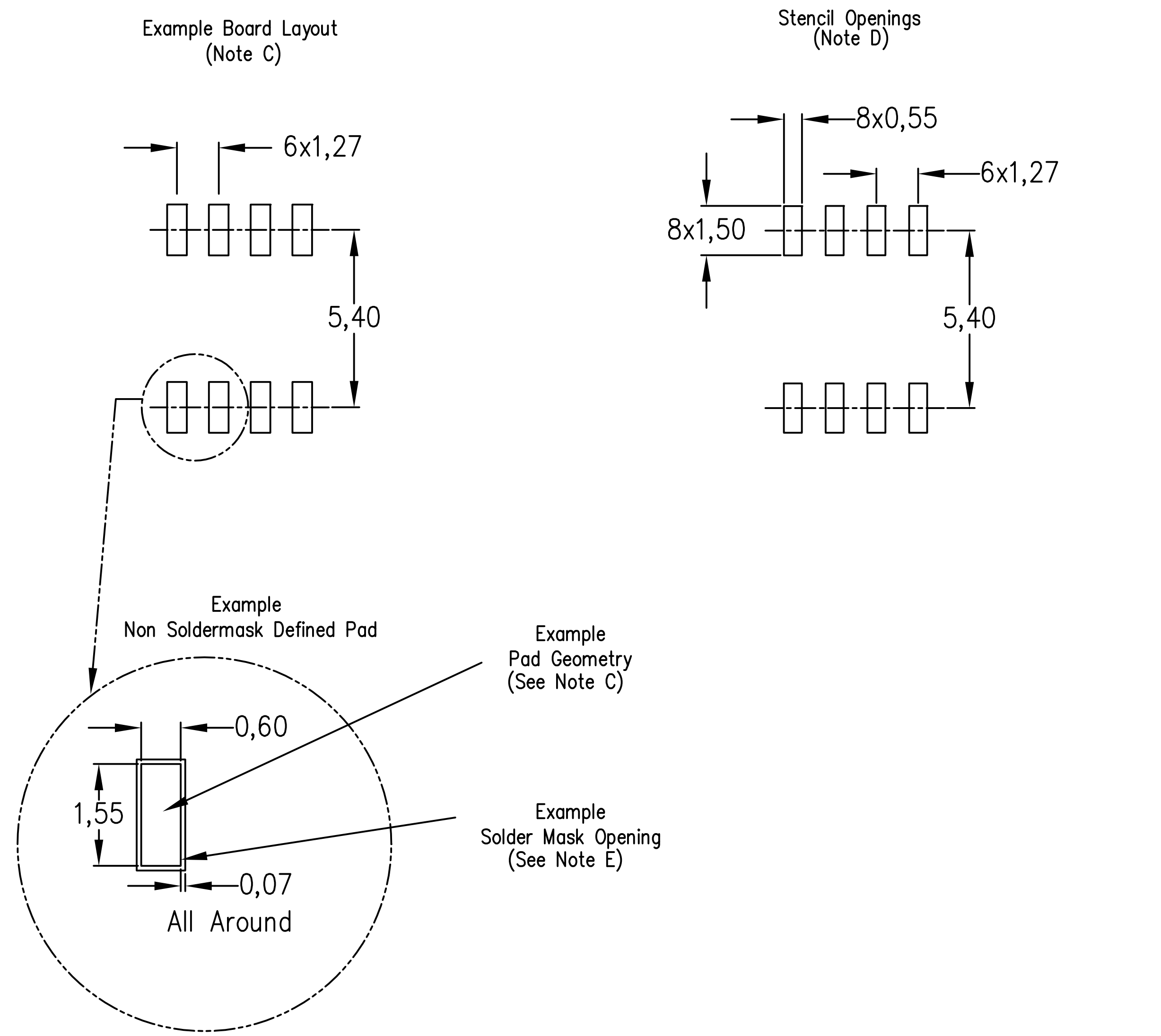
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

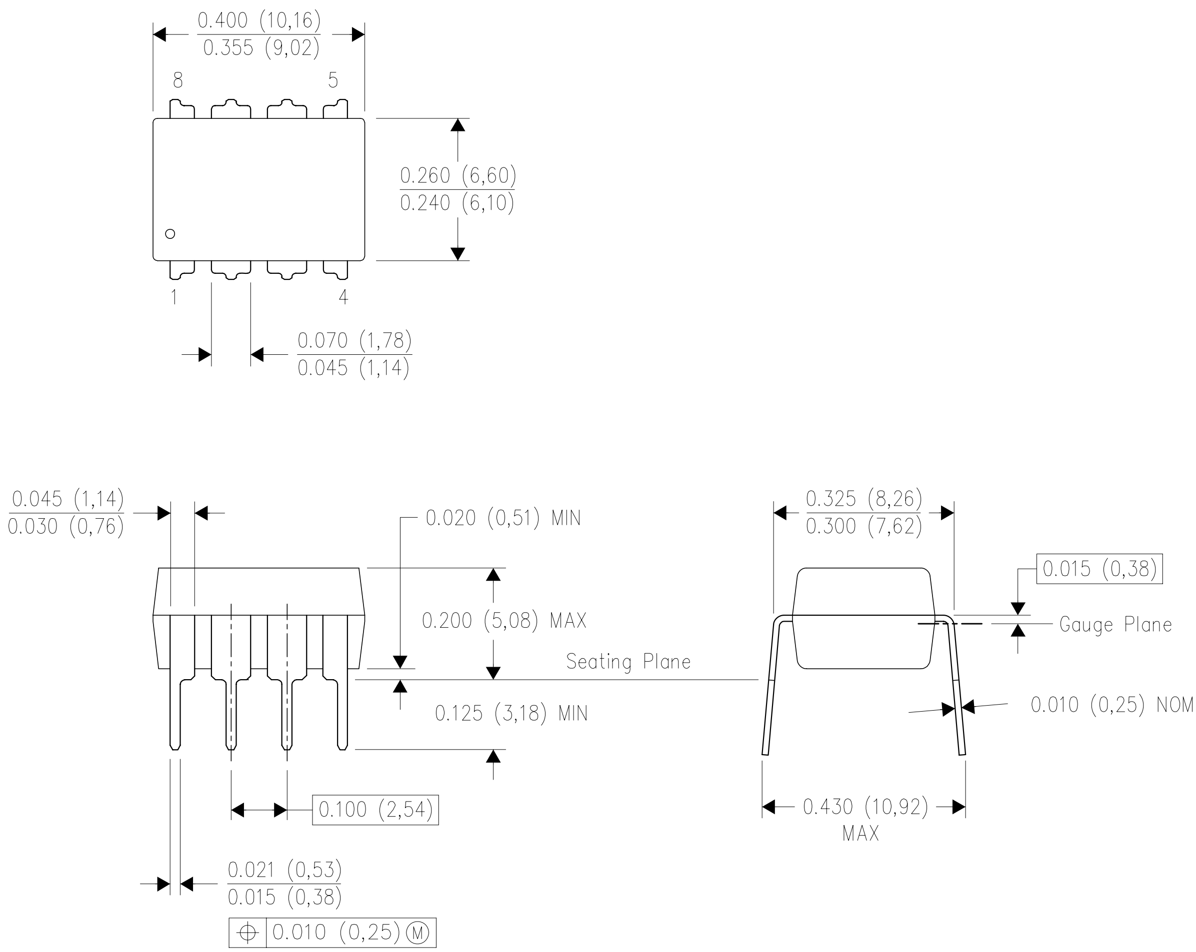
D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

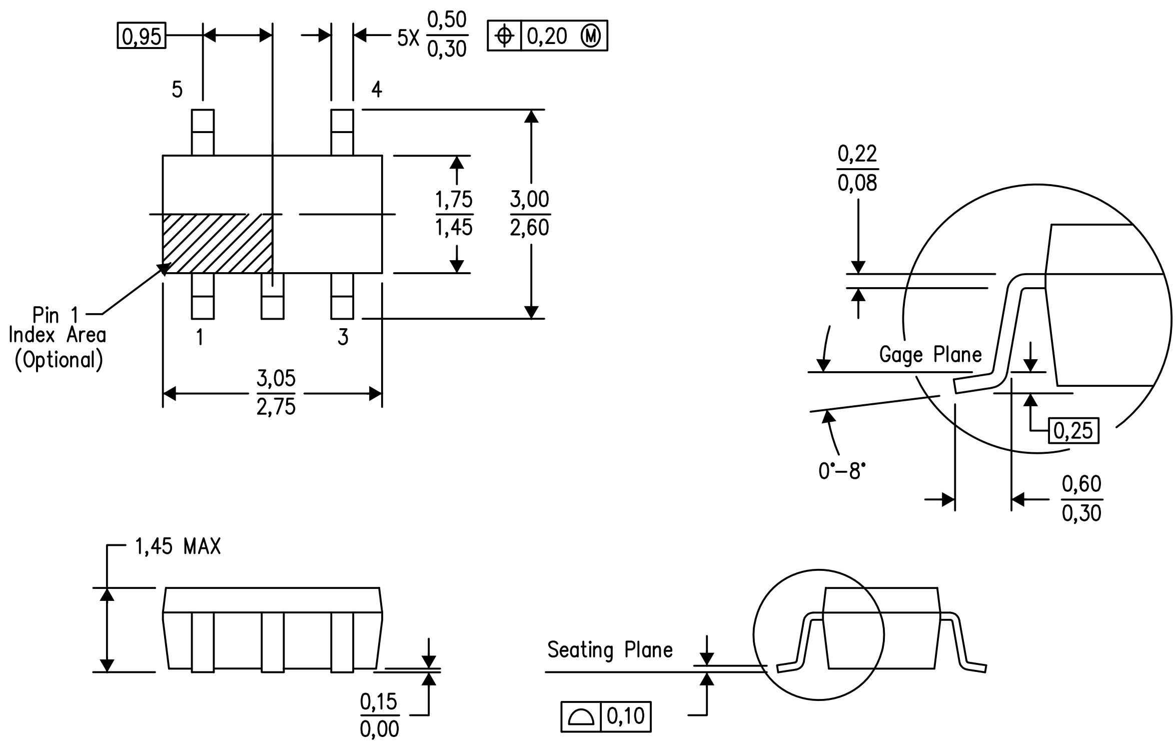
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

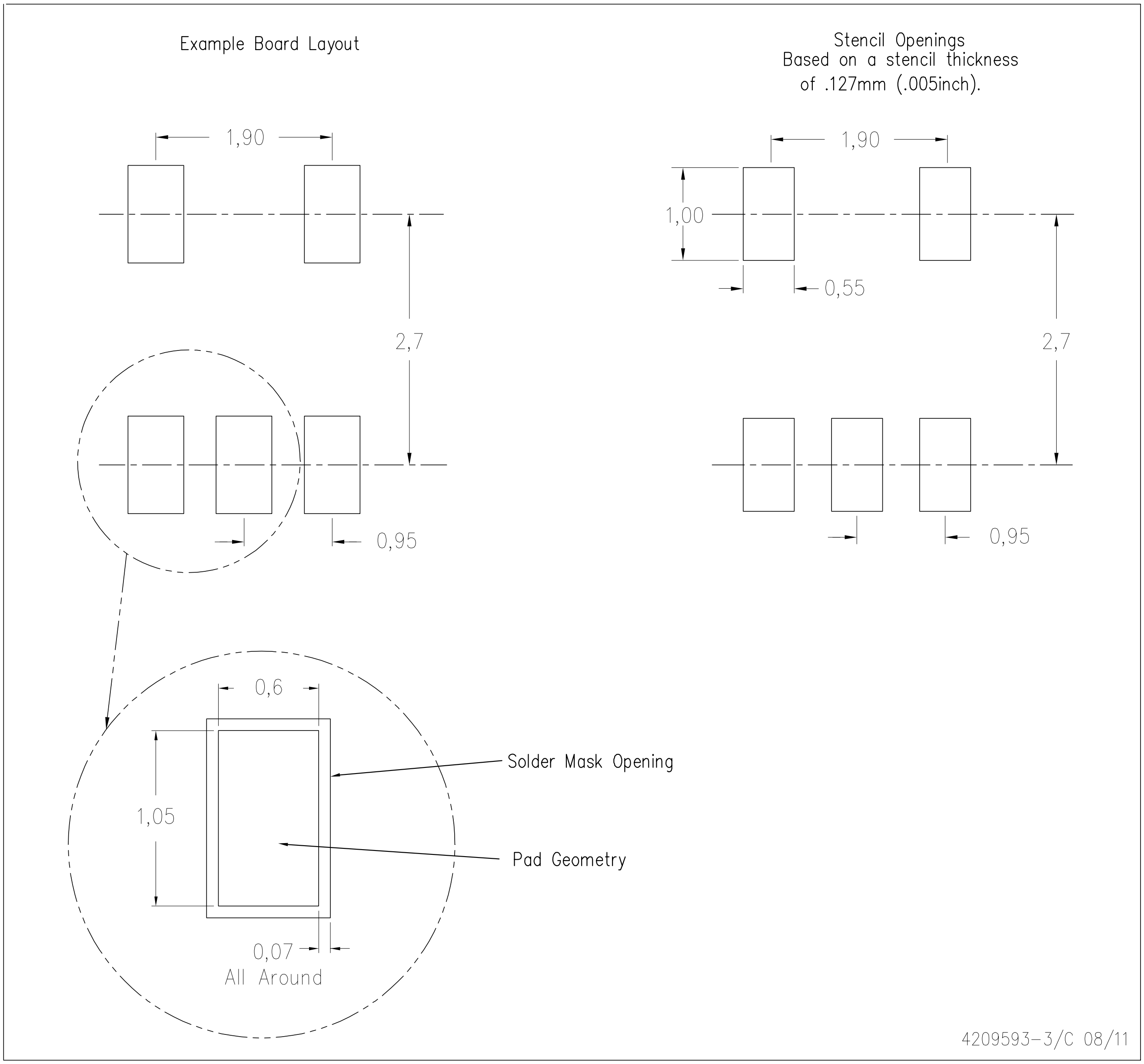
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

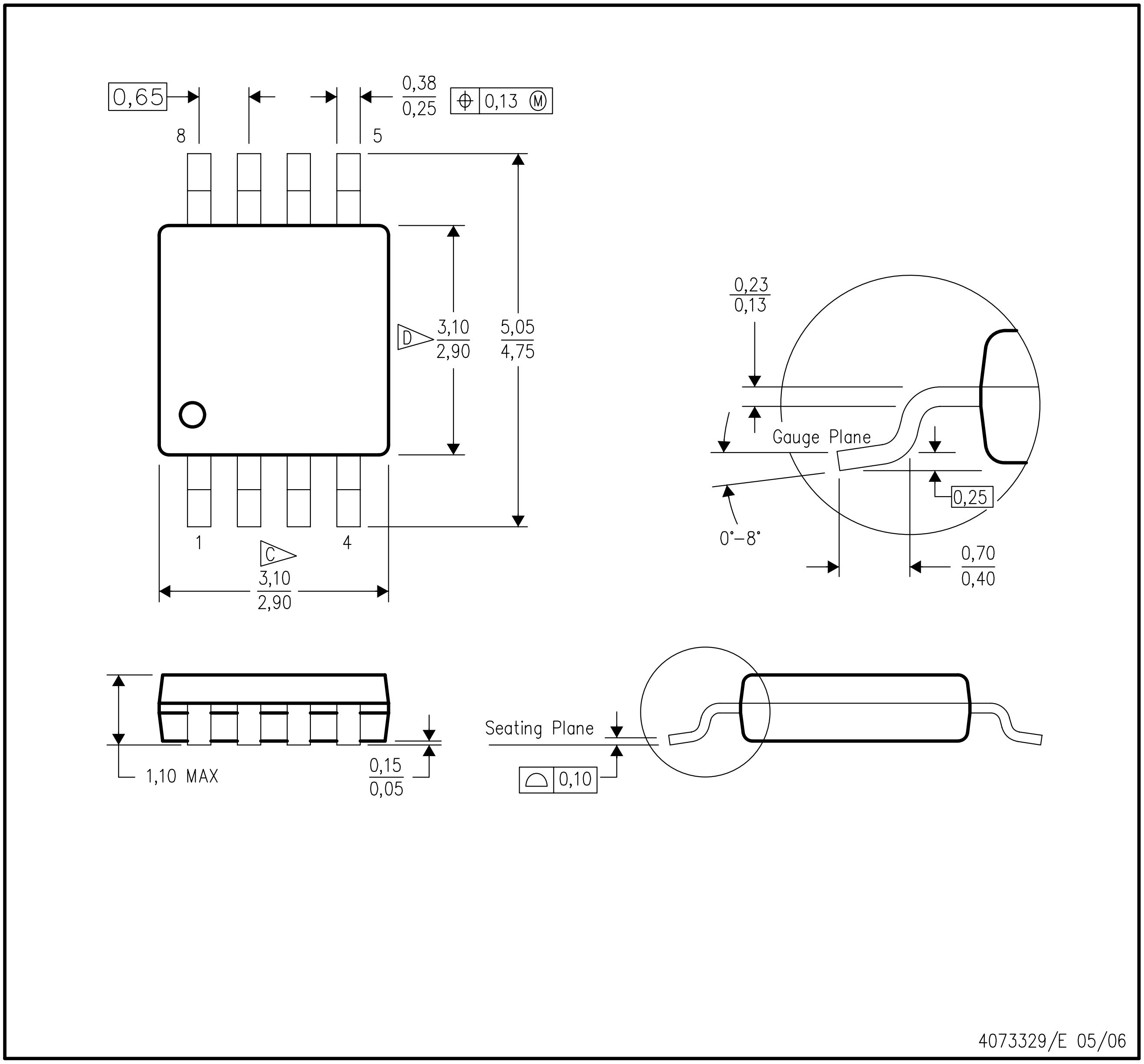
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



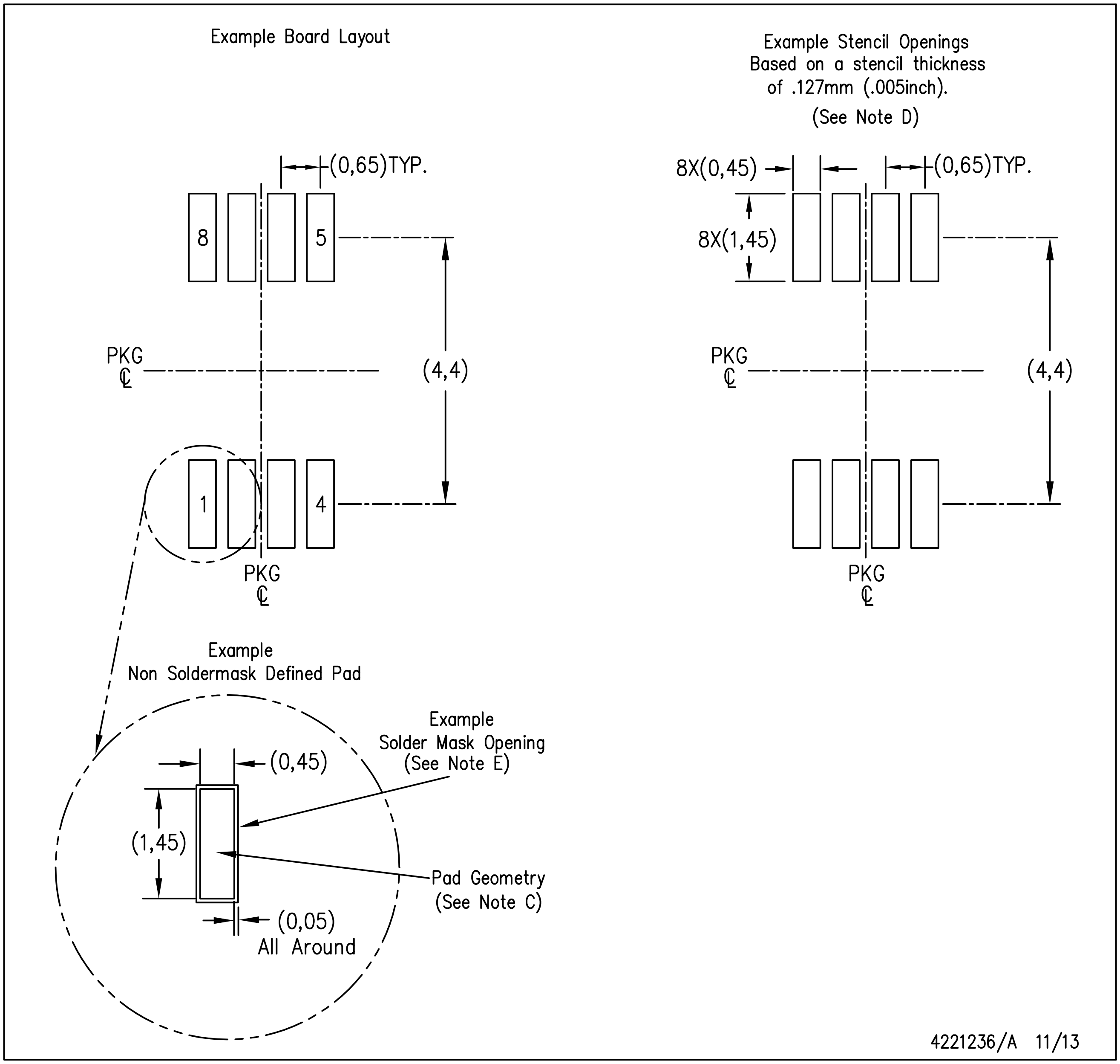
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.