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1 Preliminary Remarks

This paragraph gives an overview on the *HiRel* Discrete and Microwave Semiconductors available from Siemens. For detailed descriptions, screening procedures and quality specifications as well as full data sheets, please refer to our "*HiRel* Discrete and Microwave Semiconductors Data Book", which is currently in production (October 1996).

HiRel components are mainly provided for highly professional applications such as radio links, military applications, sea cables, naval, air and space-borne systems. The philosophy concentrates on devices with maximum reliability, assembled in hermetically sealed packages. Screening procedures and quality assurance tests play a major role in procurement procedures. Ordered quantities are very often for a single project or application only and thus comparatively low.

2 Introduction to *HiRel* and Space Qualified Devices

2.1 General

Siemens Small Signal Semiconductors is an important supplier of discrete semiconductor devices for the microwave community. The device families include silicon and GaAs electronic devices. The silicon components available include microwave diodes (PIN and Schottky) and bipolar transistors. The GaAs components that are available on a commercial basis include low noise HEMTs and low noise and power MESFETs and corresponding monolithic microwave integrated circuits (MMICs).

Unlike high volume markets where low cost plastic packages are used, the semiconductor dies are assembled in hermetically sealed packages to produce *HiRel* standard products for professional applications. It should be stressed, however, that even these *HiRel* components take full advantage of the mass production of wafers for the consumer and commercial markets. The wafers are selected from the best controlled volume production and have to pass special additional acceptance tests. For dedicated customers, bare dies made from these specially approved and reserved wafers are also available.

Based on their proven reliability, the components described herein are best suited for use in high reliability projects, e.g., for space applications. The following sections on silicon and GaAs devices report our experience with *HiRel* parts and outline the range of components actually available in space quality (ESA/SCC qualified) from the Siemens Discrete and RF Semiconductors Group. Both wafer fabs and the *HiRel* assembly line are ISO9001 qualified.

2.2 Silicon Devices

Siemens has a long history of manufacturing highly reliable, discrete semiconductor devices. Fundamental engineering work on a 1st generation of Si bipolar transistors was carried out already in the sixties and early seventies. On the basis of extensive and numerous reliability investigations, ESA/SCC qualification status was granted to some Si component families, namely, the PIN-diodes BXY 42, 43 and 44 and Schottky diodes BAS 70, BAS 40, BAT 14 (medium barrier) and BAT 15 (low barrier). Our 3rd generation microwave bipolar transistors, chief among them, the BFY193, recently passed the demanding ESA evaluation and qualification programmes and received full ESA qualification (June 1996). The new SIEGET microwave transistors, which make up our 4th generation headed by the BFY 450, passed the evaluation; the qualification programme is running on schedule. Si devices have been used in numerous space projects.

The silicon wafer production operation and the *HiRel* assembly line are approved according to Generic Specifications CECC 20 000/CECC 50 000, which also covers EN 29 001 (ISO 9001).

Numerous audits have been performed by high rel customers and organisations. The last audit in this respect was performed by the German and European space agencies, DARA and ESA, respectively, within the frameworkof the BFY 193/BFY 450 space evaluation programme in May, 1995.

2.3 GaAs Devices

Siemens has a background of more than 45 years in compound semiconductor research. The activities run the gamut from material growth and technology development to devices and circuits, including monolithic microwave integrated circuits (MMICs) and systems applications of new components.

These GaAs activities are driven by two main objectives.: The first is to have this "high technology" available in-house for current and future enhanced systems. The second is to commercialise GaAs products as a supplement to the Si semiconductor programme. As a result, the company is engaged in the most important application fields, including, in particular, low noise HEMTs and power FET devices for microwave applications, discretes as well as MMICs, and has also ESA/SCC qualified GaAs devices in its delivery programme.

The GaAs wafer production line started up in 1980 with the manufacturing of discrete low noise and general purpose GaAs FETs for the open market. The world's first commercially available GaAs MMICs were released in 1982. A very important milestone was the invention of the Siemens specific, proprietary self-aligned gate process called GaAs DIOM technology. This process exhibits exceptional device uniformity and reliability; it was released in 1984. The first DIOM-MMICs (CGY 40, CGY 31), which satisfy MIL883 quality standards, were marketed already in 1986.

The Semiconductor Group began developing GaAs power devices in 1987 after taking over corresponding responsibilities from MSC, a former Siemens company. Production of corresponding high reliability Phased Array Radar MMICs (LNA, VGA, MPA, HPA) started already in 1992. The same technology is also used for high volume commercial power FETs in low cost plastic packages introduced in 1993. Using similar chips in hermetically sealed packages results in high rel devices for the professional market, proven through the ESA/SCC evaluation programme successfully completed in 1995.

An important milestone with regard to low noise devices was the introduction of a self aligned HEMT process. GaAs LN-HEMT marketing started in 1989. A Space Evaluation and Qualification Programme to ESA/SCC specifications was completed on the HEMT types CFY66 and CFY67 under DARA and ESA contracts in 1994, with the Siemens HEMTs becoming the first ever space qualified HEMTs. First flight parts have been delivered to the Artemis project, and the naked dies are chosen as the base line for the LNA of the ASAR/Envisat project.

In 1989 the GaAs Wafer Fab Line achieved a formal quality release to internal standards. Meanwhile, the GaAs wafer production and assembling lines have also achieved certification according to CECC 20 000/CECC 50 000, which also encompasses EN 29 001 (ISO 9001). Within the framework of the ESA/SSC evaluation of the HEMTs CFY66 and CFY67, a line audit was performed by DARA and ESA. The high rel assembly line was audited by the same team in the course of the ESA/SCC qualification of the Si bipolar transistors, see above.

The long and successful history of DIOM Power FETs and MMICs at Siemens on commercial devices and project work shall be explained in more detail. Large volume production of P-FETs and P-MMICs for mobile communication (DECT, GSM, PCN) is based on surface mountable devices in low cost plastic packages and has made Siemens the largest commercial supplier of GaAs devices in Europe. Most of the devices are power MESFETs or MMICs with large gate width structures, and the process maturity is best proved by these figures.

Similar P-FET dies in hermetically sealed packages constitute a power line-up for professional applications up to 5 GHz (CLY29, 32, 35, 38). Based on the mass production of the dies and the huge amount of available corresponding internal reliability data, an ESA/SCC Space Evaluation and Qualification Programme was started under DARA and ESA contracts on the CLY32 as the pilot type. The evaluation was granted in May, 1995, the qualification is running. First flight parts have been delivered to the Spot/ Vegetation project.

Power MMIC developments include activities for an S-band radar project (high power amplifier HPA-MMICs), the C-band COBRA PAR system (among others, driver or medium power amplifier MPA-MMICs and HPA-MMICs), and work on X-band SAR systems (HPA-MMICs). The MPA-MMIC die developed and delivered for a C-band Phased Array Radar has also been selected as the base line for the driver die of the ASAR/Envisat project; the corresponding VGA is under discussion for this challenging

instrument. The results of an X-band HPA with P_{out} = 5.6 W and PAE = 33% are exceptional and recognised world-wide.

Some of the recent developments were embedded in the German government's “Drei-Fünf Elektronik” consortial programme. With regard to power devices, Siemens also participates in the ESPRIT programme “MANPOWER” and in the IEPG group. When it comes tospace applications, Siemens Discrete Semiconductors is a subcontractor in the ESA programme “Evaluation of New Microwave Power Transistors” with P-FETs, development of advanced PowerFETs are covered by a further ESA project “Assessment and Qualification of a Power MESFETs Family”. Project work at Siemens is used as a vehicle to create devices for the commercial and professional market.

3 Quality Specifications of *HiRel* Components

3.1 Overview of available *HiRel* Quality Levels

The quality philosophy behind our production for the commercial market is treated in detail in the corresponding paragraph. Our quality assurance program for our *HiRel* devices relies heavily on this basic quality system. In addition, special measures are taken to ensure the higher quality levels of our *HiRel* products.

First of all, wafers are selected from the normal production runs and are exposed to a specific release procedure. The semiconductor dies are then assembled in hermetically sealed microwave packages and tested. These components are available in four well-defined upgrading quality levels, see also **table 5** for a direct comparison of these levels:

For the **Professional Quality Level** the components pass basic mechanical, thermal and electrical tests and inspections and are fully DC/RF tested. This quality level provides the same electrical performance as the other levels. Equivalent devices may be used for engineering work, for example.

The **High Rel Quality Level** provides extended tests and, in addition, a 100% Burn-In (screening) The testing procedure secures full traceability and is explicitly certified for each delivery lot by the corresponding "Certificate of Compliance" CoC. This level may be used in professional equipment.

The **Space Quality Level** provides further extended tests, partly a Pre Burn-In, a multiple 100% Burn-In screening on serialised devices, and a temperature characterisation. Final electrical measurements are given on a read and record basis. The testing procedure is again explicitly certified for each delivery lot by a CoC. Lot Acceptance Tests to different levels will be performed, if ordered. This level will be used especially in commercial spacecraft systems.

The **ESA Space Quality Level** follows the testing procedures specified in the ESA/SCC Generic Specification 5010 and in the corresponding Detail Specifications. They provide again further extended tests, partly a Pre Burn-In and multiple 100% Burn-In on serialised devices including an individual drift evaluation, a temperature characterisation and final electrical measurements. Full ESA specified data documentation is provided

including all measurements on a read and record base. The testing procedure is again explicitly certified for each delivery lot by a CoC. Lot Acceptance Tests to different levels will be performed, if ordered. This level will be used especially in spacecraft systems supervised by ESA and corresponding agencies.

Table 5
***HiRel* Semiconductors Quality Levels: Test Programmes**

Quality Level	Wafer Release	Mech. Insp.	Read and Record	100% DC/RF[1)]	100% Burn-In[2)]	Burn-In Drift[2)]	Temp. Charact.	LAT	Docum.
Profi	Profi	+	-	+	-	-	-	-	-
High Rel	High Rel	+	-	+	+	-	-	-	CoC
Space	Space	+	+	+	+ multiple	+	+	+	CoC and Final Data
ESA	ESA	+	+	+	+ multiple	+	+	+	CoC and Full Doc.

1) RF for bare dies partly on a sample base only
2) Burn-In may not be possible for bare dies

3.2 Wafer Release

The wafers are processed and inspected, including quality inspections, according to the Process Identification Document P.I.D.. Full documentation of all process steps and inspection is stored. Wafers meant for *HiRel* devices are then selected and exposed to a specific release procedure, including pilot run assembling and endurance testing. The generic wafer process and release flow for *HiRel* devices is showngiven in **Figure 1**. Specific upgrades and limits are used for the different quality levels.

§ 1	**Wafer Process and Inspections acc. P.I.D.**	
	1.1	Wafer Process and Inspections
	1.2	Electrical Measurements 100%
	1.3	Dicing and Visual Inspection
	Diced Wafer	

§ 2	**Review of Process Data**	
	2.1	SPC Analysis
	2.2	PCM Analysis
	2.3	Review of 100% Electrical Measurements
	2.4	Review of Inspections
	Initial Wafer Release	

§ 3	**Wafer Acceptance Test**	
	3.1	SEM Inspection
	3.2	Pilot Run Assembling and Tests
		Die Visual Inspection and Selection
		Die Attach
		Wire Bonding
		Internal Visual Inspection
		Bond Pull/Die Shear Test
		Encapsulation
		Thermal Shock
		Fine Leak and Gross Leak Seal Test
		External Visual Inspection
	3.3	Pilot Run Electrical Characterisation
		Serialisation
		Electrical Measurements at Room Temperature
		Electrical Measurements at High and Low Temperatures
	3.4	Endurance Test (Quality Level "High Rel" and higher)
		High Temperature Bias Endurance Test (min. 1000 h at T_{jmax} or 168 h T_{jmax} + 25 °C)
		Electrical Measurements after Endurance Test
		Parameter Drift Evaluation
		Bond Pull/Die Shear Test
	3.5	Check Periodic Reliability Monitor
	Final Wafer Release	

Figure 5
Generic Wafer Process and Release Flow for *HiRel* Discrete Semiconductors

3.3 *HiRel* Quality Levels

The flow charts for production, inspections and testing of the four standard *HiRel* quality levels are given in **Figures 2 - 5**. As can be seen, the quality levels provide successively higher degrees of testing, screening and documentation, thus providing the increased reliability assurance needed for the different applications

The sub-paragraphs use the same No. for quick reference.

Full traceabilty of a delivery lot to an assembly lot and the specific semiconductor wafers used is ensured for the High Rel Quality Level and the further upgrades.

Diced Wafer Released for Professional Quality Level		
§ 1	**Assembling**	
	1.1	Die Selection
	1.2	Die Mounting
	1.3	Wire Bonding
	1.4	Internal Visual Inspection
	1.5	Bond Strength Test (Sample)
	1.6	Die Shear Test (Sample)
	1.7	Encapsulation
	1.8	High Temperature Stabilisation Bake
	1.9	External Visual Inspection
	1.10	Review of Assembling
	Release for Final Production Tests	
§ 2	**Final Production Tests**	
	2.6	Fine Leak and Gross Leak Seal Test
	2.8	Full Electrical Measurements at Room Temperature
	2.9	Marking
	2.10	External Visual Inspection
	2.11	Review of Final Production Tests
	Delivery	

Figure 6
Assembling and Testing Flow at the Professional Quality Level

Diced Wafer Released for High Rel Quality Level		
§ 1	**Assembling**	
	1.1	Die Selection
	1.2	Die Mounting
	1.3	Wire Bonding
	1.4	Visual Inspection, Internal
	1.5	Bond Strength Test (Sample)
	1.6	Die Shear Test (Sample)
	1.7	Encapsulation
	1.8	High Temperature Stabilisation Bake
	1.9	External Visual Inspection
	1.10	Review of Assembling
	Release for Final Production Tests	
§ 2	**Final Production Tests**	
	2.2	Thermal Shock
	2.5	Particle Impact Noise Detection Test PIND
	2.6	Fine Leak and Gross Leak Seal Test
	2.8	Full Electrical Measurements at Room Temperature
	2.9	Marking
	2.11	Review of Final Production Tests
	Release for Burn-In	
§ 3	**Burn-In and Electrical Measurements**	
	3.1	High Temperature Reverse Bias or Power Burn-In
	3.6	Full Electrical Measurements at Room Temperature
	3.7	Fine Leak and Gross Leak Seal Test
	3.8	External Visual Inspection
	3.9	Review of Burn-In and Measurements/Check for Lot Acceptance
	3.12	Certificate of Compliance
	Delivery	

Figure 7
Assembling and Testing Flow at the High Rel Quality Level

Diced Wafer Released for Space Quality Level		
§ 1	**Assembling**	
	1.1	Die Selection
	1.2	Die Mounting
	1.3	Wire Bonding
	1.4	Internal Visual Inspection
	1.5	Bond Strength Test (Sample)
	1.6	Die Shear Test (Sample)
	1.7	Encapsulation
	1.8	High Temperature Stabilisation Bake
	1.9	External Visual Inspection
	1.10	Review of Assembling
	Release for Final Production Tests	
§ 2	**Final Production Tests**	
	2.2	Thermal Shock
	2.3	Constant Acceleration (for large components only)
	2.4	Vibration (for large components only)
	2.5	Particle Impact Noise Detection Test PIND
	2.6	Fine Leak and Gross Leak Seal Test
	2.7	Electrical Measurements and Pre Burn-In (if specified)
	2.8	Full Electrical Measurements at Room Temperature
	2.9	Marking
	2.11	Review of Final Production Tests
	Release for Burn-In	
§ 3	**Burn-In and Electrical Measurements**	
	3.1	High Temperature Reverse Bias or Power Burn-In
	3.2	Power Burn-In 1 and Parameter Drift/PDA Evaluation
	3.4	Electrical Measurements at High and Low Temperatures
	3.5	Radiographic Inspection (if specified)
	3.6	Full Electrical Measurements at Room Temperature
	3.7	Fine Leak and Gross Leak Seal Test
	3.8	External Visual Inspection
	3.9	Review of Burn-In and Measurements/Check for Lot Acceptance
	3.10	Perform Lot Acceptance Tests (if ordered)
	3.11	Prepare Data Package (Final Electrical Measurements Results)
	3.12	Certificate of Compliance
	Delivery	

Figure 8
Assembling and Testing Flow at the Space Quality Level

Diced Wafer Released for ESA Space Quality Level		
§ 1	**Assembling**	
	1.1	Die Selection
	1.2	Die Mounting
	1.3	Wire Bonding
	1.4	Internal Visual Inspection
	1.5	Bond Strength Test (Sample)
	1.6	Die Shear Test (Sample)
	1.7	Encapsulation
	1.8	High Temperature Stabilisation Bake
	1.9	External Visual Inspection
	1.10	Review of Assembling
	Release for Final Production Tests	
§ 2	**Final Production Tests**	
	2.1	Electrical Measurements Go/Nogo
	2.2	Thermal Shock
	2.3	Constant Acceleration (for large components only)
	2.4	Vibration (for large components only)
	2.5	Particle Impact Noise Detection Test PIND
	2.6	Fine Leak and Gross Leak Seal Test
	2.7	Electrical Measurements and Pre Burn-In (if specified)
	2.8	Full Electrical Measurements at Room Temperature
	2.9	Marking
	2.10	Dimension Check
	2.11	Review of Final Production Tests
	Release for Burn-In	
§ 3	**Burn-In and Electrical Measurements**	
	3.1	High Temperature Reverse Bias or Power Burn-In
	3.2	Power Burn-In 1 and Parameter Drift/PDA Evaluation
	3.3	Power Burn-In 2 and Parameter Drift/PDA Evaluation
	3.4	Electrical Measurements at High and Low Temperatures
	3.5	Radiographic Inspection (if specified)
	3.6	Full Electrical Measurements at Room Temperature
	3.7	Fine Leak and Gross Leak Seal Test
	3.8	External Visual Inspection
	3.9	Review of Burn-In and Measurements/Check for Lot Acceptance
	3.10	Perform Lot Acceptance Tests (if ordered)
	3.11	Prepare Full ESA Data Package
	3.12	Certificate of Compliance
	Delivery	

Figure 9
Assembling and Testing Flow at the ESA Space Quality Level

4 Selection Guides for *HiRel* Discrete Semiconductors

The Selection Guide provides main maximum ratings and electrical key parameters (typical data).

4.1 *HiRel* Silicon Diodes

Low Barrier Silicon Schottky Diodes

($T_{op,max}$ = 150 °C)

Type	Max. Ratings		Characteristics					Package	ESA/SCC
	V_R	I_F	V_{BR} (-10 µA)	V_F (1 mA)	C_D (0 V)	R_F (10/50 mA)	NF (9.4 GHz)		Detail Spec. - Type Variant
	V	mA	V	V	pF	Ω	dB		
BAT15-013/014 BAT15-033/034	3	100	> 3.5	0.23	0.35	3.0 4.0	5.3 6.3	T/T1	5106/014-19/20 5106/014-21/22
BAT15-043/044 BAT15-063/064	3	100	> 3.5	0.27	0.30	3.5 4.5	5.3 6.3	T/T1	5106/014-23/24 5106/014-25/26
BAT15-073/074 BAT15-093/094	3	50	> 3.5	0.29	0.27	4.5 5.5	5.3 6.3	T/T1	5106/014-27/28 5106/014-29/30
BAT15-103/104 BAT15-113/114	3	50	> 3.5	0.30	0.23	6.0 7.0	5.7 7.2	T/T1	5106/014-31/32 5106/014-33/34
BAT15-123/124	3	50	> 3.5	0.31	0.20	8.0	8.0	T/T1	5106/014-35/36

Medium Barrier Silicon Schottky Diodes

($T_{op,max}$ = 150 °C)

Type	Max. Ratings		Characteristics					Package	ESA/SCC
	V_R	I_F	V_{BR} (-10 µA)	V_F (1 mA)	C_D (0 V)	R_F (10/50 mA)	NF (9.4 GHz)		Detail Spec. - Type Variant
	V	mA	V	V	pF	Ω	dB		
BAT14-013/014 BAT14-033/034	3	100	> 3.5	0.42	0.35	3.0 4.0	5.3 6.3	T/T1	5106/014-01/02 5106/014-03/04
BAT14-043/044 BAT14-063/064	3	100	> 3.5	0.44	0.30	3.5 4.5	5.3 6.3	T/T1	5106/014-05/06 5106/014-07/08
BAT14-073/074 BAT14-093/094	3	50	> 3.5	0.45	0.27	4.5 5.5	5.3 6.3	T/T1	5106/014-09/10 5106/014-11/12
BAT14-103/104 BAT14-113/114	3	50	> 3.5	0.46	0.23	6.0 7.0	5.7 7.2	T/T1	5106/014-13/14 5106/014-15/16
BAT14-123/124	3	50	> 3.5	0.48	0.20	8.0	8.0	T/T1	5106/014-17/18

General Purpose Silicon Schottky Diodes

($T_{j,max}$ = 150 °C)

Type	Max. Ratings		Characteristics				Package	ESA/SCC
	V_R	I_F	V_{BR} (-10 µA)	V_F (1 mA)	R_F (10/50 mA)	C_D (0 V)		Detail Spec. - Type Variant
	V	mA	V	V	Ω	pF		
BAS 40-T1	40	120	> 40	0.33	9.0	3.0	T1	t.b.d.
BAS 70-T1 BAS 70B-H (bridge quad)	70	70	> 70	0.38	30	1.4	T1 HPAC140	5512/020-01 5512/020-02

Silicon PIN Diodes

($T_{op,max}$ = 175 °C)

Type	Max. Ratings		Characteristics				Package	ESA/SCC
	V_R	P_{tot}	V_{BR} (-10 µA)	R_F (10 mA)	C_T (- 50 V)	t ($I_{f/r}$ = +10/ - 6 mA)		Detail Spec. - Type Variant
	V	mW	V	Ω	pF	ns		
BXY 42 T1 BXY 42 T	50	350 600	> 50	1.5	0.22 (20 V)	50	T1 T	5513/017-01 5513/017-02
BXY 43 T BXY 43 T1 BXY 43 P1 BXY 43 FP (matched pair)	150	500	> 150	0.9	0.30 0.30 0.50 0.60	650	T T1 P1 FP	5513/030-01 5513/030-02 5513/030-03 5513/030-04
BXY 44 T BXY 44 T1 BXY 44 T2 BXY 44 FP (matched pair)	200	500	> 200	3.0	0.20	430	T T1 T2 FP	5513/030-05 5513/030-06 5513/030-07 5513/030-08

4.2 *HiRel* Silicon Bipolar Transistors

Conventional Silicon Bipolar Microwave Transistors

($T_{j,max}$ = 200 °C)

Type	Max. Ratings			Characteristics					Package	ESA/SCC
	V_{CE0}	I_C	P_{tot}	$R_{thJS\ max}$	f_T (500 MHz, 5 V)	NF (2 GHz, 5 V)	$G_{ma/ms}$ (2 GHz, 5 V)	P_{out} (2 GHz, 5 V)		Detail Spec. - Type Variant
	V	mA	mW	K/W	GHZ	dB	dB	dBm		
BFY180	8	4	30	805	6.5	2.6	13.5	-	Micro-X1	5611/006-01
BFY280	8	10	80	450	7.0	2.5	14.0	-	Micro-X1	5611/006-02
BFY181	12	20	175	360	7.5	2.2	14.5	-	Micro-X1	5611/006-03
BFY182	12	35	250	255	7.5	2.4	14.5	-	Micro-X1	5611/006-04
BFY183	12	65	450	225	7.5	2.3	14.0	14.5	Micro-X1	5611/006-05
BFY193	12	80	580	165	7.5	2.3	13.5	17.5	Micro-X1	5611/006-06
BFY196*	12	100	700	135	6.5	3.0	11.0	18.5	Micro-X1	5611/006-t.b.d.

* Component under development, expected performance to be confirmed.

SIEGET Silicon Bipolar Microwave Transistors

($T_{j,max}$ = 175 °C)

Type	Max. Ratings			Characteristics					Package	ESA/SCC
	V_{CE0}	I_C	P_{tot}	$R_{thJS\ max}$	f_T (2 GHz, 3 V)	NF (1.8 GHz, 2 V)	$G_{ma/ms}$ (1.8 GHz, 2 V)	P_{out} (1.8 GHz, 2 V)		Detail Spec. - Type Variant
	V	mA	mW	K/W	GHz	dB	dB	dBm		
BFY405	4.5	12	55	545	22	1.15	23	5	Micro-X	5611/008-01
BFY420	4.5	35	160	285	22	1.05	21	12	Micro-X	5611/008-02
BFY450	4.5	100	450	145	22 (1GHz)	1.25	16	19 (3V)	Micro-X	5611/008-03
BFY490*	4.5	600	2700	t.b.d.	17 (200 MHz)	1.9	10	26.5	MWP25	t.b.d.

* Component under development, expected performance to be confirmed.

4.3 *HiRel* GaAs Microwave Devices

General Purpose GaAs Microwave C/Ku-Band MESFETs
($T_{j,max}$ = 175 °C)

Type	Max. Ratings				Characteristics				Package	ESA/SCC
	V_{DS}	V_{DG}	I_D	P_{tot}	$R_{thJS\ max}$	NF (12 GHz)	G_a (12 GHz)	P_{out} (12 GHz)		Detail Spec. - Type Variant
	V	V	mA	mW	K/W	GHz	dB	dBm		
CFY25-23	5	7	80	250	375	2.3	8.7		Micro-X	t.b.d.
CFY25-20	5	7	80	250	375	2.0	9.0		Micro-X	t.b.d.
CFY27*	5	7	320	800	125			24.0	Micro-X	t.b.d.

* Component under development, expected performance to be confirmed.

Low Noise GaAs Microwave X/K-Band HEMTs
($T_{j,max}$ = 150 °C)

Type	Max. Ratings				Characteristics				Package	ESA/SCC
	V_{DS}	V_{DG}	I_D	P_{tot}	$R_{thJS\ max}$	NF (12 GHz)	G_a (12 GHz)	P_{out} (12 GHz)		Detail Spec. - Type Variant
	V	V	mA	mW	K/W	GHz	dB	dBm		
CFY66-10	3.5	4.5	60	200	515	0.9	10.5		Micro-X	5613/002-02
CFY66-10P	3.5	4.5	60	200	515	0.9	10.5	11.0	Micro-X	5613/002-04
CFY66-08	3.5	4.5	60	200	515	0.7	11.0		Micro-X	5613/002-01
CFY66-08P	3.5	4.5	60	200	515	0.7	11.0	11.0	Micro-X	5613/002-03
CFY67-10	3.5	4.5	60	200	515	0.9	11.0		Micro-X	5613/004-02
CFY67-10P	3.5	4.5	60	200	515	0.9	11.0	11.0	Micro-X	5613/004-04
CFY67-08	3.5	4.5	60	200	515	0.7	11.5		Micro-X	5613/004-01
CFY67-08P	3.5	4.5	60	200	515	0.7	11.5	11.0	Micro-X	5613/004-03
CFY67-06*	3.5	4.5	60	200	515	0.5	12.0	11.0	Micro-X	tbd.

* Component under development, expected performance to be confirmed.

Power GaAs Microwave L/C-Band MESFETs

($T_{j,max}$ = 175 °C)

Type	Max. Ratings				Charakteristics				Package	ESA/SCC
	V_{DS}	V_{DG}	I_D	P_{tot}	$R_{thJS\ max}$	P_{-1dB} (2.3 GHz)	G_{-1dB} (2.3 GHz)	PAE (2.3 GHz)		Detail Spec. - Type Variant
	V	V	mA	W	K/W	dBm	dB	%		
CLY29	14	16	600	3.75	36 (40)	30.0	13.5	55	MWP-25	t.b.d.
CLY32	14	16	1200	7.5	16 (20)	33.0	11.5	55	MWP-25	5614/006-01
CLY35	14	16	2400	15	6.0 (7.5)	35.7	11.0	55	MWP-35	t.b.d.
CLY38*	14	16	4800	30	3.8 (4.5)	38.7	10.7	55	MWP-35	t.b.d.

* Component under development, expected performance to be confirmed.

Power GaAs Microwave C/Ku-Band MESFETs

($T_{j,max}$ = 175 °C)

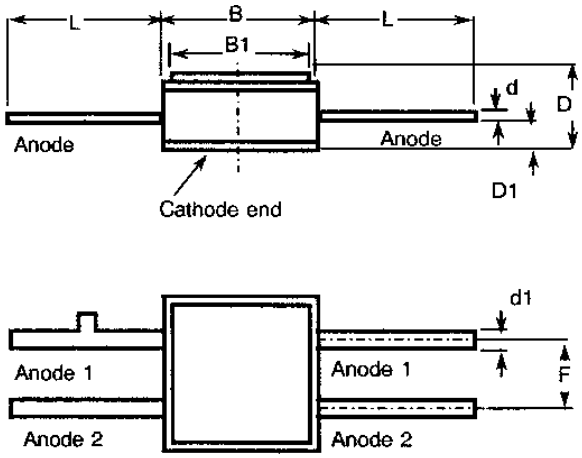
Type	Max. Ratings				Charakteristics				Package	ESA/SCC
	V_{DS}	V_{DG}	I_D	P_{tot}	$R_{thJS\ max}$	P_{-1dB} (2.3 GHz)	G_{-1dB} (2.3 GHz)	PAE (2.3 GHz)		Detail Spec. - Type Variant
	V	V	mA	W	K/W	dBm	dB	%		
CLY27*	11	13	480	3	36 (40)	27.5	11.0	55	MWP-25	t.b.d.
CLY30*	11	13	960	6	18 (20)	30.5	10.5	52	MWP-25	t.b.d.

* Component under development, expected performance to be confirmed.

5 Package Outlines *HiRel*

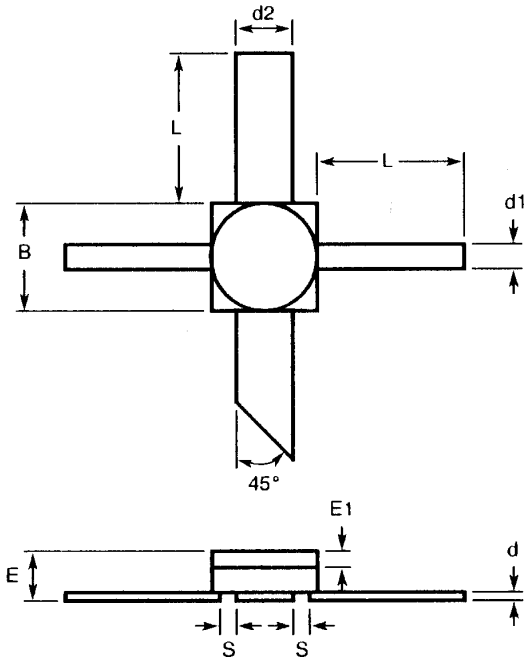
5.1 Package Outlines of Diode Packages

SYMBOL	MILLIMETRES	
	MIN	MAX
B	3.10	3.55
B1	3.00	3.30
D	1.30	1.70
D1	0.55	0.65
d	0.10	0.15
d1	0.25	0.40
F	2.40	2.60
L	5.50	-

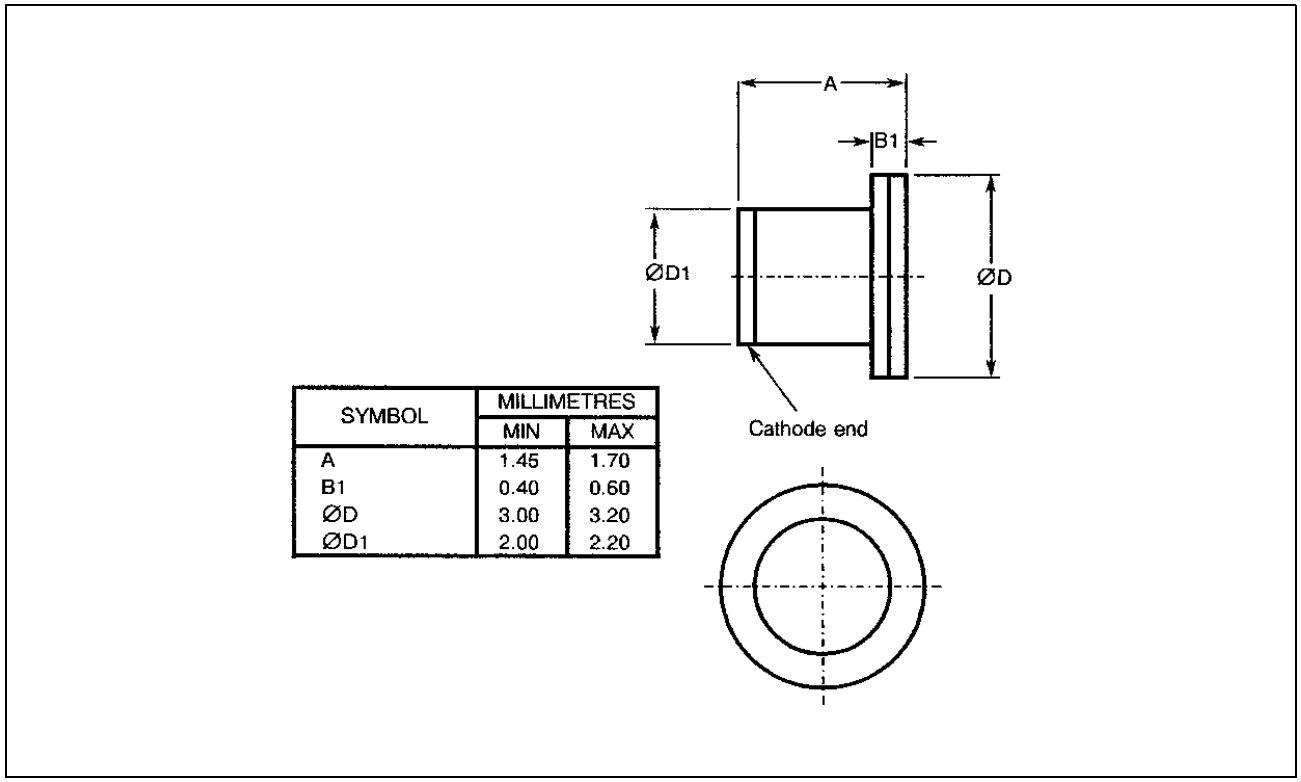


FP Package

SYMBOL	MILLIMETRES	
	MIN	MAX
B	3.40	3.60
d	0.07	0.15
d1	0.50	0.70
d2	1.90	2.10
E	-	1.60
E1	0.10	0.20
L	6.00	-
S	0.10	0.40

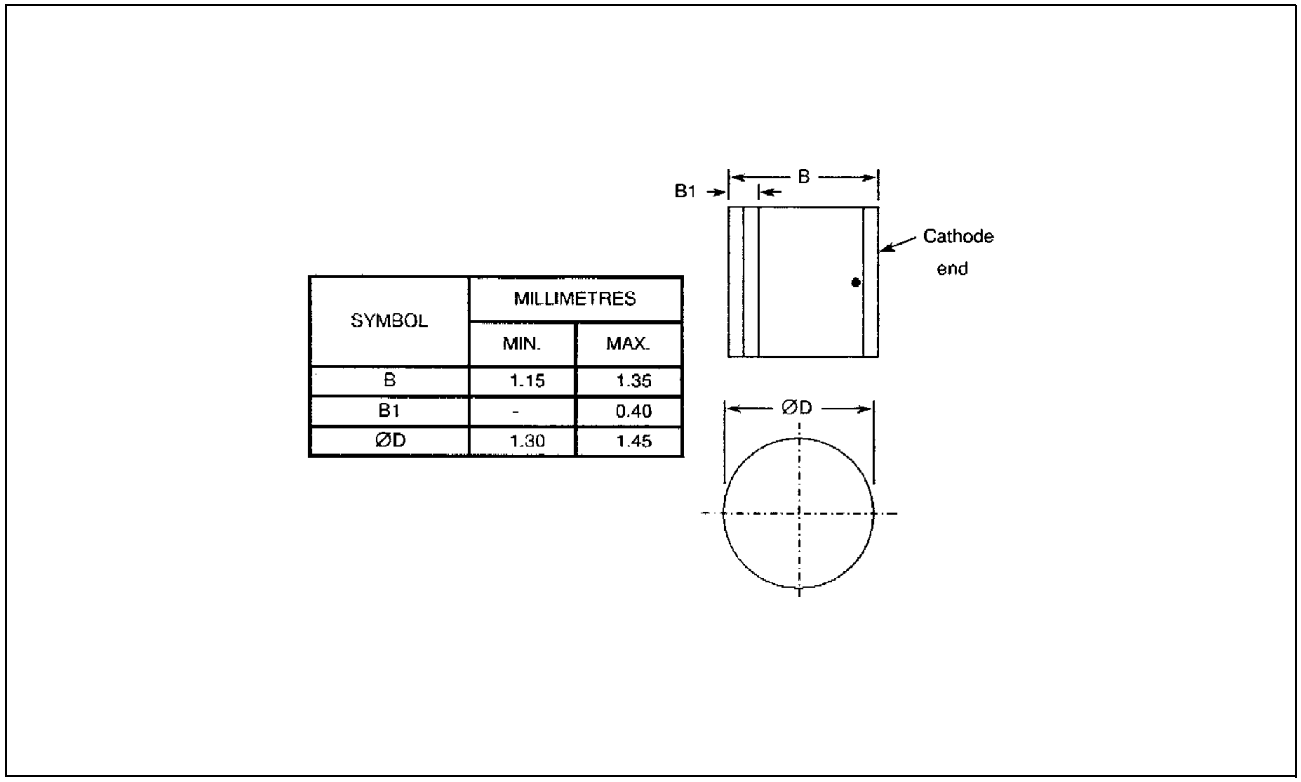


HPAC140 Package



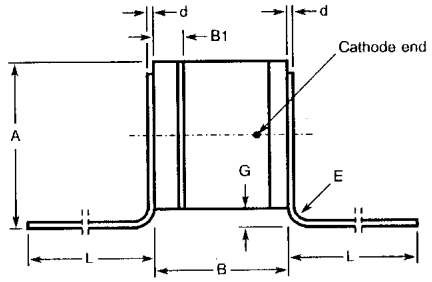
SYMBOL	MILLIMETRES	
	MIN	MAX
A	1.45	1.70
B1	0.40	0.60
ØD	3.00	3.20
ØD1	2.00	2.20

P1 Package

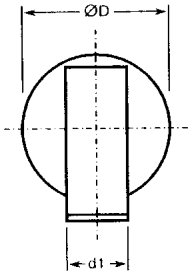


SYMBOL	MILLIMETRES	
	MIN.	MAX.
B	1.15	1.35
B1	-	0.40
ØD	1.30	1.45

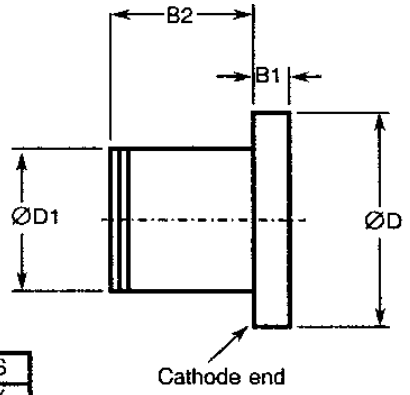
T Package



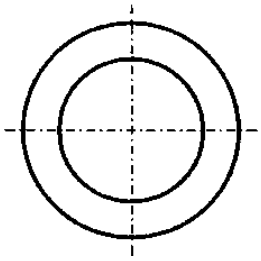
SYMBOL	MILLIMETRES		NOTES
	MIN	MAX	
A	1.40	1.95	
B	1.15	1.35	
B1	-	0.40	
d	0.06	0.10	
d1	0.40	0.60	All terminations
ØD	1.30	1.45	
E	-	0.30	Radius
G	0.10	0.50	
L	5.50	-	



T1 Package

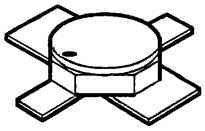


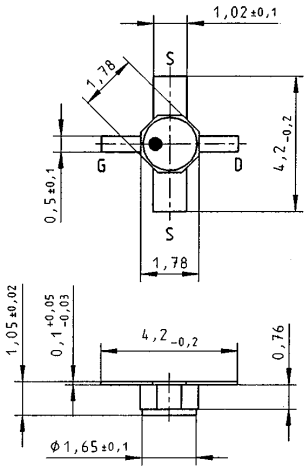
SYMBOL	MILLIMETRES	
	MIN	MAX
B1	0.08	0.20
B2	0.60	1.25
ØD	2.00	2.20
ØD1	1.30	1.45



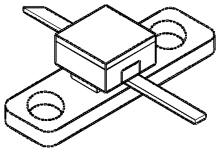
T2 Package

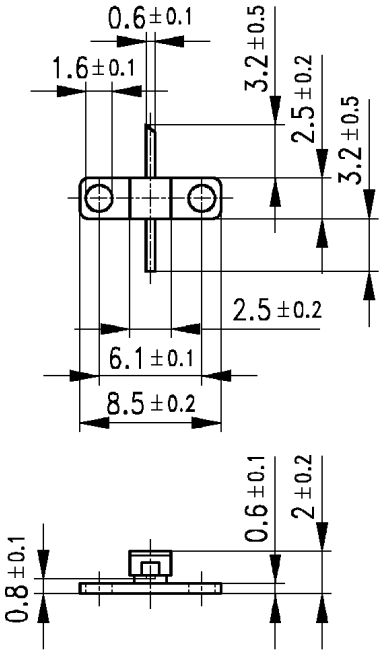
5.2 Package Outlines of Transistor Packages



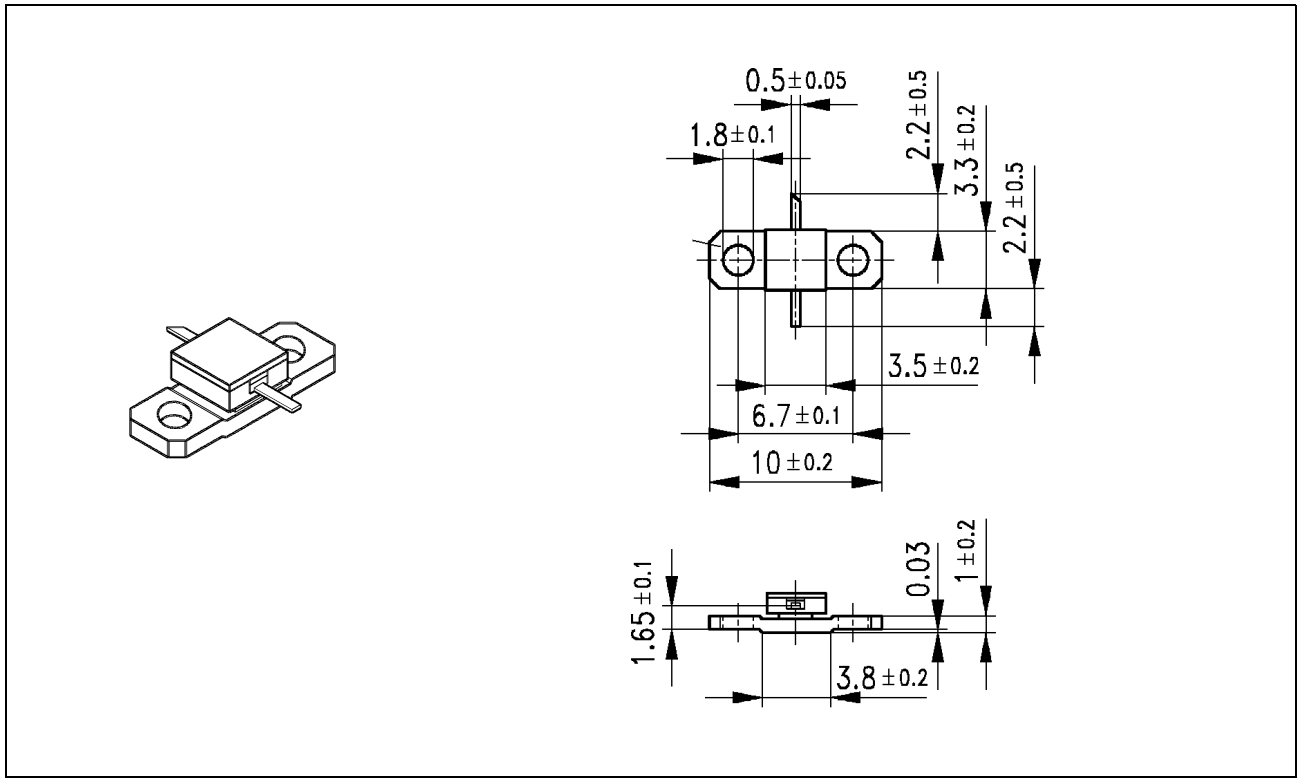


Micro-X1 Package





MWP-25 Package



MWP-35 Package