



AN3332

Application note

Generating PWM signals using STM8S-DISCOVERY

Application overview

This application user manual provides a short description of how to use the Timer 2 peripheral (TIM2) to generate three PWM signals.

Even though the STM8S-DISCOVERY is built around an STM8S105C6T6, it allows evaluation of the main features of all the STM8S MCUs.

Reference documents

- STM8S-DISCOVERY evaluation board user manual (UM0817).
- Developing and debugging STM8S-DISCOVERY application user manual (UM0834).

1 Application description

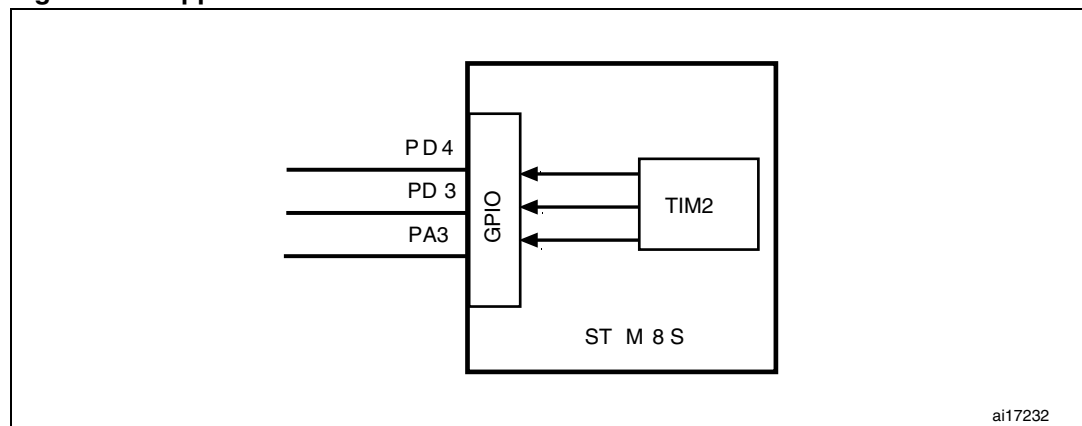
1.1 Hardware requirement

No additional hardware is required on the STM8S-DISCOVERY board.

An oscilloscope is needed as an external resource.

1.2 Application schematics

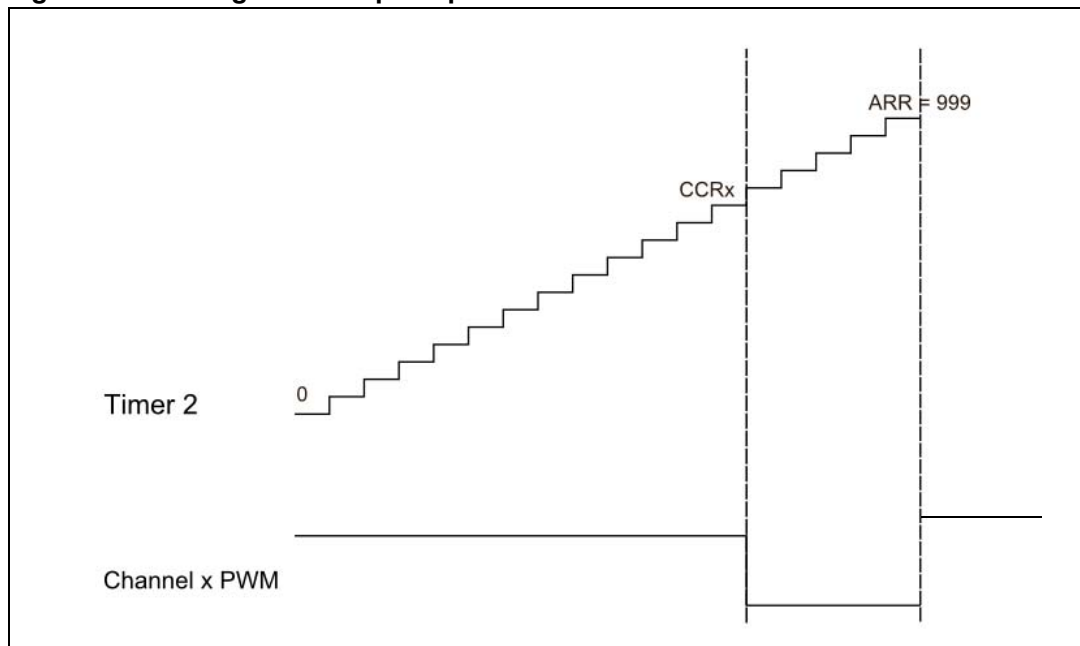
Figure 1. Application schematics



1.3 Application principle

This application is based on the use of the STM8S TIM2 in PWM (pulse width modulation) mode to generate 3 PWM signals.

The generation process is presented in [Figure 2](#).

Figure 2. PWM generation principle

TIM2 counts up from 0 to the Auto-reload register value (TIM2_ARR) according to the TIM2 counter clock.

- When the counter value equals the Compare/Capture register (TIM2_CCRxx) value channel x signal is set to 0.
- When the counter value reaches the TIM2_ARR value the counter is reset and channel x signal is set to 1.

By configuring the TIM2_CCRxx and TIM2_ARR registers you can easily modify the duty cycle and frequency of the PWM signals generated (see [Section 2: Software description](#)).

By default the application provides the 3 PWM signals as specified in [Table 1](#).

Note: It is possible to configure the AFR option byte to get channel 3 on PD2 also.

Table 1. Default PWM signals

Signal	Duty cycle	Frequency	I/O pin	Header connector
Channel 1 PWM	50%	2 KHz	PD4	CN4.9
Channel 2 PWM	25%	2 KHz	PD3	CN4.8
Channel 3 PWM	75%	2 KHz	PA3	CN1.9

2 Software description

This example uses the STM8S standard firmware library to control the general purpose functions.

To generate the PWM signals the TIM2 peripheral must be configured as follows:

- Output state enabled for each channel
- Output compare active low for each channel
- Preload register enabled for each channel
- PWM output signal frequency = 2 KHz:
 - The timer source clock frequency is 2 MHz (f_{CPU} by default) and the prescaler is set to 1 to obtain a TIM2 counter clock of 2 MHz.
 - PWM output signal frequency can be set according to the following equation:
PWM output signal frequency = TIM2 counter clock/(TIM2_ARR + 1)
(in our case TIM2_ARR = 999, so PWM output signal frequency is 2 KHz)
- PWM mode for each channel. To obtain a different PWM duty cycle value on each channel the TIM2_CCRxx register must be set according to this equation:
Channel x duty cycle = [TIM2_CCRxx/(TIM2_ARR + 1)] * 100
By default we have:
 - Channel 1: TIM2_CCR1x register value is 500, so channel 1 of TIM2 generates a PWM signal with a frequency of 2 KHz and a duty cycle of 50%.
 - Channel 2: TIM2_CCR2x register value is 750, so channel 2 of TIM2 generates a PWM signal with a frequency of 2 KHz and a duty cycle of 75%.
 - Channel 3: TIM2_CCR3x register value is 250, so channel 3 of TIM2 generates a PWM signal with a frequency of 2 KHz and a duty cycle of 25%.

2.1 STM8S standard firmware library configuration

The *stm8s_conf.h* file of the STM8S standard firmware library is used to configure the library by enabling the peripheral functions used by the application.

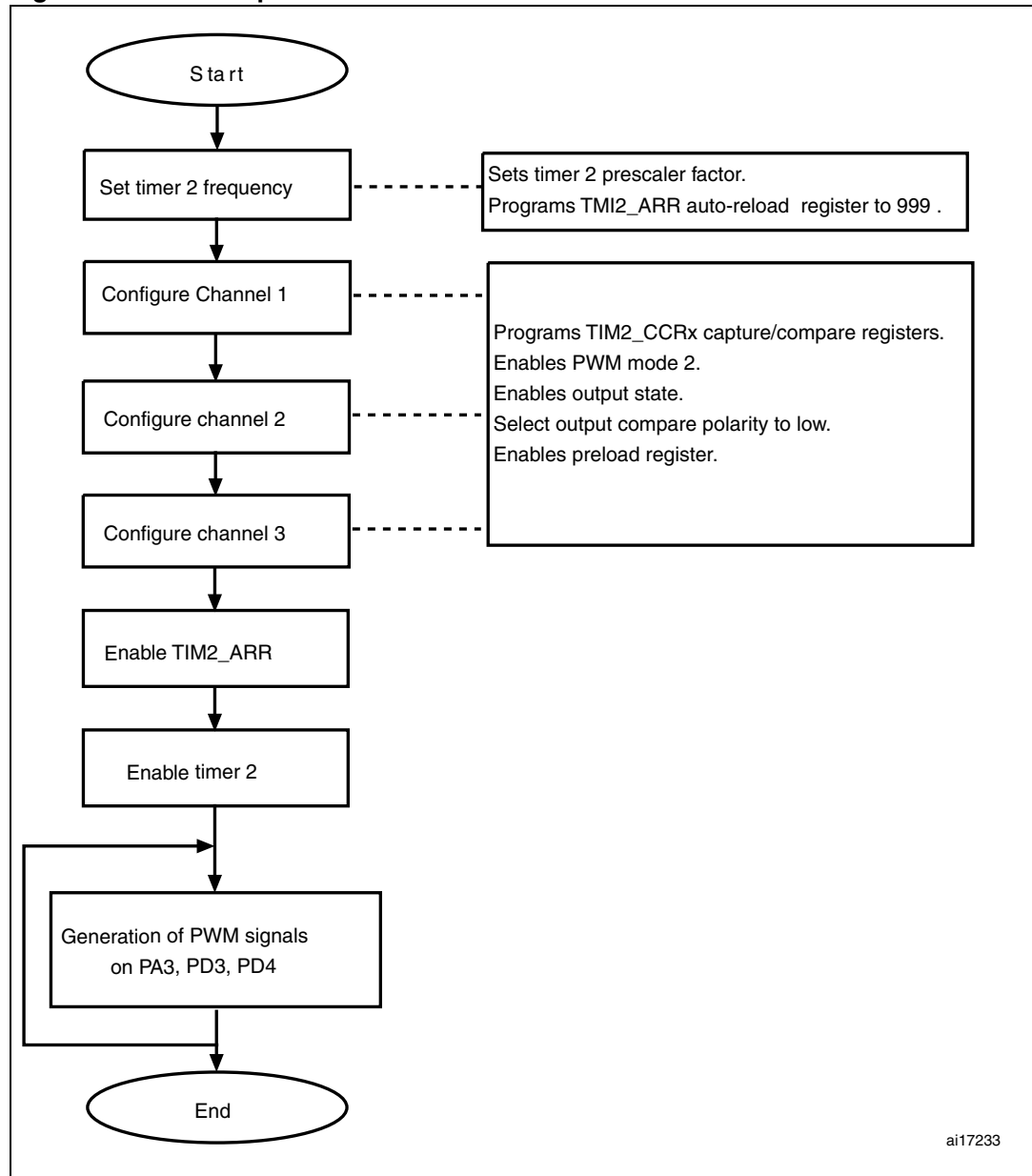
The following `define` statements must be present:

- `#define _GPIO 1` enables the GPIOs
- `#define _TIM2 1` enables the TIM2

2.2 Application software flowcharts

2.2.1 Main loop flowchart

Figure 3. Main loop flowchart



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
15-Jan-2011	1	Initial release. This document replaces UM0856.

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