AN4080
Application note

Getting started with STM32F0xxx hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use the STM32F0xxx product family and describes the minimum hardware resources required to develop an STM32F0xxx application.

The STM32F0xxx family comprises a sub-group, the STM32F06xxx, which can be distinguished from the main devices (STM32F05xxx). This sub-family bypasses the internal voltage regulator to target applications that already have one onboard.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

Table 1. Applicable products

Type	Part number
Microcontrollers	STM32F05xxx family
	STM32F06xxx family

Contents

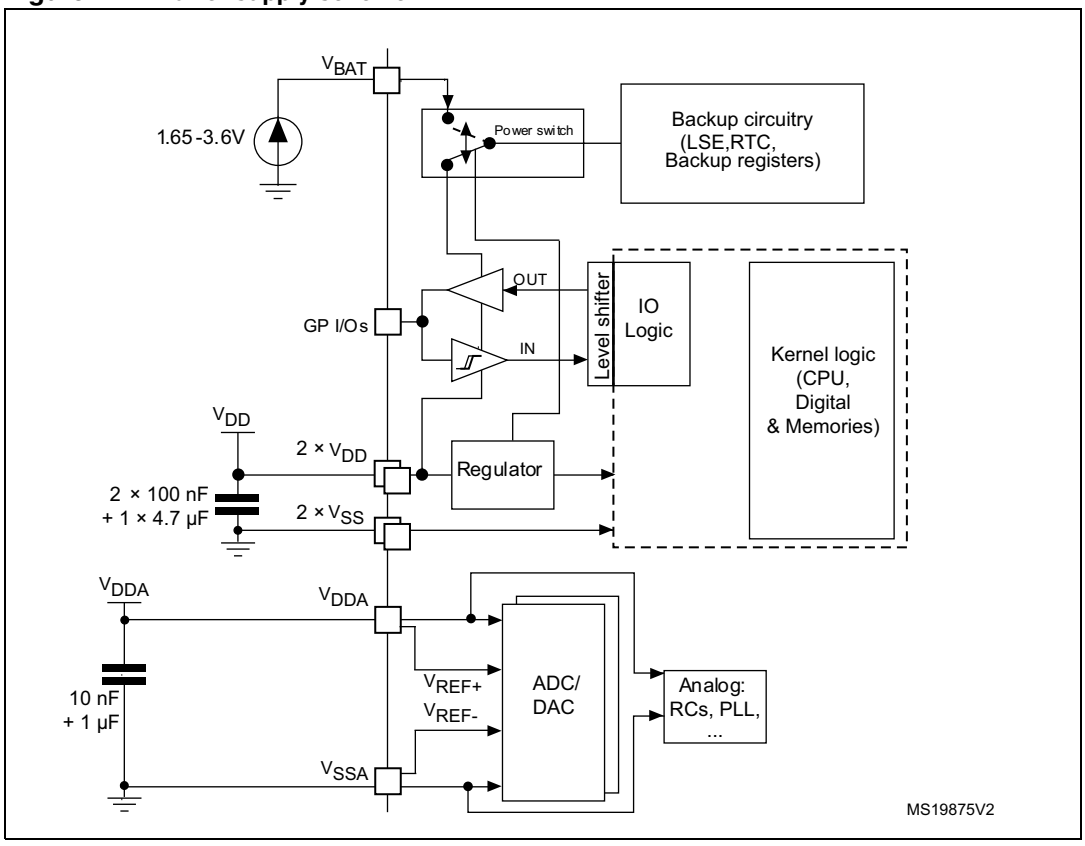
1 Power supplies of the STM32F05xxx family

1.1 Power supply schemes

There are a variety of power supply schemes:

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC/DAC, Reset blocks, HSI, HSI14, LSI and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used).
  The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, LSE 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Figure 1. Power supply scheme



1.1.1 Independent analog converter supply

To improve conversion accuracy and to extend the supply flexibility, the analog domain has an independent power supply which can be separately filtered and shielded from noise on the PCB.

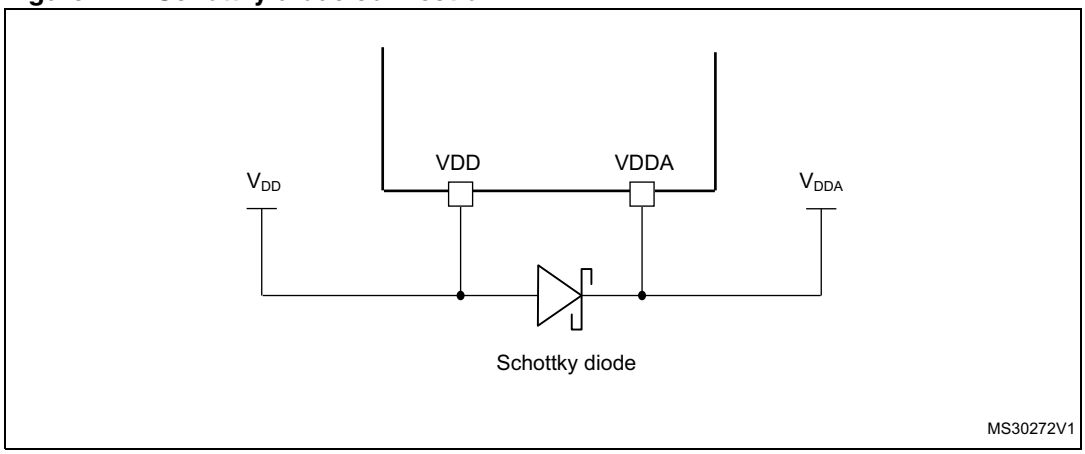
- The ADC and DAC voltage supply input is available on a separate VDDA pin.
- An isolated supply ground connection is provided on pin VSSA.

The V_{DDA} supply can be equal to or higher than V_{DD}. This allows V_{DD} to stay low while still providing the full performance for the analog blocks.

When a single supply is used, V_{DDA} must be externally connected to V_{DD},. It is recommended to use an external filtering circuit in order to ensure a noise free V_{DDA}.

When V_{DDA} is different from V_{DD}, V_{DDA} must be always higher or equal to V_{DD}. To keep safe potential difference between V_{DDA} and V_{DD} during power-up/power-down, an external Schottky diode may be used between V_{DD} and V_{DDA}. Refer to the datasheet for the maximum allowed difference.

Figure 2. Schottky diode connection



1.1.2 Battery backup

To retain the content of the Backup registers when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or another source.

The V_{BAT} pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off.

The switch to the V_{BAT} supply is controlled by the power down reset (PDR) circuitry embedded in the Reset block.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

1.1.3 Voltage regulator

The voltage regulator is always enabled after reset.

It works in three different modes depending on the application modes:

- Run mode: the regulator supplies full power to the 1.8 V domain (core, memories and digital peripherals)
- Stop mode: the regulator supplies low power to the 1.8 V domain, preserving the contents of the registers and SRAM
- Standby mode: the regulator is powered off. The contents of the registers and SRAM are lost except for the Standby circuitry and the Backup domain. This includes the following features which can be selected by programming individual control bits:
  - Independent watchdog (IWDG): the IWDG is started by writing to its Key register or by a hardware option. Once started it cannot be stopped except by a reset.
  - Real-time clock (RTC): configured by the RTCEN bit in the Backup domain control register (RCC_BDCR).
  - Internal low speed oscillator (LSI): configured by the LSION bit in the Control/status register (RCC_CSR).
  - External 32.768 kHz oscillator (LSE): configured by the LSEON bit in the Backup domain control register (RCC_BDCR).

1.2 Reset and power supply supervisor

1.2.1 Power-on reset (POR) / power-down reset (PDR)

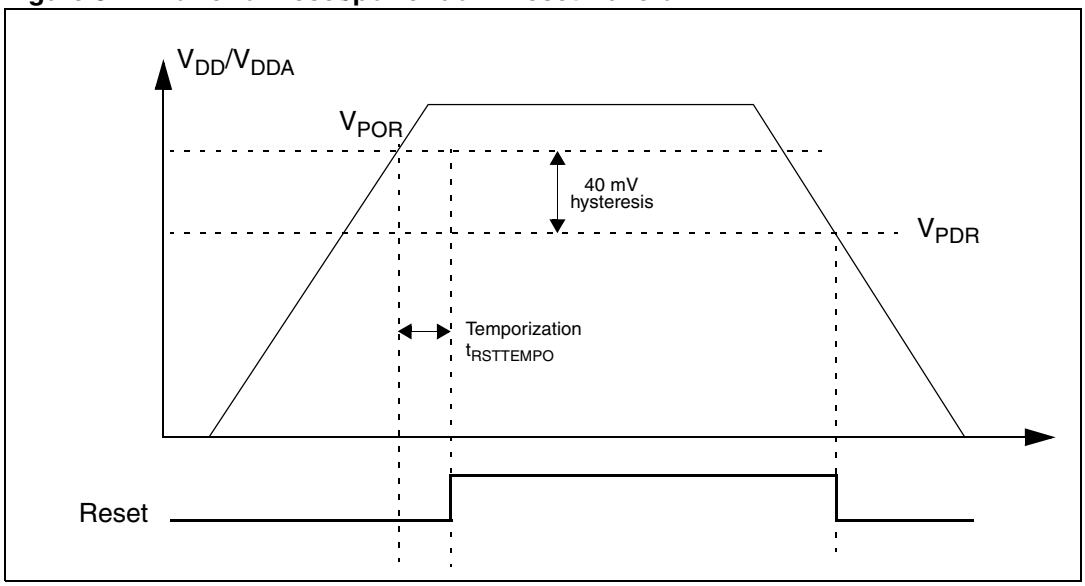
The device has an integrated power-on reset (POR) and power-down reset (PDR) circuits which are always active and ensure proper operation above a threshold of 2 V.

The device remains in Reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase V_{DDA} must arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages. However, the V_{DDA} power supply supervisor can be disabled (by programming a dedicated option bit $V_{DDA\_MONITOR}$) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

For more details on the power on / power down reset threshold, refer to the electrical characteristics section in the datasheet.

Figure 3. Power on reset/power down reset waveform



1.2.2 System reset

A system reset sets all registers to their reset values, except the reset flags in the clock controller CSR register and the registers in the Backup domain. A system reset is generated when one of the following events occurs:

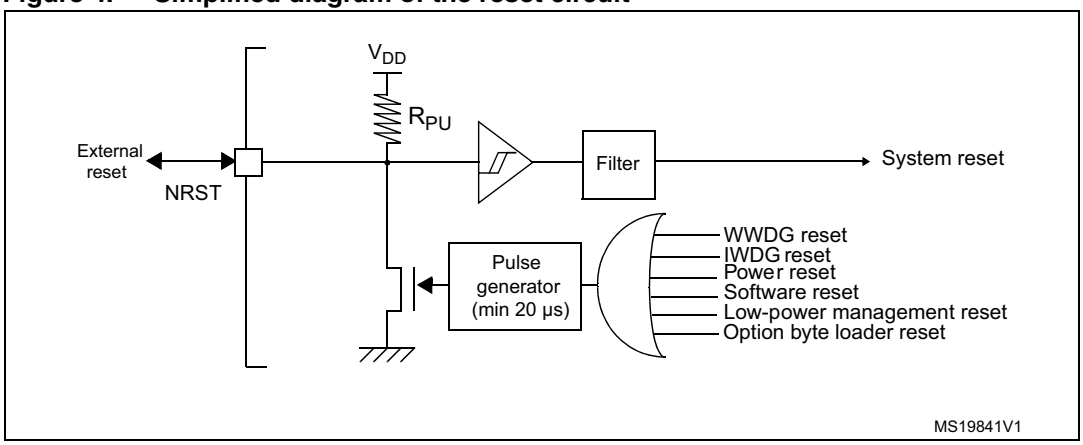
1. A low level on the NRST pin (external reset).
2. System window watchdog event (WWDG reset).
3. Independent watchdog event (IWDG reset).
4. A software reset (SW reset).
5. Low-power management reset.
6. Option byte loader reset.
7. Power reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In the case of an external reset, the reset is generated while the NRST pin is asserted low.

Figure 4. Simplified diagram of the reset circuit



Software reset

The SYSRESETREQ bit in Cortex-M0 Application Interrupt and Reset Control Register must be set to force a software reset on the device. Refer to the *Cortex™-M0 technical reference manual* for more details.

Low-power management reset

There are two ways to generate a low-power management reset:

1. Entering Standby mode: This type of reset is enabled by resetting nRST_STDBY bit in User Option Bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
2. Entering Stop mode: This type of reset is enabled by resetting nRST_STOP bit in User Option Bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.

Option byte loader reset

The option byte loader reset is generated when OBL_LAUNCH (bit 13) is set in the FLASH_CR register. This bit launches the option byte loading by software.

Power reset

A power reset sets all registers to their reset values, except the Backup domain. It is generated when one of the following events occurs.

1. Power-on/power-down reset (POR/PDR reset).
2. Exiting Standby mode.

Backup domain reset

A backup domain reset only affects the backup domain. It is generated when one of the following events occurs.

1. Software reset, triggered by setting the BDRST bit in the Backup domain control register (RCC_BDCR).
2. VDD power up if VBAT has been disconnected when it was low.
3. RTC tamper detection event.
4. Change of the read out protection from level 1 to level 0.

1.2.3 Programmable voltage detector (PVD)

You can use the PVD to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the Power control register (PWR_CR).

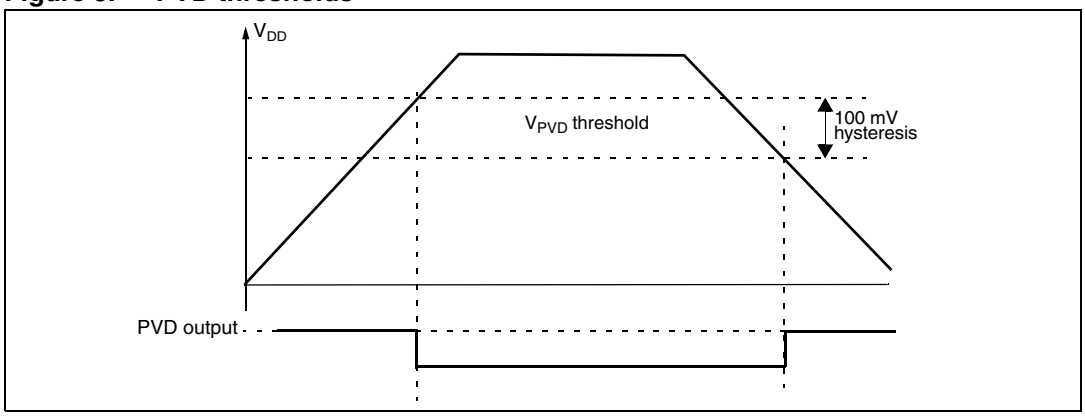
The PVD is enabled by setting the PVDE bit.

When enabled, the typical current consumption of this feature is 0.15 µA.

A PVDO flag is available, in the Power control/status register (PWR_CSR), to indicate if V_{DD} is higher or lower than the PVD threshold.

- This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers.
- The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 5. PVD thresholds



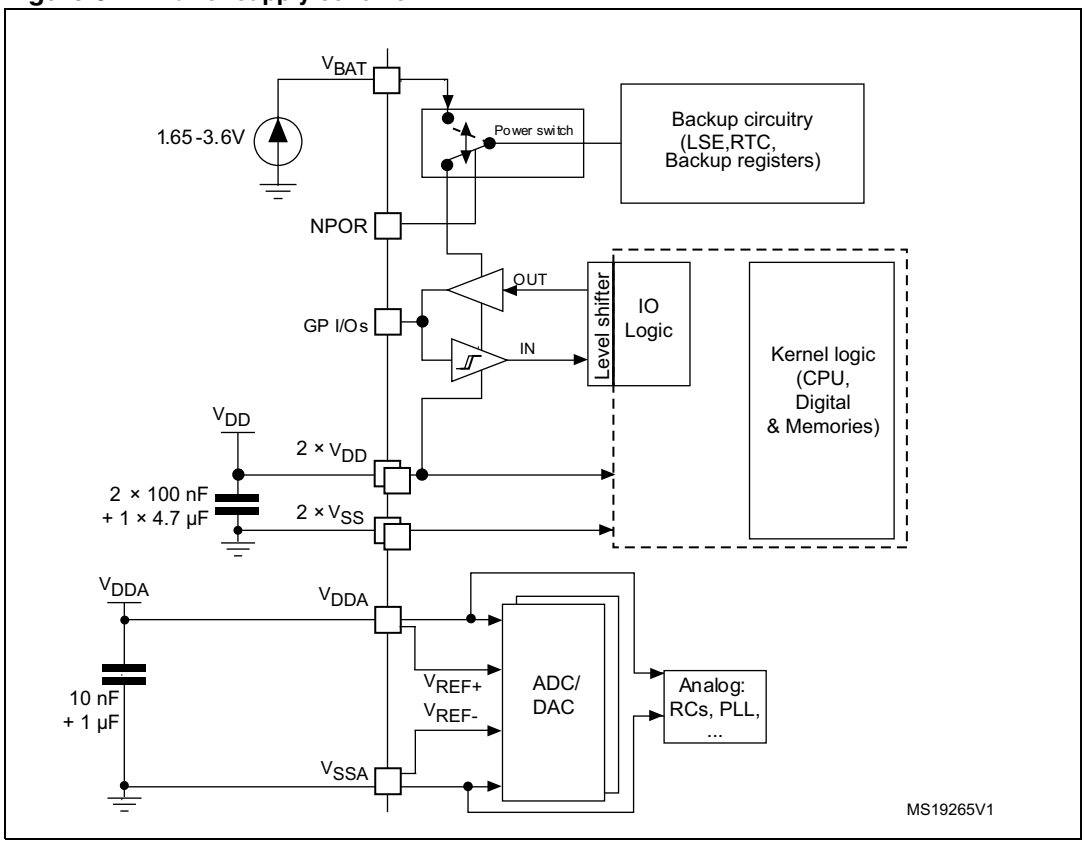
2 Power supplies of the STM32F06xxx family

2.1 Power supply schemes

There are a variety of power supply schemes:

- V_{DD} = 1.8 V +/- 8%: external power supply for I/Os.
  Provided externally through V_{DD} pins.
- V_{DDA} = 1.65 V to 3.6 V: external analog power supply for ADC/DAC, Reset blocks, HSI, HSI14, LSI and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used).
  The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, LSE 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Figure 6. Power supply scheme



2.1.1 Independent analog converter supply

To improve conversion accuracy and to extend the supply flexibility, the analog domain has an independent power supply which can be separately filtered and shielded from noise on the PCB.

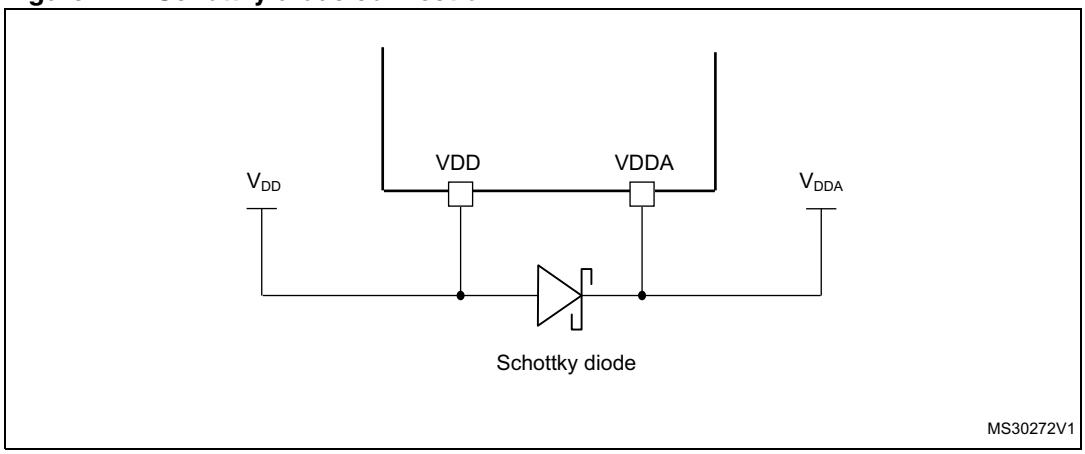
- The ADC and DAC voltage supply input is available on a separate VDDA pin.
- An isolated supply ground connection is provided on pin VSSA.

The V_{DDA} supply can be equal to or higher than V_{DD}. This allows full analog performance while still keeping V_{DD} low.

When a single supply is used, V_{DDA} must be externally connected to V_{DD},. It is recommended to use an external filtering circuit in order to ensure a noise free V_{DDA}.

When V_{DDA} is different from V_{DD}, V_{DDA} must be always higher or equal to V_{DD}. To keep safe potential difference between V_{DDA} and V_{DD} during power-up/power-down, an external Schottky diode may be used between V_{DD} and V_{DDA}. Refer to the datasheet for the maximum allowed difference.

Figure 7. Schottky diode connection



2.1.2 Battery backup

To retain the content of the Backup registers when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional standby voltage supplied by a battery or another source.

The V_{BAT} pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off.

The switch to the Vbat supply is controlled by the NPOR pin (Negative Power On Reset).

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

2.2 Reset and power supply supervisor

2.2.1 External power-on reset and power-down reset (NPOR)

To guarantee a proper power-on and power-down reset to the device, the NPOR pin must be held low until V_{DD} is stable or before turning off the supply. When V_{DD} is stable, the reset state can be exited by putting the NPOR pin in high impedance. The NPOR pin has an internal pull-up connected to VDDA.

2.2.2 System reset

A system reset sets all registers to their reset values, except the reset flags in the clock controller CSR register and the registers in the Backup domain. A system reset is generated when one of the following events occurs:

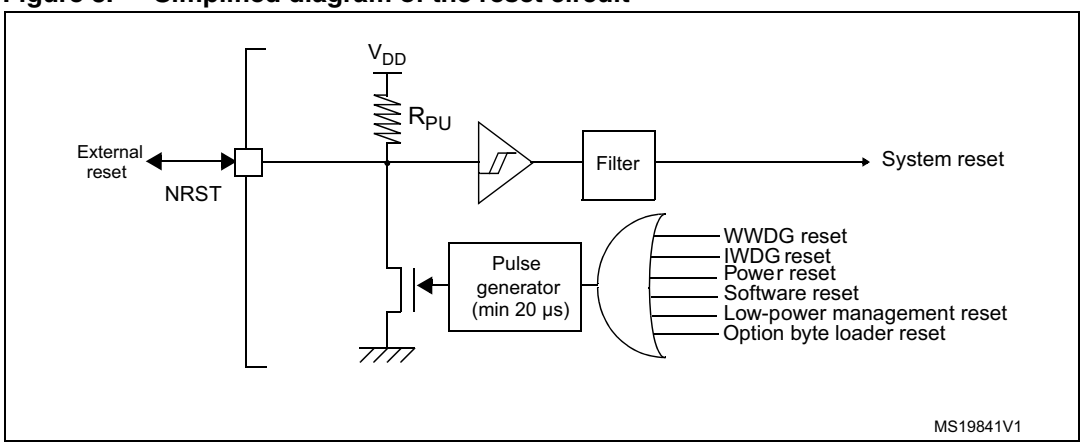
1. A low level on the NRST pin (external reset).
2. System window watchdog event (WWDG reset).
3. Independent watchdog event (IWDG reset).
4. A software reset (SW reset).
5. Low-power management reset.
6. Option byte loader reset.
7. Power reset

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In the case of an external reset, the reset is generated while the NRST pin is asserted low.

Figure 8. Simplified diagram of the reset circuit



Software reset

The SYSRESETREQ bit in Cortex-M0 Application Interrupt and Reset Control Register must be set to force a software reset on the device. Refer to the *ARMv6-M Architecture Reference Manual* for more details.

Low-power management reset

A low-power management reset can be generated by entering Stop mode. This type of reset is enabled by resetting nRST_STOP bit in User Option Bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.

Option byte loader reset

The option byte loader reset is generated when OBL_LAUNCH (bit 13) is set in the FLASH_CR register. This bit launches the option byte loading by software.

Power reset

A power reset sets all registers to their reset values, except the backup domain. It is generated while the NPOR pin is low. For more information concerning NPOR, you must refer to *Section 2.2.1: External power-on reset and power-down reset (NPOR)*.

Backup domain reset

A backup domain reset only affects the backup domain. It is generated when one of the following events occurs.

1. Software reset, triggered by setting the BDRST bit in the Backup domain control register (RCC_BDCR).
2. VDD power-up if VBAT has been disconnected when it was low.
3. RTC tamper detection event.
4. Change of the read out protection from level 1 to level 0.

3 Clocks

Three different clock sources can be used to drive the system clock (SYSCLK):

- HSI 8 MHz RC oscillator clock (high-speed internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL clock

The devices have other secondary clock sources:

- 40 kHz low-speed internal RC (LSI RC) that drives the independent watchdog and, optionally, the RTC used for Auto-wakeup from the Stop/Standby modes.
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the RTC
- HSI 14MHz RC oscillator (HSI14) dedicated for ADC

Each clock source can be switched on or off independently when it is not used, to optimize the power consumption. Refer to the STM32F0xxx reference manual (RM0091) for a description of the clock tree.

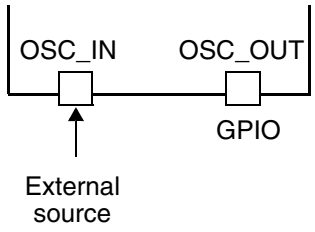
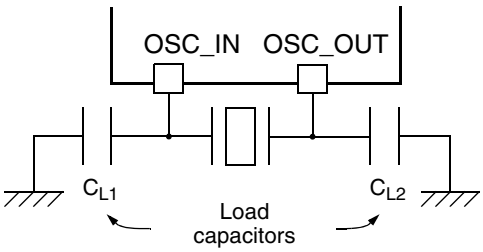
3.1 High speed external clock signal (HSE) OSC clock

The high speed external clock signal can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 9. HSE/ LSE clock sources

Clock source	Hardware configuration
External clock	
Crystal/Ceramic resonators	

External crystal/ceramic resonator (HSE crystal)

The 4 to 32 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. Refer to the electrical characteristics section of the *datasheet* for more details about the associated hardware configuration.

The HSERDY flag in the Clock control register (RCC_CR) indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock interrupt register (RCC_CIR).

The HSE Crystal can be switched on and off using the HSEON bit in the Clock control register (RCC_CR).

External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 32 MHz. You select this mode by setting the HSEBYP and HSEON bits in the *Clock control register (RCC_CR)*. The external clock signal (square, sinus or triangle) with ~40-60% duty cycle depending on the frequency (refer to the datasheet) has to drive the OSC_IN pin while the OSC_OUT pin can be used a GPIO. See *Figure 9*.

3.2 LSE clock

The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in Backup domain control register (RCC_BDCR). The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the Backup domain control register (RCC_BDCR) to obtain the best compromise between robustness and short start-up time on one side and low power-consumption on the other.

The LSERDY flag in the Backup domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock interrupt register (RCC_CIR).

External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. You select this mode by setting the LSEBYP and LSEON bits in the Backup domain control register (RCC_BDCR). The external clock signal (square, sinus or triangle) has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See *Figure 9*.

3.3 HSI clock

The HSI clock signal is generated from an internal 8 MHz RC oscillator and can be used directly as a system clock or divided by 2 to be used as PLL input. The HSI RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator.

Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations, This is why each device is factory calibrated by ST for 1% accuracy at T_A=25°C.

Furthermore, it is possible to route the HSI clock to the MCO multiplexer. The clock can then be input to Timer 14 to allow the user to calibrate the oscillator.

3.4 LSI clock

The LSI RC acts as an low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC. The clock frequency is around 40 kHz (between 30 kHz and 60 kHz). For more details, refer to the electrical characteristics section of the datasheets.

3.5 ADC clock

The ADC clock is either the dedicated 14 MHz RC oscillator (HSI14) or PCLK divided by 2 or 4. When the ADC clock is derived from PCLK, it is in an opposite phase with PCLK. The 14 MHz RC oscillator can be configured by software either to be turned on/off ("auto-off mode") by the ADC interface or to be always enabled.

3.6 Clock security system (CSS)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

- If a failure is detected on the HSE oscillator clock, the oscillator is automatically disabled.
  - A clock failure event is sent to the break inputs of TIM1 advanced control timer and TIM15, TIM16 and TIM17 general purpose timers.
  - An interrupt is generated to inform the software about the failure (clock security system interrupt CSSI), allowing the MCU to perform recovery operations.
  - CSSI is linked to the Cortex™-M0 NMI (non-maskable interrupt) exception vector.
- If the HSE oscillator is used directly or indirectly as the system clock (indirectly means that it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If the HSE oscillator clock (divided or not) is the clock entry of the PLL that is being used as a system clock when the failure occurs, the PLL is disabled too.

For details, see the STM32F0xxx (RM0091) reference manual available from the STMicroelectronics website *www.st.com*.

4 Boot configuration

In the STM32F0xxx, three different boot modes can be selected through the BOOT0 pin and nBOOT1 option bit, as shown in *Table 2*.

Table 2. Boot modes

Boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

The values of both BOOT0 pin and nBOOT1 bit are latched on the 4th rising edge of SYSCLK after a reset. The user must set nBOOT1 and BOOT0 to select the required boot mode.

The BOOT0 pin and nBOOT1 bit are also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode. After the startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from System memory: the system memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x1FFF EC00).
- Boot from embedded SRAM: the SRAM is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x2000 0000).

Embedded boot loader

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART1 (PA9/PA10)
- USART2 (PA14/PA15)

For additional information, refer to application note AN2606.

5 Debug management

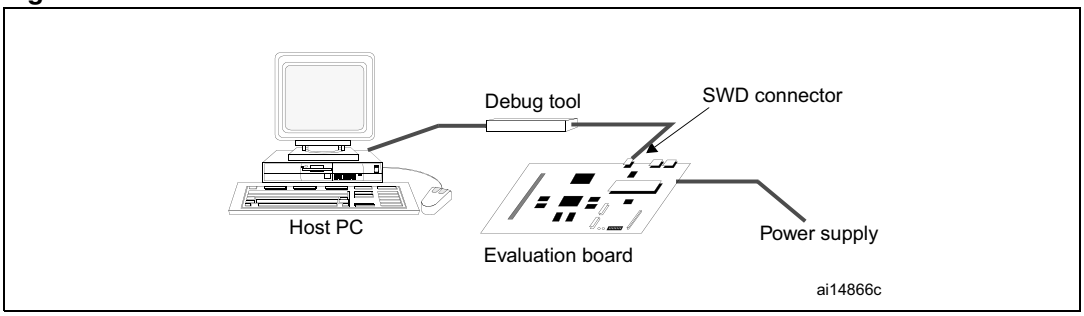
5.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, an SWD connector and a cable connecting the host to the debug tool.

Figure 10 shows the connection of the host to the evaluation board (STM320518_EVAL).

The STM320518_EVAL evaluation board embeds the debug tools (ST-LINK). Consequently, it can be directly connected to the PC through a USB cable.

Figure 10. Host-to-board connection



5.2 SWD port (serial wire debug)

The STM32F0xxx core integrates the serial wire debug port (SW-DP). It is an ARM® standard CoreSight™ debug port with a 2-pin (clock + data) interface to the debug access port.

5.3 Pinout and debug port pins

The STM32F0xxx MCU is offered in various packages with varying numbers of available pins.

5.3.1 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32F0 packages.

Table 3. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

5.3.2 SWD pin assignment

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the RM0091 section on I/O pin alternate function multiplexer and mapping.

5.3.3 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

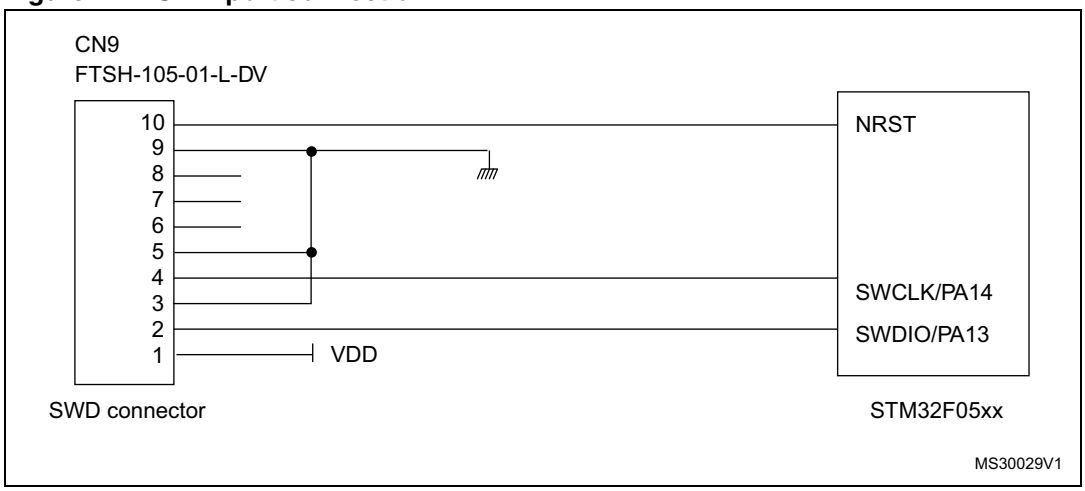
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

5.3.4 SWD port connection with standard SWD connector

Figure 11 shows the connection between the STM32F0xxx and a standard SWD connector.

Figure 11. SWD port connection



6 Recommendations

6.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

6.2 Component position

A preliminary layout of the PCB must make separate circuits:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This will reduce cross-coupling on the PCB that introduces noise.

6.3 Ground and power supply (V_{SS}, V_{DD}, V_{DDA})

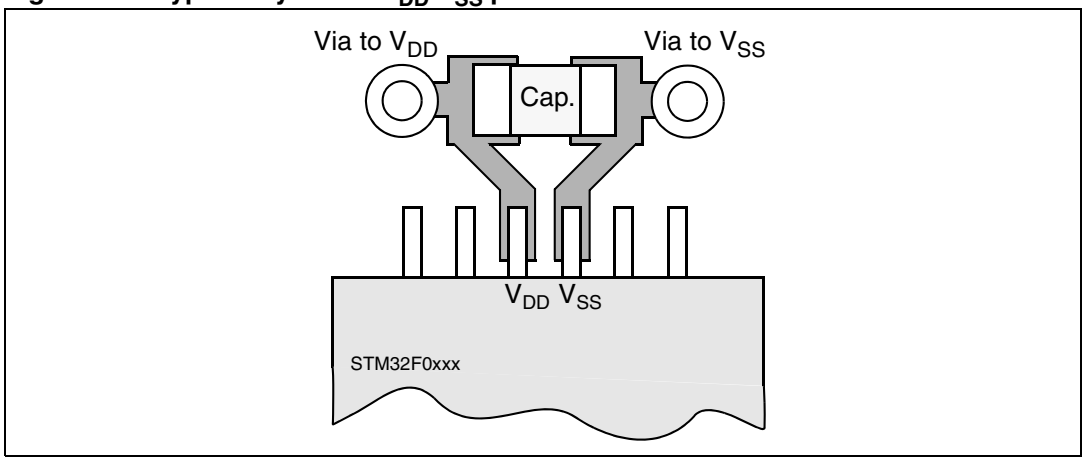
Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or have a minimum area. In order to improve analog performance, you must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device. The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

6.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with 100nF filtering ceramic capacitor and a chemical capacitor of about 4.7 µF connected between the supply pins of the STM32F0xxx device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. *Figure 12* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 12. Typical layout for V_{DD}/V_{SS} pair



6.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals, but not LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
- Digital signals: the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (clock, etc.)
- Sensitive signals (high impedance, etc.)

6.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.

7 Reference design

7.1 Description

The reference design shown in *Figure 13*, introduces the STM32F051, a highly integrated microcontroller running at 48 MHz, that combines the Cortex™-M0 32-bit RISC CPU core with 64 Kbytes of embedded Flash memory and 8 Kbytes of SRAM.

For the STM32F061 reference designs, refer to *Figure 14*. These reference designs can be tailored to any other STM32F05xx or STM32F06xx device with a different package, using the pin correspondence given in the corresponding datasheet.

7.1.1 Clock

Two clock sources are used for the microcontroller:

- HSE: X1– 8 MHz crystal for the STM32F0xxx microcontroller
- LSE: X2– 32.768 kHz crystal for the embedded RTC

Refer to *Section 3: Clocks on page 15*.

7.1.2 Reset

The reset signal in *Figure 13* or *Figure 14* is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to *Section 1.2.2: System reset on page 8* or *Section 2.2.2: System reset on page 13*

7.1.3 STM32F06xxx power-on reset

The power-on reset signal is active low. It is maintained to V_{DDA} through an integrated pull-up resistor. This signal must be provided by the user regulator.

Refer to *Section 2.2.1: External power-on reset and power-down reset (NPOR) on page 13*.

7.1.4 Boot mode

The boot option is configured by setting BOOT0 through switch SW1 and option bit nBOOT1. Refer to *Section 4: Boot configuration on page 18*.

7.1.5 SWD interface

The reference design shows the connection between the STM32F0xxx and a standard SWD connector. Refer to *Section 5: Debug management on page 19*.

Note: It is recommended to connect the reset pin in order to be able to reset the application from the tool.

7.1.6 Power supply

Refer to *Section 1: Power supplies of the STM32F05xxx family on page 4* or *Section 2: Power supplies of the STM32F06xxx family on page 11* depending on your configuration.

7.1.7 Pinouts and pin description

Please refer to the STM32F0 datasheets available on www.st.com for the pinout information and pin description of each device.

7.2 Component references

Table 4. Mandatory components

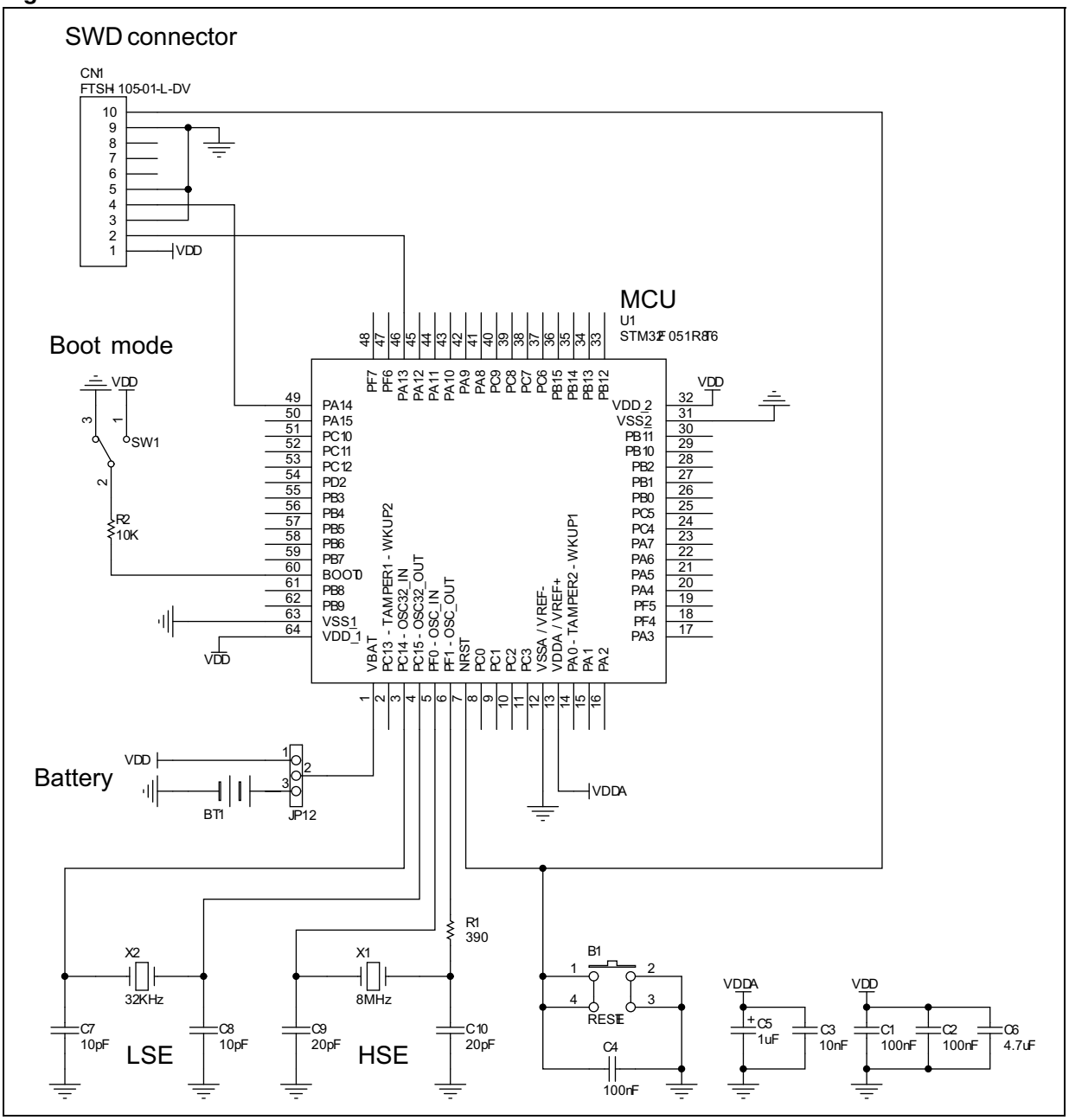
Component	Reference	Value	Quantity	Comments
Microcontroller	U1 or U2	STM32F051R8 or STM32F061R8	1	64-pin package
Capacitor	C1/C2	100 nF	2	Ceramic capacitors (decoupling capacitors)
Capacitor	C3	10 nF	1	Ceramic capacitor (decoupling capacitor)

Note: Depending on the microcontroller used, refer to the corresponding reference schematics.

Table 5. Optional components

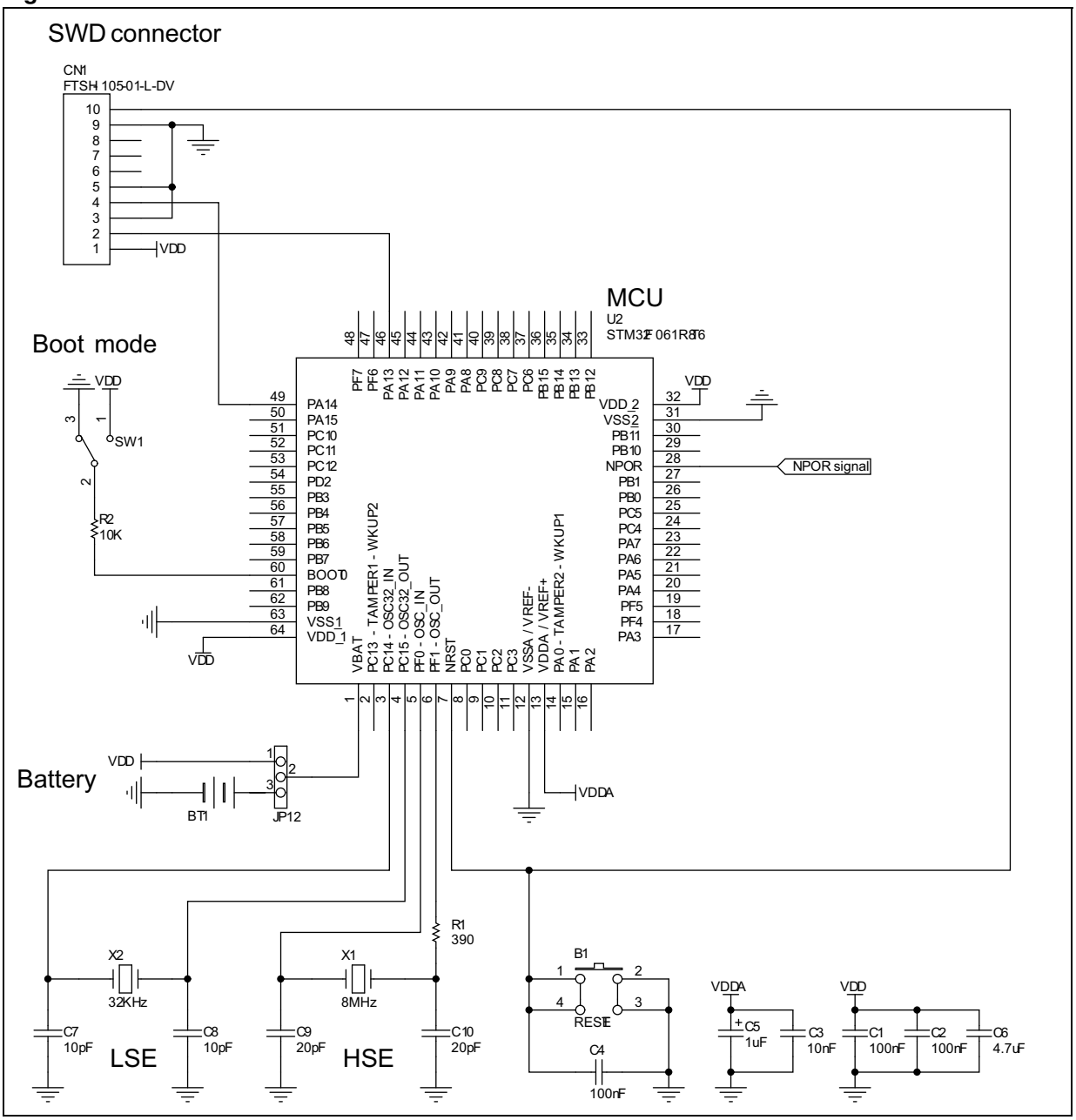
Component	Reference	Value	Quantity	Comments
Resistor	R1	390 Ω	1	Used for HSE: the value depends on the crystal characteristics. This value is given only as a typical example.
Resistor	R2	10 KΩ	1	Used for BOOT0 pin
Capacitor	C4	100 nF	1	Ceramic capacitor for RESET button
Capacitor	C5	1 µF	1	Used for VDDA
Capacitor	C6	4.7 µF	1	Used for VDD
Capacitor	C7/C8	10 pF	2	Used for LSE: the value depends on the crystal characteristics.
Capacitor	C9/C10	20 pF	2	Used for HSE: the value depends on the crystal characteristics.
Quartz	X1	8 MHz	1	Used for HSE
Quartz	X2	32 kHz	1	Used for LSE
Battery	BT1	3V	1	If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}
Switch	SW1		1	Used to select the correct boot mode.
Push-button	B1		1	Used as reset button
SWD connector	CN1	FTSH-105-01-L-DV	1	Used for program/debug of the MCU

Figure 13. STM32F051R8 microcontroller reference schematic



Note: If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

Figure 14. STM32F061R8 microcontroller reference schematic



Note: If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

8 Hardware migration from STM32F1 to STM32F0

The entry-level STM32F0 and general-purpose STM32F1xxx families are pin-to-pin compatible. All peripherals shares the same pins in the two families, but there are some minor differences between packages.

The transition from the STM32F1 series to the STM32F0 series is simple as only a few pins are impacted (impacted pins are in bold in *Table 6*).

Table 6. STM32F1 series and STM32F0 series pinout differences

STM32F1 series			STM32F0 series			
QFP48	**QFP64**	**Pinout**	**QFP48**	**QFP64**	**Pinout STM32F05xxx**	**Pinout STM32F06xxx**
5	5	**PD0** - OSC_IN	5	5	**PF0** - OSC_IN	**PF0** - OSC_IN
6	6	**PD1** - OSC_OUT	6	6	**PF1** - OSC_OUT	**PF1** - OSC_OUT
-	18	**VSS_4**	-	18	**PF4**	**PF4**
-	19	**VDD_4**	-	19	**PF5**	**PF5**
35	47	**VSS_2**	35	47	**PF6**	**PF6**
36	48	**VDD_2**	36	48	**PF7**	**PF7**
20	28	**BOOT1**/PB2	20	28	PB2	NPOR

The migration from F1 to F0 has no impact on the pinout, except that the user wins 2 or 4 GPIOs for his/her application at VSS/VDD 2 and 4 locations, depending on the package used.

9 Revision history

Table 7. Document revision history

Date	Revision	Changes
11-Jul-2012	1	Initial release.
11-Feb-2013	2	Added *Chapter 2: Power supplies of the STM32F06xxx family*. Modified *Chapter 7: Reference design*. Modified *Table 6: STM32F1 series and STM32F0 series pinout differences*.

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