AN4235
Application note

I2C timing configuration tool for STM32F3xxxx and STM32F0xxxx microcontrollers

Introduction

This application note presents the I2C timing configuration tool (STSW-STM32126) for the STM32F3xxxx and STM32F0xxxx microcontroller families.

The STM32F0xxxx and STM32F3xxxx devices embed an Inter-Integrated Circuit communication peripheral (I2C) supporting standard mode (100 KHz), fast mode (400 KHz) and fast mode plus (1 MHz). The I2C implements a new clock scheme allowing the peripheral to be used as a wake-up source from low-power mode on address match.

The purpose of this tool is to help the user configure the I2C timings, taking into consideration the I2C bus specification.

The configuration tool is implemented in the Microsoft Excel *"I2C_Timing_Config_Tool_Vx.y.z.xls"* file which can be downloaded from *www.st.com*.

For Vx.y.z, please refer to the tool version, for example: V1.0.0.

Before using the clock tool, it is essential to read the STM32 microcontroller reference manuals (RM0313 for STM32F37xxx products, RM0316 for STM32F30xxx products and RM0091 for STM32F0xxxx products). This application note is not a substitute for the reference manuals.

Contents

List of tables

List of figures

1 Glossary

Table 1. Definition of terms

Term	Description
AF	Analog filter
DNF	Digital noise filter
HSI	High-speed internal clock
I2C	Inter-Integrated Circuit
I2CCLK	I2C kernel clock
PCLK	APBx clock
PRESC	Prescaler
SCL	Serial clock line
SDA	Serial data line
SYSCLK	System clock

2 Getting started

This section describes the requirements and procedures needed to start using the timing configuration tool.

2.1 Software requirements

To use the timing configuration tool with Windows operating system, a recent version of Windows, such as Windows XP, Vista or Windows 7, must be installed on the PC with at least 256 Mbytes of RAM.

Before starting to use the timing configuration tool, make sure that Microsoft Office is installed on your machine and then follow these steps:

- Download the latest version of the **I2C timing configuration tool** for the STM32 devices from *www.st.com*.
- Enable macros and ActiveX controls as shown below:

Excel 1997-2003 version

1. Click **Tools** in the menu bar.
2. Click **Macro**.
3. Click **Security**.
4. Click **Low (not recommended)**.

Note: If ActiveX controls are not enabled, a warning message is displayed asking you to enable ActiveX. In this case, you should click "OK" to enable it.

Excel 2007-2010 version

1. Click the **Microsoft Office** button and then click **Excel options**.
2. Click **Trust Center**, click **Trust center settings**, and then click **Macro settings**.
3. Click **Enable all macros (not recommended, potentially dangerous code can run)**.
4. Click **Trust Center**, click **Trust center settings**, and then click **ActiveX settings**.
5. Click **Enable all controls without restrictions and without prompting (not recommended; potentiality dangerous controls can run)**.
6. Click **OK**.

Note: For more information about how to enable macros and ActiveX controls, refer to the Microsoft Office website.

2.2 Hardware requirements

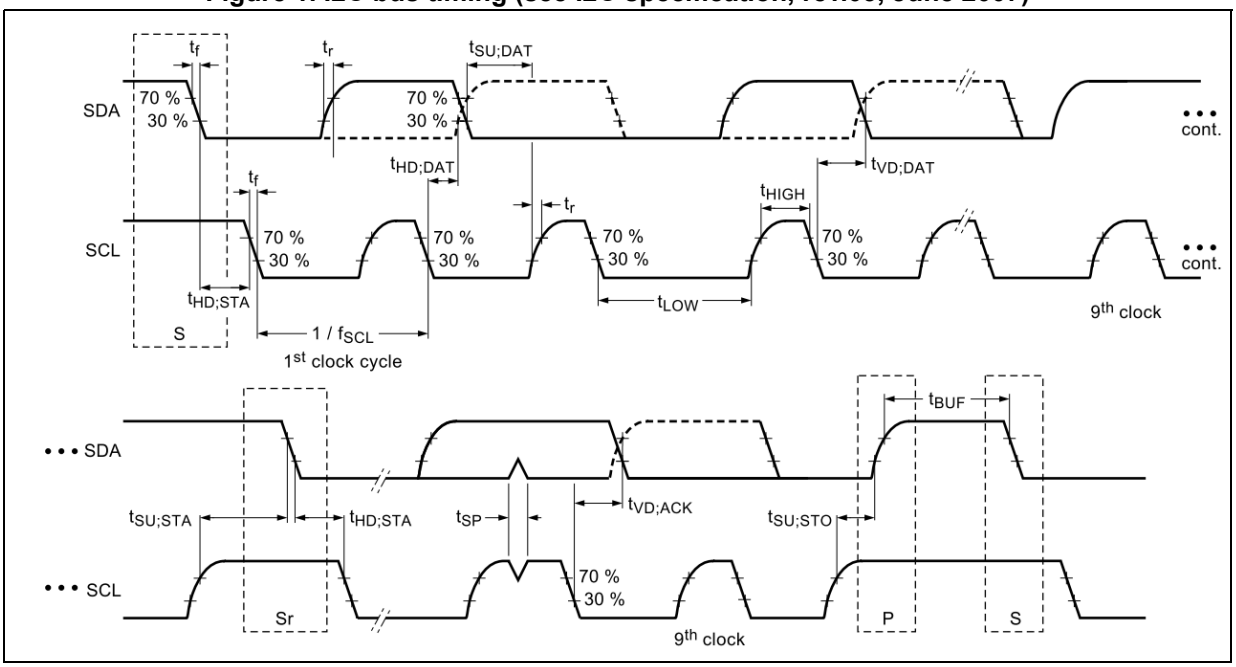
2.2.1 Introduction

The I2C timing configuration tool is designed to help the end-user easily configure the timing settings for the I2C peripheral and guarantee its operation as specified in the I2C timing specification.

2.2.2 I2C timing specification

The I2C timings should be configured with values that are compliant with the I2C bus specification:

Figure 1. I2C bus timing (see I2C specification, rev.03, June 2007)



The table below shows the value range of these timings:

Table 2. I2C timings specification (see I2C specification, rev.03, June 2007)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	µs
t_r	Rise time of both SDA and SCL signals	-	1000	20 + 0.1Cb(1)	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	-	300	20 + 0.1Cb(1)	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD:STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs

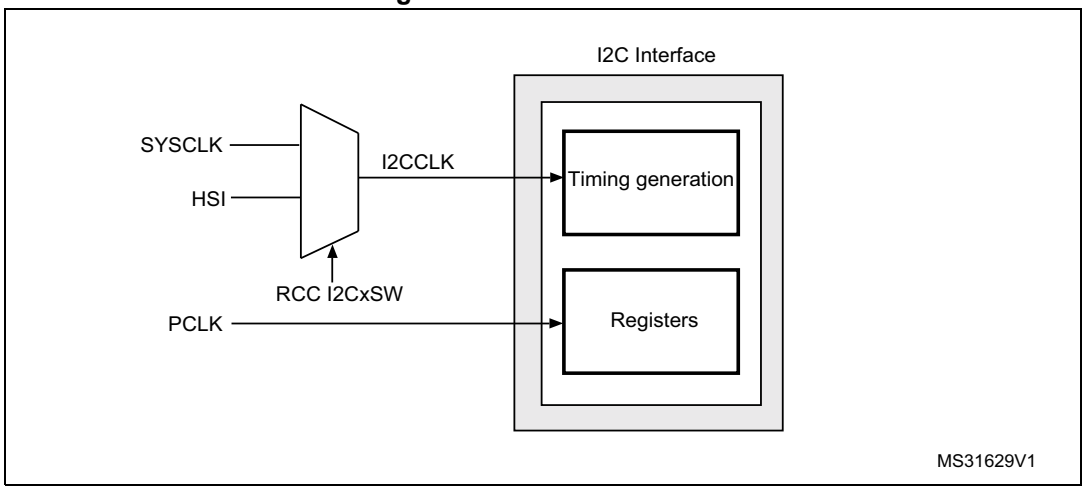
1. Cb = total capacitance of one bus line in pF.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

2.2.3 I2C clock scheme

The I2C kernel is clocked by an independent clock source. The clock source can be:

- HSI (default source)
- SYSCLK

Figure 2. I2C clock scheme



These two clocks allow I2C to operate independently from the PCLK frequency.

Setting HSI as I2C clock source frequency allows the use of wake-up from STOP mode capability at address match.

The I2CCLK period t_{I2CCLK} must respect the following conditions:

$t_{I2CCLK} < (t_{LOW} - t_{filters}) / 4$ and $t_{I2CCLK} < t_{HIGH}$

$t_{filters}$: when enabled, sum of the delays brought by the analog filter and the digital filter.

Analog filter delay is maximum 260 ns and digital filter delay is DNF x t_{I2CCLK}.

The PCLK clock period t_{PCLK} must respect the following condition:

$t_{PCLK} < 4/3\ t_{SCL}$

Please refer to the RCC section in STM32 product reference manual for more details about the selection of the I2C clock source.

2.2.4 I2C timing register

The I2C timing register is defined as the following table shows:

Table 3. Timing register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRESC[3:0]				Res.	Res.	Res.	Res.	SCLDEL[3:0]				SDADEL[3:0]			
rw								rw				rw			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLH[7:0]								SCLL[7:0]							
rw								rw							

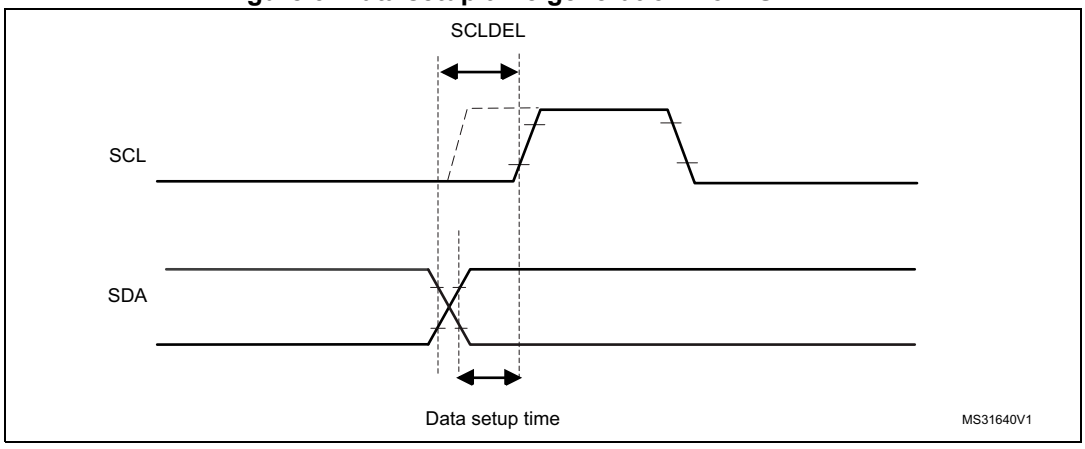
PRESC[3:0] is used to prescale I2C clock source (I2CCLK); it allows the generation of a divided clock. The period of this divided clock $t_{PRESC}$is defined by:

t_{PRESC} = (PRESC+1) x t_{I2CCLK}

The time unit t_{PRESC} is used for the generation of other I2C timings.

SCLDEL[3:0] is used to program the data setup time ($t_{SU;DAT}$) as shown in the following figure:

Figure 3. Data setup time generation from SCLDEL

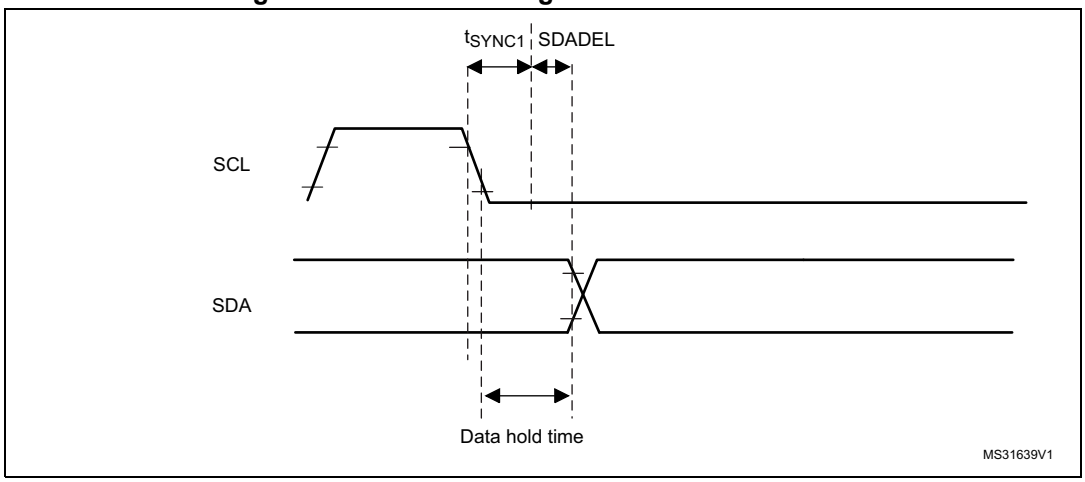


SCLDEL is defined as follows:

{[t_r+ $t_{SU;DAT(min)}$] / [t_{PRESC}]} - 1 <= SCLDEL

SDADEL[3:0] is used to program the data hold time ($t_{HD;DAT}$) as shown in the following figure:

Figure 4. Data hold time generation from SDADEL



t_{SYNC1} duration depends on these parameters:

- SCL falling time
- When enabled, input delay brought by the analog filter: 0.05 µs < t_{AF} < 0.26 µs
- When enabled, input delay brought by the digital filter: t_{DNF} = DNF x t_{I2CCLK}
- Delay due to SCL synchronization to I2CCLK clock (2 to 3 I2CCLK periods)

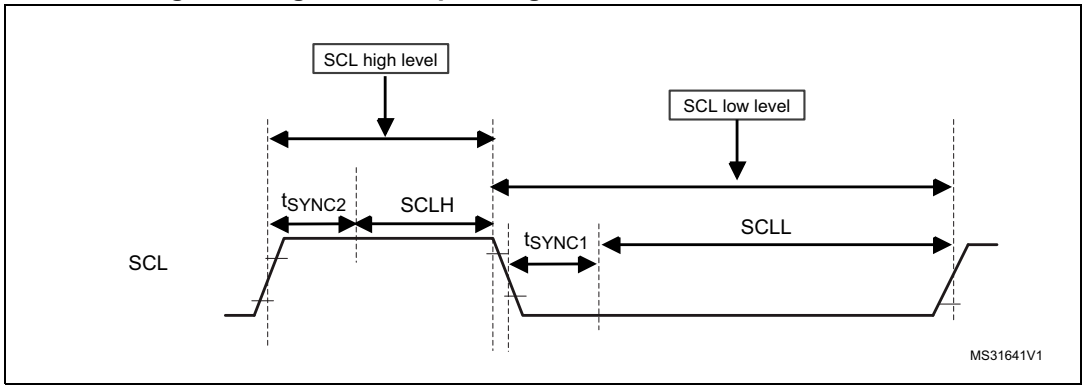
SDADEL is defined by:

SDADEL >= {t_f +$t_{HD;DAT(min)}$ - $t_{AF(min)}$ - t_{DNF} - [3 x t_{I2CCLK}]} / {t_{PRESC}}

SDADEL <= {$t_{VD;DAT(max)}$ - t_r - $t_{AF(max)}$ - t_{DNF}- [4 x t_{I2CCLK}]} / {t_{PRESC}}

SCLH[7:0] and SCLL[7:0] are used to configure I2C speed frequency when master mode is selected. SCLH generates the high period of the SCL clock (t_{HIGH}) and SCLL generates the low period of the SCL clock (t_{LOW}). The figure below shows how these timings are deduced:

Figure 5. High and low period generation from SCLH and SCLL



t_{SYNC2} duration depends on these parameters:

- SCL rising time
- When enabled, input delay brought by the analog filter: 0.05 µs < t_{AF} < 0.26 µs
- When enabled, input delay brought by the digital filter: t_{DNF} = DNF x t_{I2CCLK}
- Delay due to SCL synchronization to I2CCLK clock (2 to 3 I2CCLK periods)

SCL clock period (t_{SCL}) which defines I2C speed frequency (f_{SCL}= 1/t_{SCL}) is defined by:

$t_{SCL} = t_f + t_{LOW} + t_r + t_{HIGH}$

SCLH and SCLL are defined as follows:

$t_{HIGH(min)} <= t_{AF(min)} + t_{DNF} + 2 \times t_{I2CCLK} + [(SCLH+1) \times t_{PRESC}]$

$t_{LOW(min)} <= t_{AF(min)} + t_{DNF} + 2 \times t_{I2CCLK} + [(SCLL+1) \times t_{PRESC}]$

Note: SCLH and SCLL values depend on the rise and fall time.

The rise time is defined by:

$t_r = R_p \times C_b \times 0.8473$ (R_p is the pull_up resistor and C_b is the bus capacitance)

The fall time depends on the software configuration of the I/O. Please refer to "I/O AC characteristics" table in STM32 products datasheets to get the value of fall time.