STM32F072xx Errata sheet

STM32F072xx device limitations

Silicon identification

This errata sheet applies to revisions ‘Z’, ‘B’ and ‘Y’ of the STMicroelectronics STM32F072xx products. The STM32F072xx family features an ARM® 32-bit Cortex®-M0 core.

Section 1 gives a detailed description of the product silicon limitations.

The full list of part numbers is shown in *Table 2*. The products are identifiable by the revision code marked below the order code on the device package, as shown in *Table 1*.

Table 1. Device identification(1)

Sales type	Revision code marked on the device(2)
STM32F072xx	‘Z’, ‘B’, ‘Y’

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the reference manual (RM0091) for details on how to find the revision code).
2. Refer to *Appendix A: Revision code on device marking* for details on how to identify the revision code according to the packages.

Table 2. Device summary

Part number	Part number
STM32F072x8	STM32F072V8, STM32F072C8, STM32F072R8
STM32F072xB	STM32F072VB, STM32F072CB, STM32F072RB

Contents

1 STM32F072xx silicon limitations

Table 3 gives quick references to all documented limitations.

Legend for *Table 3*: A = workaround available; N = no workaround available; P = partial workaround available, '-' and grayed = fixed.

Table 3. Summary of silicon limitations

Section	Limitation	Rev Z	Rev B	Rev Y
Section 1.1: System limitations	*Section 1.1.1: Wakeup sequence from Standby mode when using more than one wakeup source*	A	A	A
	Section 1.1.2: Over-consumption with regulator in Low power mode	N	-	-
	Section 1.1.3: ESD performance lower than expected	N	-	-
Section 1.2: USART peripheral limitation	*Section 1.2.1: Last byte written in TDR might not be transmitted if TE is cleared just after writing in TDR*	A	A	A
	Section 1.2.2: USART4 transmission does not work on PC11	A	A	A
Section 1.3: GPIO peripheral limitations	*Section 1.3.1: Extra consumption on GPIOs PC0..5 on 48/49 pin packages*	-	-	-
	Section 1.3.2: Input filter used when AF selected on PB9, PB10, PB14	P	P	-
	Section 1.3.3: GPIOx locking mechanism not working properly for GPIOx_OTYPER register	P	P	P
Section 1.4: SPI/I^2S limitation	*Section 1.4.1: In I^2S slave mode: WS level must be set by the external master when enabling the I^2S*	A	A	A
Section 1.5: I^2C peripheral limitations	*Section 1.5.1: 10-bit slave mode: wrong direction bit value after Read header reception*	A	A	A
	Section 1.5.2: 10-bit combined with 7-bit slave mode: ADDCODE may indicate wrong slave address detection	N	N	N
	Section 1.5.3: Wakeup frames may not wakeup the MCU mode when STOP mode entry follows I^2C enabling	A	A	A
	Section 1.5.4: Wakeup frame may not wakeup from STOP if tHD;STA is close to HSI startup time	P	P	P
	Section 1.5.5: Wrong behaviors in Stop mode when wakeup from Stop mode is disabled in I^2C	A	A	A
Section 1.6: USB peripheral limitation	*Section 1.6.1: The USB BCD electrical parameter not in line with specification*	N	-	-
	Section 1.6.2: The USB BCD functionality limited below -20°C	N	N	N

1.1 System limitations

1.1.1 Wakeup sequence from Standby mode when using more than one wakeup source

Description

The various wakeup sources are logically OR-ed in front of the rising-edge detector which generates the wakeup flag (WUF). The WUF needs to be cleared prior to Standby mode entry, otherwise the MCU wakes up immediately.

If one of the configured wakeup sources is kept high during the clearing of the WUF (by setting the CWUF bit), it may mask further wakeup events on the input of the edge detector. As a consequence, the MCU might not be able to wake up from Standby mode.

Workaround

To avoid this problem, the following sequence should be applied before entering Standby mode:

- Disable all used wakeup sources,
- Clear all related wakeup flags,
- Re-enable all used wakeup sources,
- Enter Standby mode

Note: Be aware that, when applying this workaround, if one of the wakeup sources is still kept high, the MCU will enter Standby mode but then it wakes up immediately generating a power reset.

1.1.2 Over-consumption with regulator in Low power mode

Description

Current consumption in Stop mode could be higher by approximately 15 uA for LP regulator mode than for run mode under same conditions. This is seen mainly at temperature above 85°C and with VDD > 3.2V.

Workaround

None.

This limitation is present on Revision Z only.

1.1.3 ESD performance lower than expected

Description

Device shows lower ESD performance than the other products from STM32F0 family.

Workaround

None.

This limitation is present on Revision Z only.

1.2 USART peripheral limitation

1.2.1 Last byte written in TDR might not be transmitted if TE is cleared just after writing in TDR

Description

If the USART clock source is slow (for example LSE) and TE bit is cleared immediately after the last write to TDR, the last byte will probably not be transmitted.

Workarounds

1. Wait until TXE flag is set before clearing TE bit.
2. Wait until TC flag is set before clearing TE bit.

1.2.2 USART4 transmission does not work on PC11

Description

USART4_RX does not work as output on PC11.

As a consequence, single wire half duplex mode is not supported with pin PC11.

Workaround

Use USART4_RX mapped on PA0 instead on PC11.

1.3 GPIO peripheral limitations

1.3.1 Extra consumption on GPIOs PC0..5 on 48/49 pin packages

Description

For lower pin count devices of 48 and 49 pins, some GPIOs are not available on the package. The hardware force them to safe configuration.

Software reconfiguration of PC0..5 to analog mode opens a path between V_{DDA} and V_{DDIO}. Additional current consumption in the range of tens of µA per pin can be observed if V_{DDA} is higher than V_{DDIO}.

Workaround

This limitation is not present on STM32F07x devices.

1.3.2 Input filter used when AF selected on PB9, PB10, PB14

Description

When the AF5 (SPI2/I2S2) is chosen on PB9, PB10, or the AF1 (TIM15_CH1) is chosen on PB14, input signal is routed through I^2C input filters instead or direct connection and signal is impacted by the I^2C filters.

Workaround

Deactivate analog filters on I^2C pads (I2C1 for PB9, I2C2 for PB10 and PB14) with software. However, the I^2C cannot use the filters at the same time on any other pads.

This limitation is present on Revision Z and B only.

1.3.3 GPIOx locking mechanism not working properly for GPIOx_OTYPER register

Description

Locking of GPIOx_OTYPER[i] with i = 15..8 depends from setting of GPIOx_LCKR[i-8] and not from GPIOx_LCKR[i]. GPIOx_LCKR[i-8] is locking GPIOx_OTYPER[i] together with GPIOx_OTYPER[i-8]. It is not possible to lock GPIOx_OTYPER[i] with i = 15...8, without locking also GPIOx_OTYPER[i-8].

Workaround

The only way to lock GPIOx_OTYPER[i] with i=15..8 is to lock also GPIOx_OTYPER[i-8].

1.4 SPI/I^2S limitation

1.4.1 In I^2S slave mode: WS level must be set by the external master when enabling the I^2S

Description

In slave mode, the WS signal level is used only to start the communication. If the I^2S (in slave mode) is enabled while the master is already sending the clock and the WS signal level is low (for I^2S protocol) or is high (for the LSB or MSB-justified mode), the slave starts communicating data immediately. In this case, the master and slave will be desynchronized throughout the whole communication.

Workaround

The I^2S peripheral must be enabled when the external master sets the WS line at:

- High level when the I^2S protocol is selected.
- Low level when the LSB or MSB-justified mode is selected.

1.5 I^2C peripheral limitations

1.5.1 10-bit slave mode: wrong direction bit value after Read header reception

Description

Under specific conditions, the transfer direction bit DIR (bit 16 of status register I2C_ISR) is low instead of high after reception of the 10-bit addressing Read header. Nevertheless, the

I²C operates correctly in slave transmission mode, and data can be sent using the TXIS flag.

To see the limitation, all the following conditions have to be fulfilled:

- I²C has to be configured in 10-bit addressing mode (OA1MODE is set in the I2C_OAR1 register).
- The high LSBs of the I²C slave address are equal to the 10-bit addressing Read header value (i.e. OA1[7:3] = 11110, OA1[2] = OA1[9], OA1[1] = OA1[8] and OA1[0] = 1 in the I2C_OAR1 register).
- The I²C receives the 10-bit addressing Read header (0X 1111 0XX1) after the repeated start condition to enter slave transmission mode.

As a result, the DIR bit is incorrect in slave mode under specific conditions.

Workaround

If possible, do not use these four values as 10-bit addresses in slave mode:

- OA1[9:0] = 0011110001
- OA1[9:0] = 0111110011
- OA1[9:0] = 1011110101
- OA1[9:0] = 1111110111

If one of these addresses is the I²C slave address, the DIR bit must not be used in the FW.

1.5.2 10-bit combined with 7-bit slave mode: ADDCODE may indicate wrong slave address detection

Description

Under specific conditions, the ADDCODE (Address match code) in the I2C_ISR register indicates a wrong slave address.

To see the limitation, all the following conditions have to be fulfilled:

- The I²C slave address OA1 is enabled and configured in 10-bit mode (OA1EN=1 and OA1MODE=1)
- Another 7-bit slave address is enabled and the bits 1 to 7 of the 10-bit slave address OA1 are equal to the 7-bit slave address, i.e., one of the configurations below is set:
  - OA2EN=1 and OA2MSK = 0 and OA1[7:1] = OA2[7:1]
  - OA2EN=1 and OA2MSK = 1 and OA1[7:2] = OA2[7:2]
  - OA2EN=1 and OA2MSK = 2 and OA1[7:3] = OA2[7:3]
  - OA2EN=1 and OA2MSK = 3 and OA1[7:4] = OA2[7:4]
  - OA2EN=1 and OA2MSK = 4 and OA1[7:5] = OA2[7:5]
  - OA2EN=1 and OA2MSK = 5 and OA1[7:6] = OA2[7:6]
  - OA2EN=1 and OA2MSK = 6 and OA1[7] = OA2[7]
  - OA2EN=1 and OA2MSK = 7
  - GCEN=1 and OA1[7:1] = 0b0000000
  - ALERTEN=1 and OA1[7:1] = 0b0001100
  - SMBDEN=1 and OA1[7:1] = 0b1100001
  - SMBHEN=1 and OA1[7:1] = 0b0001000
- The master starts a transfer addressed to the 10-bit slave address OA1.

As a result, after the address reception, the ADDCODE value is OA1[7:1] equal to the 7-bit slave address, instead of 0b11110 & OA1[9:8].

Workaround

None. If several slave addresses are enabled, mixing 10-bit and 7-bit addresses, the 10-bit Slave address OA1 [7:1] must not be equal to the 7-bit slave address.

1.5.3 Wakeup frames may not wakeup the MCU mode when STOP mode entry follows I²C enabling

Description

If the I²C is enabled (PE = 1) and wakeup from STOP enabled in I²C (WUPEN=1) while a transfer occurs on the I²C bus and STOP mode is entered during the same transfer while SCL=0, the I²C is not able to detect the following START condition. This means that if the I²C is addressed, it will not wake up the MCU and this address is not acknowledged.

Workaround

After enabling the I²C (PE is set to 1), wait for a temporization before entering STOP mode, to ensure that the eventual on-going frame is finished.

1.5.4 Wakeup frame may not wakeup from STOP if tHD;STA is close to HSI startup time

Description

Under specific conditions and if the START condition hold time tHD;STA duration is very close to the HSI start-up time duration, the I²C is not able to detect the address match and wake up the MCU from STOP.

To see the limitation, one of the conditions listed below has to be met:

1. Timeout detection is enabled (TIMOUTEN=1 or TEXTEN=1) and the frame before the wakeup frame is abnormally finished due to a I²C Timeout detection (TIMOUT=1).
2. The slave arbitration is lost during the frame before the wakeup frame (ARLO=1).
3. The MCU enters STOP mode while another slave is addressed, after the address phase and before the STOP condition (BUSY=1).
4. The MCU is in STOP mode and another slave is addressed before the I²C is addressed.

Note: The last conditions 2, 3 and 4 can occur only in a multi-slave network.

In STOP mode, the HSI is switched on by the I²C when a START condition is detected (SDA falling edge while SCL is high). The HSI is used to receive the address. HSI is switched off after the address reception if received address is not the I²C slave address. If one of the conditions above is met and if the SCL falling edge following the START condition occurs on the first cycle of the I2CCLK clock (HSI), the address reception is not correctly done and the address match wakeup interrupt is not generated.

Workaround

None at MCU level.

If the wakeup frame is not acknowledged by the I²C and if the master can program the duration of the START hold time: the master should decrease or increase the START condition hold time for more than one HSI period and resend the wakeup frame.

1.5.5 Wrong behaviors in Stop mode when wakeup from Stop mode is disabled in I²C

Description

When wakeup from Stop mode is disabled in I²C (WUPEN = 0) and the MCU enters Stop mode while a transfer is on going on the bus, some wrong behaviors may happen:

1. BUSY flag can be wrongly set when the MCU exits Stop mode. This prevents from initiating a transfer in master mode, as the START condition cannot be sent when BUSY is set.
2. If clock stretching is enabled (NOSTRETCH = 0), the I²C clock SCL may be stretched low by the I²C as long as the MCU is in Stop mode. This limitation may occur when the Stop mode is entered during the address phase of a transfer on the I²C bus while SCL = 0. Therefore the transfer may be stalled as long as the MCU is in Stop mode. The probability of the occurrence depends also on the timings configuration, the peripheral clock frequency and the I²C bus frequency.

These behaviors can occur in Slave mode and in Master mode in a multi-master topology.

Workaround

Disable the I²C (PE=0) before entering Stop mode and re-enable it in Run mode.

1.6 USB peripheral limitation

1.6.1 The USB BCD electrical parameter not in line with specification

Description

USB BCD in Primary and Secondary detection mode can have under some conditions the regulated voltage threshold level smaller than the minimum specified.

This parameter deviation is a limitation to use the BCD, but only when connected to a CDP port in one specific configuration.

Workaround

None.

This limitation is present on Revision Z only.

1.6.2 The USB BCD functionality limited below -20°C

Description

Primary and secondary detection can return an incorrectly detected port type.

This limitation may be observed on a small number of devices when the temperature is below -20°C.

Workaround

None.

Appendix A Revision code on device marking

The following figures show the standard marking compositions for the LQFP100, LQFP64, LQFP48, UFQFPN48 and WLCSP49 packages, respectively. Only the Additional information field containing the revision code is shown.

Figure 1. LQFP100 package top view

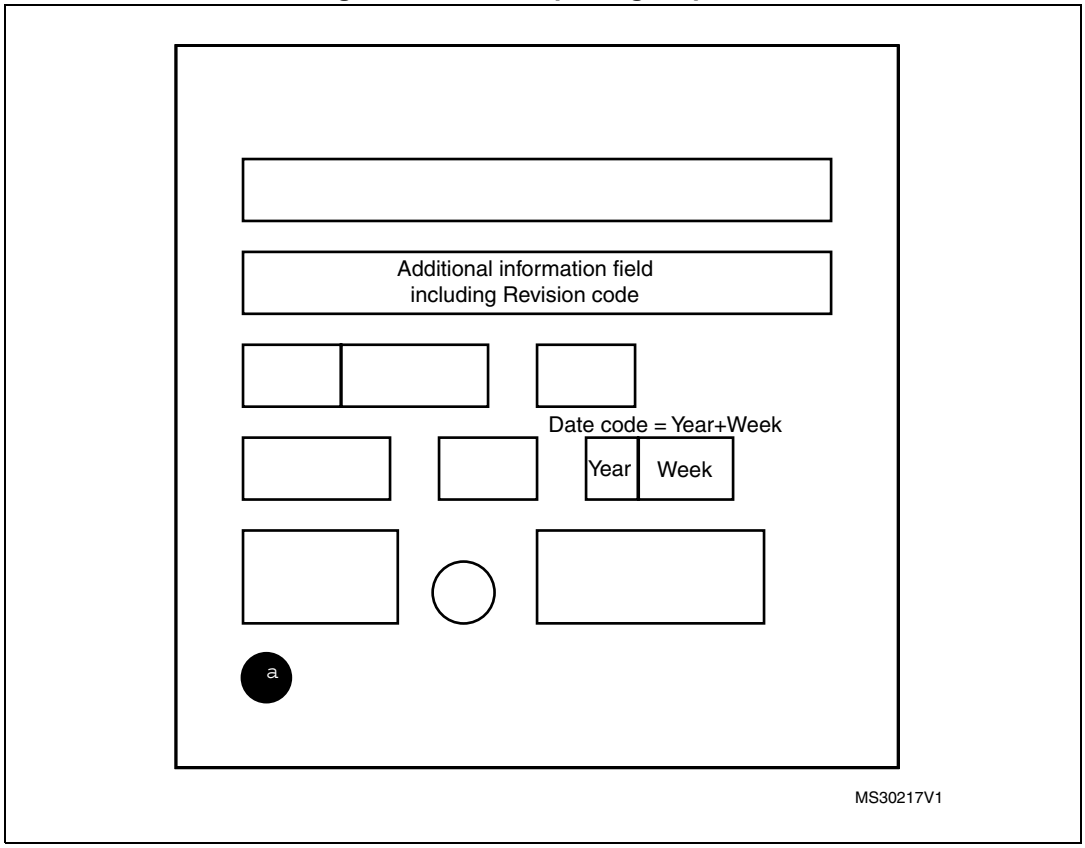


Figure 2. LQFP64 package top view

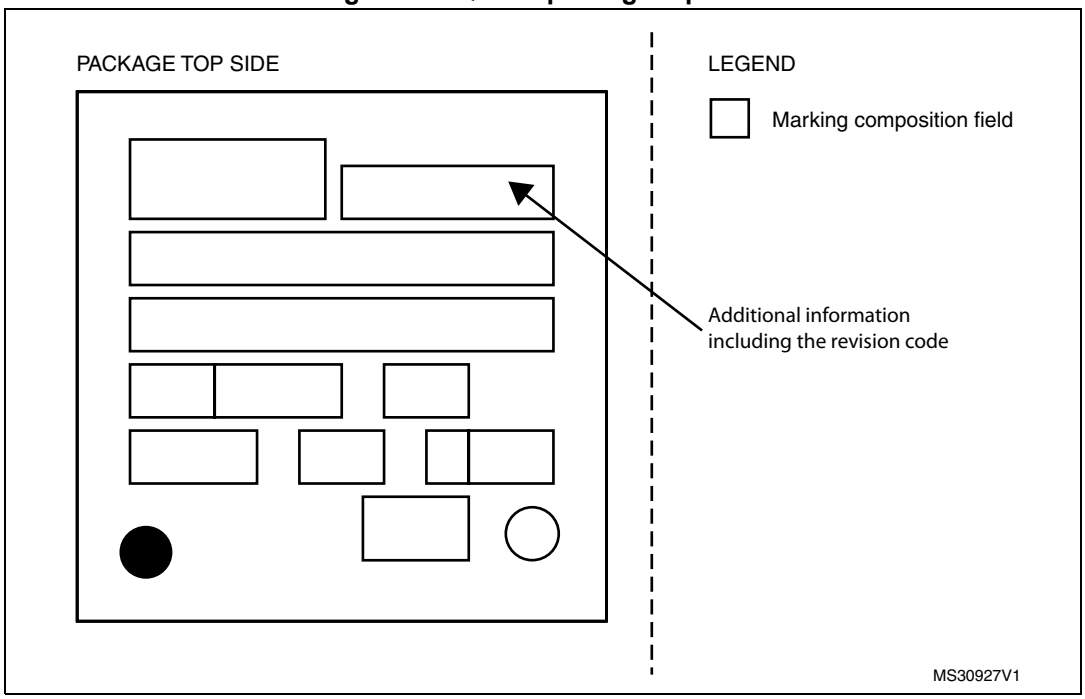


Figure 3. LQFP48 and UFQFPN48 package top view

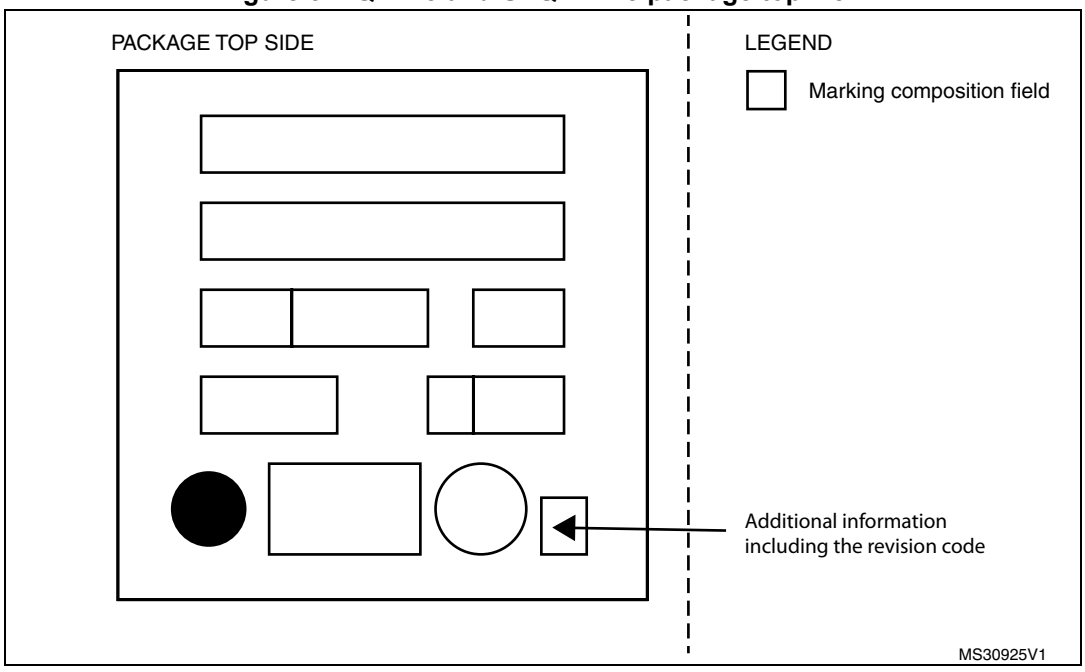
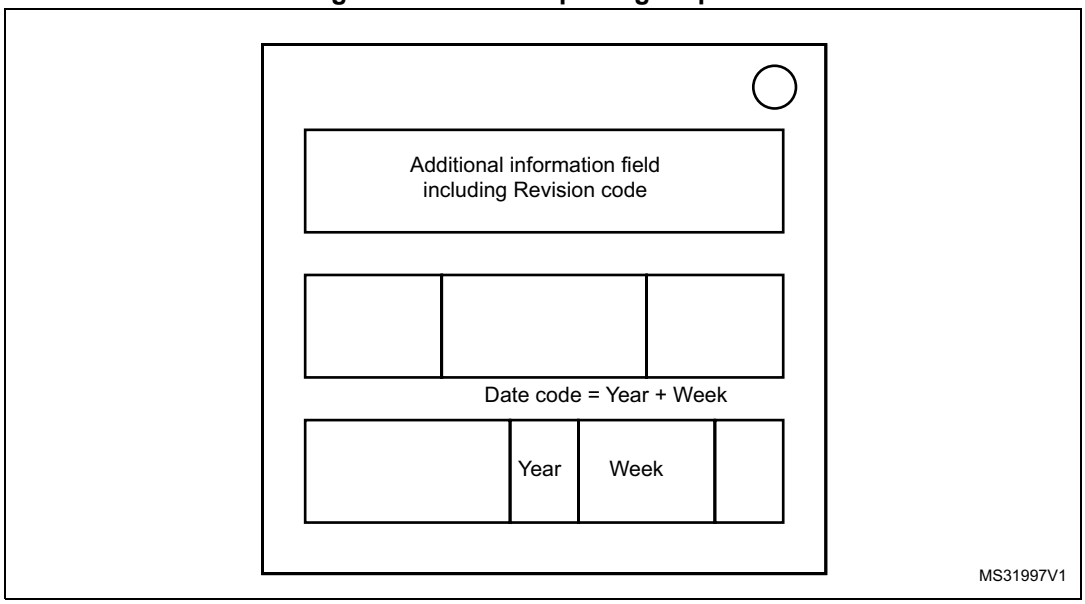


Figure 4. WLCSP49 package top view



Revision history

Table 4. Document revision history

Date	Revision	Changes
12-Nov-2013	1	Initial release.
13-Jan-2014	2	Added revision 'Y' in *Table 2* and *Table 3* Added *Section 1.6.2: The USB BCD functionality limited below -20°C*
04-Apr-2014	3	Fixed *Section 1.3.1: Extra consumption on GPIOs PC0..5 on 48/49 pin packages* Added *Section 1.2.2: USART4 transmission does not work on PC11* Deleted Workaround on *Section 1.3.1: Extra consumption on GPIOs PC0..5 on 48/49 pin packages* Added *Section 1.3.3: GPIOx locking mechanism not working properly for GPIOx_OTYPER register* Added *Section 1.2.2* and *Section 1.3.3* limitation inside *Section Table 3.*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com