

# DATA SHEET

## **TSA5523M** 1.4 GHz I<sup>2</sup>C-bus controlled multimedia synthesizer

Product specification  
File under Integrated Circuits, IC02

1996 Dec 17

## 1.4 GHz I<sup>2</sup>C-bus controlled multimedia synthesizer

TSA5523M

### FEATURES

- Complete 1.4 GHz single-chip system
- Adaptive DC/DC converter driver output
- On-board tuning amplifier output
- Varicap drive disable
- Four NPN open-collector output ports (10 mA)
- Four bus-controlled bidirectional ports (NPN open-collector outputs)
- In-lock detector
- 5-step Analog-to-Digital Converter (ADC)
- Mixer/Oscillator (M/O) band-switch output
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge-pump current (50 or 250  $\mu$ A)
- I<sup>2</sup>C-bus format
  - Address plus four data bytes transmission (write mode)
  - Address plus one status byte transmission (read mode)
  - Four independent addresses
- Low power, low radiation.

### GENERAL DESCRIPTION

The device is a single chip PLL frequency synthesizer designed for TV and VCR tuning systems. The circuit consists of a divide-by-eight prescaler with its own preamplifier, a 15-bit programmable divider, a crystal oscillator and its programmable reference divider, a phase/frequency detector combined with a charge-pump which drives the tuning amplifier, including 33 V output. Three NPN open-collector outputs are provided for band switching together with five open-collector NPN outputs. Four of these ports can also be used as input ports (one ADC and three general purpose I/O ports).

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA5523M/C1	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1



An output is provided to control a Philips mixer/oscillator IC controlled by bits P7, P5 and P4. Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 3.90625, 6.25 or 7.8125 kHz with a 4 MHz crystal.

The lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC is available for digital AFC control. The ADC code is read during a read operation on the I<sup>2</sup>C-bus. The ADC input is combined with the port P6. In the test mode, this port is also used as a test output for  $f_{ref}$  and  $f_{div/2}$  (see Table 4). In addition, the circuit includes a DC/DC converter driver connected to the IDC pin to control the amplitude of an external oscillator followed by a voltage rectifier.

The voltage rectifier is used to generate the correct tuning supply voltage to maintain a constant current into the tuning amplifier. The DC/DC converter driver can be disabled by setting the IDC pin to  $V_{CC1}$  in this event the tuning supply voltage is delivered by a fixed 33 V supply.

Five serial bytes (including address byte) are required to address the device, select the VCO frequency, program the ports, set the charge-pump current and set the reference divider ratio. The device has four independent I<sup>2</sup>C-bus addresses which can be selected by applying a specific voltage on the AS input (see Table 3).

### APPLICATIONS

- Multimedia TV tuners and front-ends
- VCR tuners.

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## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>CC1</sub>	supply voltage		4.5	–	5.5	V
I <sub>CC1</sub>	supply current		–	22	30	mA
f <sub>RF</sub>	RF frequency range		64	–	1400	MHz
V <sub>iRF</sub>	RF input voltage level	80 to 150 MHz	–25	–	+3	dBm
		150 MHz to 1 GHz	–28	–	+3	dBm
		1 to 1.4 GHz	–26	–	+3	dBm
f <sub>XTAL</sub>	crystal oscillator frequency		–	4	–	MHz
I <sub>NPN</sub>	NPN open-collector output current		–	10	15	mA
T <sub>amb</sub>	operating ambient temperature		–20	–	+85	°C
T <sub>stg</sub>	IC storage temperature		–40	–	+150	°C

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### BLOCK DIAGRAM

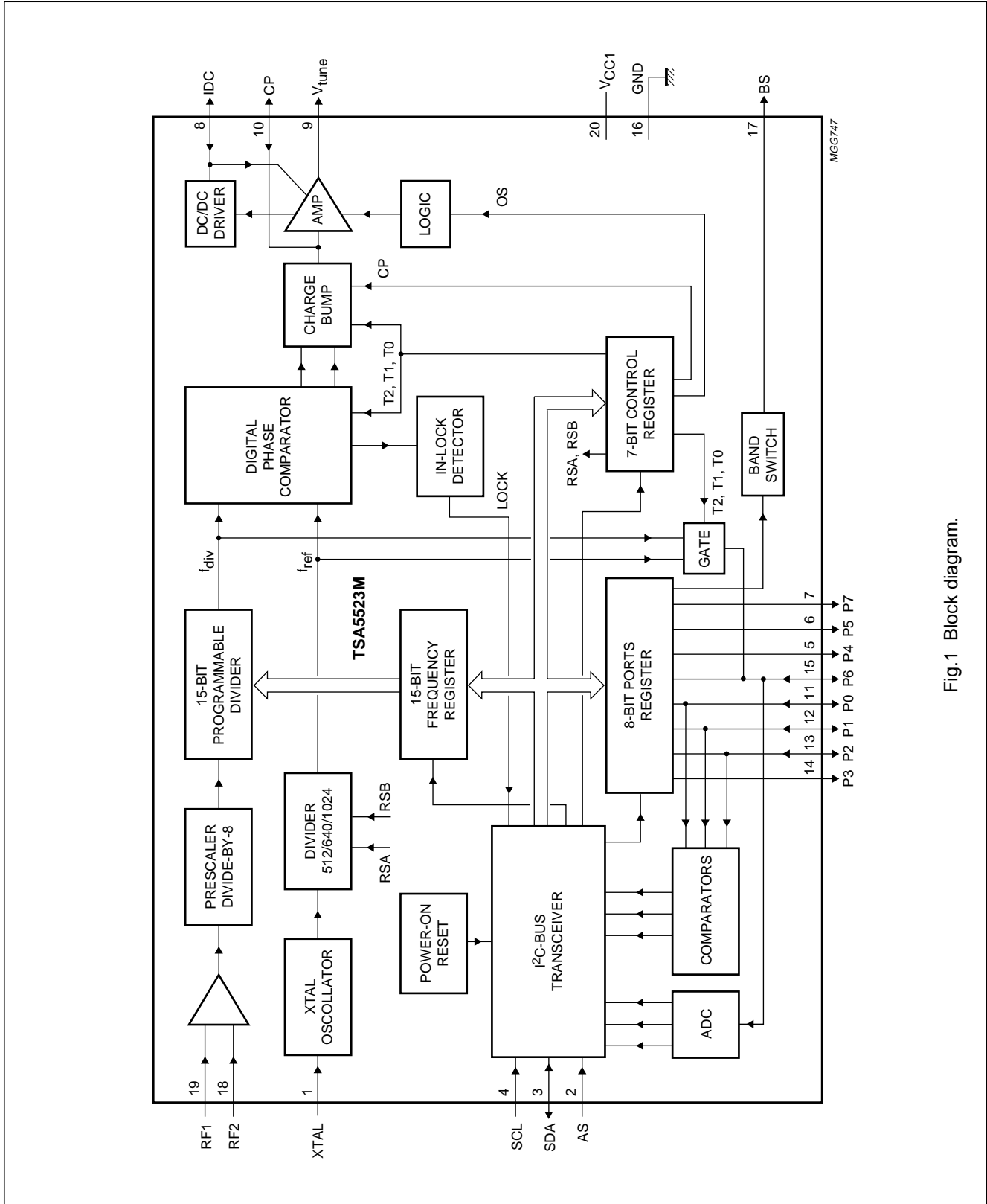


Fig.1 Block diagram.

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### PINNING

SYMBOL	PIN	DESCRIPTION
XTAL	1	crystal oscillator input
AS	2	address selection input
SDA	3	serial data input/output
SCL	4	serial clock input
P4	5	Port 4 NPN open-collector band-switch output
P5	6	Port 5 NPN open-collector band-switch output
P7	7	Port 7 NPN open-collector band-switch output
IDC	8	DC/DC converter control I/O terminal
V <sub>tune</sub>	9	tuning voltage output
CP	10	NPN open-collector I/O port
P0	11	Port 0 NPN open-collector I/O port
P1	12	Port 1 NPN open-collector I/O port
P2	13	Port 2 NPN open-collector I/O port
P3	14	Port 3 NPN open-collector output
P6	15	Port 6 NPN open-collector output/ADC input
GND	16	ground
BS	17	band-switch output to mixer/oscillator driver
RF2	18	RF signal input 2
RF1	19	RF signal input 1
V <sub>CC1</sub>	20	supply voltage (+5 V)

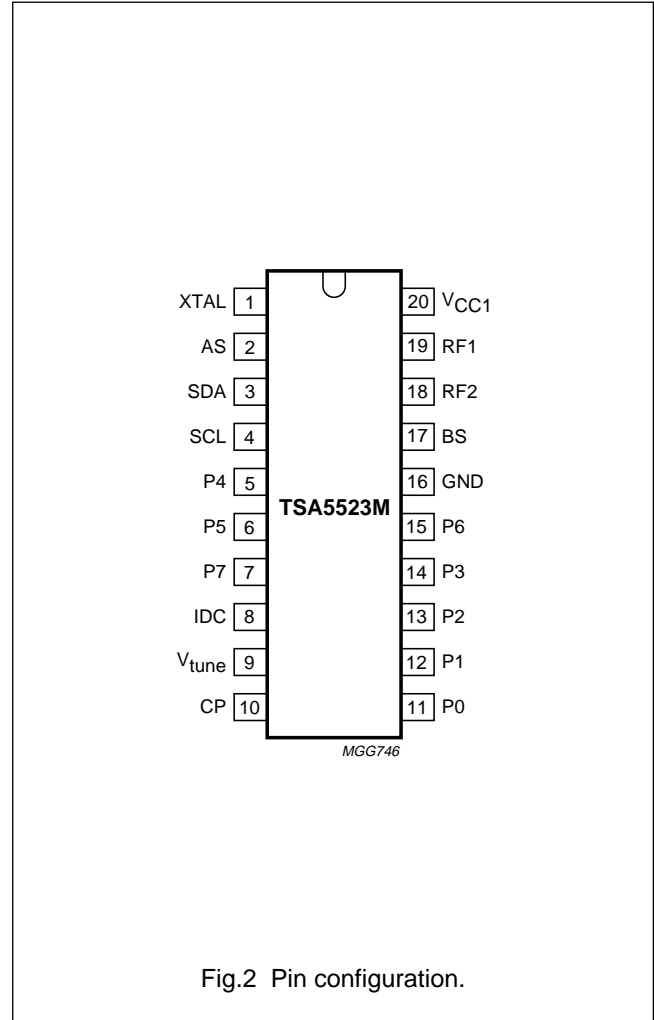


Fig.2 Pin configuration.

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### FUNCTIONAL DESCRIPTION

The device is controlled via the two-wire I<sup>2</sup>C-bus. For programming, there is one module address (7 bits) and the R/W bit for selecting the read or the write mode.

**Write mode:  $\overline{R/W} = 0$**  (see Table 1)

After the address transmission (first byte), data bytes can be sent to the device. Four data bytes are needed to fully program the device. The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address + 4 data bytes).

The device can also be partially programmed providing that the first data byte following the address is Divider Byte 1 (DB1) or Control Byte (CB). The meaning of the bits in the data bytes is given in Table 1.

The first bit of the first data byte transmitted indicates whether frequency data (first bit = 0) or control and ports data (first bit = 1) will follow. Until an I<sup>2</sup>C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. The frequency register is loaded after the 8th clock pulse of the second Divider Byte (DB2), the control register is loaded after the 8th clock pulse of the control byte and the ports register is loaded after the 8th clock pulse of the Ports Byte (PB).

### I<sup>2</sup>C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage to the AS input. The relationship between MA1 and MA0 and the input voltage on the AS input is given in Table 2.

**Table 1** I<sup>2</sup>C-bus data format

DATA BYTES	MSB							LSB		ACK
Address Byte (ADR)	1	1	0	0	0	MA1	MA0	0	A <sup>(1)</sup>	
Divider Byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A <sup>(1)</sup>	
Divider Byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A <sup>(1)</sup>	
Control Byte (CB)	1	CP	T2	T1	T0	RSA	RSB	OS	A <sup>(1)</sup>	
Ports Byte (PB)	P7	P6	P5	P4	P3	P2	P1	P0	A <sup>(1)</sup>	

### Note

1. A = Acknowledge.

**Table 2** Explanation to Table 1

SYMBOL	DESCRIPTION
MA1 and MA0	programmable address bits (see Table 3)
N14 to N0	programmable divider bits $N = N14 \times 2^{14} + 2^{13} + \dots + N1 \times 2 + N0$
CP	charge-pump current
CP = 0	50 $\mu$ A
CP = 1	250 $\mu$ A
T2, T1 and T0	test bits; normal operation; T2 = 0, T1 = 0, T0 = 1 (see Table 4)
RSA and RSB	reference divider ratio select bits (see Table 5)
OS	tuning amplifier control bit
OS = 0	normal operation; tuning voltage is ON
OS = 1	tuning voltage is OFF (high impedance), IDC output voltage is LOW
P7 to P0	NPN open-collector control bits
Pn = 0	output n is OFF
Pn = 1	output n is ON

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**Table 3** Address selection

INPUT VOLTAGE APPLIED TO PIN AS	MA1	MA0
0 V to 0.1V <sub>CC1</sub>	0	0
open-circuit or 0.2V <sub>CC1</sub> to 0.3V <sub>CC1</sub>	0	1
0.4V <sub>CC1</sub> to 0.6V <sub>CC1</sub>	1	0
0.9V <sub>CC1</sub> to V <sub>CC1</sub>	1	1

**Table 4** Test bits

T2	T1	T0	DEVICE OPERATION
0	0	1	normal mode
0	1	X	charge-pump is OFF
1	1	0	charge-pump is sinking current
1	1	1	charge-pump is sourcing current
1	0	0	f <sub>ref</sub> is available on P6 output
1	0	1	f <sub>div/2</sub> is available on P6 output

**Table 5** Ratio select bits

RSA	RSB	REFERENCE DIVIDER
X	0	640
0	1	1024
1	1	512

**Table 6** Band-switch output levels

P7	P5	P4	OUTPUT VOLTAGE ON PIN BS	PHILIPS M/O IC's BAND
1	1	0	0.25 V	band A
1	0	1	0.4V <sub>CC1</sub>	band B
0	1	1	0.8V <sub>CC1</sub>	band C
1	1	1	V <sub>CC1</sub>	band C
all other codes			V <sub>CC1</sub>	band C

**Read mode: R $\bar{W}$  = 1** (see Table 7)

Data can be read out of the device by setting the R $\bar{W}$  bit to logic 1. After the slave address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal. A second data byte can be read out of the device if the processor generates an acknowledge on the SDA line (master acknowledge).

End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the processor to generate a STOP condition. When Ports P0 to P2 are used as inputs, the corresponding bits **must** be logic 0 (high-impedance state). The Power-On Reset flag (POR) is set to logic 1 at power-on. It is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with the in-lock flag FL (FL = 1) which indicates when the loop is locked. The bits I2, I1 and I0 represent the status of the I/O Ports P2, P1 and P0 respectively.

A logic 0 indicates a LOW level and a logic 1 indicates a HIGH level (see threshold level in the "Characteristics"). A built-in ADC is available on pin P6. This converter can be used to feed AFC information to the controller from the IF section of the television. The relationship between bits A2, A1 and A0 is given in Table 9.

At power-on, the device is reset as follows: all ports are set to the high-impedance state, except P4, P5 and P7 which are set to logic 1. The tuning amplifier is in the high-impedance state (OS = 1). The POR level is fixed to  $3 \times V_{BE}$  (2.1 V typ.). If V<sub>CC1</sub> goes below the POR level the circuit is reset.

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**Table 7** Read data format

BYTE	MSB <sup>(1)</sup>						LSB		ACK
Address Byte (ADB)	1	1	0	0	0	MA1	MA0	1	A <sup>(2)</sup>
Status Byte (SB)	POR	FL	I2	I1	I0	A2	A1	A0	–

**Notes**

- MSB is transmitted first.
- A: Acknowledge.

**Table 8** Explanation to Table 7

SYMBOL	DESCRIPTION
POR	power-on reset flag (POR = 1 at power-on)
FL	in-lock flag (FL = 1 when the loop is phase-locked)
I2, I1 and I0	digital levels for I/O ports P2, P1 and P0 respectively
A2, A1 and A0	digital outputs of the 5-level ADC

**Table 9** Analog-to-digital converter levels; note 1

VOLTAGE APPLIED ON PORT P6	A2	A1	A0
0.6V <sub>CC1</sub> to V <sub>CC1</sub>	1	0	0
0.45V <sub>CC1</sub> to 0.6V <sub>CC1</sub>	0	1	1
0.3V <sub>CC1</sub> to 0.45V <sub>CC1</sub>	0	1	0
0.15V <sub>CC1</sub> to 0.3V <sub>CC1</sub>	0	0	1
0 to 0.15V <sub>CC1</sub>	0	0	0

**Note**

- Accuracy is 0.03V<sub>CC1</sub>.



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## LIMITING VALUES

In according with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>iRF</sub>	prescaler input voltage		-0.3	V <sub>CC1</sub>	V
V <sub>CC1</sub>	supply voltage (+5 V)		-0.3	+6	V
V <sub>oIDC</sub>	IDC output voltage		-0.3	V <sub>CC1</sub>	V
V <sub>oNPN</sub>	NPN open-collector output voltage		-0.3	+16	V
I <sub>oNPN</sub>	NPN open-collector output current		-1	+15	mA
V <sub>oCP</sub>	charge-pump output voltage		-0.3	V <sub>CC1</sub>	V
V <sub>o(tune)</sub>	tuning voltage output	see Fig.3	-0.3	+40	V
V <sub>oBS</sub>	band-switch output voltage		-0.3	V <sub>CC1</sub>	V
V <sub>iSCL</sub>	serial clock input voltage		-0.3	+6	V
V <sub>i/oSDA</sub>	serial data input/output voltage		-0.3	+6	V
I <sub>oSDA</sub>	data output current		-1	+5	mA
V <sub>iAS</sub>	address selection input voltage		-0.3	V <sub>CC1</sub>	V
V <sub>iXTAL</sub>	crystal input voltage		-0.3	V <sub>CC1</sub>	V
T <sub>stg</sub>	IC storage temperature		-40	+150	°C
T <sub>j(max)</sub>	maximum junction temperature		-	+150	°C
t <sub>sc</sub>	short-circuit time every pin to V <sub>CC1</sub> or GND		-	10	s

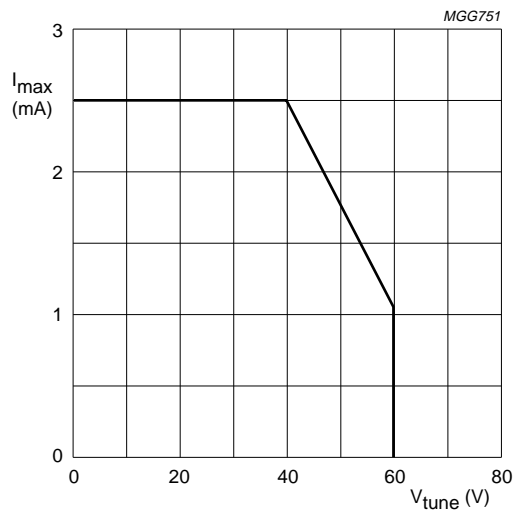


Fig.3 Rating power on V<sub>tune</sub> output pin.

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## HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling bipolar devices.

Every pin withstands the ESD test in accordance with "MIL-STD-883C category B" (2000 V).

Every pin withstands the EDS test in accordance with Philips Semiconductors Machine Model 0  $\Omega$ , 200 pF (200 V).

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

## CHARACTERISTICS

$V_{CC1} = 4.5$  to  $5.5$  V;  $T_{amb} = -20$  to  $+85$  °C; see note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>General</b>						
$V_{CC1}$	supply voltage		4.5	–	5.5	V
$I_{CC1}$	supply current	$V_{CC1} = 5$ V	–	22	30	mA
$V_{PORth}$	power-on reset threshold voltage	$T_{amb} = 25$ °C slope is $-6$ mV/°C	1.5	2.0	–	V
$T_{amb}$	operating ambient temperature		$-20$	–	$+85$	°C
$f_{iRF}$	RF input frequency		64	–	1400	MHz
N	divider ratio	15-bit frequency word	256	–	32767	–
<b>XTAL oscillator</b>						
$f_{XTAL}$	frequency range	$R_{XTAL} = 25$ to $200$ $\Omega$	3.2	4.0	4.48	MHz
$Z_{XTAL}$	input impedance	$f = 4$ MHz	600	1200	–	$\Omega$
$DL_{XTAL(p-p)}$	drive level on pin XTAL (peak-to-peak value)	series capacitor = 18 pF; crystal Philips 4333 1430 4881	–	110	–	mV
<b>Prescaler</b>						
$V_{RFIn}$	input level	$V_{CC1} = 4.5$ to $5.5$ V; $T_{amb} = -20$ to $+85$ °C; see Fig.4 $f = 80$ to $150$ MHz $f = 150$ to $1000$ MHz $f = 1000$ to $1400$ MHz	$-25$ $-28$ $-26$	– – –	$+3$ $+3$ $+3$	 dBm dBm dBm
$Z_{iRF}$	input impedance	see Fig.5	–	–	–	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>NPN open-collector outputs P7 to P0; note 2</b>						
I <sub>LI</sub>	leakage current	V <sub>CC1</sub> = 5.5 V; V <sub>o</sub> = 13.5 V	–	–	10	μA
	leakage current P4, P5, P7	V <sub>CC1</sub> = 5.5 V; V <sub>o</sub> = 1.5 V	–	–	1	μA
V <sub>cesatN</sub>	output saturation voltage on Ports P4, P5 and P7	I <sub>sink</sub> = 100 μA	–	–	0.2	V
	output saturation voltage	I <sub>sink</sub> = 10 mA I <sub>sink</sub> = 2 mA	–	0.2	0.4 0.3	V V
C <sub>Pn</sub>	allowed capacitive loading on output pins	V <sub>Pn</sub> = 5.5 V	–	–	10	nF
<b>Input ports P2, P1 and P0; note 3</b>						
V <sub>IL</sub>	LOW level input voltage		–	–	1.5	V
V <sub>IH</sub>	HIGH level input voltage		3	–	–	V
I <sub>IL</sub>	LOW level input current	V <sub>i</sub> = 0 V	–10	–	–	μA
I <sub>IH</sub>	HIGH level input current	V <sub>CC1</sub> = 5.5 V; V <sub>o</sub> = 13.5 V	–	–	10	μA
<b>AS input (Address Selection)</b>						
I <sub>IH</sub>	HIGH level input current	V <sub>IH</sub> = V <sub>CC1</sub>	–	–	50	μA
I <sub>IL</sub>	LOW level input current	V <sub>IL</sub> = 0 V	–50	–	–	μA
<b>SCL and SDA inputs</b>						
V <sub>IL</sub>	LOW level input voltage		–	–	1.5	V
V <sub>IH</sub>	HIGH level input voltage		3.0	–	5.5	V
I <sub>IH</sub>	HIGH level input current	V <sub>IH</sub> = 5.5 V; V <sub>CC1</sub> = 0 V	–	–	10	μA
		V <sub>IH</sub> = 5.5 V; V <sub>CC1</sub> = 5.5 V	–	–	10	μA
I <sub>IL</sub>	LOW level input current	V <sub>IL</sub> = 0 V; V <sub>CC1</sub> = 5.5 V	–10	–	–	μA
f <sub>CLK</sub>	clock frequency		–	100	400	kHz
<b>SDA output (I<sup>2</sup>C-bus mode)</b>						
I <sub>LI</sub>	leakage current	V <sub>SDA</sub> = 5.5 V	–	–	10	μA
V <sub>oSDA</sub>	output voltage	I <sub>sink</sub> = 3 mA	–	–	0.4	V
<b>BS output (mixer/oscillator IC band selection)</b>						
V <sub>oBSA</sub>	output voltage for band A	I <sub>L</sub> = 20 μA	–	0.25	0.5	V
V <sub>oBSB</sub>	output voltage for band B	I <sub>L</sub> = 20 μA	0.36V <sub>CC1</sub>	0.4V <sub>CC1</sub>	0.43V <sub>CC1</sub>	V
V <sub>oBSC</sub>	output voltage for band C	I <sub>L</sub> = 20 μA	0.7V <sub>CC1</sub>	0.8V <sub>CC1</sub>	0.9V <sub>CC1</sub>	V
		I <sub>L</sub> = 50 μA	3.1	–	–	V
<b>IDC output</b>						
V <sub>IDCoff</sub>	voltage to switch-off DC/DC converter driver		V <sub>CC1</sub> – 0.5	–	V <sub>CC1</sub>	V
I <sub>oIDC</sub>	IDC output current	R <sub>ext</sub> = 100 kΩ	–10	–	+100	μA
G <sub>t</sub>	transfer gain	I <sub>g</sub> = 100 μA	–	1000	–	μA/V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Charge-pump output CP</b>						
I <sub>IH</sub>	HIGH level input current (absolute value)	CP = 1	–	250	–	μA
I <sub>IL</sub>	LOW level input current (absolute value)	CP = 0	–	50	–	μA
V <sub>oCP</sub>	output voltage	in-lock; T <sub>amb</sub> = 25 °C	–	1.95	–	V
I <sub>Llos</sub>	off-state leakage current	T2 = 0; T1 = 1	–5	+1	+15	nA
<b>Tuning voltage output; V<sub>tune</sub></b>						
I <sub>g(off)</sub>	leakage current when switched-off	OS = 1; V <sub>tune</sub> = 33 V	–	–	10	μA
V <sub>o9</sub>	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R <sub>L</sub> = 27 kΩ; V <sub>tune</sub> = 33 V	0.3	–	32.7	V
I <sub>bias</sub>	tuning amplifier bias current	DC/DC converter loop is active	70	100	130	μA
V <sub>ripple(p-p)</sub>	acceptable ripple voltage on V <sub>CC1</sub> (peak-to-peak value)	f <sub>ripple</sub> = 20 Hz to 500 kHz; note 4	–	–	30	mV

**Notes**

1. When a port is active, the collector voltage must not exceed 6 V.
2. All other ports are switched ON with 10 mA during test.
3. When a port is used as input port, the corresponding bit must be programmed to the high-impedance state.
4. FM deviation is 2 kHz (max).

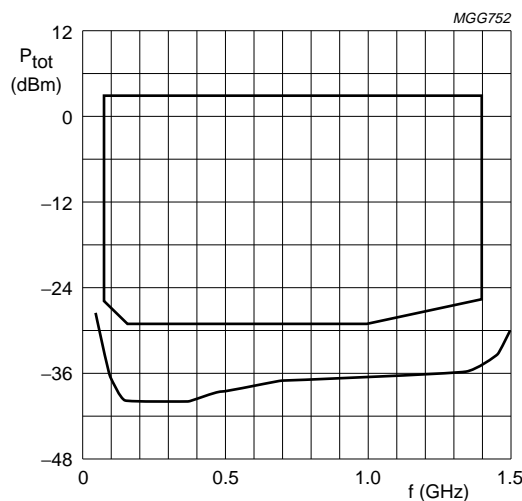


Fig.4 Prescaler typical input sensitivity curve (pin 2).

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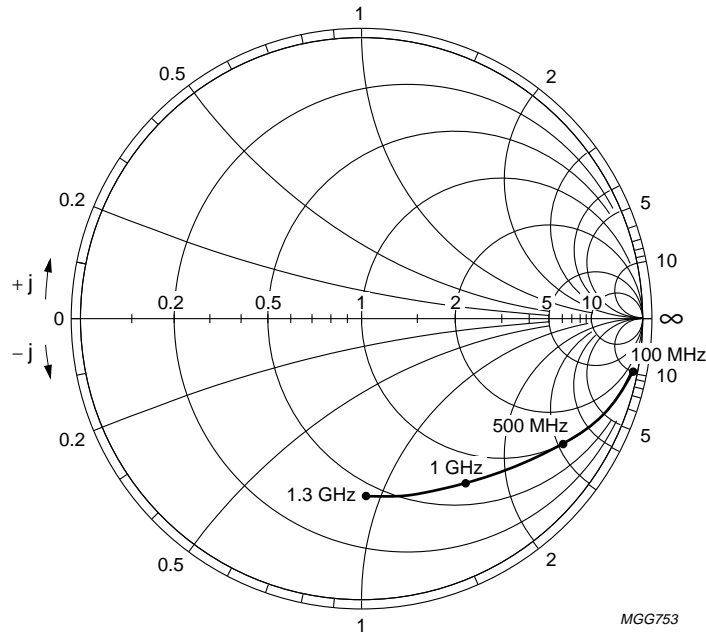


Fig.5 Prescaler Smith chart (S11) of typical input impedance ( $Z_L = 50 \Omega$ ; pin 2).

**APPLICATION INFORMATION**

**Tuning amplifier**

The tuning amplifier is able to drive the varicap voltage without an external transistor. The  $V_{tune}$  output must be connected to an external load of 27 kΩ connected to the tuning voltage supply. Figures 6 and 7 illustrate a possible loop filter. The component values depend on the oscillator characteristics and the selected reference frequency.

**Crystal oscillator**

The crystal oscillator uses a 4.0 MHz crystal in series with an 18 pF capacitor. The crystal operates in the series resonance mode. The connection to  $V_{CC1}$  is preferred, but it can also be connected to GND.

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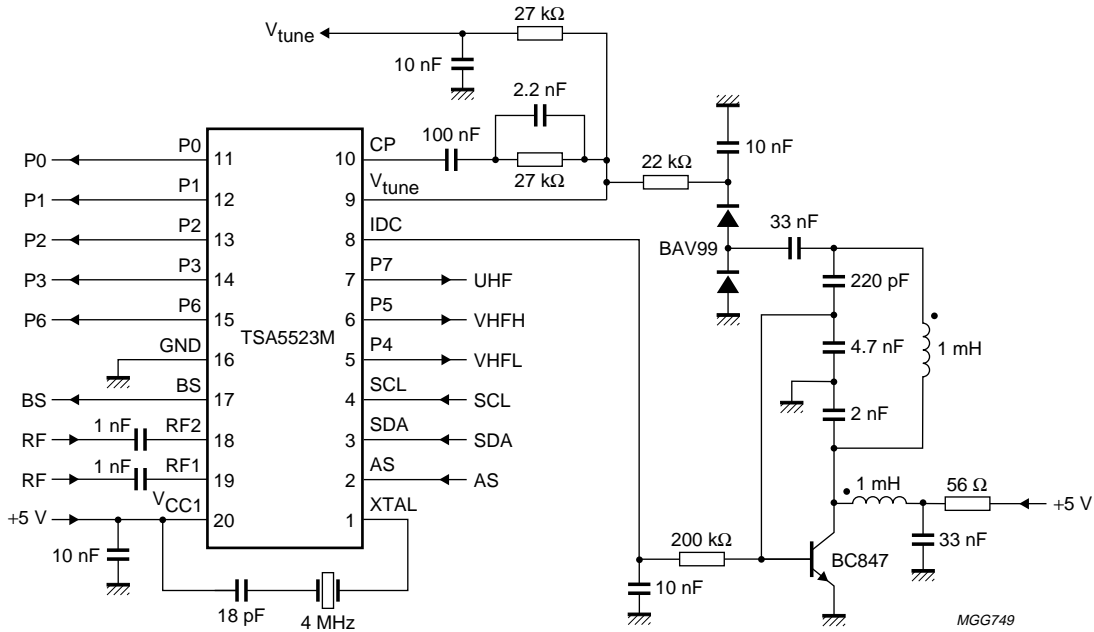


Fig.6 Typical application with DC/DC converter.

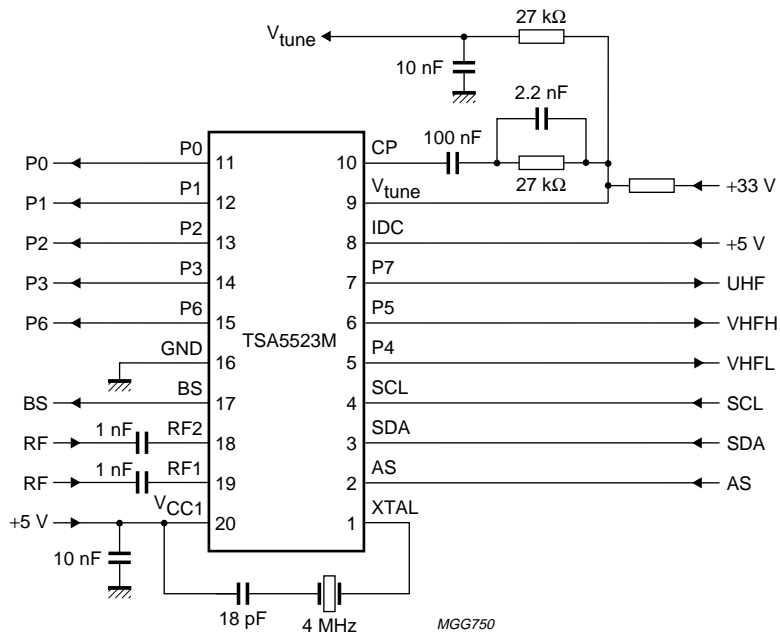


Fig.7 Standard application.

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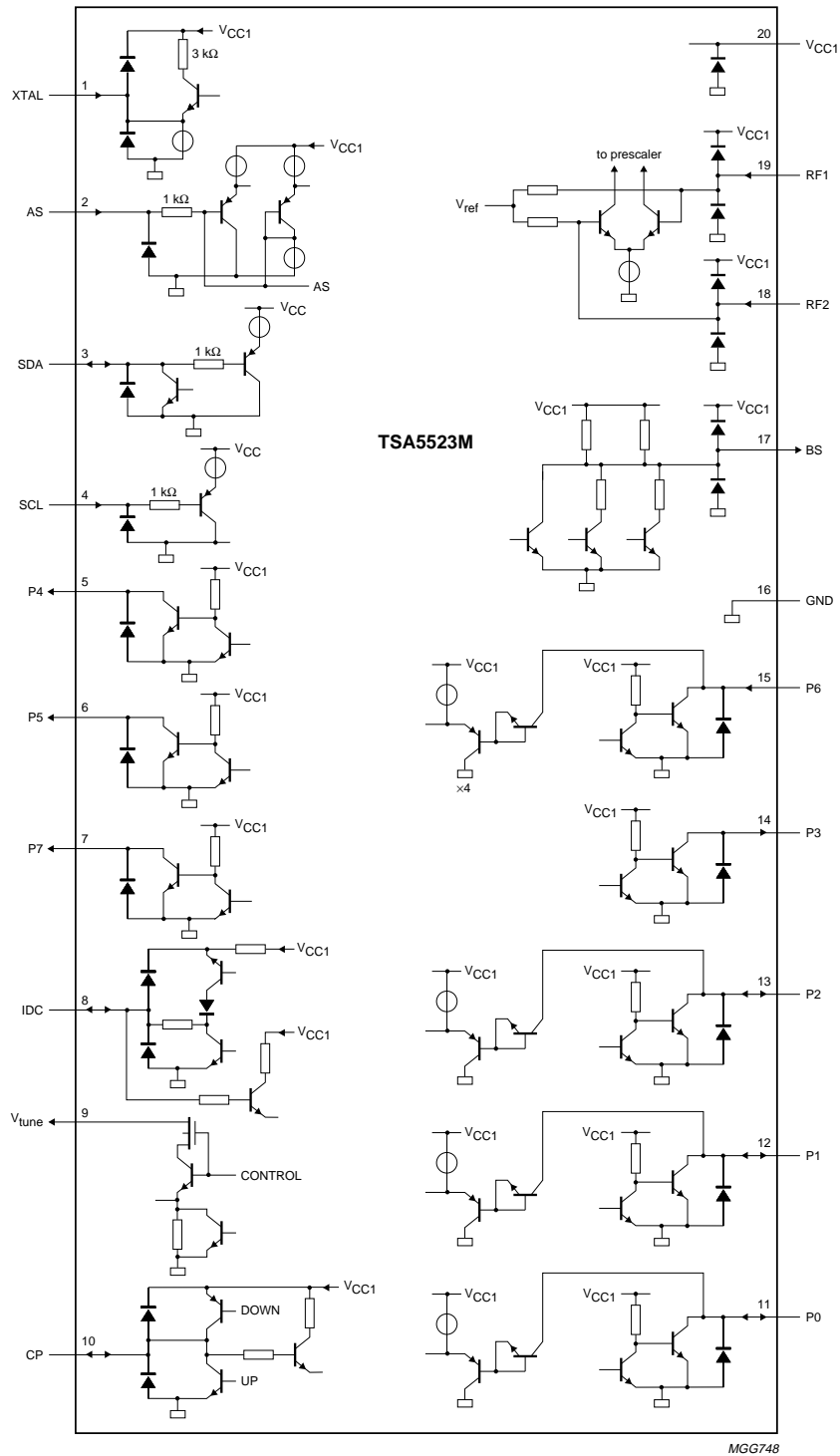


Fig.8 Input/output pin schematic.

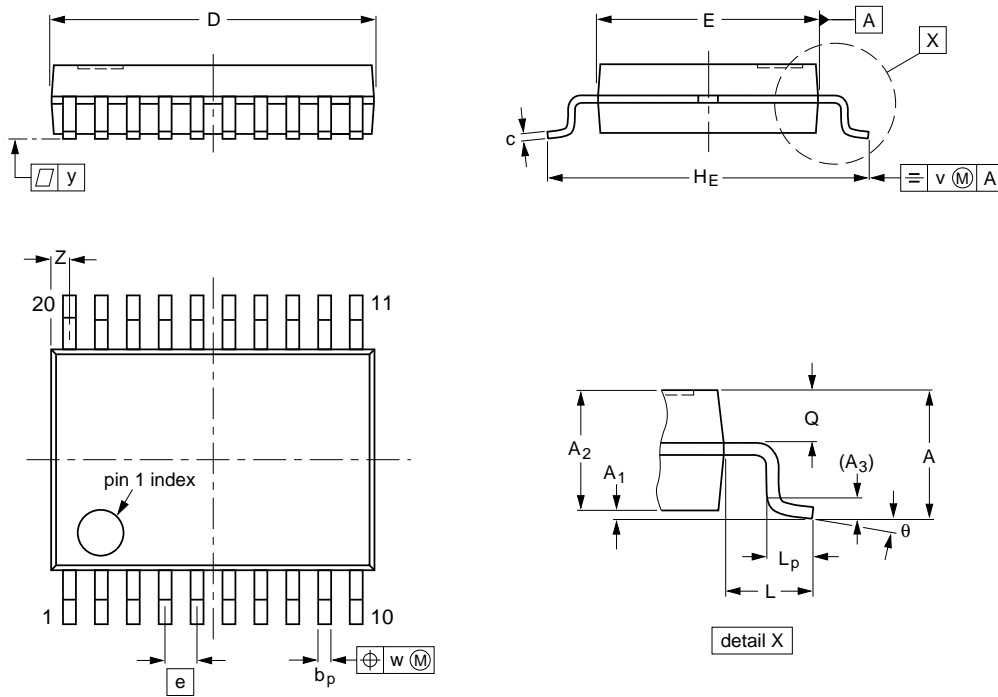
# 1.4 GHz I<sup>2</sup>C-bus controlled multimedia synthesizer

TSA5523M

## PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT266-1						90-04-05 95-02-25



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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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1.4 GHz I<sup>2</sup>C-bus controlled multimedia  
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