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VFD Driver/Controller IC **PT6311**

DESCRIPTION

PT6311 is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/8 to 1/16 duty factor housed in 52-pin plastic QFP Package. Twelve segment output lines, 8 grid output lines, 8 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6311 via a three-line serial interface.

FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (12 x 4 matrix)
- Multiple Display Modes: (12 segments, 16 digits to 20 segments, 8 digits)
- 8-Step Dimming Circuitry
- LED Ports Provided (5 channels, 20 mA max.)
- 4- Bits General Purpose Input Ports Provided
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 52-pin QFP Package

APPLICATION

- Microcomputer Peripheral Device

BLOCK DIAGRAM

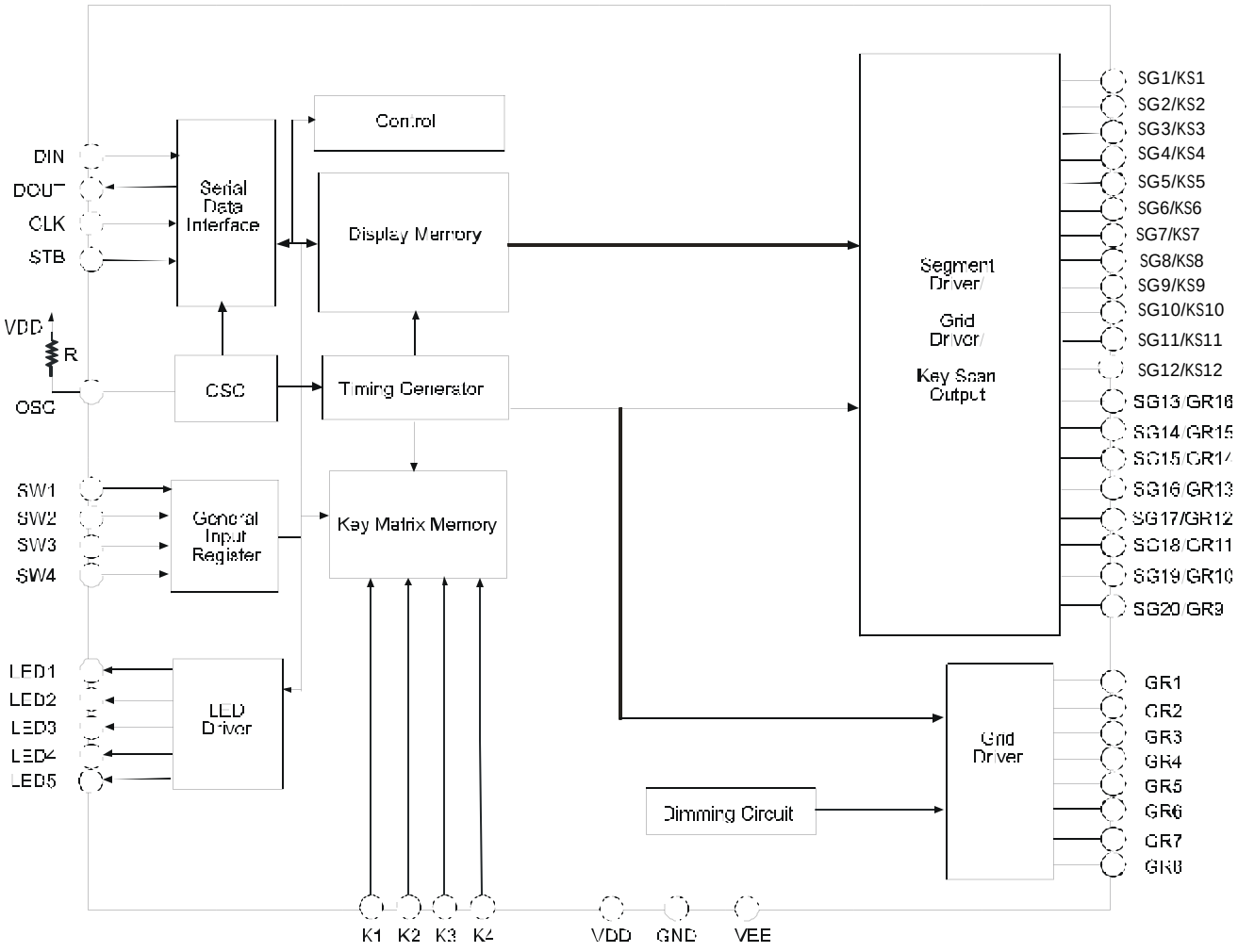


Figure 1: PT6311 Internal Block Diagram

PIN CONFIGURATION

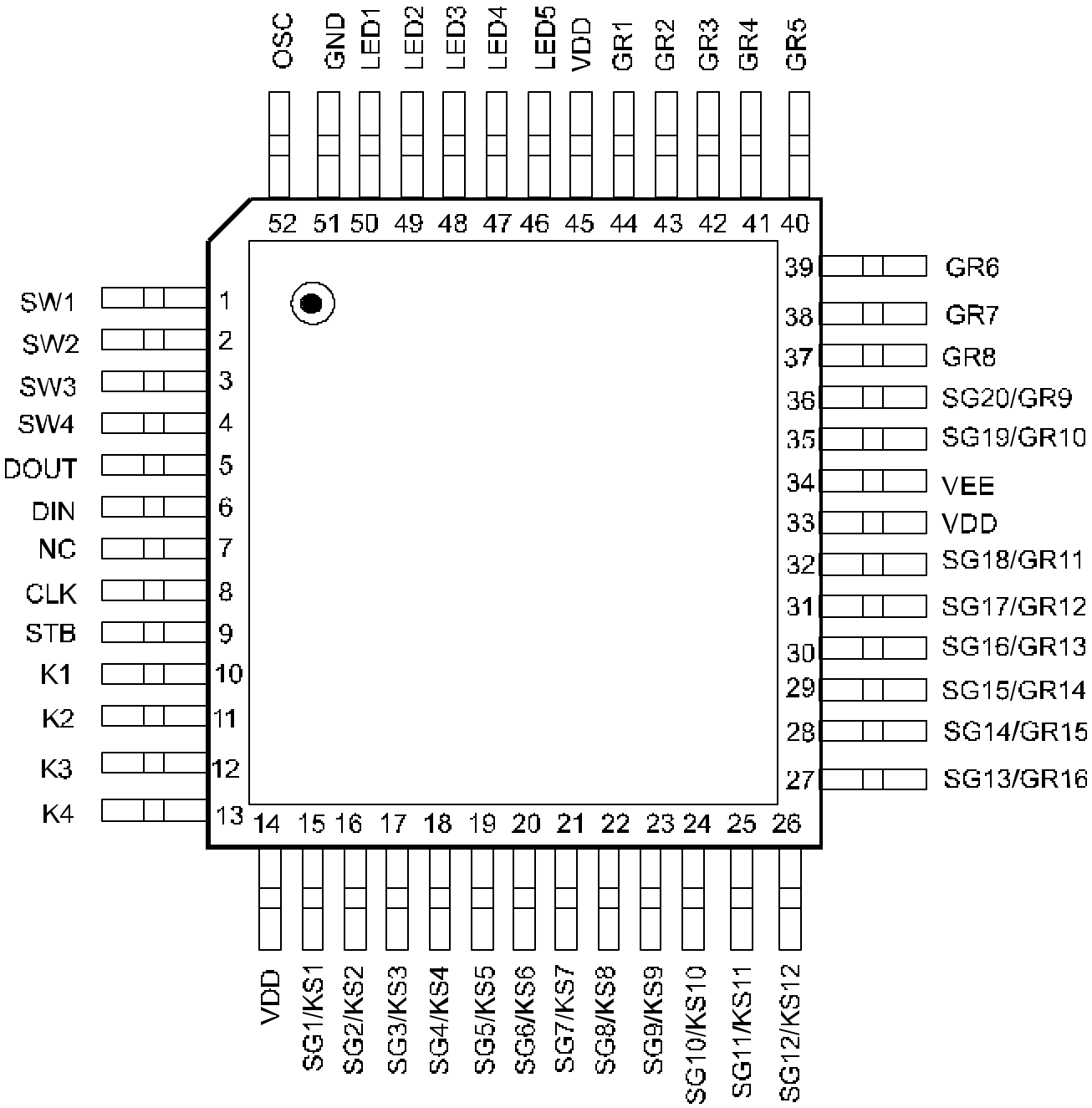


Figure 2: PT6311 Pin Configuration

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
SW1 to SW4	I	General Purpose Input Pins	1 to 4
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	5
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	6
NC	-	No Connection	7
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	9
K1 to K4	I	Key Data Input Pins The data inputted to these pins are latched at the end of the display cycle.	10 to 13
VDD	-	Logic Power Supply	14,33, 45
SG1/KS1 to SG12/KS12	O	High-Voltage Segment Output Pins Also acts as the Key Source	15 to 26
SG20/GR9 to SG19/GR10 SG18/GR11 to SG13/GR16	O	High Voltage Segment/Grid Output Pins	36 to 35 32 to 27
VEE	-	Pull-Down Level	34
GR1 to GR8	O	High-Voltage Grid Output Pins	44 to 37
LED1 to LED5	O	LED Output Pin	50 to 46
GND	-	Ground Pin	51
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	52

FUNCTIONAL DESCRIPTION

Commands

Commands determine the display mode and status of PT6311. A command is the first byte (b0 to b7) inputted to PT6311 via the DIN Pin after STB Pin has changed from "HIGH" to "LOW" State. If for some reason the STB Pin is set to "HIGH" while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6311 provides 8 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6311 via the DIN Pin when STB is "LOW". However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of "0".

The Display Mode Setting Commands determine the number of segments and grids to be used (1/8 to 1/16 duty, 20 to 12 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display command "ON" must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned "ON", the 16-digit , 12-segment modes is selected.

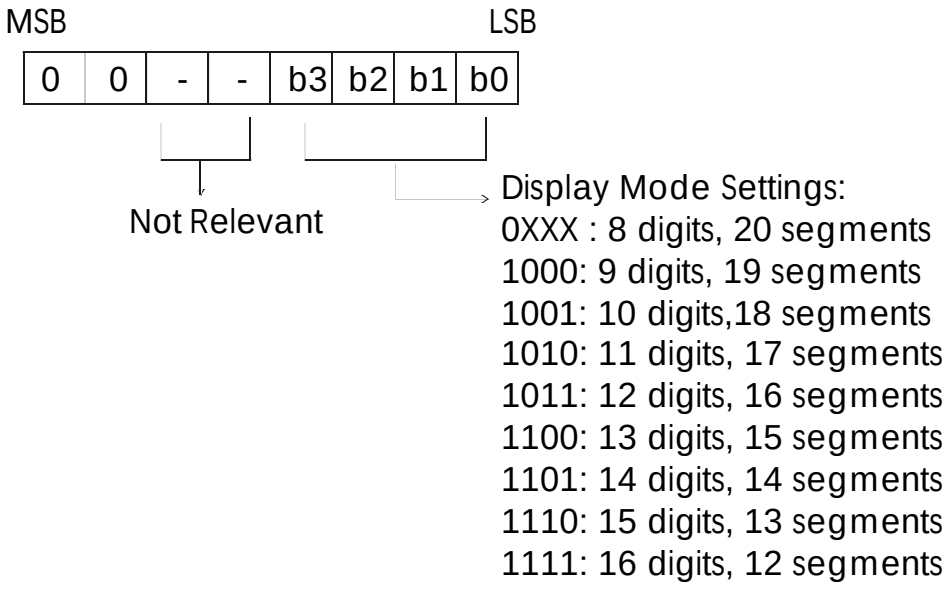


Figure 3: Display Mode Settings

Display Mode and RAM Address

Data transmitted from an external device to PT6311 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6311 are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	SG13	SG16	SG17	SG20	
00H$_L$		00H$_U$		01H$_L$		01H$_U$		02H$_L$		DIG1
03H$_L$		03H$_U$		04H$_L$		04H$_U$		05H$_L$		DIG2
06H$_L$		06H$_U$		07H$_L$		07H$_U$		08H$_L$		DIG3
09H$_L$		09H$_U$		0AH$_L$		0AH$_U$		0BH$_L$		DIG4
0CH$_L$		0CH$_U$		0DH$_L$		0DH$_U$		0EH$_L$		DIG5
0FH$_L$		0FH$_U$		10H$_L$		10H$_U$		11H$_L$		DIG6
12H$_L$		12H$_U$		13H$_L$		13H$_U$		14H$_L$		DIG7
15H$_L$		15H$_U$		16H$_L$		16H$_U$		17H$_L$		DIG8
18H$_L$		18H$_U$		19H$_L$		19H$_U$		1AH$_L$		DIG9
1BH$_L$		1BH$_U$		1CH$_L$		1CH$_U$		1DH$_L$		DIG10
1EH$_L$		1EH$_U$		1FH$_L$		1FH$_U$		20H$_L$		DIG11
21H$_L$		21H$_U$		22H$_L$		22H$_U$		23H$_L$		DIG12
24H$_L$		24H$_U$		25H$_L$		25H$_U$		26H$_L$		DIG13
27H$_L$		27H$_U$		28H$_L$		28H$_U$		29H$_L$		DIG14
2AH$_L$		2AH$_U$		2BH$_L$		2BH$_U$		2CH$_L$		DIG15
2DH$_L$		2DH$_U$		2EH$_L$		2EH$_U$		2FH$_L$		DIG16

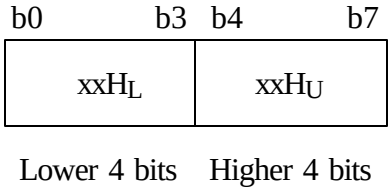


Figure 4: PT6311 RAM Address

COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6311. The data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of "0".

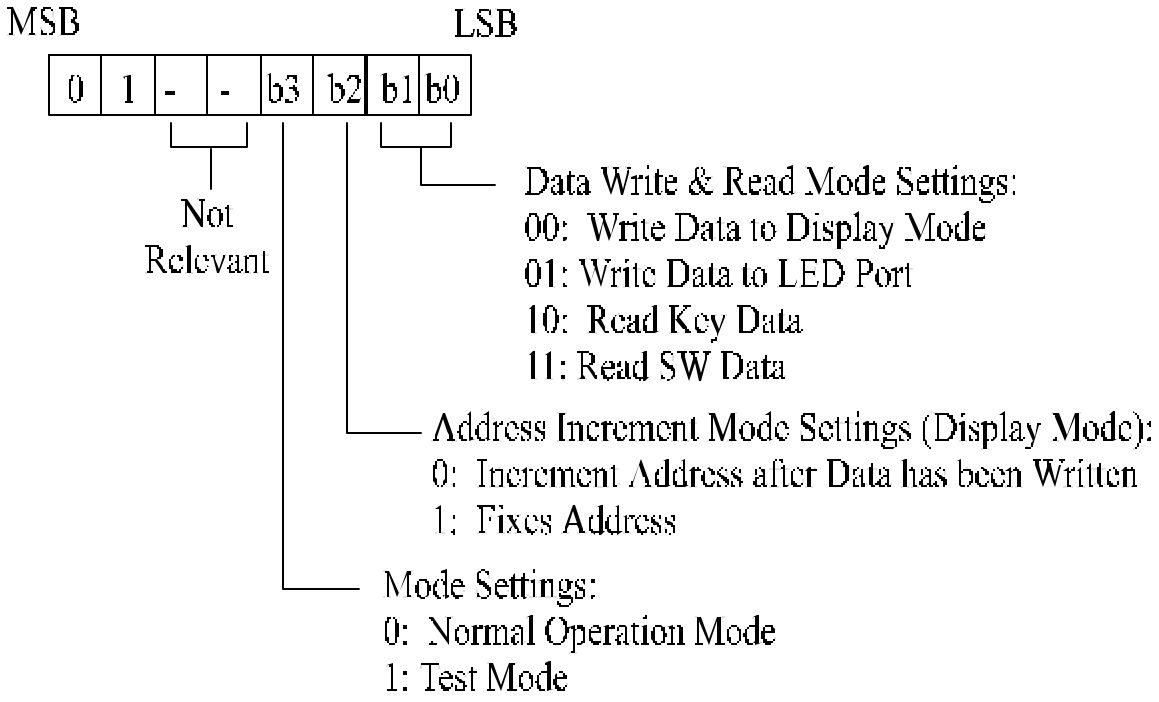


Figure 5: Data Settings

PT6311 Key Matrix & Key Input Data Storage RAM

PT6311 Key Matrix consists of 12 x 4 array as shown below:

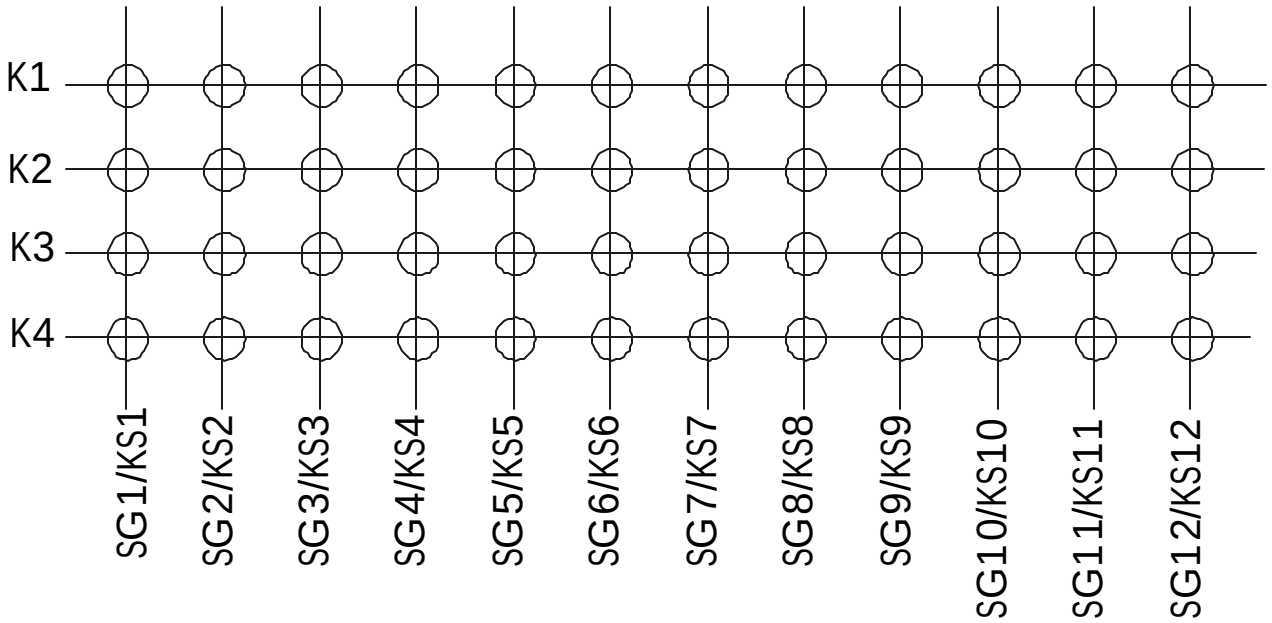


Figure 6: PT6311 Key Matrix

Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG1, b0) has been read, the least significant bit of the next data (SG12, b7) is read.

K1 ..... K4	K1 ..... K4
SG1/KS1	SG2/KS2
SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6
SG7/KS7	SG8/KS8
SG9/KS9	SG10/KS10
SG11/KS11	SG12/KS12
b0 .....b3	**b4 .....b7**

READING SEQUENCE

Figure 7: PT6311 Key Input Data Storage

LED Display

PT6311 provides 5 LED Display Terminals, namely LED1 to LED5. Data is written to the LED Port starting from the least significant bit (b0) of the port using a WRITE Command. Each bit starting from the least significant (b0) activates a specific LED Display Terminal -- b0 corresponds LED1 Display, b1 activates LED2 and so forth. Since there are only 5 LED display terminals, bits 6 to 8 (b5 ~ b7) are not used and therefore ignored. This means that b5 to b7 does NOT in anyway activate any LED Display, they are totally ignored.

When a bit (b0 ~ b4) in the LED Port is "0", the corresponding LED is ON. Conversely, when the bit is "1", the LED Display is turned OFF. For example, Bit 1 (as designated by b0) has the value of "0", then this means that LED1 is ON. It must be noted that when power is turned ON, bit 5 to bit 1 (b4 to b0) are given the value of "1". Please refer to the diagrams below.

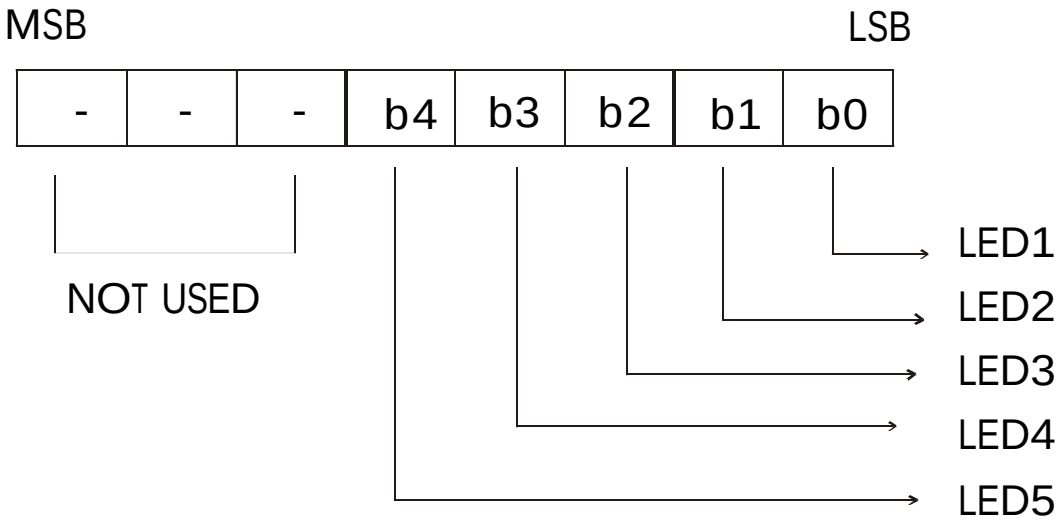


Figure 8: PT6311 LED Display Designation

Switch Data

PT6311 provides 4 Switch Inputs, namely: SW1 to SW4. SW Data is read starting from the least significant bit (b0) using a READ Command. Each bit starting from the least significant (b0) correspond to a specific Switch Input -- b0 corresponds SW1, b1 to SW2 and so forth. Since there are only 4 Switch Inputs, Bits 5 to 8 (b4 to 7) are given the value of "0". Please refer to the diagram below.

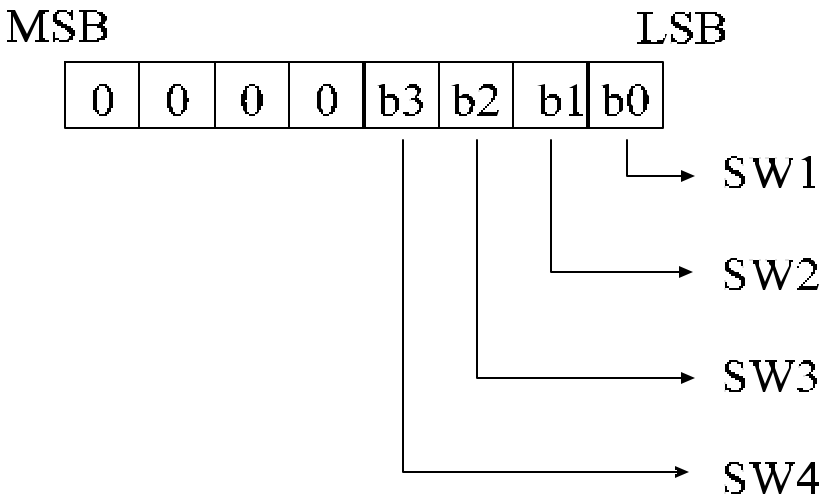


Figure 9: PT6311 SW Designations

COMMAND 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of "00H" to "2FH". If the address is set to 30H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at"00H".

Please refer to the diagram below.

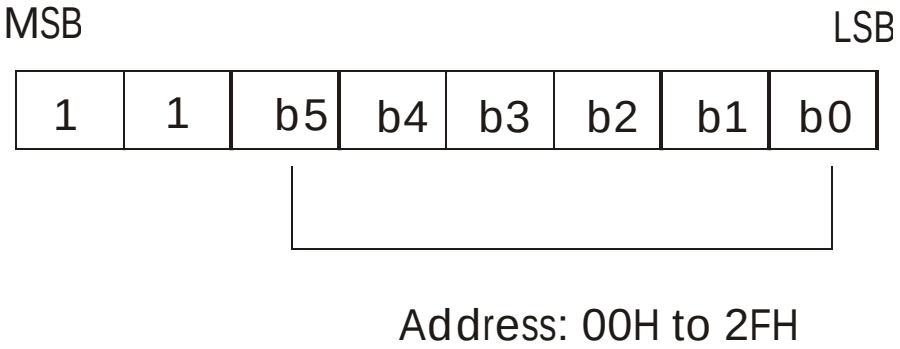


Figure 10: Address Settings

COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is stopped).

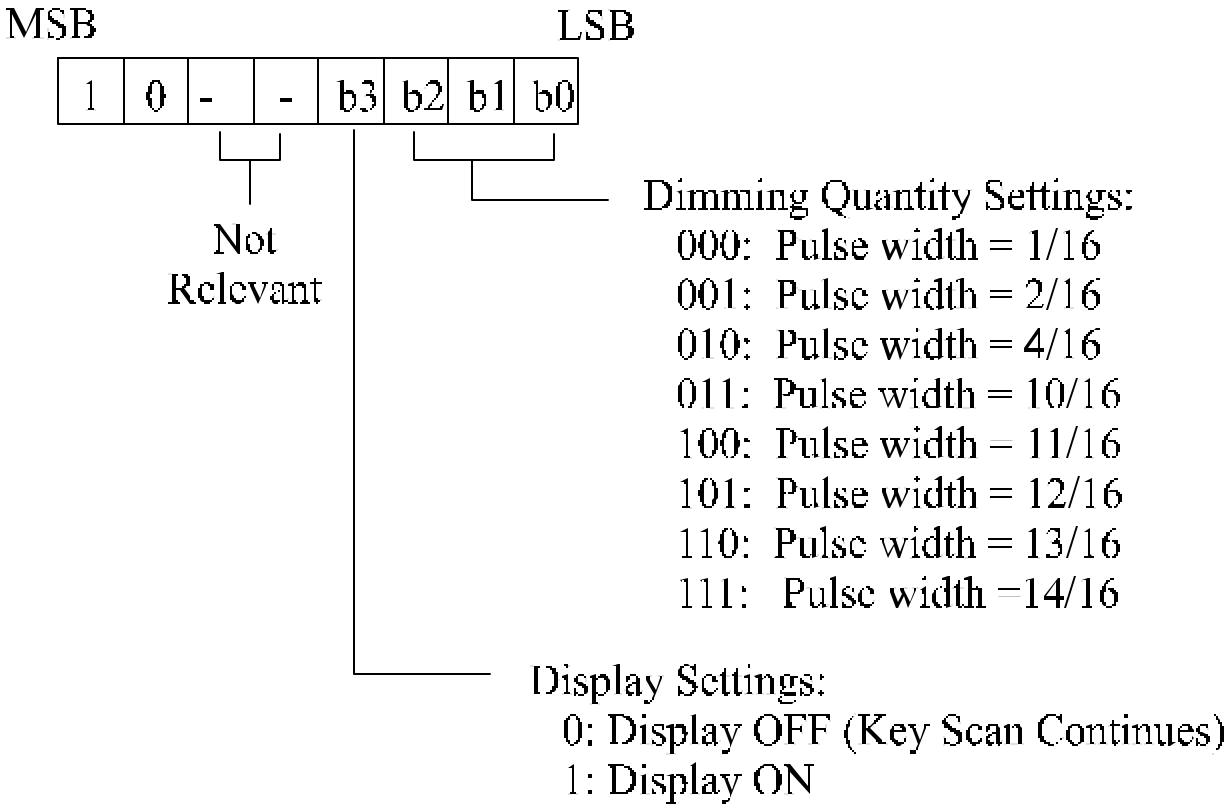


Figure 11: Display Control Settings

SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the are 12 x 4 matrix is stored in the RAM.

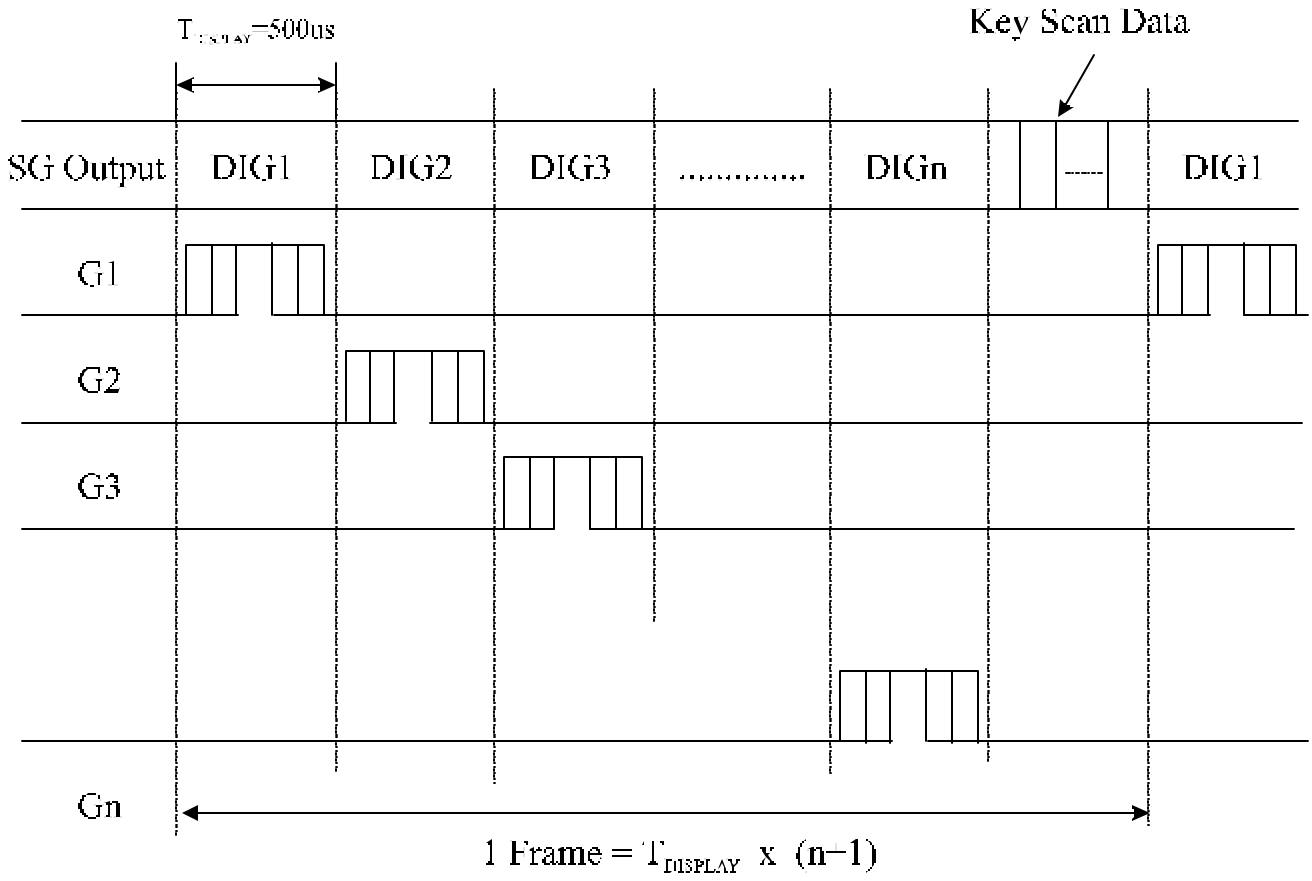


Figure 12: PT6311 Scanning & Display Timing Diagram

SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6311 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KOhms to 10 KOhms) must be connected to DOUT.

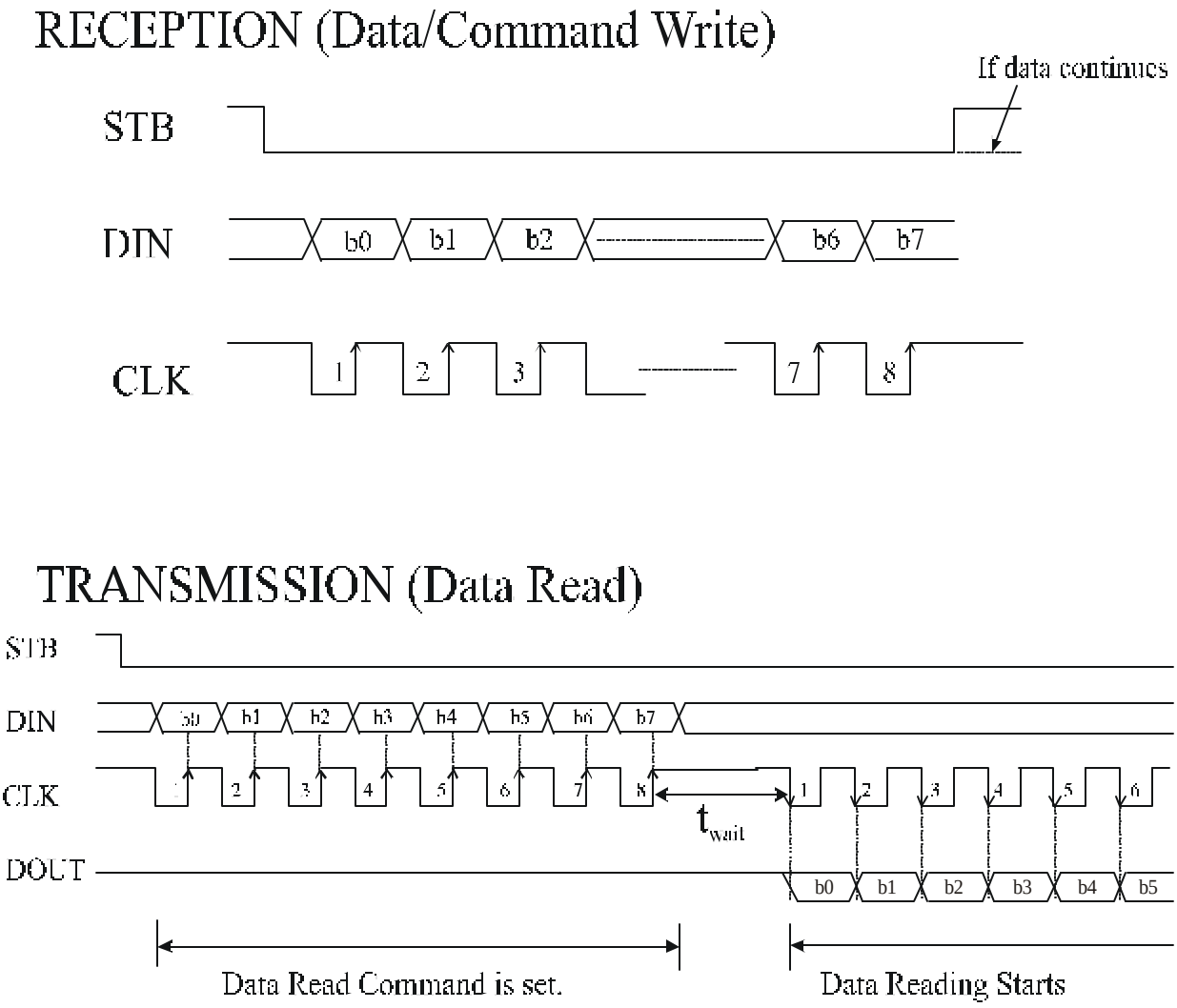


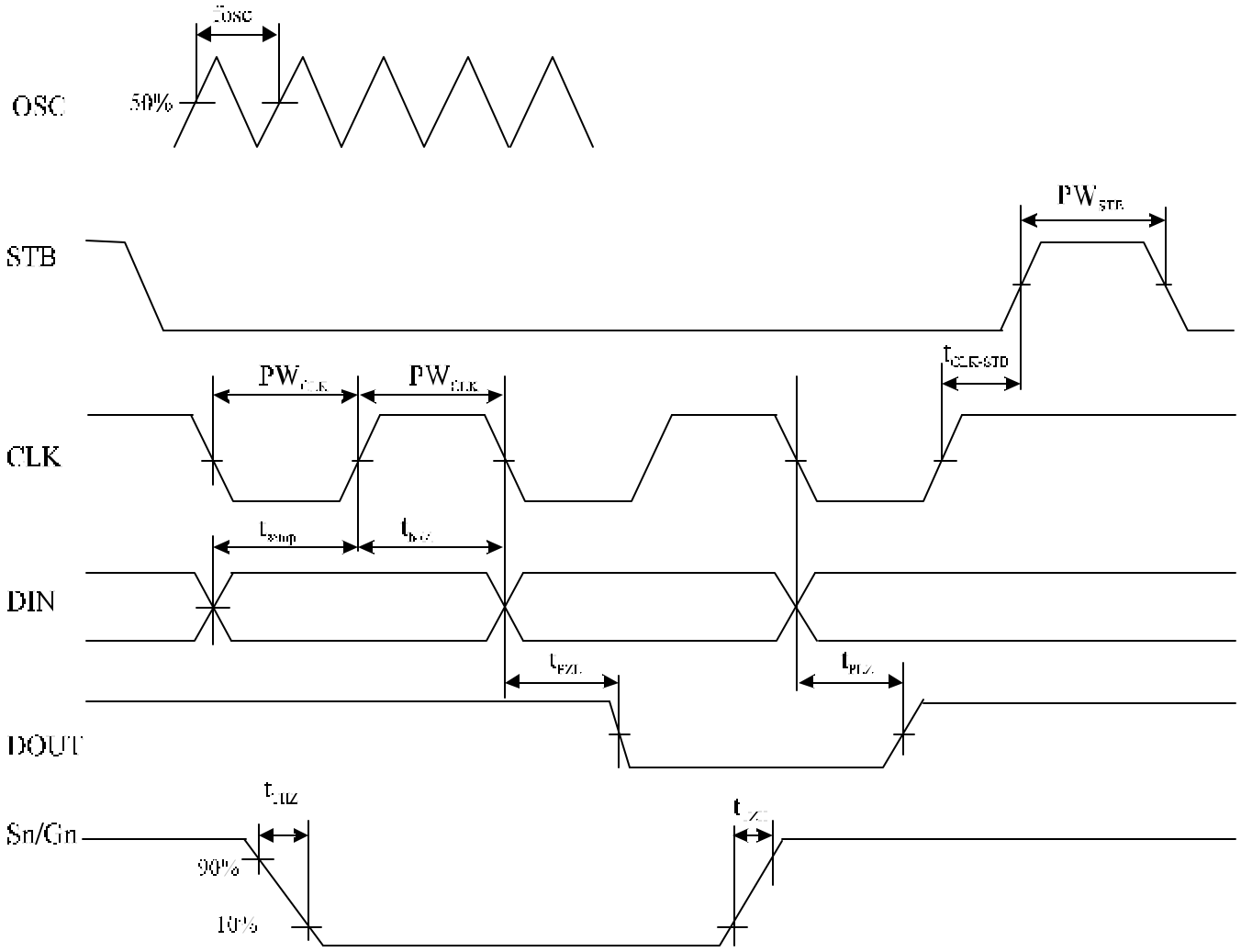
Figure 13: PT6311 Serial Communication Format

where: twait (waiting time) $\geq$ 1µs

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1µs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6311 Switching Characteristics Waveform is given below.



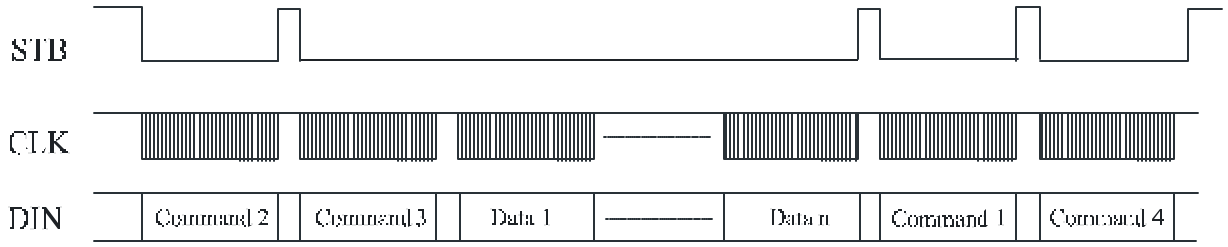
where: PW_{CLK} (Clock Pulse Width) ≥ 4 00ns
t setup (Data Setup Time) ≥ 100ns
$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1µs
t_{TZH} (Grid Rise Time) ≤ 0.5µs
t_{TZH} (Segment Rise Time) ≤ 2µs
fosc = Oscillation Frequency

PW_{STB} (Strobe Pulse Width) ≥ 1µs
thold (Data Hold Time) ≥ 100ns
t_{THZ} (Fall Time) ≤ 120µs
t_{PZL} (Propagation Delay Time) ≤ 100ns
t_{PLZ} (Propagation Delay Time) ≤ 300ns

Figure 14: PT6311 Switching Characteristic Waveform

APPLICATIONS

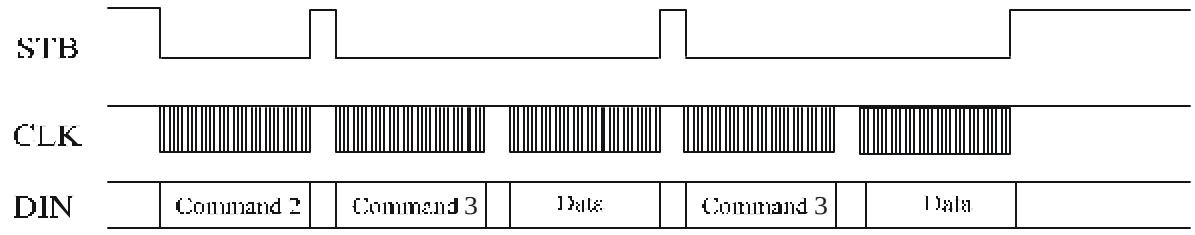
Display memory are updated by incrementing addresses. Please refer to the following diagram.



where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (48 Bytes max.)
Command 4: Display Control Command

Figure 15: Display Memory Updated by Address Increments

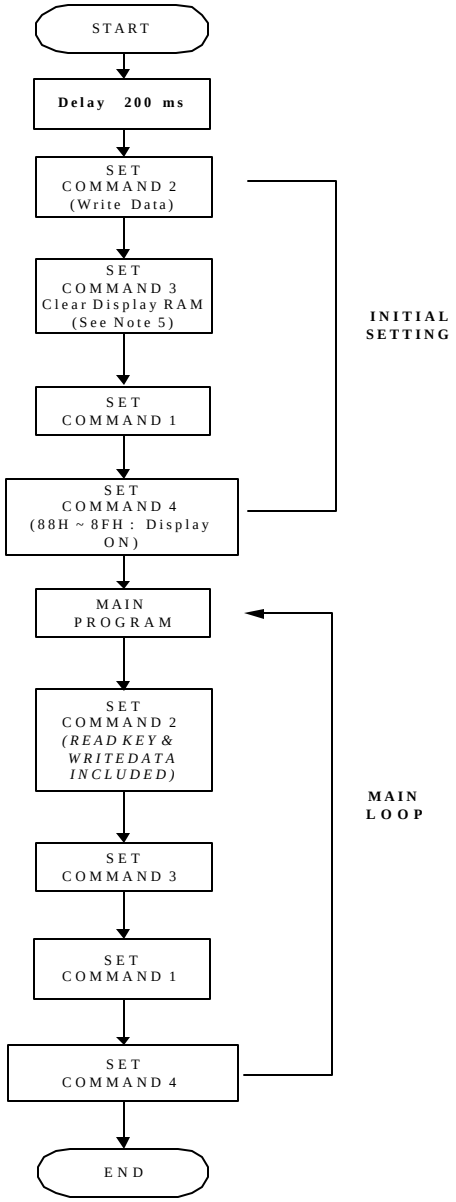
The following diagram shows the waveforms when updating specific addresses.



where: Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

Figure 16: Address Update

RECOMMENDED SOFTWARE FLOWCHART



Note: 1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3 : Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

Figure 17: Recommended Software Flowchart

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD}	-0.5 to +7	Volts
Driver Supply Voltage	V_{EE}	V_{DD}+0.5 to V_{DD}- 40	Volts
Logic Input Voltage	V_I	-0.5 to V_{DD}+0.5	Volts
VFD Driver Output Voltage	Vo	V_{EE}-0.5 to V_{DD}+0.5	Volts
LED Driver Output Current	I_{OLED}	+25	mA
VFD Driver Output Current	I_{OVFD}	-40 (Grid) -15 (Segment)	mA

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-20 to +70°C, GND=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	0.7V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	-	0.3V_{DD}	V
Driver Supply Voltage	V_{EE}	V_{DD}-35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, V_{DD}=5V, GND=0V, V_{EE}=V_{DD}-35 V, Ta=25°C)μ

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-Level Output Voltage	V_{OHLED}	I_{OHLED} = -1mA LED1 to LED5	0.9V_{DD}	-	-	V
Low-Level Output Voltage	V_{OLLED}	I_{OLLED} = +20mA LED1 to LED5	-	-	1	V
Low-Level Output Voltage	V_{OLDOUT}	D_{OUT}, I_{OLDOUT} = 4mA	-	-	0.4	V
High-Level Output Current	I_{OHSG}	Vo = V_{DD}-2V SG1 to SG12	-3	-	-	A
High-Level Output Current	I_{OHGR}	Vo = V_{DD}-2V GR1 to GR8, SG13/GR116 to SG20/GR9	-15	-	-	mA
High-Level Input Voltage	V_{IH}	-	0.7V_{DD}	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	-	0.3V_{DD}	V
Oscillation Frequency	fosc	R=56 KOhms	350	500	650	KHz
Input current	I_I	V_I = V_{DD} or V_{SS}	-	-	±1	μA
Dynamic Current Consumption	I_{DDdyn}	Under no load Display OFF	-	-	5	mA

12-GRID X 16-SEGMENT VFD APPLICATION CIRCUIT

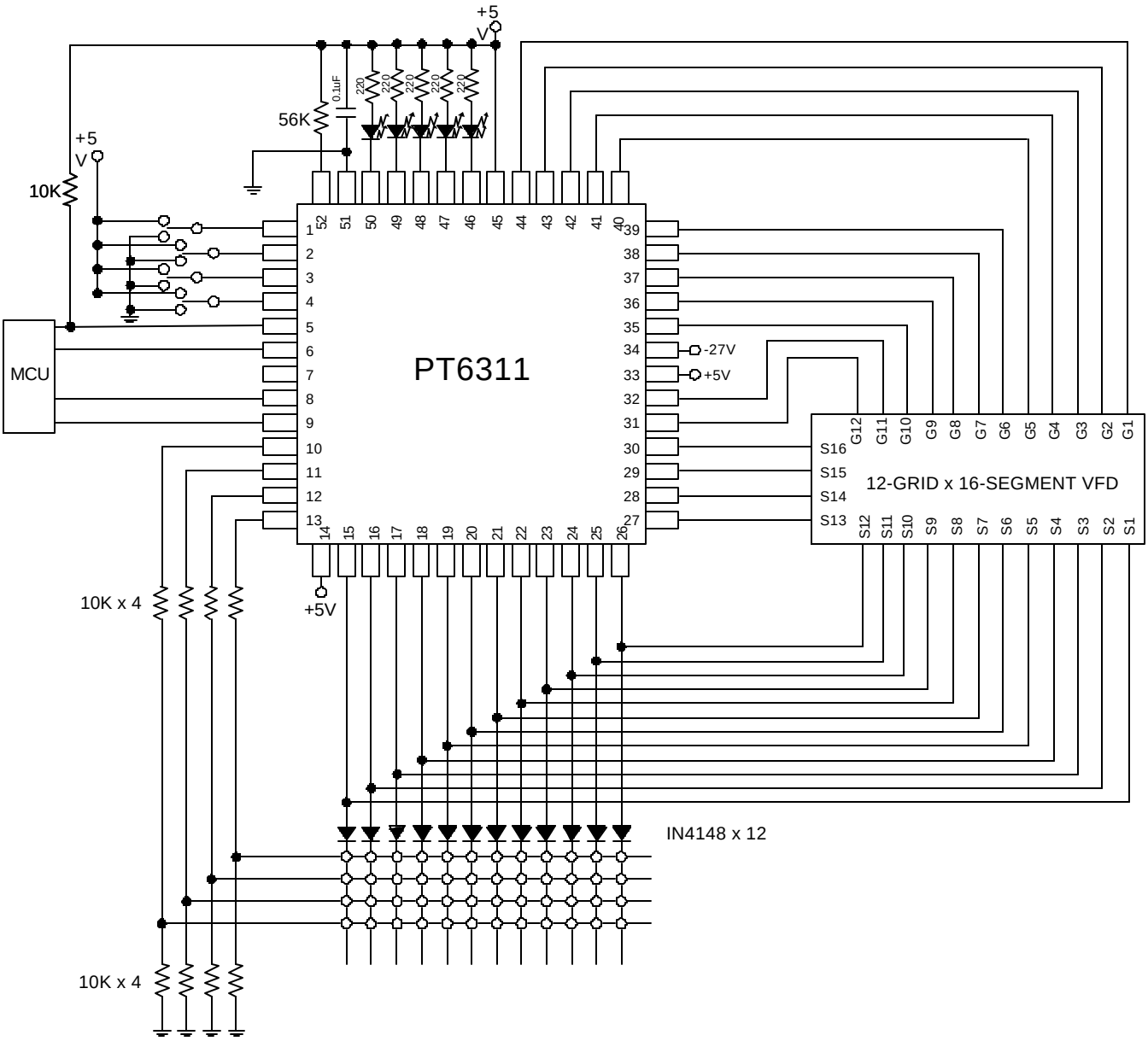
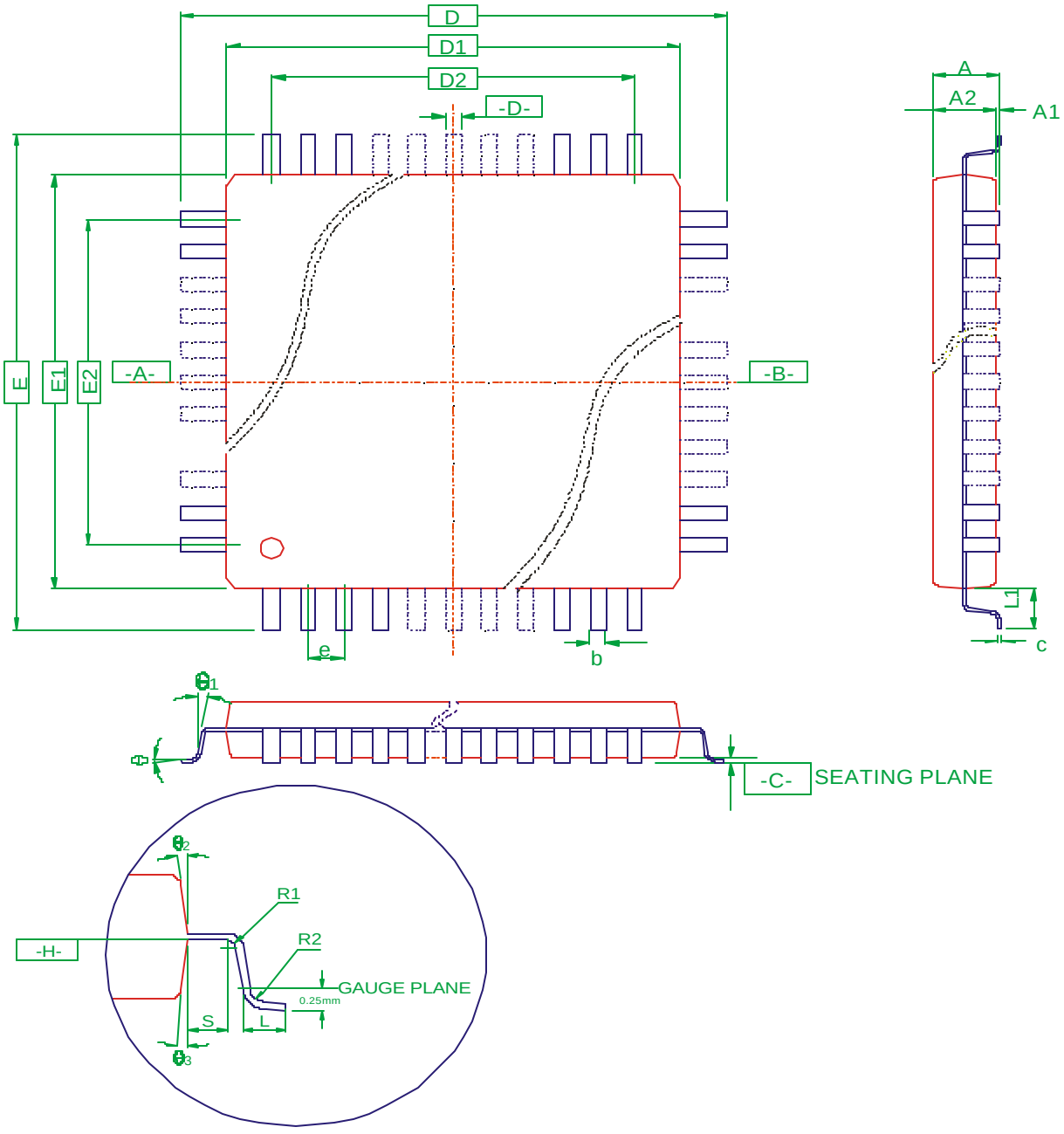


Figure 18: PT6311 Application Circuit

PACKAGE INFORMATION

52-Pin , QFP Package (Body Size; 14mm x 14mm, Pitch=1.00mm)



Symbol	Min.	Nom.	Max
A	-	-	3.15
A1	0.00	-	0.25
A2	2.50	2.70	2.90
b	0.34	-	0.50
D		17.20 BSC	
D1		14.00 BSC.	
D2		12.00 REF	
E		17.20 BSC	
E1		14.00 BSC	
E2		12.00 REF	
e		1.00 BSC	
L	0.73	0.88	1.03
L1		1.60 BSC	
R1	0.13	-	-
R2	0.13	-	0.30
θ	0°	–	7°
θ1	0°	–	–
θ2	5°	–	16°
θ3	5°	–	16°

Notes:

1. All dimensioning and tolerancing dimension conform to ASME Y14.5M-1994
2. Datum plane "H" is located at the bottom of the mold parting line coincident with where the lead exits the body.
3. Datums "A-B" and "D" to be determined at datum plane "H".
4. To be determine at seating plane "C".
5. Dimensions "D1" and "E1" do not include mold protrusion, allowable protrusion is 0.25 mm per side, dimensions "D1" and "E1" do include mold mismatch and are determined at datum plane "H".
6. Details of Pin1 identifier are optional but must be located within the zone indicated.
7. Regardless of the relatie size of the upper and lower body sections, dimensions "D1" and "E1" are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
8. All dimensions are in millimeters.
9. Dimension "b" do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed "b" maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
10. Exact shape and size of this feature is optional.
11. N= the number of lead (N=52)
12. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
13. "A1" is defined as the distance from the seating plane to the lowest point of the package body.
14. Please refer to JEDEC MS-022, Variation BD.

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