SG73/D
REV 22

MOTOROLA

SEMICONDUCTOR PRODUCTS SECTOR

MASTER PRODUCT SELECTION GUIDE

Digital DNA
From Motorola

NOTES

NOTES

MOTOROLA

Master Product Selection Guide

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of semiconductor devices any license under the patent rights to the manufacturer.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Printed in U.S.A.

Please note that only some of the information in this Selector Guide has been updated to reflect the new Motorola Semiconductor Product Sector realignment.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of semiconductor devices any license under the patent rights to the manufacturer.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Printed in U.S.A.

REV 7

Master Product Selection Guide

What We Do . . .

As the world's #1 producer of embedded processors, Motorola's SPS offers multiple DigitalDNA™ solutions which enable its customers to create new products that bring new comfort and convenience to every aspect of your life. Today there are more than 8 billion SPS chips in systems worldwide. Motorola chips are creating systems capabilities never envisioned just a few years ago.

We call this the DigitalDNA promise – the essential ingredient from Motorola that makes products smarter, that works as your ingenious ally to help make products you use anticipate your needs and improve your quality of life.

But, we provide more than just chips. We also provide the software, development tools and use 50+ years of experience to assure our customers have a satisfying experience. In addition, we provide a wide range of analog and digital semiconductors that are used in virtually every type of electronic equipment.

How To Use This Guide. . .

This selection guide is a compendium of products from Motorola Semiconductor Products Sector organized by product family. This printed selection guide contains information which was garnered from the Motorola SPS web site as of September 1, 1999. The most current information is available at http://motorola.com/sps/.

The guide is arranged to provide three–way assistance to engineers and technicians in making a first–order selection of components best suited for a specific circuit or system design.

If you have a device number that needs identification or if you want to know if Motorola manufactures a particular device type:

1. Turn to the Device Index for a complete listing of Motorola products, and the page numbers where more detailed information is given for these products.

If you have a device name or acronym and wish to know if Motorola makes such a device:

2. Look for it in the Subject Index.

If you want an overview of Motorola products for a specific product category:

3. Refer to the General Index located at the back of this publication, or use the table of contents located at the front of each section.

Product Information and Literature Requests

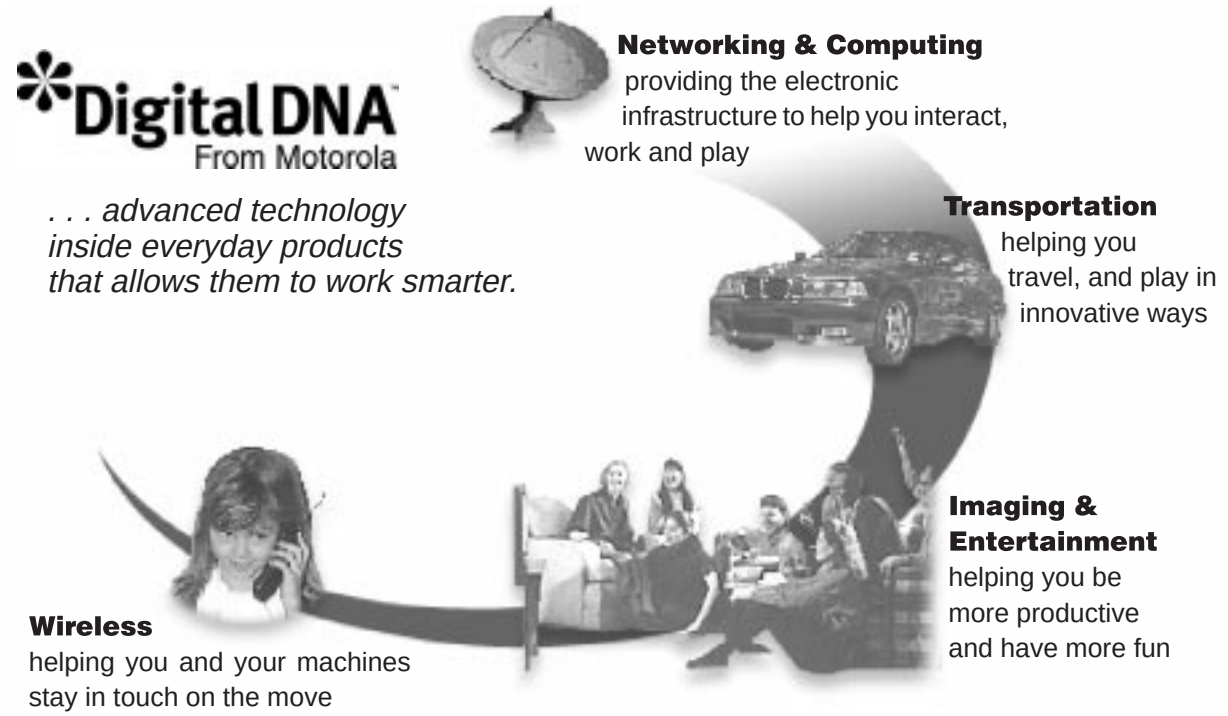
For general product information and to order technical literature by specific document title, i.e., SGXX/D or DLXXX/D, or by part number only:

Phone: Worldwide 1–303–675–2140
North America Only 1–800–441–2447

Hours: 7:00 am MST, USA (14:00 GMT) to 5:00 pm MST, USA (00:00 GMT)

Email: ldcformotorola@hibbertco.com

SPS Major Market Business Units



SPS has four major market business units to serve key customer segments around the world. These include:

Networking and Computing Systems Group:

Focuses on networking systems, communication transmission and access, wireless infrastructure, personal and enterprise computing and high performance memory technologies.

Transportation Systems Group:

Centered on automotive powertrain and intelligent transportation systems, safety and chassis, body electronics and systems electronics and sensor technologies.

Wireless Subscriber Systems Group:

Provides customers with world–class wireless platforms, radio and intermediate frequency technologies, in addition to leadership wireless messaging and emerging new media technologies.

Imaging and Entertainment Solutions:

Focuses on Imaging Systems (hard–copy imaging and multifunction peripherals), Consumer Broadcast (SDTV and HDTV), and Media Platforms (home–based entertainment systems).

Table of Contents

Table of Contents

Table of Contents

Digital Television and Set–Top Box

1

In Brief . . .

Designing the Future of Entertainment

Digital Television is upon us. After years of writing standards and designing protocols, a new era in broadcast will now drastically change the way we view TV. Motorola has joined with Sarnoff Corporation in developing components for true high definition Digital Television sets. Also included in this portfolio are devices for standard definition Digital Televisions and converter boxes which allow the reception of a high definition signal to be displayed as standard analog video. The Motorola/Sarnoff team is focused on the worldwide market which includes both the ATSC and DVB standards. This intelligent partnership will lead the Digital Television movement.

Set–Top Box is one of the most innovative and fastest growing markets in consumer electronics today. Sales in digital Set–Top Box are expected to reach 53 million units by the year 2005 compared to 11.5 million at the end of 1998. The digital revolution brings new and exciting ideas that provide not only exceptional picture quality but also an impressive interactive feature that makes your Set–Top Box a home media terminal. Through advanced CMOS design, Motorola provides the end–to–end solution for all of the home terminal needs. Design and application teams are all focused in system design for all broadcast standards throughout the world.

MCT2100

ATSC Digital VSB Digital Demodulator with Forward Error Correction

1

The MCT2100 demodulator is a single–chip all digital passband demodulator which implements a digital vestigial sideband (VSB) demodulator and forward error correction (FEC) for the reception of terrestrial broadcasts using 8 VSB over a 6 MHz channel. It fully meets the approved FCC standard for terrestrial DTV broadcast using VSB modulation. The MCT2100 will be available in a 144–pin plastic surface mount package (PQFP).

The MCT2100 design offers a high performance, low–cost and low–complexity system–level solution for the design of DTV or Data Broadcast receiver systems using MPEG 2 system data packets such as:

- HDTV
- SDTV
- PCTV
- Set–top box

An example of an SDTV Block Diagram is shown in Figure 1.

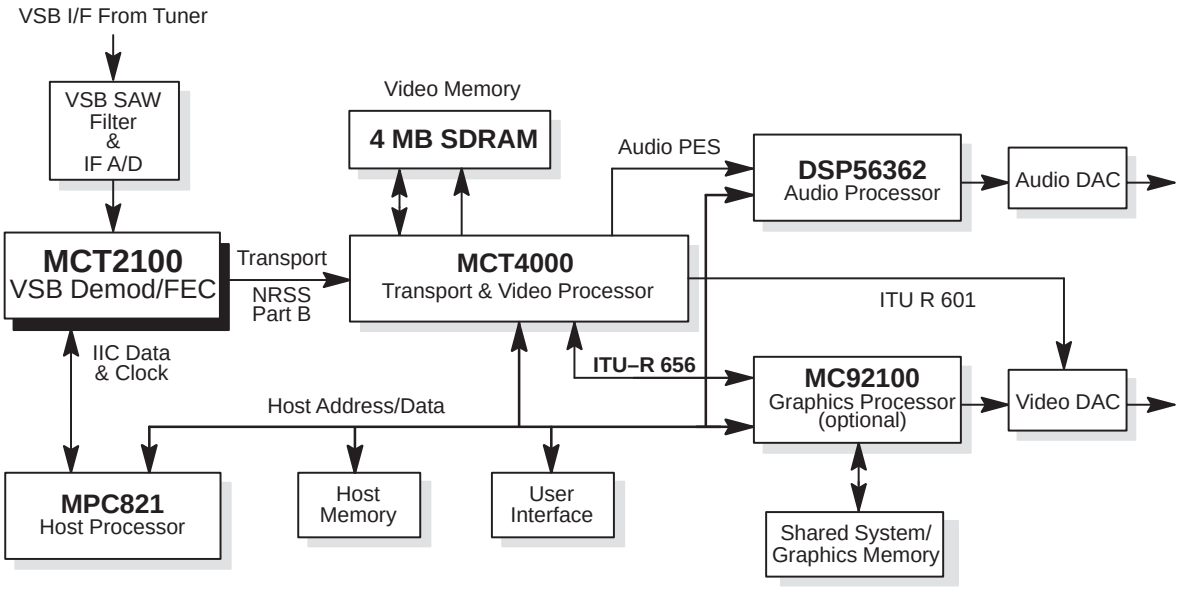


Figure 1. SDTV Block Diagram

Other DTV Devices

- MCT2100 VSB Demodulator
- MPC821 PowerPC™ Host Processor
- DSP56362 Audio Decoder
- MC92100 Scorpion Video/Graphics Display Engine
- MC92110 Scorpion II Video/Graphics Display Engine
- MCxxxxx Scorpion HDTV Graphics Display Engine
- MCT6000 HDTV Transport Demux and Video Processor

MCT4000

ATSC Digital Television Video Processor

The MCT4000 is a transport and video processor for digital television applications implementing the Advanced Television Systems Committee (ATSC) standards. It is applicable to converter boxes enabling the reception of ATSC signals for display on an NTSC receiver, or to Standard Definition Televisions (SDTV). An example diagram of an SDTV receiver is shown in Figure 2.

This device provides the MPEG–2 transport parsing function for an entire system, and decodes an MPEG–2 Main Profile at High Level video Program Elemental Stream (PES). All ATSC recommended formats are accepted, and resized as necessary, to provide a 480 line x 720 pixel interlaced or progressive output. A proprietary compression scheme is utilized to produce a downsized image of excellent quality, while requiring only 4MB of external SDRAM for video memory. The MCT4000 video post–processing capability includes adaptation of aspect ratio and frame rates, overlay of on–screen display, and conversion to NTSC output signals. The IC interfaces to an external video SDRAM, the system host processor, the audio decoder, demodulator/FEC, and an optional enhanced graphics processor.

Key Features

- MPEG–2 Systems transport processor
- MPEG–2 Main Profile at High Level decoder
- Compression of image data reduces video memory usage to 4MB
- Decompression and postfiltering provide excellent picture quality
- On–Screen display and graphics processing
- Interfaces for external host microprocessor, audio processor
- NTSC encoder
- Bi–directional ITU R–656 interface for accepting digitized analog video input or connections to a robust graphics engine and scanning electronics
- Industry standard 272 PBGA or 240 PQFP package
- 1.8 V operation, 3.3 V I/O

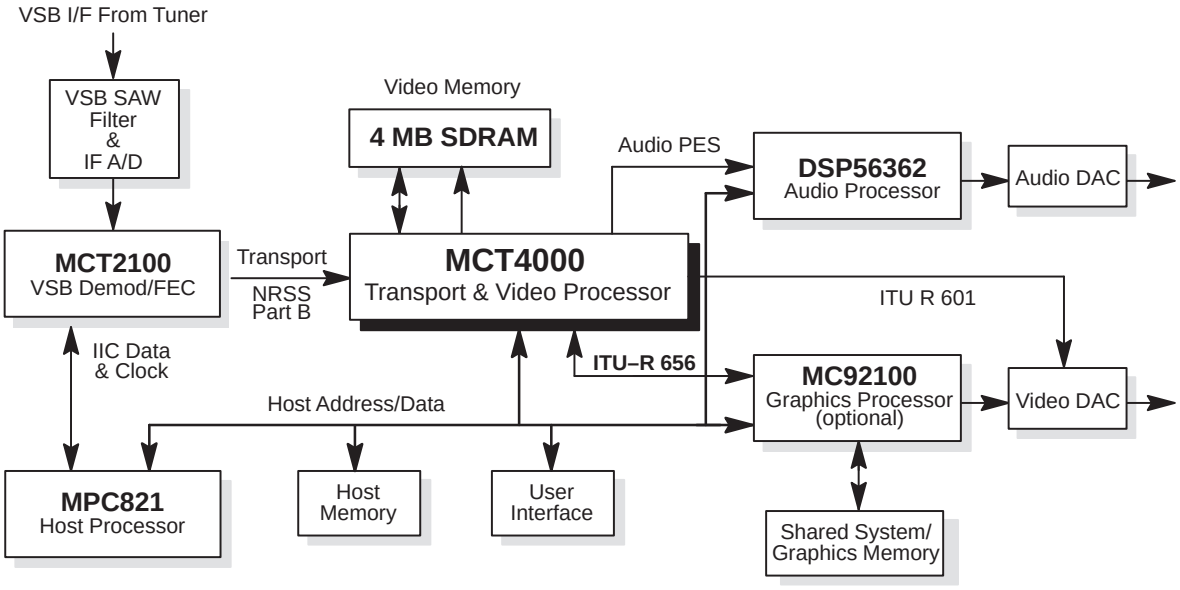


Figure 2. SDTV Block Diagram

MC92314/MC92315

Integrated DVB–T Demodulator

The MC92314/5 is a DVB–T compliant demodulator for 2 K or 8 K transmission mode according to the ETSI specification for digital terrestrial broadcasting (ETS 300744). The MC92314/5 contains all the functionality required to demodulate and decode DVB–T compliant broadcast signals.

1

Feature Summary

- Usable for 8 MHz/7 MHz/6 MHz channels by adjusting the clock rate
- 2 K and 8 K transmission modes supported by MC92315 (MC92314 is 2 K only)
- Digital I/Q separation on–chip
- Digital AFC on chip
- Supports QPSK, 16–QAM and 64–QAM (non–hierarchical for MC92314)
- Supports all guard interval lengths (1/32, 1/16, 1/8, 1/4)
- Automatic locking to any DVB–T guard interval
- Accepts 8–bit TTL–compatible twos–complement and offset–binary data input
- Provides control signals for AGC and ADC clock frequency control
- Viterbi Decoder for DVB convolutional code rates 1/2, 2/3, 3/4, 5/6 and 7/8
- Reed/Solomon Decoder for DVB Reed–Solomon code (204,188,8)
- I^2C serial bus compatible interface (M–Bus) for external programming and control
- Operating voltage 3.3 V for MC92314, 1.8 V for MC92315
- Power requirement 1.7 W
- Pin compatability with a 160PQFP

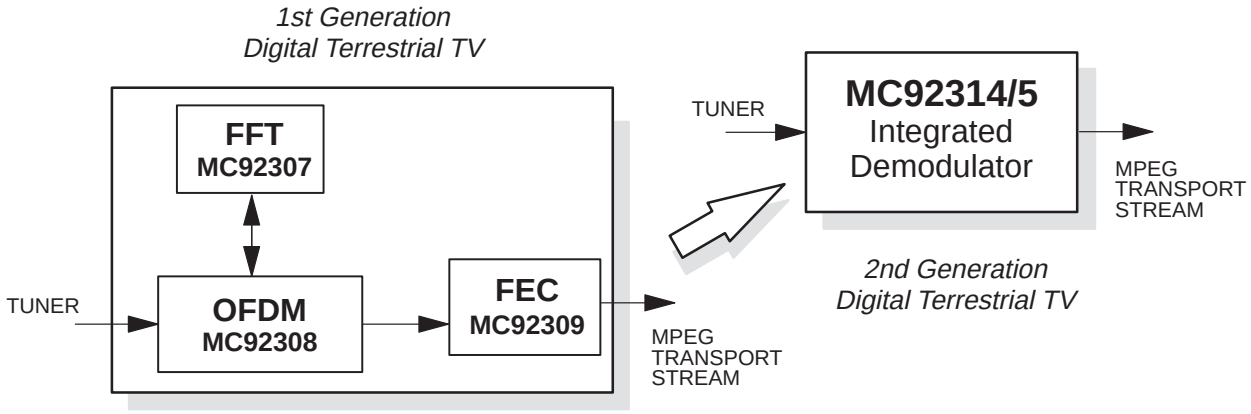


Figure 3. DVB–T Demodulator Block Diagram

PCF20012

MPEG–2 Audio/Video Decoder, Transport Stream Demultiplexer and Digital Video Encoder

The PCF20012 is designed to achieve high performance at a low system cost. It combines an MPEG–2 main profile/main level and DigiCipherll™ video decoder, a Dolby AC–3 audio decoder, a transport stream demultiplexer, a high quality digital video encoder and audio/video DACs for use in digital set–top box systems.

PCF20012 Features

- MPEG–2 Main Profile, Main Level (MP@ML) / DigiCipherll compliant video decoder
- Dolby AC–3 5.1 channel audio decoder with downmixing into two channels
- Accepts either a VideoCipherll or standard broadcast signal when in analog mode
- Glueless interface to the MC68331 asynchronous bus
- DigiCipherll/MPEG2 Transport Stream (TS) demultiplexer
- CCIR–656 video output for interface with an external graphics engine
- Flexible memory configurations for low system costs
- OSD with 8–bit graphics generation
- Video–graphics mixing in 16 levels
- High performance Digital Video Encoder (DVE) with triple video DAC
- 16–bit Sigma–Delta converter — D/A for high quality audio
- Support of Composite and S–VHS video outputs
- 256BGA package

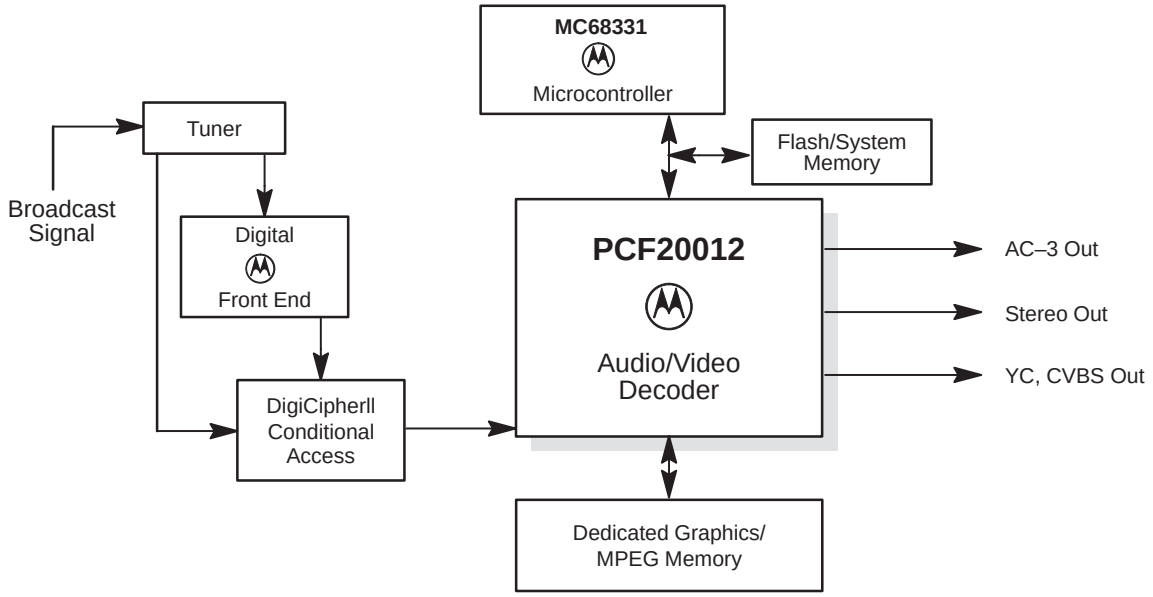


Figure 4. The PCF20012 in a Broadcast Video System

MC92100

Graphics Display Generator, SDRAM Controller, and Digital Video Encoder

1

The Scorpion chip (MC92100) is a graphics display generator and NTSC/PAL digital video encoder for analog and digital video systems including Digital Versatile Disk (DVD), Set–Top Box (STB), and Internet TV applications. The display architecture has been designed to provide a high–quality television–oriented graphics overlay. The graphics overlay matches the resolution and color depth of NTSC/PAL baseband video and optimizes memory usage. The MC92100 can provide generation of true color graphics, mixing of video and graphics, and control and display on four image layers. The MC92100 is controlled by high–level language instructions from a host processor (PowerPC™ or Coldfire™).

The Scorpion's digital video encoder accepts a CCIR–656 data stream with embedded synchronization codes or it may be genlocked with a television horizontal flyback and vertical synchronization signal. The MC92100 supports either composite and separate luma and chroma output (S–VHS) analog video generation, or composite and RGB. It also supports a closed caption inserter. The MC92100 includes Macrovision™ generation for copy protection and The MC92101 removes this feature.

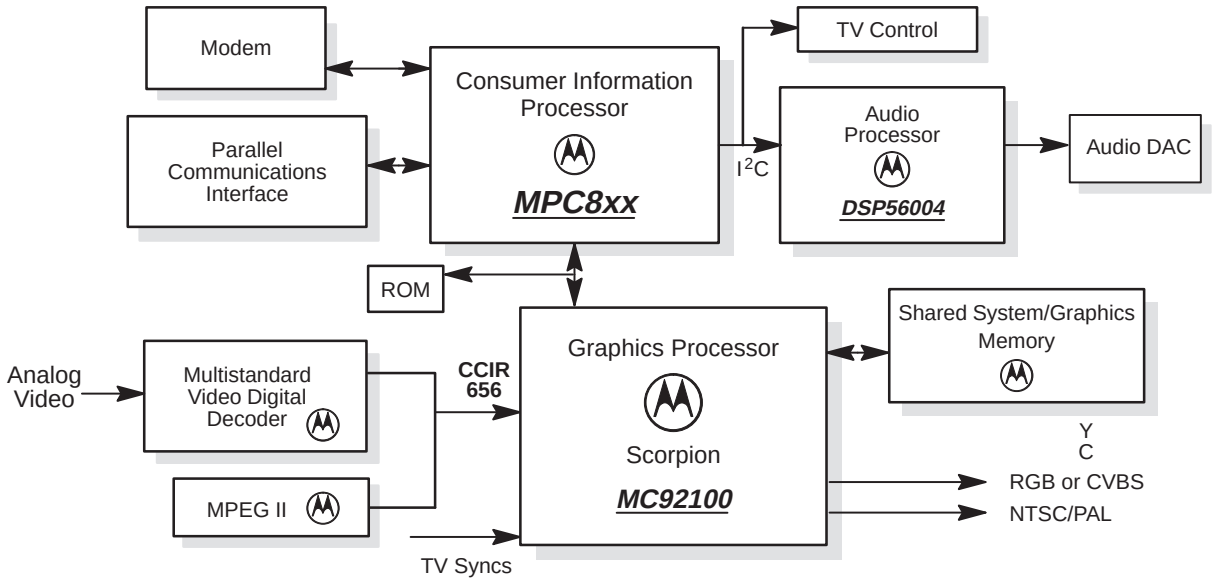


Figure 5. Scorpion in an Analog/Digital Video System

ORION — MCF40001

Integrated MPEG–2 Decoder with Graphic Processor for Digital Set Top Box Applications

The MCF40001 is an integrated MPEG–2 decoder which combines a graphic processor with a programmable MPEG–2 Transport Stream (TS) demultiplexer, MPEG–2 video decoder, AC–3 audio decoder and two smart card interface modules. The MCF40001 is designed specifically to be used in Digital Set Top Box (DSTB) applications while delivering enhanced performance and maintaining low system costs. The MCF40001 greatly reduces the time required for system design and implementation by packaging common system functions on chip and providing interfaces to a PowerPC MPC8xx family Host processor, SDRAMs, Smart Cards, video and audio I/O devices.

To enable the MCF40001 to demultiplex MPEG–2 Transport Stream, a separate dedicated on–chip RISC processor is included — the demultiplexing function is implemented as a programmable module containing its own microcode for maximum flexibility. The MPEG–2 video decoder is a Main Profile, Main Level decoder which supports both PAL and NTSC systems at full resolution. The MCF40001 employs a dual–plane graphic architecture which allows multiple images to be overlaid using a combination of transparency and translucency, implemented on either a pixel by pixel basis or a screen region basis. The MCF40001 also contains a 5.1 channel AC–3 audio decoder and PCM audio generator with SPDIF, I^2S and analog audio outputs.

MCF40001 Features

- Two MPEG–2 Transport Stream inputs for In–band and Out–of–band streams up to 60 Mbps for combined stream
- 32 PID filters applied to the combined bitstream
- 32 section filters with up to 16 bytes of filter data and bit–masking capability
- In–Band Transport Stream high–speed serial output
- MPEG–2 Main Profile, Main Level (MP@ML) compliant video decoder
- Decoding of full and low resolution NTSC/PAL pictures
- 16:9 aspect ratio pictures are imaged on 4:3 displays by pan–scan or letterbox conversion
- External Video input through ITU–R BT .656 interface as an alternative video source to MPEG video
- Scaling down of video source to any arbitrary size
- Two Graphic layers overlay with true–color graphics for NTSC/PAL in full or low resolution
- Video and graphics mixing in 128 mixing levels with per viewport, pixel or color mix ratio definition
- Hardware cursor with position register and image–address register
- Graphic images in RGB or YCbCr color formats or 2/4/8 bit per pixel Color Look–up Table
- Transparent pixels allow cursor and graphic images to appear in any arbitrary shape
- Capturing of a video frame for further usage as a graphic image
- A Bit Blitter block for moving, copying or mixing graphic images
- Aspect ratio conversion and anti–flicker vertical filter for computer–generated graphic images
- On–chip Digital Video Encoder and triple video DAC for generation of composite and S–VHS analog video
- AC–3 5.1 channel audio decoder with downmix to 2 channels
- PCM audio generator and two on–chip audio DACs
- SPDIF interface to external audio decoder and two I^2S interfaces to external audio DACs
- 2 Smart Card Interfaces
- 3.3 V operation
- 272 pin Ball Grid Array package

1

Microcomputer Components

2

In Brief . . .

Motorola continues to be a leading supplier of components for microcomputer systems. The product portfolio includes digital signal processors; RISC and PowerPC advanced microprocessors and complementary full–function peripherals; a comprehensive selection of high–performance microcontrollers; VLSI functions for Local Operating Network applications; and a broad range of fast static RAM chips.

Our commitment is to provide state–of–the–art devices as well as continuing support of established products, with six–sigma quality and total customer satisfaction.

2

Digital Signal Processors

2

In Brief . . .

Drawing on both design excellence and expertise in manufacturing, Motorola has created a range of architecturally compatible digital signal processing chips. The philosophy behind the Digital Signal Processor (DSP) families has been to create compatibility between products, as well as to conform to international standards.

Motorola offers a complete portfolio of 16- and 24-bit fixed point DSPs.

In addition, we offer a comprehensive array of development tools to give the designer access to the full power and versatility of the DSPs with minimum fuss. All the tools were designed for ease of use and functionality. They provide a low-cost means of evaluation and greatly simplify the design and development phase of a DSP project.

16-/24-/32-Bit Families—Your Complete DSP Solution

DSP56000—24-Bit Digital Signal Processors

The DSP56000 family of 24-bit, fixed point, general purpose Digital Signal Processors is Motorola's original DSP family and has set the standard for high end DSP devices with its triple Harvard architecture of seven internal buses and three parallel execution units—Data ALU, Address Generation Unit, and Program Controller. Motorola has retained architectural compatibility with the 24-bit family into the high performance DSP56800 products helping to preserve our customer software investment.

2

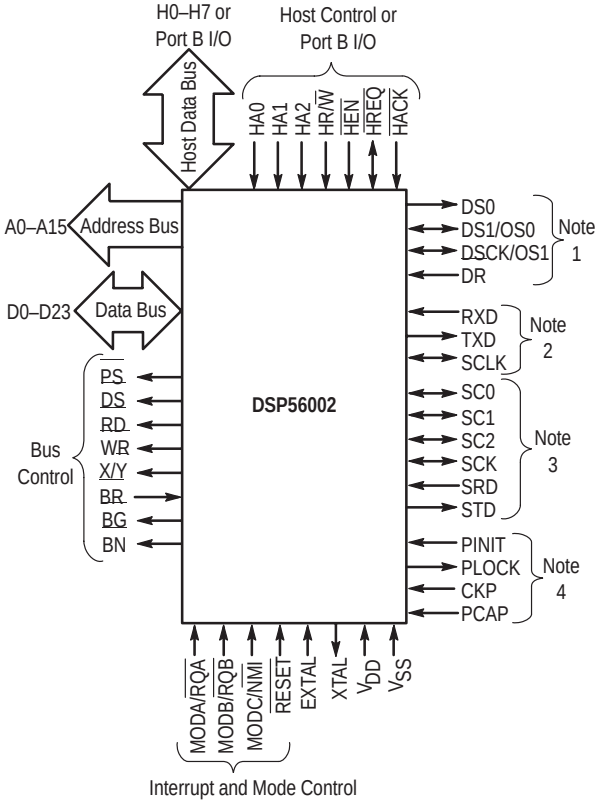
The DSP56000 family of HCMOS, 24-bit DSP devices consists of the DSP56002, DSP56004, DSP56007, DSP56009, and DSP56011. All these products are source code compatible and are used extensively in telecommunications, control, and audio applications. The DSP56000 family's unique 24-bit architecture has made these products the industry standard for CD-quality digital audio processing.

DSP56000 Core Features

- Efficient, object code compatible, 24-bit 56000 family DSP engine
  - — Up to 40 Million Instructions Per Second (MIPS)
  - — 25 ns instruction cycle at 80 MHz
  - — Up to 240 Million Operations Per Second (MOPS) at 80 MHz
  - — Performs a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56-bit accumulators including extension byte
  - — Parallel 24 x 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48 x 48-bit multiply with 96-bit result in 6 instruction cycles
  - — 56-bit Addition/Subtraction in 1 instruction cycle
  - — Fractional and integer arithmetic with support for multiprecision arithmetic
  - — Hardware support for block-floating point FFT
  - — Hardware nested DO loops
  - — Zero-overhead fast interrupts (2 instruction cycles)
  - — Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- Two 256 x 24-bit on-chip data RAMs
- Two 256 x 24-bit on-chip data ROMs containing sine, A-law, and μ-law tables
- Two 256 x 24-bit on-chip data ROMs containing sine, A-law, and μ-law tables
- External memory expansion with 16-bit address and and 24-bit data buses
- 512 x 24-bit on-chip Program RAM and 64 x 24-bit bootstrap ROM
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface



NOTES:
1. On-Chip Emulation (OnCE™) port
2. SCI Serial or Port C I/O
3. SSI Serial or Port C I/O
4. Phase Lock Loop (PLL)

DSP56000—24-Bit Digital Signal Processors (continued)

Peripheral and Support Circuits

- Byte-wide host interface (HI) with Direct Memory Access (DMA) support (or fifteen Port B GPIO lines)
- SSI support:
  - — Supports serial devices with one or more industry–standard codecs, other DSPs, microprocessors, and Motorola–SPI–compliant peripherals
  - — Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
  - — Network mode using frame sync and up to 32 software–selectable time slots
  - — 8–bit, 12–bit, 16–bit, and 24–bit data word lengths
- SCI for full duplex asynchronous communications (or three additional Port C GPIO lines)
- One 24–bit timer/event counter (or one additional GPIO line)
- Up to twenty–five General Purpose Input/Output (GPIO) pins
- Double–buffered peripherals
- One non–maskable and two maskable external interrupt/mode control pins
- On–Chip Emulation (OnCE™) port for unobtrusive, processor speed–independent debugging
- Software–programmable, Phase Lock Loop–based (PLL) frequency synthesizer for the DSP core clock with a wide input frequency range (12.2 KHz to 80 MHz)

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for specified operating frequency down to dc
- Three packages available:
  - — 132-pin Plastic Quad Flat Pack (PQFP); 1.1 x 1.1 x 0.19 inches
  - — 144-pin Thin Quad Flat Pack (TQFP); 20 x 20 x 1.5 mm
  - — 132-pin Ceramic Pin Grid Array (PGA); 1.36 x 1.35 x 0.125 inches

DSP56004/DSP56007 Features

Digital Signal Processing Core

- Efficient, object-code compatible, 24-bit DSP56000 family DSP engine

Memory

- DSP56004 memory: 512 words Program RAM, 2 x 256 words data RAM, 2 x 256 words data ROM
- DSP56007 memory: 6400 words Program ROM, 3200 words data RAM, 1024 words data ROM

Peripheral and Support Circuits

- Serial Audio Interface (SAI) includes 2 receivers and 3 transmitters, master or slave capability, and implementation of I^2S, Sony, and Matshushita audio protocols; two sets of SAI interrupt vectors
- Serial Host Interface (SHI) features single master capability, 10-word receive FIFO, and support for 8-, 16-, and 24-bit words
- External Memory Interface (EMI), implemented as a peripheral supporting:
  - — Page-mode DRAMs (one or two chips): 64 K x 4, 256 K x 4, and 4M x 4 bits
  - — SRAMs (one to four): 256 K x 8 bits
  - — Data bus may be 4 or 8 bits wide
  - — Data words may be 8, 12, 16, 20, or 24 bits wide
- Four dedicated, independent, programmable General Purpose I/O (GPIO) lines
- On-chip peripheral registers memory mapped in data memory space
- Three external interrupt request pins
- On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the core clock
- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 40, 50, 66, and 80 MHz down to DC
- 80-pin plastic Quad Flat Pack surface-mount package; 14 x 14 x 2.45 mm; 0.65 mm lead pitch
- 3.3 V (DSP56L007) and 5 V (DSP56007) power supply options

DSP56009 Features

Digital Signal Processing Core

- Efficient, object-code compatible, 24-bit DSP56000 family DSP engine
- Completely pin-compatible with DSP56004 and DSP56007 for easy upgrades
- 5 V power supply

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories

DSP56000—24-Bit Digital Signal Processors (continued)

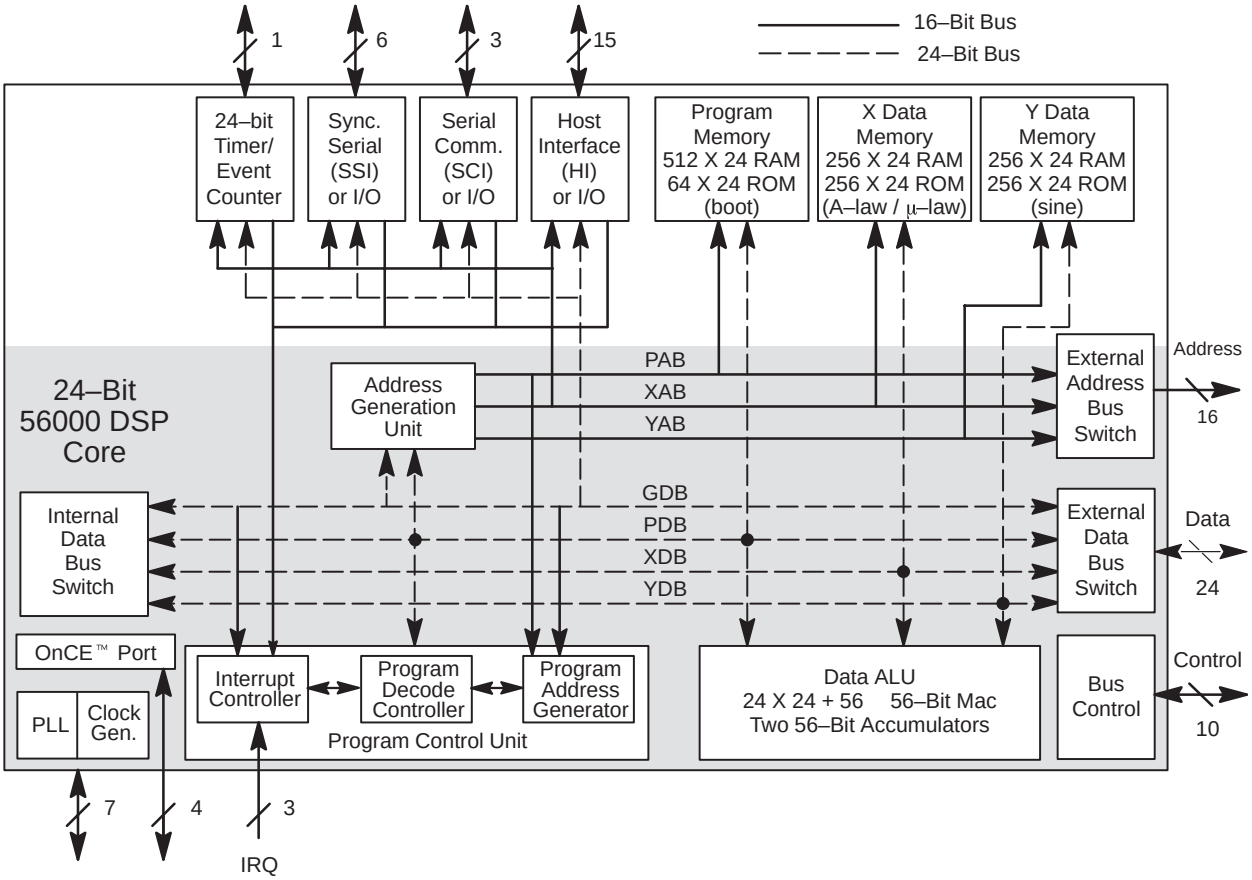
- 10240 x 24-bit on-chip Program ROM*
- 4608 x 24-bit on-chip X data RAM and 3072 x 24-bit on-chip X data ROM*
- 4352 x 24-bit on-chip Y data RAM and 1792 x 24-bit on-chip Y data ROM*
- 512 x 24-bit on-chip Program RAM and 64 x 24-bit bootstrap ROM
- Up to 2304 x 24-bit from X and Y data RAM can be switched to Program RAM giving a total of 2816 x 24 bits of Program RAM
- Bootstrap loading from Serial Host Interface or External Memory Interface

*These ROMs may be factory programmed with data/program provided by the application developer.

DSP56002/L002—24-Bit Digital Signal Processor

2

The DSP56002 and the DSP56L002 are MPU–style general purpose Digital Signal Processors (DSPs), composed of an efficient 24–bit digital signal processor core, program and data memories, various peripherals, and support circuitry. The 56000–Family–compatible DSP core is fed by on–chip program RAM, two independent data RAMs, and two data ROMs with sine and A–law and μ–law tables. The DSP56002/L002 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), Timer/Event Counter, Phase–Locked Loop (PLL), and On–chip Emulation (OnCE™) port. This combination of features, illustrated in the following figure, makes the DSP56002/L002 a cost–effective, high–performance solution for high–precision general–purpose digital signal processing.



DSP56002/L002 Block Diagram

DSP56002/L002—24-Bit Digital Signal Processor (continued)

Features

Digital Signal Processing Core

- Efficient, object code compatible, 24–bit 56000–Family DSP engine
  - — Up to 33 Million Instructions Per Second (MIPS) - 30.3 ns instruction cycle at 66 MHz
  - — Up to 198 Million Operations Per Second (MOPS) at 66 MHz
  - — Performs a 1024–point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56–bit accumulators including extension byte
  - — Parallel 24 x 24–bit multiply–accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48 48–bit multiply with 96–bit result in 6 instruction cycles
  - — 56–bit Addition/Subtraction in 1 instruction cycle
  - — Fractional and integer arithmetic with support for multiprecision arithmetic
  - — Hardware support for block–floating point FFT
  - — Hardware nested DO loops
  - — Zero–overhead fast interrupts (2 instruction cycles)
  - — Four 24–bit internal data buses and three 16–bit internal address buses for maximum information transfer on–chip

Memory

- On–chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 512 x 24–bit on–chip program RAM and 64 x 24–bit bootstrap ROM
- Two 256 x 24–bit on–chip data RAMs
- Two 256 x 24–bit on–chip data ROMs containing sine, A–law and μ–law tables
- External memory expansion with 16–bit address and 24–bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

Peripheral and Support Circuits

- Byte–wide Host Interface (HI) with direct memory access support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
  - — Up to 32 software–selectable time slots in network mode
- Serial Communication Interface (SCI) for full–duplex asynchronous communications
- 24–bit Timer/Event Counter also generates and measures digital waveforms
- On–chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Up to 25 general purpose I/O (GPIO) pins
- Three external interrupt request pins; one non–maskable
- On–Chip Emulation (OnCE) port for unobtrusive, processor speed–independent debugging
- Software–programmable, Phase–Locked Loop–based (PLL) frequency synthesizer for the core clock
- Power–saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 66 MHz or 40 MHz down to DC
- 132–pin Ceramic Pin Grid Array (PGA) package; 13 13 array
- 132–pin Plastic Quad Flat Pack (PQFP) surface–mount package; 24 24 4 mm
- 144–pin Thin Quad Flat Pack (TQFP) surface–mount package; 20 x 20 x 1.4 mm
- 3.3 V (DSP56L002) and 5 V (DSP56002) Power supply options

Target Applications

The DSP56002 and DSP56L002 are identical except that the DSP56002 operates at 5 volts, while the DSP56L002 operates at 3.3 volts with a resultant reduction in power consumption and the need for fewer batteries in a portable application.

Documentation

The three documents listed in the following table are required for a complete description of the DSP56002/L002 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center listed on the back page.

DSP56002/L002—24-Bit Digital Signal Processor (continued)

DSP56002/L002 Documentation

Topic	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000–family architecture and the 16–bit core processor and instruction set	DSP56KFAMUM/AD
DSP56002 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56002UM/AD
DSP56002/L002 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56002/D

DSP56300—24-Bit Digital Signal Processors

2

The first programmable Motorola DSP product to provide a true single-clock-cycle execution, the DSP56300 core effectively doubles the number of instructions executed without increasing clock speed, providing 100 MIPS of performance at 100 MHz, while retaining code compatibility with the rest of the Motorola DSP offerings. The DSP56300 family offers a new level of performance in MIPS, a rich instruction set and low power dissipation, enabling a new generation of products in wireless, telecommunications, and multimedia.

Several significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and DMA functionality.

DSP56301 Features

High Performance DSP56300 Core

- 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock at 3.3 V
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU)
  - — Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
  - — 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
  - — Conditional ALU instructions
  - — 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU)
  - — Position Independent Code (PIC) support
  - — Addressing modes optimized for DSP applications (including immediate offsets)
  - — On-chip instruction cache controller
  - — On-chip memory-expandable hardware stack
  - — Nested hardware DO loops
  - — Fast auto-return interrupts
- Direct Memory Access (DMA)
  - — Six DMA channels supporting internal and external accesses
  - — One-, two-, and three- dimensional transfers (including circular buffering)
  - — End-of-block-transfer interrupts
  - — Triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL)
  - — Allows change of low power Divide Factor (DF) without loss of lock
  - — Output clock with skew elimination
- Hardware debugging support
  - — On-Chip Emulation (OnCE™) module
  - — Joint Action Test Group (JTAG) Test Access Port (TAP) port
  - — Address Tracing mode reflects internal Program RAM accesses at the external port

On-Chip Memories

- Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable
- 192 x 24–bit bootstrap ROM

DSP56300—24-Bit Digital Signal Processors (continued)

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache[1]	Switch Mode[2]
4096 x 24–bit	0	2048 x 24-bit	2048 x 24–bit	disabled (CE = 0)	disabled (MS = 0)
3072 x 24–bit	1024 x 24–bit	2048 x 24-bit	2048 x 24–bit	enabled (CE = 1)	disabled (MS = 0)
2048 x 24–bit	0	3072 x 24-bit	3072 x 24–bit	disabled (CE = 0)	enabled (MS = 1)
1024 x 24–bit	1024 x 24–bit	3072 x 24-bit	3072 x 24–bit	enabled (CE = 1)	enabled (MS = 1)

NOTES:
1. Controlled by the Cache Enable (CE) bit in the Status Register (SR)
2. Controlled by the Memory Select (MS) bit in the Operating Mode Register (OMR)

2

Off-Chip Memory Expansion

- Data memory expansion to two 16 M x 24-bit word memory spaces in 24–bit mode or two 64 K x 16–bit memory spaces in 16–bit Compatibility mode
- Program memory expansion to one 16 M x 24-bit words memory space in 24–bit mode or 64 K x 16–bit in 16–bit Compatibility mode
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- On-chip DRAM controller for glueless interface to DRAMs

On-Chip Peripherals

- 32-bit parallel PCI/Universal Host Interface (HI32), PCI Rev. 2.1 compliant with glueless interface to other DSP563xx buses
- ISA interface requires only 74LS45-style buffer
- Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to forty-two programmable General Purpose Input/Output pins (GPIO), depending on which peripherals are enabled

Reduced Power Dissipation

- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to 0 Hz (DC)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

Target Applications

- Multi–channel telecommunication infrastructure
- Multimedia audio and video conferencing

DSP56303 Features

High Performance DSP56300 Core

- 66/80/100 Million Instructions Per Second (MIPS) with a 66/80/100 MHz clock at 3.3 V
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU)
  - — Fully pipelined 24 x 24-bit parallel Multiplier Accumulator (MAC)
  - — 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
  - — Conditional ALU instructions
  - — 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU)
  - — Position Independent Code (PIC) support
  - — Addressing modes optimized for DSP applications (including immediate offsets)
  - — On-chip instruction cache controller
  - — On-chip memory-expandable hardware stack
  - — Nested hardware DO loops
  - — Fast auto-return interrupts
- Direct Memory Access (DMA)
  - — Six DMA channels supporting internal and external accesses
  - — One-, two-, and three-dimensional transfers (including circular buffering)
  - — End-of-block-transfer interrupts
  - — Triggering from interrupt lines and all peripherals

DSP56300—24-Bit Digital Signal Processors (continued)

- Phase Lock Loop (PLL)
  - — Allows change of low power Divide Factor (DF) without loss of lock
  - — Output clock with skew elimination
- Hardware debugging support
  - — On-Chip Emulation (OnCE™) module
  - — Joint Action Test Group (JTAG) Test Access Port (TAP)
  - — Address Tracing mode reflects internal Program RAM accesses at the external port

On-Chip Memories

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable
- 192 x 24-bit bootstrap ROM

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	4096 × 24-bit	0	2048 × 24-bit	2048 × 24-bit
enabled	disabled	3072 × 24-bit	1024 × 24-bit	2048 × 24-bit	2048 × 24-bit
disabled	enabled	2048 × 24-bit	0	3072 × 24-bit	3072 × 24-bit
enabled	enabled	1024 × 24-bit	1024 × 24-bit	3072 × 24-bit	3072 × 24-bit

Off-Chip Memory Expansion

- Data memory expansion to two 256 K x 24-bit word memory spaces (or up to two 4 M x 24–bit word memory spaces by using the Address Attribute AA0–AA3 signals)
- Program memory expansion to one 256 K x 24-bit words memory space (or up to one 4 M x 24–bit word memory space by using the Address Attribute AA0–AA3 signals)
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- On-chip DRAM controller for glueless interface to DRAMs

On-Chip Peripherals

- Enhanced DSP56000-like 8-bit parallel Host Interface (HI08) supports a variety of buses (e.g., ISA) and provides glueless connection to a number of industry standard microcomputers, microprocessors, and DSPs
- Two Enhanced Synchronous Serial Interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to thirty-four programmable General Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled

Reduced Power Dissipation

- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to 0 Hz (DC)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

Target Applications

The DSP56303 is intended for use in telecommunication applications, such as multi-line voice/data/fax processing, videoconferencing, audio applications, control, and general digital signal processing.

DSP56304 Features

- High performance DSP56300 core
  - — 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
  - — Object code compatible with the DSP56000 core
  - — Highly parallel instruction set
  - — Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
  - — 56-bit parallel barrel shifter

DSP56300—24-Bit Digital Signal Processors (continued)

— 24-bit or 16-bit arithmetic support under software control
— Position independent code support
— Addressing modes optimized for DSP applications
— On-chip instruction cache controller
— On-chip memory-expandable hardware stack
— Nested hardware DO loops
— Fast auto-return interrupts
— On-chip concurrent six-channel DMA controller
— On-chip Phase Lock Loop (PLL) and clock generator
— On-Chip Emulation (OnCE™) module
— JTAG Test Access Port (TAP)
— Address Tracing mode reflects internal accesses at the external port

On-Chip Memories

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable
- 33,792 x 24-bit Program ROM with Patch mode update capability using instruction cache memory space
- 9,216 x 24-bit X data ROM and 9,216 x 24-bit Y data ROM
- 192 x 24-bit bootstrap ROM Instruction Cache

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	1024 × 24-bit	0	3328 × 24-bit	1792 × 24-bit
enabled	disabled	0	1024 × 24-bit	3328 × 24-bit	1792 × 24-bit
disabled	enabled	3584 × 24-bit	0	2048 × 24-bit	512 × 24-bit
enabled	enabled	2560 × 24-bit	1024 × 24-bit	2048 × 24-bit	512 × 24-bit

Off-Chip Memory Expansion

- Data memory expansion to two 256 K x 24-bit word memory spaces
- Program memory expansion to one 256 K x 24-bit word memory space
- External memory expansion port
- Chip select logic requires no additional circuitry to interface to SRAMs and SSRAMs
- On-chip DRAM controller requires no additional circuitry to interface to DRAMs

On-Chip Peripherals

- 8-bit parallel Host Interface (HI08), ISA-compatible bus interface, providing a cost-effective solution for applications not requiring the PCI bus
- Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to thirty-four programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled

Reduced Power Dissipation

- Very low power CMOS design
- Wait and Stop low power standby modes
- Fully-static logic, operation frequency down to DC
- Optimized power management circuitry

Target Applications

The DSP56304 is intended for use in embedded multifunction DSP applications requiring large on-board ROM spaces, such as wireless products that combine standard cellular phone operation with options such as two-way digital paging and fax capability in one unit.

DSP56300—24-Bit Digital Signal Processors (continued)

DSP56307 Features

High Performance DSP56300 Core

- 100 Million Instructions Per Second (MIPS)* with a 100 MHz clock at 2.5 V (core) and 3.3 V (Input/Output)
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
- 56-bit parallel barrel shifter
- 24-bit or 16-bit arithmetic support under software control
- Position independent code support
- Addressing modes optimized for DSP applications
- On–chip instruction cache controller
- On–chip memory–expandable hardware stack
- Nested hardware DO loops
- Fast auto–return interrupts
- On–chip concurrent six–channel DMA controller
- On–chip Phase Lock Loop (PLL) and clock generator
- On–chip Emulation (OnCE™) module
- JTAG Test Access Port (TAP)
- Address Tracing mode reflects internal accesses at the external port

2

*170 Million Instructions Per Second using the EFCOP in filtering applications

On-Chip Memories

- 64 K on–chip RAM total
- Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable
- 192 x 24–bit bootstrap ROM

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache	Switch Mode	MSW1	MSW0
16 K x 24–bit	0	24 K x 24-bit	24 K x 24–bit	disabled	disabled	0/1	0/1
15 K x 24–bit	1024 x 24–bit	24 K x 24-bit	24 K x 24–bit	enabled	disabled	0/1	0/1
48 K x 24–bit	0	8 K x 24-bit	8 K x 24–bit	disabled	enabled	0	0
47 K x 24–bit	1024 x 24–bit	8 K x 24-bit	8 K x 24–bit	enabled	enabled	0	0
40 K x 24–bit	0	12 K x 24-bit	12 K x 24–bit	disabled	enabled	0	1
39 K x 24–bit	1024 x 24–bit	12 K x 24-bit	12 K x 24–bit	enabled	enabled	0	1
32 K x 24–bit	0	16 K x 24-bit	16 K x 24–bit	disabled	enabled	1	0
31 K x 24–bit	1024 x 24–bit	16 K x 24-bit	16 K x 24–bit	enabled	enabled	1	0
24 K x 24–bit	0	20 K x 24-bit	20 K x 24–bit	disabled	enabled	1	1
23 K x 24–bit	1024 x 24–bit	20 K x 24-bit	20 K x 24–bit	enabled	enabled	1	1

*Includes 4 K x 24–bit shared memory (i.e., memory shared by the core and the EFCOP)

Off-Chip Memory Expansion

- Data memory expansion to two 256 K x 24-bit word memory spaces
- Program memory expansion to one 256 K x 24-bit word memory space
- External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- On-chip DRAM controller for glueless interface to DRAMs

On-Chip Peripherals

- 3.0 through 3.6 V I/O interface
- General–purpose, fully programmable Enhanced Filter Coprocessor (EFCOP) performs filtering tasks concurrently with the DSP core with minimum core overhead
- 8–bit parallel Host Interface (HI08) supports a variety of buses (e.g., industry–standard architecture) and provides glueless connection to a number of industry–standard microcomputers, microprocessors, and DSPs
- Two Enhanced Synchronous Serial Interfaces (ESSI)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to 34 programmable General–Purpose I/O pins (GPIO), depending on which peripherals are enabled

DSP56300—24-Bit Digital Signal Processors (continued)

Reduced Power Dissipation

- Very low–power CMOS design
- Wait and Stop low–power standby modes
- Fully–static logic, operation frequency down to DC
- Optimized power management circuitry

Target Applications

The DSP56307 is intended for wireless infrastructure applications with general filtering operations.

DSP56309 Features

High Performance DSP56300 Core

- 80/100 Million Instructions Per Second (MIPS) with a 80/100 MHz clock at 3.3 V
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
- 56-bit parallel barrel shifter
- 24-bit or 16-bit arithmetic support under software control
- Position independent code support
- Addressing modes optimized for DSP applications
- On–chip instruction cache controller
- On–chip memory–expandable hardware stack
- Nested hardware DO loops
- Fast auto–return interrupts
- On–chip concurrent six–channel DMA controller
- On–chip Phase Lock Loop (PLL) and clock generator
- On–chip Emulation (OnCE™) module
- JTAG Test Access Port (TAP)
- Address Tracing mode reflects internal accesses at the external port

2

On-Chip Memories

- Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable
- 192 x 24–bit bootstrap ROM

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode
20480 x 24–bit	0	7168 x 24-bit	7168 x 24–bit	disabled	disabled
19456 x 24–bit	1024 x 24–bit	7168 x 24-bit	7168 x 24–bit	enabled	disabled
24576 x 24–bit	0	5120 x 24-bit	5120 x 24–bit	disabled	enabled
23552 x 24–bit	1024 x 24–bit	5120 x 24-bit	5120 x 24–bit	enabled	enabled

---

Off-Chip Memory Expansion

- Data memory expansion to two 256 K x 24-bit word memory spaces
- Program memory expansion to one 256 K x 24-bit word memory space
- External memory expansion port
- Simultaneous glueless interface to four blocks of either SRAM or DRAM through chip select logic
- Supports interleaved, non–interfering access to both types of memory without losing in–page DRAM access, including DMA–driven access

On-Chip Peripherals

- 8–bit parallel Host Interface (HI08) supports a variety of buses (e.g., industry–standard architecture) and provides glueless connection to a number of industry–standard microcomputers, microprocessors, and DSPs
- Two Enhanced Synchronous Serial Interfaces (ESSI)
- Serial Communications Interface (SCI) with baud rate generator
- Triple timer module
- Up to 34 programmable General–Purpose I/O pins (GPIO), depending on which peripherals are enabled

Reduced Power Dissipation

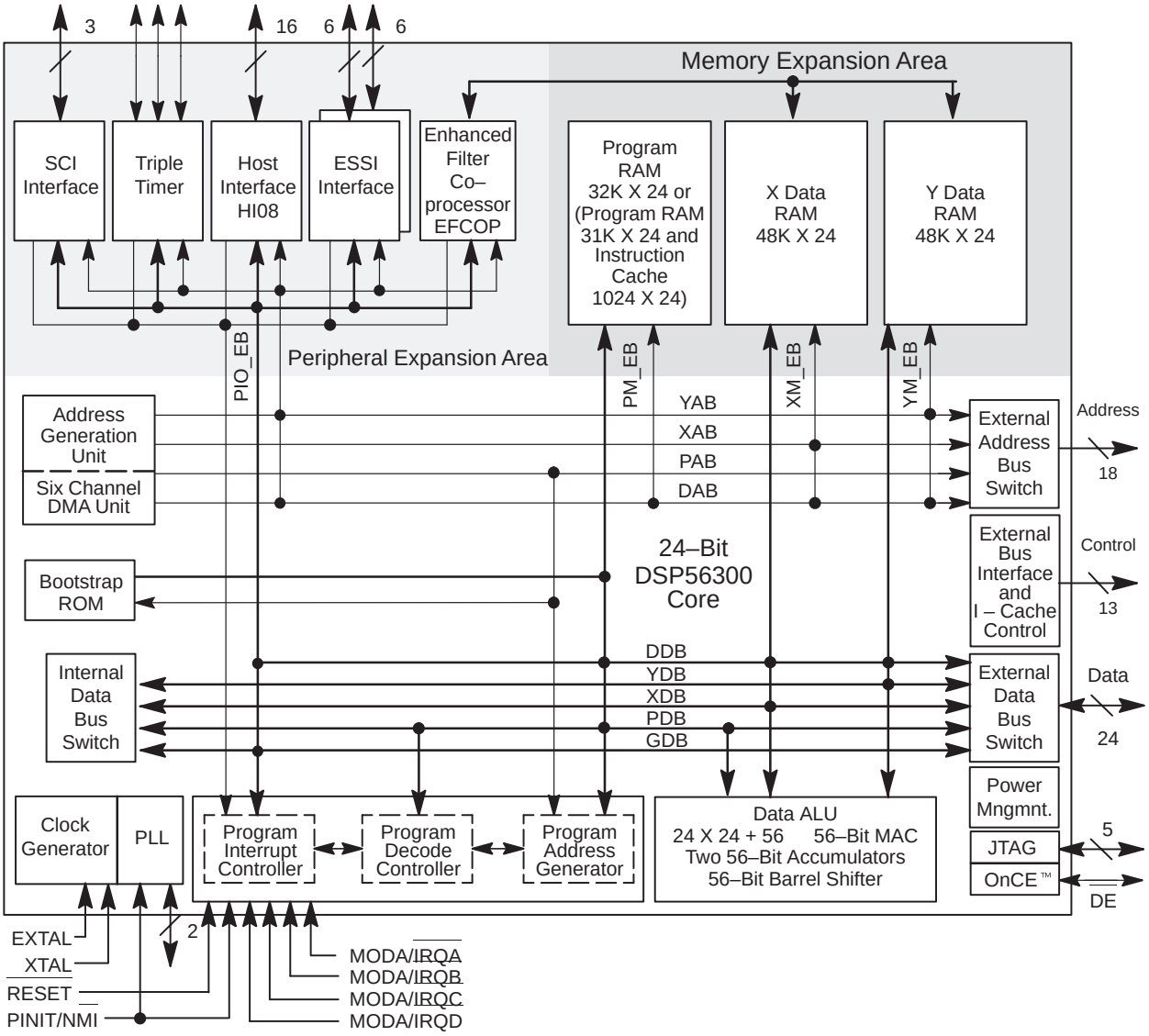
- Very low–power CMOS design
- Wait and Stop low–power standby modes
- Fully–static logic, operation frequency down to DC
- Optimized power management circuitry

Target Applications

The DSP56309 is intended for applications requiring a large amount of on–chip memory, mainly in telecommunications infrastructure and wireless local loop.

DSP56311—24-BIT DIGITAL SIGNAL PROCESSOR

The Motorola DSP56311, a member of the DSP56300 core family of programmable Digital Signal Processors (DSPs), supports wireless infrastructure applications with general filtering operations. The on–chip Enhanced Filter Coprocessor (EFCOP) processes filter algorithms in parallel with core operation, thus increasing overall DSP performance and efficiency. Like the other family members, the DSP56311 uses a high–performance, single clock cycle per instruction engine (code compatible with Motorola's popular DSP56000 core family), a barrel shifter, 24–bit addressing, Instruction Cache, and Direct Memory Access (DMA) controller. The DSP56311 offers 150 MIPS performance (255 MIPS using the EFCOP in filtering applications) using an internal 150 MHz clock, a 1.8 V core, and independent 3.3 V Input/Output (I/O).



DSP56311 Block Diagram

Features

- High–performance DSP56300 Core:
  - — 150 Million Instructions Per Second (MIPS) (255 MIPS using the EFCOP in filtering applications) with a 150 MHz clock at 1.8 V
  - — Object code compatible with the DSP56000 core with highly parallel instruction set

DSP56311—24-Bit Digital Signal Processor (continued)

— Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 x 24–bit parallel Multiplier–Accumulator (MAC), 56–bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24–bit or 16–bit arithmetic support under software control
— Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), on–chip instruction cache controller, on–chip memory–expandable hardware stack, nested hardware DO loops, and fast auto–return interrupts
— Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one–, two–, and three–dimensional transfers (including circular buffering); end–of–block–transfer interrupts; and triggering from interrupt lines and all peripherals
— Phase Lock Loop (PLL) allows change of low–power Divide Factor (DF) without loss of lock
— Hardware debugging support including On–Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

- On–Chip Memories and Off–Chip Memory Expansion:
  — 128 K on–chip RAM total
  — Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

2

Program RAM Size	Instruction Cache Size	X Data RAM Size*	IY Data RAM Size*	Instruction Cache	Switch Mode	MSW1	MSW0
32 K x 24–bit	0	48 K x 24–bit	48 K x 24–bit	disabled	disabled	0/1	0/1
31 K x 24–bit	1024 x 24–bit	48 K x 24–bit	48 K x 24–bit	enabled	disabled	0/1	0/1
96 K x 24–bit	0	16 K x 24–bit	16 K x 24–bit	disabled	enabled	0	0
95 K x 24–bit	1024 x 24–bit	16 K x 24–bit	16 K x 24–bit	enabled	enabled	0	0
80 K x 24–bit	0	24 K x 24–bit	24 K x 24–bit	disabled	enabled	0	0
79 K x 24–bit	1024 x 24–bit	24 K x 24–bit	24 K x 24–bit	enabled	enabled	0	1
64 K x 24–bit	0	32 K x 24–bit	32 K x 24–bit	disabled	enabled	1	0
63 K x 24–bit	1024 x 24–bit	32 K x 24–bit	32 K x 24–bit	enabled	enabled	1	0
48 K x 24–bit	0	40 K x 24–bit	40 K x 24–bit	disabled	enabled	1	1
47 K x 24–bit	1024 x 24–bit	40 K x 24–bit	40 K x 24–bit	enabled	enabled	1	1

*Includes 10 K x 24–bit shared memory (i.e., memory shared by the core and the EFCOP)

- 192 x 24–bit bootstrap ROM
- Enhanced Filter Coprocessor (EFCOP) — an on–chip 24 x 24–bit filtering and echo–cancellation coprocessor that runs in parallel to the DSP core
- Off–chip memory expansion:
  — Data memory expansion to two 256 K x 24–bit word memory spaces (or up to two 4 M x 24–bit word memory spaces by using the Address Attribute AA0-AA3 signals)
  — Program memory expansion to one 256 K x 24–bit word memory space (or up to one 4 M x 24–bit word memory space by using the Address Attribute AA0-AA3 signals)
  — External memory expansion port
  — Chip Select Logic for glueless interface to SRAMs
- On–Chip Peripherals:
  — 3.3 V I/O interface
  — Enhanced DSP56000–like 8–bit parallel Host Interface (HI08) supports a variety of buses (e.g., ISA) and provides glueless connection to a number of industry–standard microcomputers, microprocessors, and DSPs
  — Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1), each with one receiver and three transmitters
  — Serial Communications Interface (SCI) with baud rate generator

DSP56311—24-Bit Digital Signal Processor (continued)

— Triple timer module
— Up to thirty–four programmable General–Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled

- Reduced Power Dissipation:
  — Very low–power CMOS design
  — Wait and Stop low–power standby modes
  — Fully static design specified to operate at 0 Hz (DC)
  — Optimized power management circuitry (instruction–dependent, peripheral–dependent, and mode–dependent)
- Packaging: 196–pin PBGA

2

Target Applications

DSP56311 applications require high–performance, low–power, small packaging, and a large amount of on–chip memory — for example, wireless and wireline infrastructure applications, multi–channel wireless local loop systems, DSP resource boards, and high–speed modem banks. The EFCOP can accelerate general filtering applications, such as echo–cancellation applications, correlation, and general–purpose convolution–based algorithms.

Product Documentation

The three manuals listed in the following table are required for a complete description of the DSP56311 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, or a Motorola Literature Distribution Center. For documentation updates, visit our Web site. See the contact information below.

DSP56311 Documentation

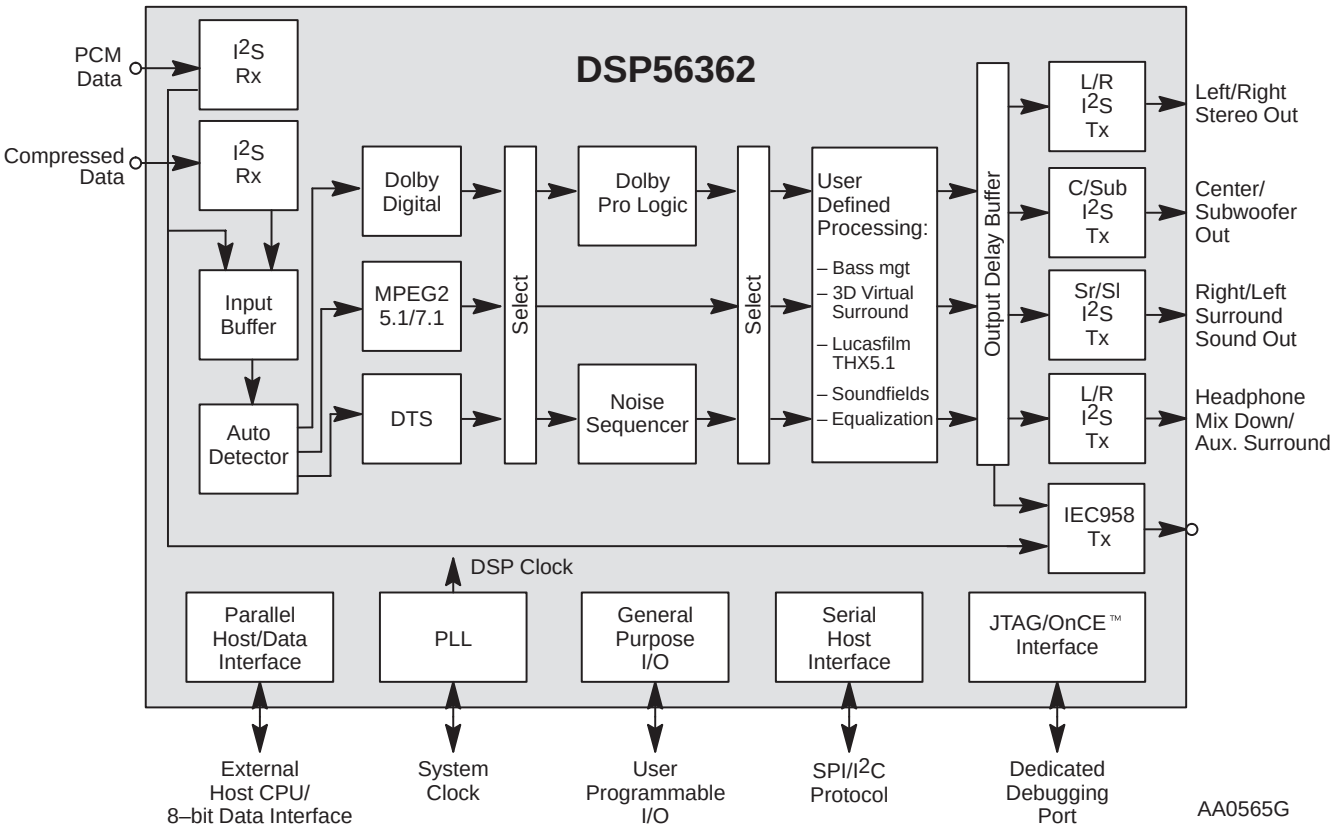
Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56311 User's Manual	Detailed functional description of the DSP56311 memory configuration, operation, and register programming	DSP56311UM/D
DSP56311 Technical Data	DSP56311 features list and physical, electrical, timing, and package specifications	DSP56311/D

DSP56362—24-Bit Audio Digital Signal Processor

The DSP56362 is a multimode, multichannel audio decoder for consumer applications such as Audio/Video (A/V) receivers, surround sound decoders, Digital Versatile Disk (DVD), digital TV, and other audio applications. The DSP56362 supports all of the popular multichannel audio decoding formats, including Dolby Digital Surround, Moving Picture Experts Group Standard 2 (MPEG2), and Digital Theater Systems (DTS), in a single device with sufficient resources (MIPS and memory) for customer defined post–processing features such as bass management, 3D virtual surround, Lucasfilm THX5.1, soundfield processing, and advanced equalization.

The DSP56362 is the first device in the second generation Motorola Symphony™ DSP Family. The DSP56362 utilizes the single–clock–per–cycle DSP56300 core, while retaining code compatibility with the DSP56000 core family. The DSP56362 contains audio–specific peripherals and on–board software engines as shown in the following diagram and will be offered initially in an 80 MIPS version at a nominal 3.3 V.

DSP56362—24-Bit Audio Digital Signal Processor (continued)



DSP56362 Surround Decoder Functionality

Features

- Multimode, multichannel decoder software functionality
  - — Dolby Digital and Pro Logic
  - — MPEG2 5.1/7.1
  - — DTS
  - — Bass management
- Digital audio post–processing capabilities
  - — 3D Virtual surround sound
  - — Lucasfilm THX5.1
  - — Soundfield processing
  - — Equalization
- Digital Signal Processing Core
  - — 80 Million Instructions Per Second (MIPS) with an 80 MHz clock at a nominal 3.3 V
  - — Object code compatible with the DSP56000 core with highly parallel instruction set
  - — Data Arithmetic Logic Unit (Data ALU)
  - — Program Control Unit (PCU)
  - — Direct Memory Access (DMA)
  - — Phase Lock Loop (PLL)
  - — Hardware debugging support: On–Chip Emulation (OnCE™) module, Joint Action Test Group (JTAG) Test Access Port (TAP), and Address Trace mode
- On–Chip Memories
  - — Modified Harvard architecture allows simultaneous access to program and data memories
  - — Program, X data, and Y data ROMs that may be factory programmed with data/program provided by the application developer
  - — 192 x 24–bit bootstrap ROM (disabled in Sixteen–Bit Compatibility mode)
- Off–Chip Memory Expansion
  - — Data memory expansion to two 256 K x 24–bit word memory spaces (or up to two 4 M x 24–bit word memory spaces by using the Address Attribute AA0–AA3 signals)

DSP56362—24-Bit Audio Digital Signal Processor (continued)

— Program memory expansion to one 256 K x 24–bit words memory space (or up to one 4 M x 24–bit word memory space by using the Address Attribute AA0–AA3 signals)
— External memory expansion port (twenty–four data pins for high speed external memory access allowing for a large number of external accesses per sample)
— Chip Select Logic for glueless interface to SRAMs
— On–chip DRAM Controller for glueless interface to DRAMs

- Peripheral and Support Circuits
  — Enhanced Serial Audio Interface (ESAI) includes:
    - Up to four receivers and six transmitters
    - Master or slave capability
    - I^2S, Sony, AC97, and other audio protocol implementations
    - Configuration supports up to twelve General Purpose Input/Output (GPIO) lines
  — Serial Host Interface (SHI) features:
    - Multi–master capability
    - SPI and I^2C protocols
    - Ten–word receive FIFO
    - Support for 8–, 16–, and 24–bit words
  — Byte–wide parallel Host Interface (HDI08) with DMA support; alternate configuration supports up to sixteen GPIO lines
  — DAX features one serial transmitter capable of supporting S/PDIF, IEC958, IEC1937, CP–340, and AES/EBU digital audio formats; configuration supports up to two GPIO lines
  — Triple Timer module with single external interface or one GPIO line
  — On–chip peripheral registers memory mapped in data memory space
- Reduced Power Dissipation
  — Very low power (3.3 V) CMOS design
  — Wait and Stop low–power standby modes
  — Fully–static logic, operation frequency down to 0 Hz (dc)
  — Optimized power management circuitry (instruction–dependent, peripheral–dependent, and mode–dependent)
- Additional Features
  — Software programmable PLL–based frequency synthesizer for the core clock
  — 144–pin plastic Thin Quad Flat Pack (TQFP) surface–mount package

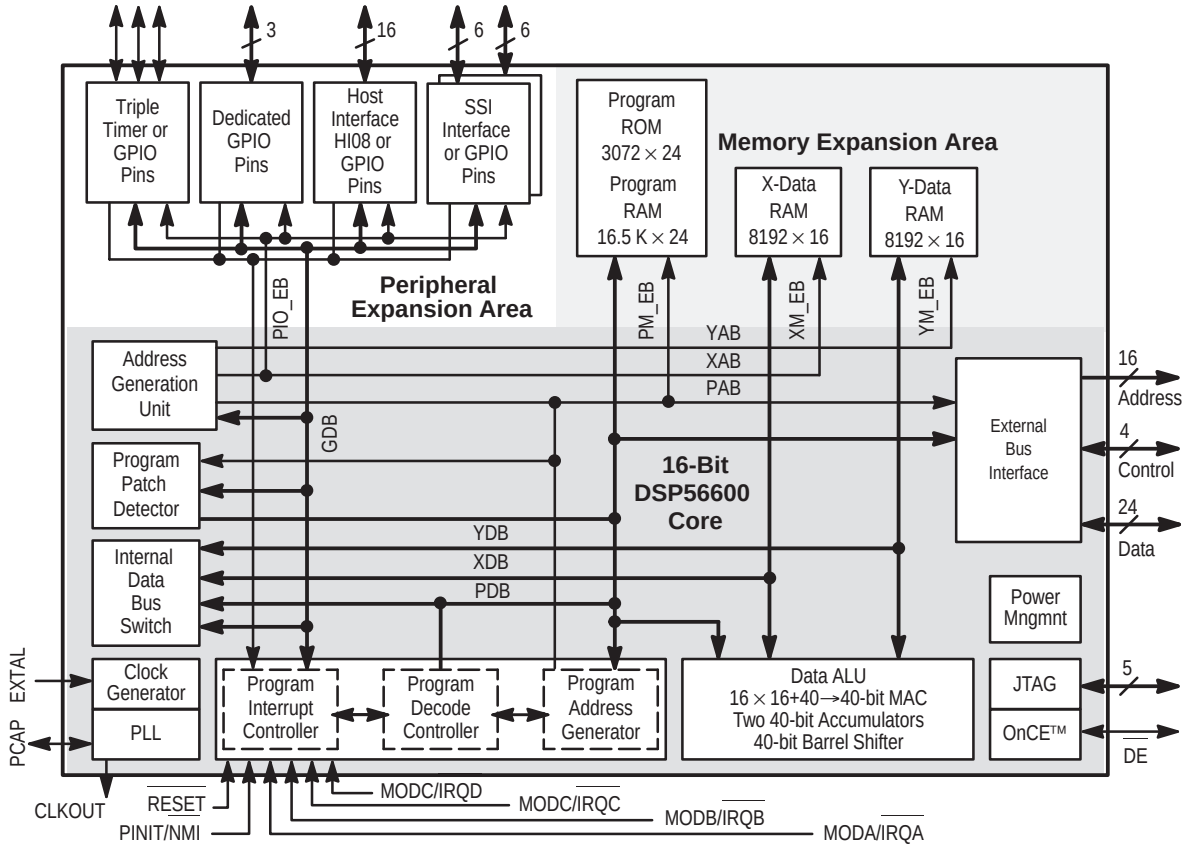
Documentation

The following table lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or (for the latest information) through the Motorola audio DSP home page on the Internet (http://dspaudio.motorola.com).

Additional DSP56362 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000–family architecture and the 24–bit core processor and instruction set	DSP56300FM/AD
DSP56362 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56362UM/AD
DSP56362 Technical Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56362/D

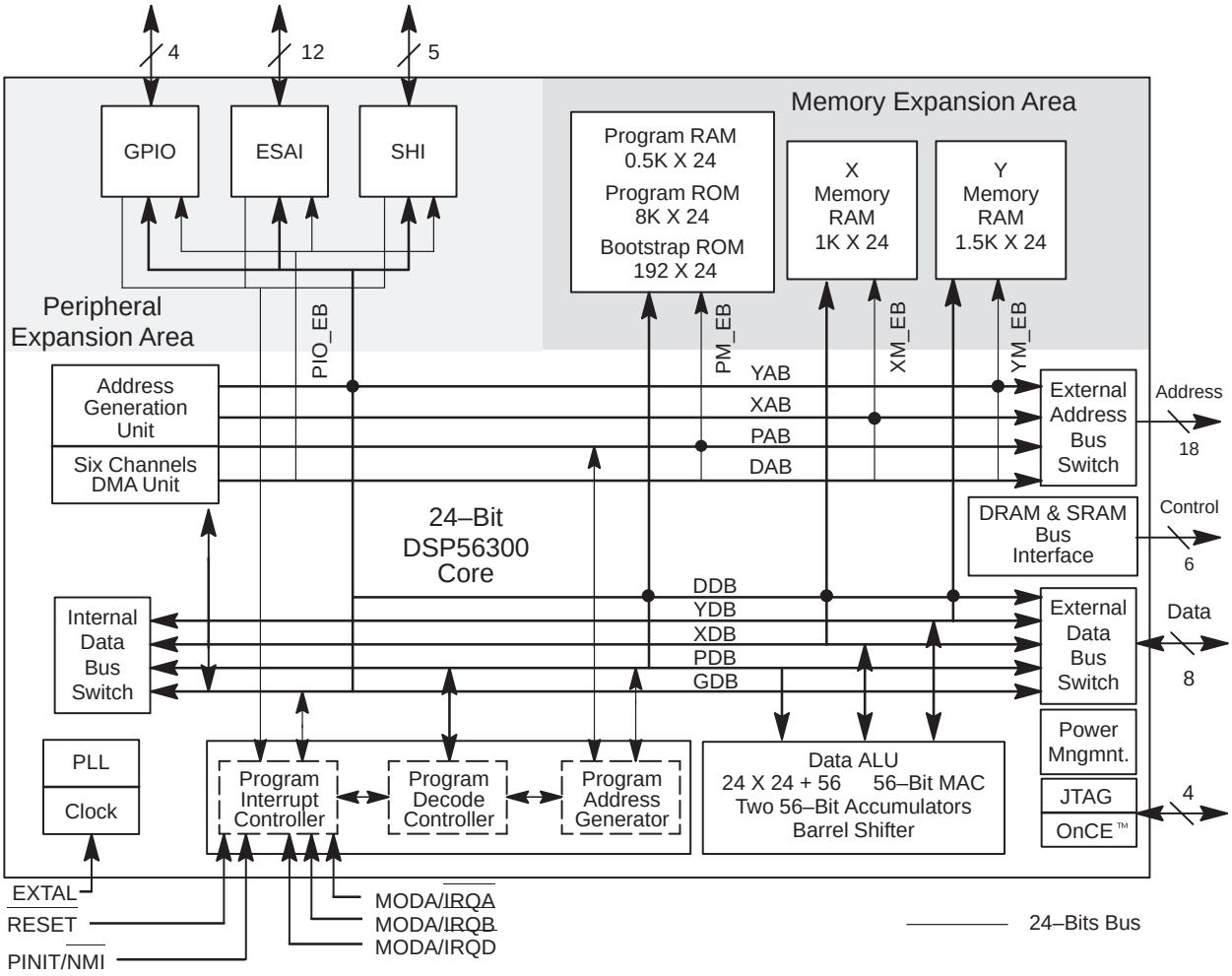
DSP56362—24-Bit Audio Digital Signal Processor (continued)



DSP56364—24-Bit Digital Signal Processor

The DSP56364 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56364 uses the high performance, single–clock–per–cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Motorola Symphony™ DSP family, as shown in the following figure. This design provides a two–fold performance increase over Motorola's popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24–bit addressing, instruction cache, and direct memory access (DMA). The DSP56364 offers 100 million instructions per second (MIPS) using an internal 100 MHz clock at 3.3 V.

DSP56364—24-Bit Audio Digital Signal Processor (continued)



DSP56364 Block Diagram

Features

- 100 Million Instructions Per Second (MIPS) with an 100 MHz clock at 3.3V.
- Object Code Compatible with the 56000 core.
- Data ALU with a 24 x 24 bit multiplier–accumulator and a 56–bit barrel shifter. 16–bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six–channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low–power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low–power standby modes.

On–Chip Memory Configuration

- 1.5 K x 24–bit Y data RAM.
- 1 K x 24–bit X data RAM.
- 8 K x 24–bit Program ROM.
- 0.5 K x 24–bitit Program RAM and 192 x 24–bit Bootstrap ROM.
- 0.75 K x 24–bit from Y data RAM can be switched to Program RAM resulting in up to 1.25 K x 24–bit of Program RAM.

Off–Chip Memory Expansion

- External Memory Expansion Port with 8–bit data bus.

Digital Signal Processing Core

- Off–chip expansion up to 2 x 16 M x 8–bit word of Data/Program memory when using DRAM.

DSP56364—24-Bit Audio Digital Signal Processor (continued)

- Off–chip expansion up to 2 x 256 K x 8–bit word of Data/Program memory when using SRAM.
- Simultaneous glueless interface to SRAM and DRAM.

Peripheral Modules

- Enhanced Serial Audio Interface (ESAI): 6 serial lines, 4 selectable as receive or transmit and transmit only, master or slave I^2S, Sony, AC97, network and other programmable protocols. Unused pins of ESAI may be used as GPIO lines
- Serial Host Interface (SHI): SPI and I^2C protocols, 10–word receive FIFO, support for 8, 16 and 24–bit words.
- Four dedicated GPIO lines.

Packaging

- 100–pin plastic TQFP package.
- 112–pin LD TQFP package

Documentation

The following table lists the documents that provide a complete description of the DSP56364 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

2

DSP56364 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000–family architecture and the 24–bit core processor and instruction set	DSP56300FM/AD
DSP56364 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56364UM/AD
DSP56364 Technical Data Sheet	Electrical and timing specifications; pin and package descriptions	DSP56364/D
There is also a product brief for this chip.		
DSP56364 Product Brief	Brief description of the chip	DSP56364P/D

DSP56600—16-Bit Digital Signal Processors

The DSP56600 core can execute one 24-bit instruction per clock cycle using 16-bit data. The 60 MHz chip includes a mixture of peripherals and memories optimized for processing-intensive, yet cost-effective, low power consumption digital mobile communications applications. The DSP56600 core includes the Data Arithmetic Logic Unit (Data ALU), Address Generation Unit (AGU), Program Controller, program patch detector, bus interface unit, On-Chip Emulation (OnCE™)/JTAG port, and a Phase Lock Loop (PLL)-based clock generator.

DSP56602 Features

Digital Signal Processing Core

- High-performance DSP56600 core
- Up to 60 million instructions per second (MIPS) at 2.7 V
- 24-bit instructions using 16-bit data
- Fully pipelined 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 40-bit accumulators including extension bits
- 40-bit parallel barrel shifter
- Highly parallel instruction set with unique DSP addressing modes
- Code-compatible with the DSP56300 core
- Position-Independent Code support PIC)
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip support for software patching and enhancements
- On-chip Phase Lock Loop (PLL) circuit
- Real-time trace capability via external address bus
- On-Chip Emulation (OnCE™) module
- JTAG port

Memory

- 512 x 24 Program RAM
- 24 K x 24 Program ROM
- 4 K x 16 X data RAM
- 6 K x 16 X data ROM
- Glueless interface to external SRAM memories
- 4 K x 16 Y data RAM
- 6 K x 16 Y data ROM
- Off-chip expansion for both program fetch and program data transfers

DSP56600—16-Bit Digital Signal Processors (continued)

Peripheral Circuits

- Three dedicated General Purpose Input/Output (GPIO) pins and up to thirty one additional GPIO pins (user-selectable as peripherals or GPIO pins)
- Host interface (HI) support: One 8-bit parallel port (or up to sixteen additional GPIO pins)
  - — Direct interface to Motorola HC11, Hitachi H8, 8051 family, Thomson P6 family
  - — Minimal logic interface to standard ISA bus, Motorola 68 K family, and Intel x86 microprocessor family
- Synchronous Serial Interface (SSI) support: Two 6-pin ports (or twelve additional GPIO pins)
  - — Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola-SPI-compliant peripherals
  - — Independent transmitter and receiver sections and a common RSI clock generator
  - — Network mode using frame sync and up to 32 time slots
  - — 8-bit, 12-bit, and 16-bit data word lengths
- Three programmable timers (or up to three additional GPIO pins)
- Three external interrupt/mode control lines
- One external reset pin for hardware reset

Energy Efficient Design

- Operating voltage range: 1.8 V to 3.3 V
- Very low power CMOS design
  - — < 0.85 mA/MIPS at 2.7 V
  - — < 0.55 mA/MIPS at 1.8 V
- Low power Wait for interrupt standby mode
- Ultra low power Stop standby mode
- Fully static, HCMOS design for operating frequencies from 60 MHz down to DC
- Special power management circuitry

DSP56603 Features

Digital Signal Processing Core

- High-performance DSP56600 core
- Up to 60 Million Instructions Per Second (MIPS) at 2.7–3.3 V
- Fully pipelined 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 40-bit accumulators including extension bits
- 40-bit parallel barrel shifter
- Highly parallel instruction set with unique DSP addressing modes
- Code-compatible with the DSP56300 core
- Position-Independent Code support (PIC)
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip support for software patching and enhancements
- On-chip Phase Lock Loop (PLL) circuit
- Real-time trace capability via external address bus
- On-Chip Emulation (OnCE™) module and JTAG port

Memory

- Switch mode memory allows reconfiguring program, X-data, and Y-data RAM sizes
  - — Switch mode off
    - — 16 K x 24-bit Program RAM
    - — 8 K x 16-bit X data RAM
    - — 8 K x 16-bit Y data RAM
  - — Switch mode on
    - — 11 K x 24-bit Program RAM
    - — 10.5 K x 16-bit X data RAM
    - — 10.5 K x 16-bit Y data RAM
    - — 3 K x 24-bit Program ROM
- Off-chip expansion for both program fetch and program data transfers
- No additional logic needed for interface to external SRAM memories

Peripheral Circuits

- Three dedicated General Purpose Input/Output (GPIO) pins and as many as thirty-one additional GPIO pins (user-selectable as peripherals or GPIO pins)
- Host Interface (HI) support: one 8-bit parallel port (or as many as sixteen additional GPIO pins)
  - — Direct interface to Motorola HC11, Hitachi H8, 8051 family, Thomson P6 family
  - — Minimal logic interface to standard ISA bus, Motorola 68 K family, and Intel x86 microprocessor family
- Synchronous Serial Interface (SSI) support: two 6-pin ports (or twelve additional GPIO pins)
  - — Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
  - — Independent transmitter and receiver sections and a common SSI clock generator
  - — Network mode using frame sync and up to 32 time slots
  - — 8-bit, 12-bit, and 16-bit data word lengths
- Three programmable timers (or as many as three additional GPIO pins)
- Three external interrupt/mode control lines
- One external reset pin for hardware reset

DSP56600—16-Bit Digital Signal Processors (continued)

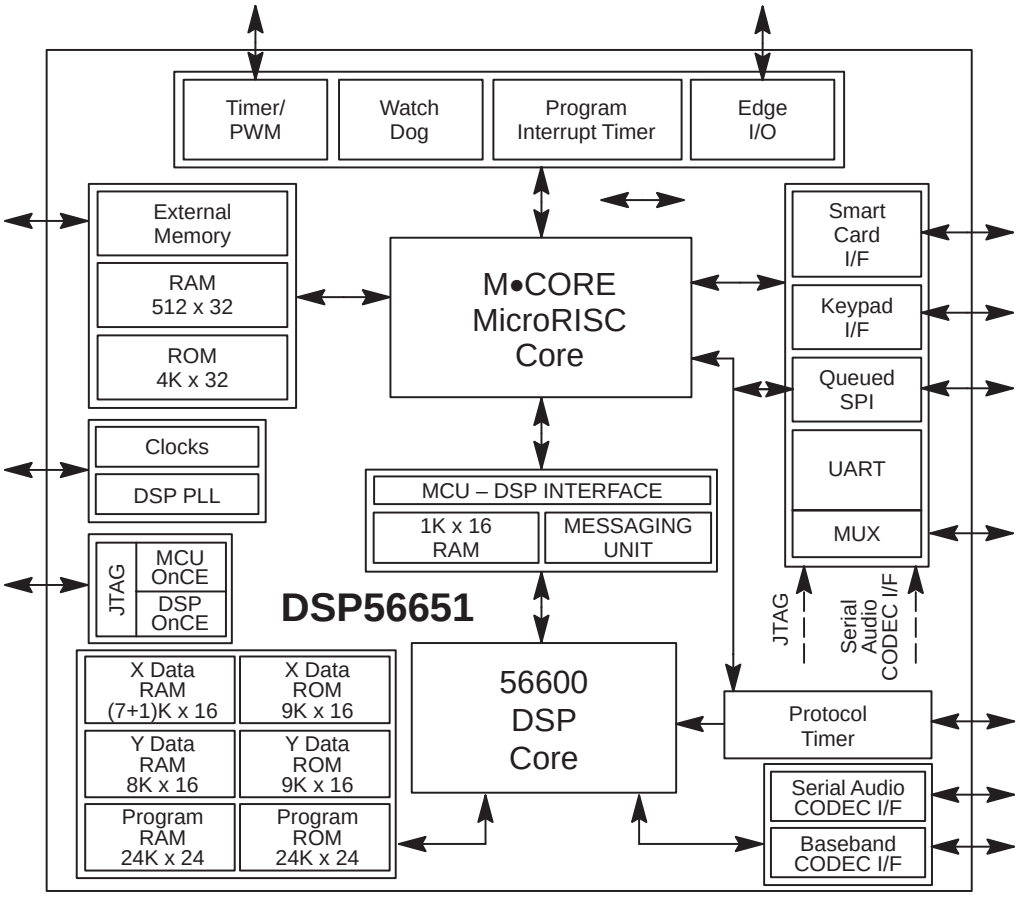
Energy Efficient Design

- Very low power CMOS design
  - — Operating voltage range: 1.8 V to 3.3 V
  - — < 0.85 mA/MIPS at 2.7 V
  - — < 0.55 mA/MIPS at 1.8 V
- Low power Wait for interrupt standby mode, and ultra low power Stop standby mode
- Fully static, HCMOS design for operating frequencies from 60 MHz down to DC
- Special power management circuitry

DSP56651—Integrated Cellular Baseband Processor Development IC

Motorola designed the RAM–based DSP56651 emulation device to support the rigorous demands of developing applications for the cellular subscriber market. The high level of on–chip integration in the DSP56651 and its volume production companion device DSP56652 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low–power consumption and cost–effective system performance. The DSP56651 chip combines the power of Motorola's 32–bit M•CORE™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor (DSP) core with on–chip memory, protocol timer, and custom peripherals to provide a single–chip cellular base–band processor. The following shows the basic block diagram of the DSP56651.

2



AA1617

DSP56651 System Block Diagram

Development Part Only — Not intended for production. Requires a higher voltage than the production part.

DSP56651—Integrated Cellular Baseband Processor Development IC (continued)

Features

- RISC M•CORE MCU
  - — 32–bit load/store RISC architecture
  - — Fixed 16–bit instruction length
  - — 16–entry 32–bit general–purpose register file
  - — 32–bit internal address and data buses
  - — Efficient four–stage, fully interlocked execution pipeline
  - — Single–cycle execution for most instructions, two cycles for branches and memory accesses
  - — Special branch, byte, and bit manipulation instructions
  - — Support for byte, half–word, and word memory accesses
  - — Fast interrupt support via vectoring/ auto–vectoring and a 16–entry dedicated alternate register file
- High–performance DSP56600 core
  - — 1 x engine (e.g., 70 MHz = 70 MIPS)
  - — Fully pipelined 16 x 16–bit parallel multiplier–accumulator (MAC)
  - — Two 40–bit accumulators including extension bits
  - — 40–bit parallel barrel shifter
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Position–independent code support
  - — Nested hardware DO loops
  - — Fast auto–return interrupts
  - — On–chip support for software patching and enhancements
  - — Realtime trace capability via external address bus
- On–chip memories
  - — 4 K x 32–bit MCU ROM
  - — 512 x 32–bit MCU RAM
  - — 24 K x 24–bit DSP program ROM
  - — 24 K x 24–bit DSP program RAM
  - — 18 K x 16–bit DSP data ROM, split into 9 K x 16–bit X and 9 K x 16–bit Y data ROM
  - — 16 K x 16–bit DSP data RAM, split into (7+1) K x 16–bit X and 8 K x 16–bit Y data RAM
- On–chip peripherals
  - — Fully programmable phase–locked loop (PLL) for DSP clock generation
  - — External interface module (EIM) for glueless system integration
  - — External 22–bit address and 16–bit data MCU buses
  - — Thirty–two source MCU interrupt controller
  - — Intelligent MCU/DSP interface (MDI) dual 1 K x 16–bit RAM (shares 1 K DSP X data RAM) with messaging status and control
  - — Serial audio codec port
  - — Serial baseband codec port
  - — Protocol timer frees the MCU from radio channel timing events
  - — Queued serial peripheral interface (SPI)
  - — Keypad port capable of scanning up to an 8 x 8 matrix keypad
  - — General–purpose MCU and DSP timers
  - — Pulse width modulation (PWM) output
  - — Universal asynchronous receiver/transmitter (UART) with FIFO
  - — IEEE 1149.1–compliant boundary scan JTAG test access port (TAP)
  - — Integrated DSP/M•CORE On–Chip Emulation (OnCE™) module
  - — DSP address bus visibility mode for system development
  - — ISO 7816–compatible Smart Card port
- Operating features
  - — Comprehensive static and dynamic power management
  - — M•CORE operating frequency: dc to 16.8 MHz at 2.4 V
  - — DSP operating frequency: dc to 58.8 MHz at 2.4 V
  - — Operating temperature: −40° to 85°C ambient
  - — Package option: 17 x 17 mm, 196–lead PBGA

Target Applications

The DSP56651 is intended for the development of cellular subscriber applications and other applications needing both DSP and control processing.

Product Documentation

The four manuals listed in the following table are required for a complete description of the DSP56651 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

DSP56651—Integrated Cellular Baseband Processor Development IC (continued)

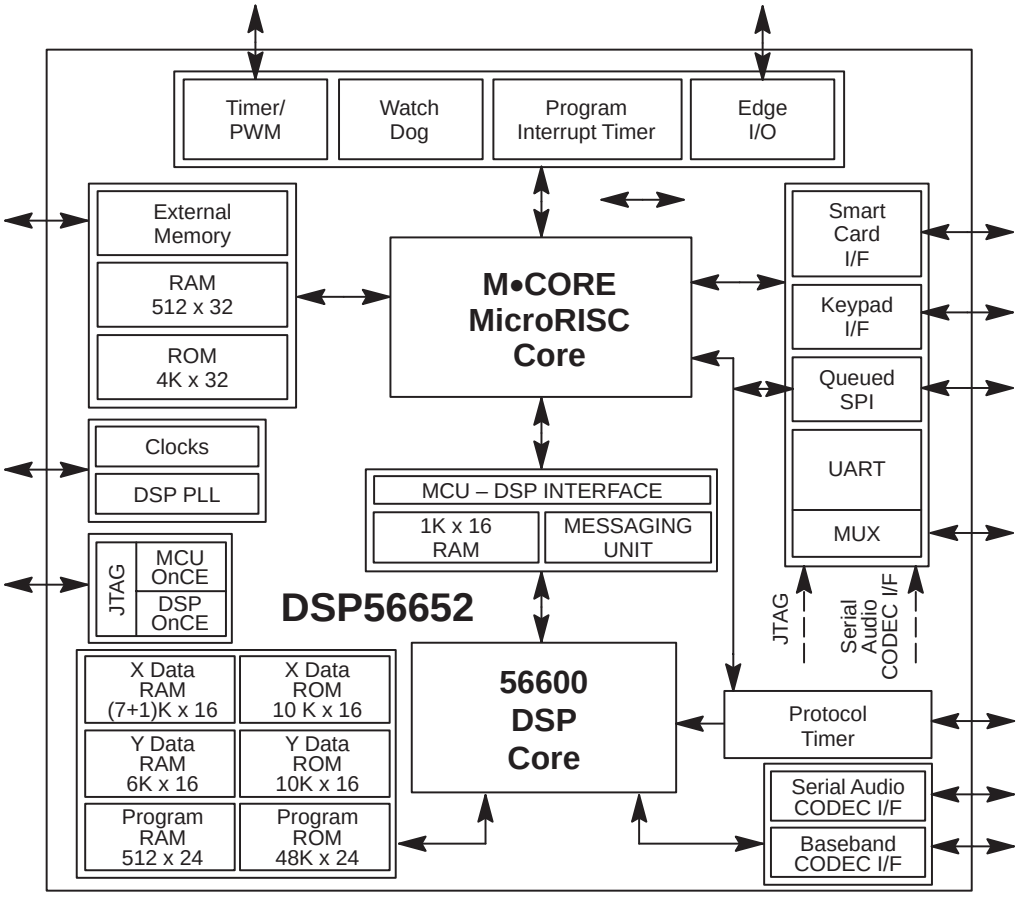
DSP56651 Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core processor architecture and instruction set	DSP56600FM/AD
M•CORE Reference Manual	Detailed description of the MicroRisc M•CORE MCU and instruction set	MCORERM/AD
DSP56651 User's Manual	Detailed description of DSP56651 memory, peripherals, and interfaces	DSP56651UM/AD
DSP56651 Technical Data	DSP56651 pin and package descriptions; electrical and timing specifications	DSP56651/D

DSP56652—Integrated Cellular Baseband Processor

2

Motorola designed the ROM–based DSP56652 to support the rigorous demands of the cellular subscriber market. The high level of on–chip integration in the DSP56652 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low–power consumption and cost–effective system performance. The DSP56652 chip combines the power of Motorola's 32–bit M•CORE™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor (DSP) core with on–chip memory, protocol timer, and custom peripherals to provide a single–chip cellular base–band processor. The following shows the basic block diagram of the DSP56652.



DSP56652 System Block Diagram

AA1618

DSP56652—Integrated Cellular Baseband Processor (continued)

Features

- RISC M•CORE MCU
  - — 32–bit load/store RISC architecture
  - — Fixed 16–bit instruction length
  - — 16–entry 32–bit general–purpose register file
  - — 32–bit internal address and data buses
  - — Efficient four–stage, fully interlocked execution pipeline
  - — Single–cycle execution for most instructions, two cycles for branches and memory accesses
  - — Special branch, byte, and bit manipulation instructions
  - — Support for byte, half–word, and word memory accesses
  - — Fast interrupt support via vectoring/ auto–vectoring and a 16–entry dedicated alternate register file
- High–performance DSP56600 core
  - — 1 x engine (e.g., 70 MHz = 70 MIPS)
  - — Fully pipelined 16 x 16–bit parallel multiplier–accumulator (MAC)
  - — Two 40–bit accumulators including extension bits
  - — 40–bit parallel barrel shifter
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Position–independent code support
  - — Nested hardware DO loops
  - — Fast auto–return interrupts
  - — On–chip support for software patching and enhancements
  - — Realtime trace capability via external address bus
- On–chip memories
  - — 4 K x 32–bit MCU ROM
  - — 512 x 32–bit MCU RAM
  - — 48 K x 24–bit DSP program ROM
  - — 512 x 24–bit DSP program RAM
  - — 20 K x 16–bit DSP data ROM, split into 10 K x 16–bit each of X and Y data ROM spaces
  - — 14 K x 16–bit DSP data RAM, split into (7+1) K x 16–bit X data RAM and 6 K x 16–bit Y data RAM spaces
- On–chip peripherals
  - — Fully programmable phase–locked loop (PLL) for DSP clock generation
  - — External interface module (EIM) for glueless system integration
  - — External 22–bit address and 16–bit data MCU buses
  - — Thirty–two source MCU interrupt controller
  - — Intelligent MCU/DSP interface (MDI) dual 1 K x 16–bit RAM (shares 1 K DSP X data RAM) with messaging status and control
  - — Serial audio codec port
  - — Serial baseband codec port
  - — Protocol timer frees the MCU from radio channel timing events
  - — Queued serial peripheral interface (SPI)
  - — Keypad port capable of scanning up to an 8 x 8 matrix keypad
  - — General–purpose MCU and DSP timers
  - — Pulse width modulation (PWM) output
  - — Universal asynchronous receiver/transmitter (UART) with FIFO
  - — IEEE 1149.1–compliant boundary scan JTAG test access port (TAP)
  - — Integrated DSP/M•CORE On–Chip Emulation (OnCE™) module
  - — DSP address bus visibility mode for system development
  - — ISO 7816–compatible Smart Card port
- Operating features
  - — Comprehensive static and dynamic power management
  - — M•CORE operating frequency: dc to 16.8 MHz at 1.8 V or dc to 40 MHz at 2.5 V
  - — DSP operating frequency: dc to 58.8 MHz at 1.8 V or dc to 70 MHz at 2.5 V
  - — Internal operating voltage range: 1.8–2.5 V with 3.3 V–tolerant I/O
  - — Operating temperature: −40° to 85°C ambient
  - — Package option: 15 x 15 mm, 196–lead PBGA

Target Applications

The DSP56652 is intended for use in cellular subscriber applications and other applications needing both DSP and control processing.

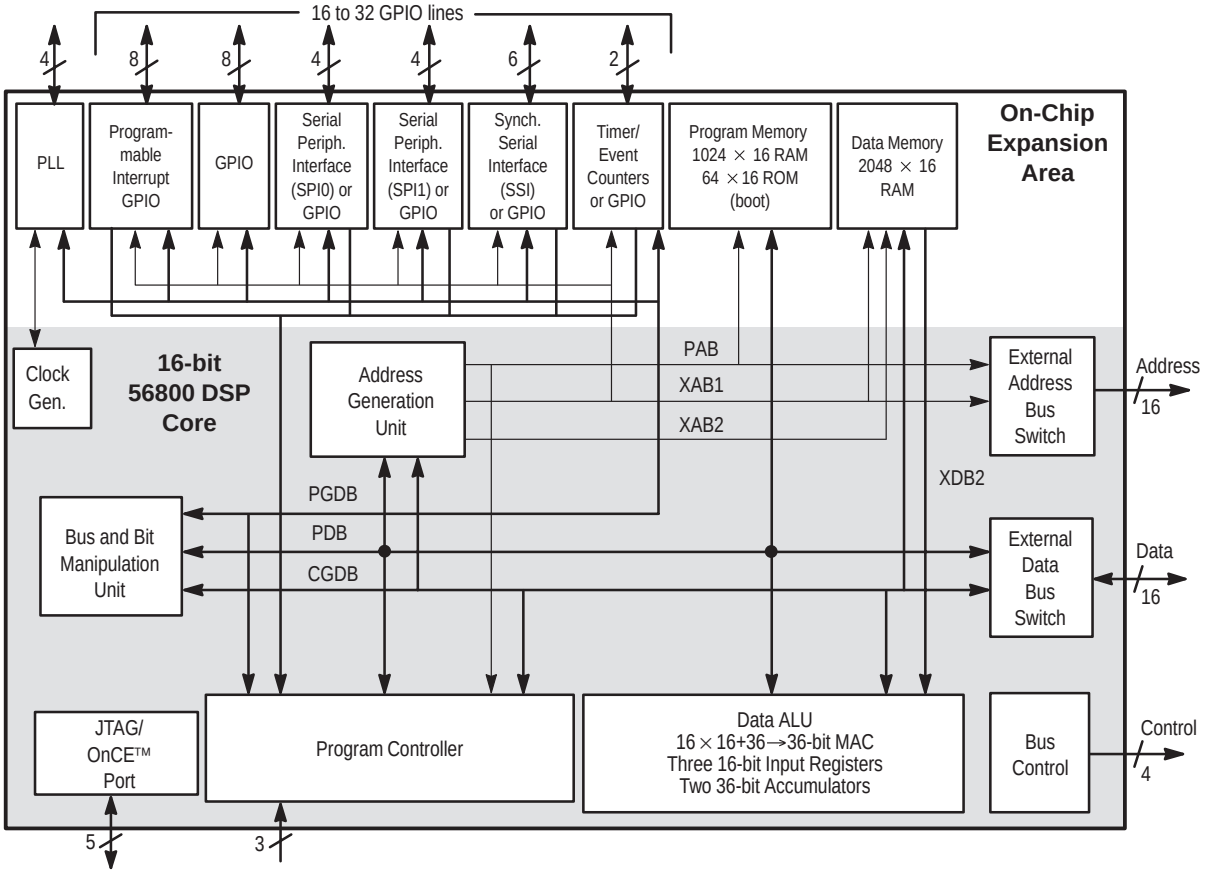
Product Documentation

The four manuals listed in the following table are required for a complete description of the DSP56652 and are necessary to design with the part properly. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or the World Wide Web.

DSP56652—Integrated Cellular Baseband Processor (continued)

DSP56652 Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family core processor architecture and instruction set	DSP56600FM/AD
M•CORE Reference Manual	Detailed description of the M•CORE MCU and instruction set	MCORERM/AD
DSP56652 User's Manual	Detailed description of DSP56652 memory, peripherals, and interfaces	DSP56652UM/AD
DSP56652 Technical Data	DSP56652 pin and package descriptions; electrical and timing specifications	DSP56652/D

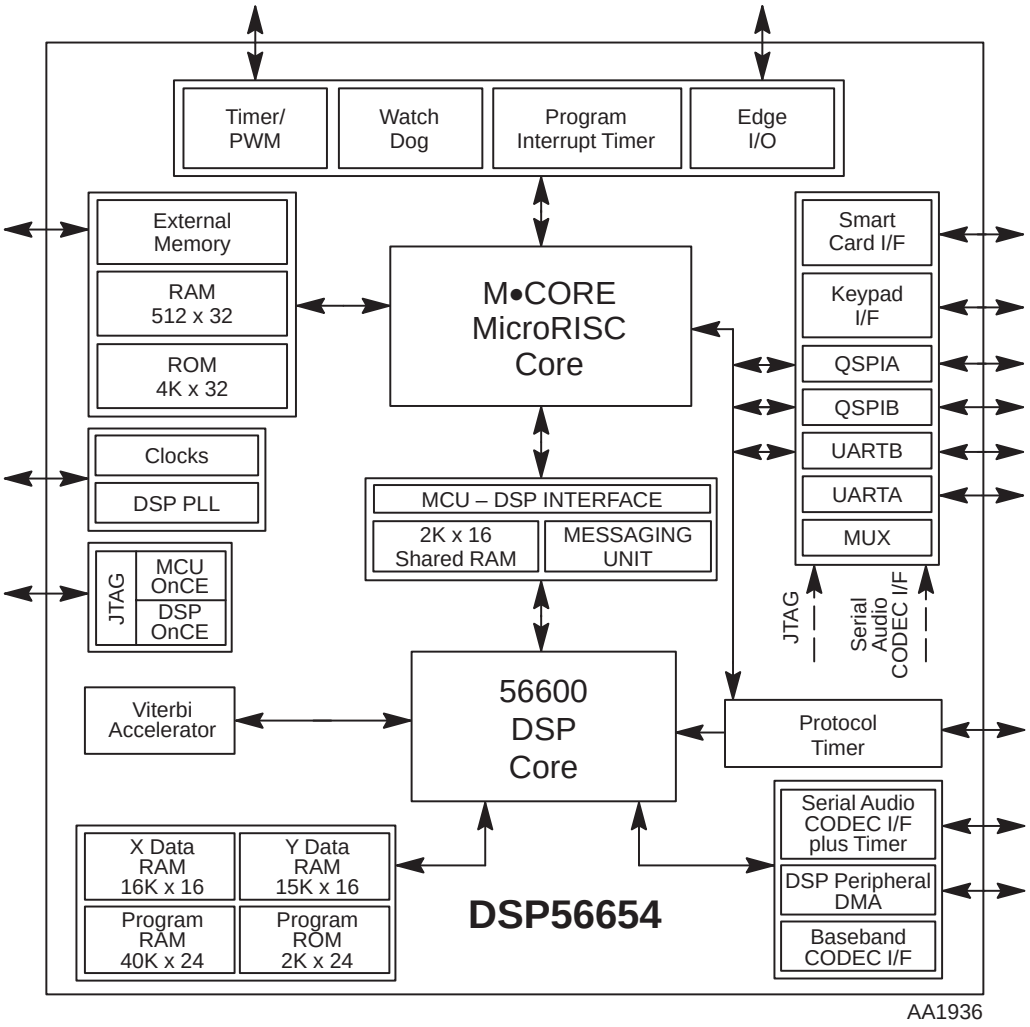


DSP56654 Integrated Cellular Baseband Processor Product Brief

Motorola designed the DSP56654 to support the rigorous demands of the cellular subscriber market. Optimized for narrow–band wireless systems such as GSM and TDMA/AMPS, the high level of on–chip integration in the DSP56654 minimizes application system design complexity and component count, resulting in very compact implementations. This integration also yields very low power consumption and cost–effective system performance. The DSP56654 chip combines the power of Motorola's 32–bit M•CORE™ MicroRISC Engine (MCU) and the DSP56600 digital signal processor) core with on–chip memory, protocol timer, and custom peripherals to provide a single–chip cellular base–band processor. the following figure shows the DSP56654 basic block diagram.

DSP56654—Integrated Cellular Baseband Processor (continued)

2



DSP56654 System Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Features

- RISC M•CORE MCU
  - — 32–bit load/store RISC architecture
  - — Fixed 16–bit instruction length
  - — 16–entry 32–bit general–purpose register file
  - — 32–bit internal address and data buses
  - — Efficient four–stage, fully interlocked execution pipeline
  - — Special branch, byte, and bit manipulation instructions
  - — Support for byte, half–word, and word memory accesses
  - — Fast interrupt support via vectoring/ auto–vectoring and a 16–entry dedicated alternate register file
- High–performance DSP56600 core
  - — 1 x engine (e.g., 70 MHz = 70 MIPS)
  - — Fully pipelined 16 x 16–bit parallel multiplier–accumulator (MAC)

DSP56654—Integrated Cellular Baseband Processor (continued)

  - — Two 40–bit accumulators including extension bits
  - — 40–bit parallel barrel shifter
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Position–independent code support
  - — Nested hardware DO loops
  - — Fast auto–return interrupts
  - — On–chip support for software patching and enhancements
  - — Realtime trace capability via external address bus
- On–chip memories
  - — 4 K x 32–bit MCU ROM
  - — 512 x 32–bit MCU RAM
  - — 40 K x 24–bit DSP Program RAM
  - — 2 K x 24–bit DSP Program ROM
  - — 31 K x 16–bit DSP data RAM, split into 16 K x 16–bit X data RAM and 15 K x 16–bit Y data RAM spaces
  - — 2K x 16 DSP/MCU interface, dual port RAM (part of the 16 K x 16 X data RAM)
- On–chip peripherals
  - — Fully programmable phase–locked loop (PLL) for DSP clock generation
  - — External interface module (EIM) for glueless system integration
  - — External 22–bit address and 16–bit data MCU buses
  - — Thirty–two source MCU interrupt controller
  - — Intelligent MCU/DSP interface (MDI) dual 2K x 16–bit dual port RAM (shares 2K DSP X data RAM) with messaging status and control
  - — Serial audio codec port
  - — Serial baseband codec port
  - — Protocol timer frees the MCU from radio channel timing events
  - — Two queued serial peripheral interface (QSPI) communicate with external peripherals
  - — Keypad port capable of scanning up to an 8 x 8 matrix keypad
  - — Software watchdog timer, DSP timer, O/S programmable interrupt timer, and MCU general–purpose timers
  - — Pulse width modulation (PWM) output
  - — Two universal asynchronous receiver/transmitter (UARTs) with FIFO
  - — IEEE 1149.1–compliant boundary scan JTAG test access port (TAP)
  - — Integrated DSP/M•CORE On–Chip Emulation (OnCE™) module
  - — DSP address bus visibility and DSP data bus visibility modes for system development
  - — ISO 7816–compatible SmartCard port
- Operating features
  - — Comprehensive static and dynamic power management
  - — M•CORE operating frequency: dc to 16.8 MHz at 1.8 V
  - — DSP operating frequency: dc to 58.8 MHz at 1.8 V
  - — Internal operating voltage range: 1.8-2.5 V with 3.3 V–tolerant I/O
  - — Operating temperature: -40° to 85°C ambient
  - — 256–pin 17 x 17mm plastic ball grid array (PBGA) package

Target Applications

The DSP56654 is intended for use in cellular subscriber applications, primarily GSM and TDMA/AMPS, and other applications needing both DSP and control processing.

DSP56800—16-Bit Digital Signal Processors

The DSP56800 core family is the first architecture designed to enable digital signal processing and embedded microcontroller functionality. This multi-functional approach supports applications requiring both signal processing and control functionality, such as wireless messaging, digital answering machines, feature phones, and low-cost wireline modems.

The first DSP56800 family members, the DSP56L811, DSP56812, and DSP56824, are identical except for memory configuration. The DSP56L811 contains 1 K of Program RAM and 2 K of data RAM. The DSP56812 features 22 K of Program ROM, 2 K of data ROM, and 2 K of data RAM. The DSP56824 has 32 K of Program ROM, 2 K of data ROM and 3.5 K of data RAM.

DSP56L811 Features

Digital Signal Processing Core

- Efficient 16-bit DSP56800 family DSP engine
- Up to 20 Million Instructions Per Second (MIPS) at 40 MHz

DSP56800—16-Bit Digital Signal Processors (continued)

- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- DO loops nestable in software
- Address buses:
  - — One 16-bit internal memory address bus (XAB1)
  - — One 16-bit internal memory address bus (XAB2)
  - — One 19-bit internal Program Address Bus (PAB)
  - — One 16-bit External Address Bus (EAB)
- Data buses:
  - — One 16-bit bidirectional internal memory data bus (CGDB)
  - — One 16-bit unidirectional internal memory data bus (XDB2)
  - — One 16-bit bidirectional dedicated peripheral data bus (PGDB)
  - — One 16-bit bidirectional internal Program Data Bus (PDB)
  - — One 16-bit bidirectional External Data Bus (EDB)
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with unlimited depth

Memory

- On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
  - — 1 K x 16 Program RAM
  - — 64 x 16 bootstrap ROM
  - — 2 K x 16 X data RAM
  - — Programs can run out of X data RAM

Peripheral and Support Circuits

- External Memory Interface (EMI)
- Sixteen dedicated General Purpose Input/Output (GPIO) pins (eight pins programmable as interrupts)
- Serial Peripheral Interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
  - — Supports LCD drivers, A/D subsystems, and MCU systems
  - — Supports inter-processor communications in a multiple master system
  - — Demand-driven master or slave devices with high data rates
- Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
  - — Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
  - — Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
  - — Network mode using frame sync and up to 32 time slots
  - — 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
- Three programmable timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
- Two external interrupt/mode control lines
- One external reset for hardware reset
- JTAG/On-Chip Emulation (OnCE™) 5-pin port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock
- Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers

Energy Efficient Design

- Power-saving Wait and multiple Stop modes available
- Fully static, HCMOS design for operating frequencies from 70 MHz down to DC
- 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
- 2.7 V–3.6 V power supply

DSP56812/DSP56824 Features

Digital Signal Processing Core

- Efficient 16-bit DSP56800 core
- Up to 35 Million Instructions Per Second (MIPS) at 70 MHz
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes

DSP56800—16-Bit Digital Signal Processors (continued)

- Hardware DO and REP loops
- DO loops nestable in software
- Address buses:
  - — One 16-bit internal memory address bus (XAB1)
  - — One 16-bit internal memory address bus (XAB2)
  - — One 19-bit internal Program Address Bus (PAB)
  - — One 16-bit External Address Bus (EAB)
- Data buses:
  - — One 16-bit bidirectional internal memory data bus (CGDB)
  - — One 16-bit unidirectional internal memory data bus (XDB2)
  - — One 16-bit bidirectional dedicated peripheral data bus (PGDB)
  - — One 16-bit bidirectional internal Program Data Bus (PDB)
  - — One 16-bit bidirectional External Data Bus (EDB)
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and structured programming support
- Software subroutine and interrupt stack with unlimited depth

Memory

- On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
  - — 22 K x 16 Program ROM (DSP56812)
  - — 32 K x 16 Program ROM (DSP56824)
  - — 2 K x 16 X data ROM and 2 K x 16 X data RAM (DSP56812)
- Programs can run out of X data RAM

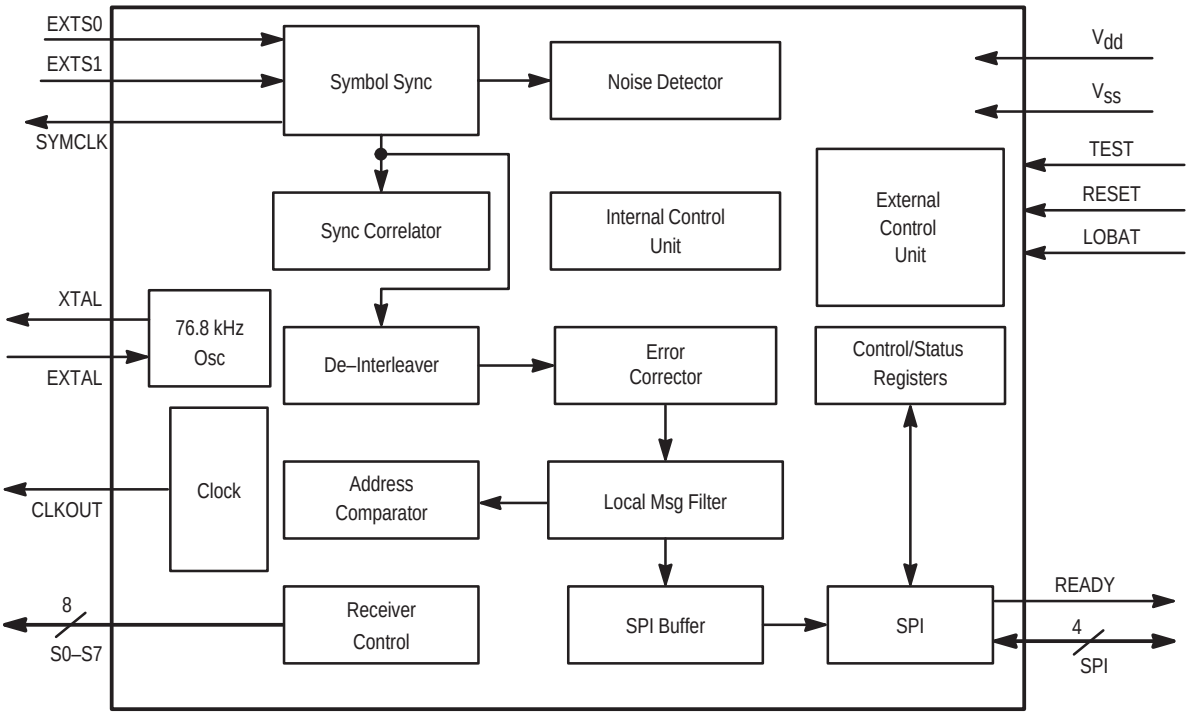
Peripheral and Support Circuits

- External Memory Interface (EMI)
- Sixteen dedicated General Purpose Input/Output (GPIO) pins (eight pins programmable as interrupts)
- Serial Peripheral Interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
  - — Supports LCD drivers, A/D subsystems, and MCU systems
  - — Supports inter-processor communications in a multiple master system
  - — Demand-driven master or slave devices with high data rates
- Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
  - — Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola-SPI-compliant peripherals
  - — Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
  - — Network mode using frame sync and up to 32 time slots
  - — 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
- Three programmable 16-bit timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
- Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers
- Two external interrupt/mode control pins
- One external reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) 5-pin port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock

Energy Efficient Design

- Power-saving Wait and multiple Stop modes available
- Fully static, HCMOS design for 40 MHz to DC operating frequencies
- 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
- Pin-compatible with the DSP56L811
- 2.7 V–3.6 V power supply

DSP56800—16-Bit Digital Signal Processors (continued)

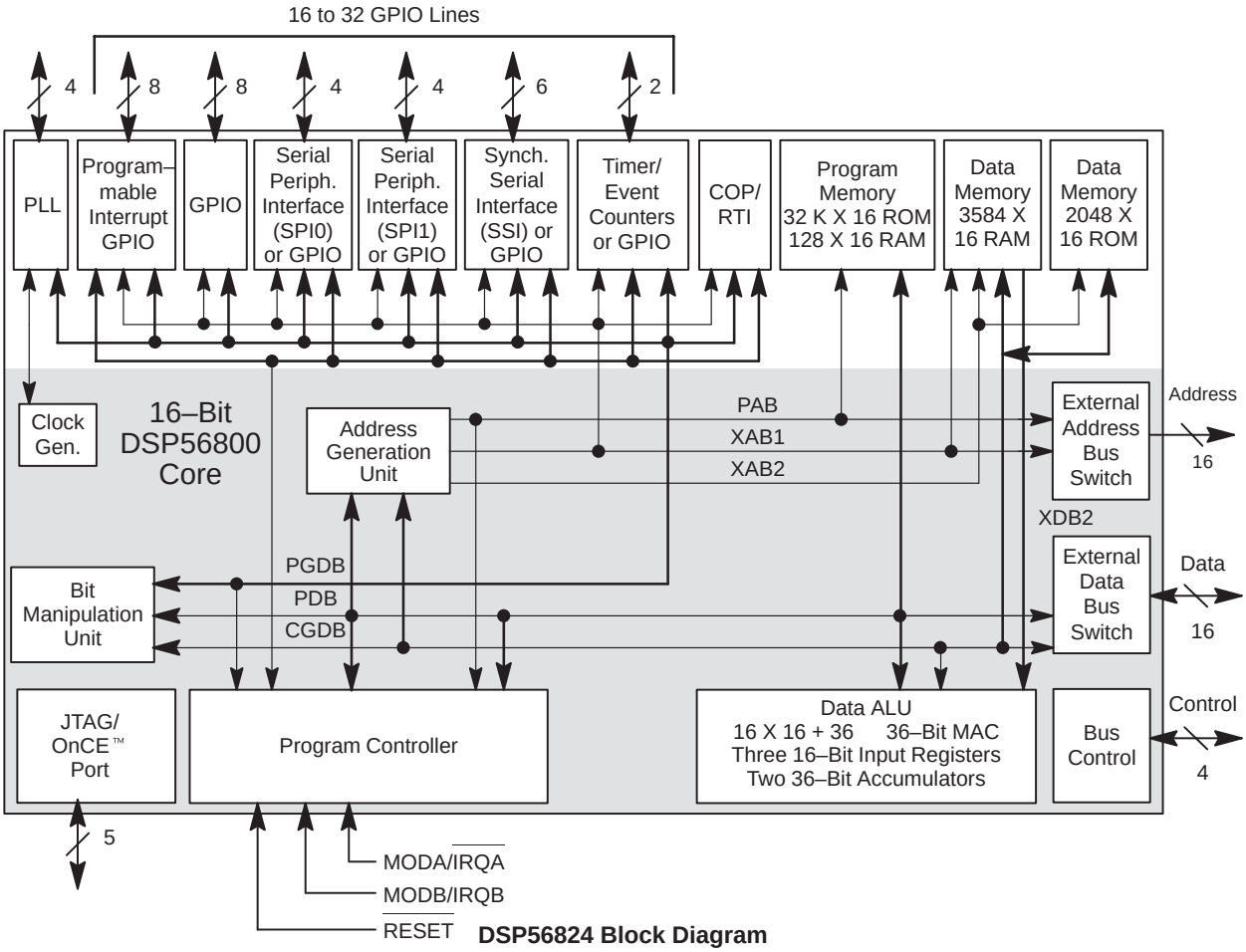


2

DSP56824—16-Bit Digital Signal Processor

The DSP56824 is a member of the DSP56800 core–based family of Digital Signal Processors (DSPs). This general purpose DSP combines processing power with configuration flexibility, making it an excellent cost–effective solution for signal processing and control functions. Because of its low cost, configuration flexibility, and compact program code, the DSP56824 is well–suited for cost–sensitive applications, such as digital wireless messaging, servo and motor control, digital answering machines/feature phones, modems, and digital cameras. The DSP56800 core consists of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MPU–style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C Compilers. The DSP56824 supports program execution from either internal or external memories. Two data operands can be accessed from the on–chip data RAM per instruction cycle. The rich set of programmable peripherals and ports provides support for interfacing multiple external devices, such as codecs, microprocessors, or other DSPs. The DSP56824 also provides two external dedicated interrupt lines and sixteen to thirty–two General Purpose Input/Output (GPIO) lines, depending on peripheral configuration (see the following figure).

DSP56824—16-Bit Digital Signal Processor (continued)



DSP56824 Block Diagram

DSP56824 Features

Digital Signal Processing Core

- Efficient 16–bit DSP56800 family DSP engine
- As many as 35 Million Instructions Per Second (MIPS) at 70 MHz
- Single–cycle 16 16–bit parallel Multiplier–Accumulator (MAC)
- Two 36–bit accumulators including extension bits
- 16–bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with unlimited depth

Memory

- On–chip Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On–chip memory
  - — 32 K x 16 Program ROM
  - — 128 x 16 Program RAM
  - — 3.5 K x 16 X RAM usable for both data and programs
  - — 2 K x 16 X data ROM
- Off–chip memory expansion capabilities
  - — As much as 64 K x 16 X data memory
  - — As much as 64 K x 16 program memory

DSP56824—16-Bit Digital Signal Processor (continued)

— External memory expansion port programmable for 1 to 15 wait states
- Programs can run out of X data RAM

Peripheral Circuits

- External Memory Interface (Port A)
- Sixteen dedicated GPIO pins (eight pins programmable as interrupts)
- Serial Peripheral Interface (SPI) support: Two configurable four–pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
  — Supports LCD drivers, A/D subsystems, and MCU systems
  — Supports inter–processor communications in a multiple master system
  — Supports demand–driven master or slave devices with high data rates
- Synchronous Serial Interface (SSI) support: One 6–pin port (or six additional GPIO lines)
  — Supports serial devices with one or more industry–standard codecs, other DSPs, microprocessors, and Motorola SPI–compliant peripherals
  — Allows implementing synchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
  — Supports Network mode using frame sync and as many as 32 time slots
  — Can be configured for 8–bit, 10–bit, 12–bit, and 16–bit data word lengths
- Three programmable 16–bit timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
- Computer–Operating Properly (COP) and Real–Time Interrupt (RTI) timers
- Two external interrupt/mode control pins
- One external reset pin for hardware reset
- JTAG/On–Chip Emulation (OnCE™) 5–pin port for unobtrusive, processor speed–independent debugging
- Extended debug capability with second breakpoint and 8–level OnCE FIFO history buffer
- Software–programmable, Phase Lock Loop–based (PLL–based) frequency synthesizer for the DSP core clock

Energy Efficient Design

- A single 2.7-3.6 V power supply
- Power–saving Wait and multiple Stop modes available
- Fully static, HCMOS design for 70 MHz to dc operating frequencies
- Available in plastic 100–pin Thin Quad Flat Pack (TQFP) surface–mount package

Product Documentation

The three documents listed in the following table are required for a complete description of the DSP56824 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

DSP56824 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the DSP56800 family architecture, and 16–bit DSP core processor and the instruction set	DSP56800FM/AD
DSP56824 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56824	DSP56824UM/AD
DSP56824 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56824/D

MC68175 FLEX™ Chip

FLEX protocol is a multi-speed, high-performance protocol adopted by leading service providers worldwide as a de facto paging standard. FLEX protocol gives service providers the increased capacity, added reliability, and enhanced pager battery performance they need today. It also provides an upward migration path to the service provider that is completely transparent to the end user.

MC68175 FLEX Chip (continued)

The MC68175 FLEX chip IC is part of a total solution available from Motorola for providing FLEX capabilities in a low-power, low-cost system. The FLEX chip simplifies implementation of a FLEX paging device by interfacing with any of several off-the-shelf paging receivers, such as the MC13150 or MC3374, and any of several off-the-shelf host microcontroller/microprocessors. The primary function of the FLEX chip is to process information received and demodulated from a radio paging channel, select messages addressed to the paging device, and communicate the message information to the host. The host interprets the message information in an appropriate manner (numeric, alphanumeric, binary, etc.) and handles all the I/O activity. The FLEX chip IC also operates the paging receiver in an efficient Power Consumption mode and enables the host to operate in a low power mode when message information for the paging device is not being received.

FLEX Chip Features

- FLEX paging protocol signal processor
- Sixteen programmable user address words
- Sixteen fixed temporary addresses
- 1600, 3200, and 6400 bits per second (bps) decoding
- Any-phase decoding
- Uses standard Serial Peripheral Interface (SPI) in Slave mode
- Wide operating voltage range from 3.3 V down to 1.8 V
- Allows low current Stop mode operation of host processor
- Highly programmable receiver control
- Real time clock time base
- FLEX fragmentation, and group messaging support
- Real time clock over-the-air update support
- Compatible with synthesized receivers
- Low battery indication (external detector)
- 32-pin Thin Quad Flat Pack (TQFP) package
- Operating temperature range 0° to +70°C (32° to 158°F)

2

DSP Development Tools

Application Development Systems

The 56002 is supported by a multi-component Application Development System (ADS), which acts as a tool for designing, debugging, and evaluating real-time DSP target system equipment. The ADS simplifies evaluation of the user's prototype hardware/software product by making all of the essential timing and I/O circuitry easily accessible. Using an IBM PC™, a Sun-4™, or Hewlett-Packard Series 700 as a medium between the user and the DSP hardware significantly reduces the overall complexity and cost of development while increasing the capabilities of the system. With the ADS, DSP programs can be executed in real-time, single-instruction-traced or multiple-instruction-stepped, with registers and/or memory block contents displayed. The ADS is fully compatible with the CLAS design-in software package and may act as an accelerator for testing DSP algorithms.

The Application Development System offers an On-Chip Emulation (OnCE™) circuit for unobtrusive, processor speed independent debugging. The ADS takes full advantage of this circuit to allow the user non-intrusive control of the target.

General ADS Features

Software

- Single/multiple stepping through DSP object programs
- Conditional/unconditional software and hardware breakpoints
- Program patching using a single-line Assembler/disassembler
- Session and/or command logging for later reference
- Loading and saving of files to/from Application Development Module (ADM) memory
- Macro command definition and execution
- Display enable/disable of registers and memory
- Debug commands which support multiple DSP development
- Hexadecimal/decimal/binary calculator
- Multiple input/output file access from DSP object programs
- On-line help screens for each command and register

Hardware

- Full speed operation at 40–66 MHz
- Multiple ADM support with programmable ADM addressing

DPS Development Tools—Application Development Systems (continued)

- Stand-alone operation of ADM after initial development

DSP56002ADS Features

- Host operating system commands from within ADS user interface program
- 8 K/32 K words of configurable RAM for DSP56002 code development
- 96-pin euro-card connector for accessing all DSP56002 pins
- 1 K words of monitor ROM expandable to 4 K words
- Separate connectors for accessing serial or host/ DMA ports

DSP56002ADM Description and Features

The DSP56002ADM has various options to facilitate evaluation of the different features of the chip. These options are outlined in this chapter with a statement on the default factory jumpers with which the Application Development Module (ADM) will be shipped.

Memory decoding is minimal to achieve zero wait accesses. Therefore, memory may overlap into other address blocks within a 32 K address space. There are a variety of jumper options for partitioning the memory to make it appear in all three Digital Signal Processor (DSP) memory maps.

Sockets for 256 K Static Random Access Memories (SRAMS) are available for increasing memory size to the maximum 64 K words for each of the three external memory spaces. Electronically Programmable Read Only Memory (EPROM) sockets are also available for stand alone operation. The EPROM is only accessible in program memory space.

Connectors exist for each on–chip peripheral port as well as two 96 pin access points to hook boards and/or logic analyzers. An Audio Engineering Society/European Broadcasters Union (AES/EBU) connector is also provided so that a user may hook the DSP56401 AES/EBU evaluation board for developing digital stereo application software.

The OnCE™ port interface connector normally hooks to the ADS Command Converter, providing the user a way of controlling the DSP56002 in a target system. This connector has a standard pinout that should be used to design the target application hardware. It will allow the user to evaluate the hardware and software of the application without using a special emulator.

An overview description of the DSP56002ADM is also provided in the DSP56002ADM Product Information document (order number DSP56002ADMP/D) included with this kit. The main features of the DSP56002ADM include the following:

- Full speed operation at 40–66 MHz
- 16 K words of configurable SRAM expandable to 64 K words
- Additional SOJ sockets for 256 K words of Fast SRAM
- 2 K words of EPROM with sockets expandable to 32 K words
- Stand–alone operation of ADM after initial development
- Full support of multiple data memory maps
- 96–Pin connector which provides access to all DSP56002 pins
- RS232 voltage converter for Asynchronous Serial Interface
- OnCE port Connector for easy hookup to DSP56002 Command Converter
- Separate connectors for easy access to on–chip peripherals

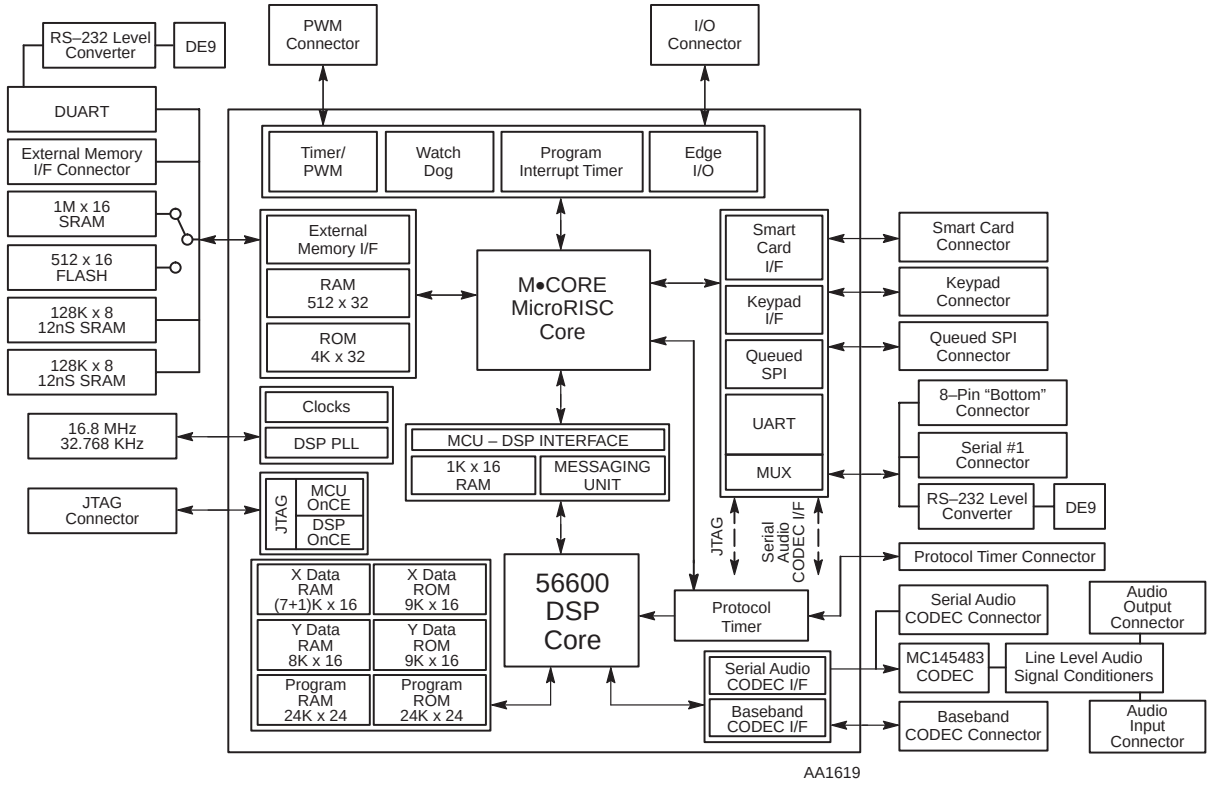
Call your local Motorola sales office or distributor for additional information about the Motorola Application Development System (ADS) kit. The ADS kit includes two additional boards: a host interface card and an external universal Command converter. The host interface card plugs in the host bus (on an IBM–compatible PC, HP7xx workstation, or Sun/Sun–compatible system) inside the computer chassis. The external universal Command Converter card connects to the host card via a 37–pin ribbon cable. The Command Converter card connects to the JTAG connector on the DSP56002ADM via another short 14–pin ribbon cable. The ADS is only compatible with Motorola software tools.

DSP56651 Applications Development System

The DSP56651 applications development system (DSP56651ADSA) is designed as a full–featured platform for developing real–time software and hardware products to support a new generation of applications in wireless and telecommunications products. The DSP56651 chip combines the power of Motorola's 32–bit M•CORE™ MicroRISC Engine (MCU) with a 24/16–bit DSP56600 digital signal processor (DSP) core, on–chip memory, protocol timers, and custom peripherals to provide a single–chip cellular base–band processor. The DSP56651ADS features on–board flash memory, two banks of SRAM, UARTs, and voice codec, as well as a daughter card with a 16–button keypad and 128 x 64 pixel graphic/character LCD display.

The ADS also includes the M•CORE C compiler, the DSP56600 C compiler, assembler, linker, debugger, and simulator, as well as all the necessary documentation. The user can connect hardware, such as external memories and analog–to–digital (A/D) or digital–to–analog (D/A) converters, thus making the DSP56651ADM ideal for developing products that will use the DSP56652, for implementing and demonstrating communications and audio processing algorithms, and for learning the architecture and instruction sets of the DSP5665X family. The DSP56651ADS is available for IBM–compatible PCs with a host interface card for industry standard architecture (ISA) interfaces, allowing the user to download software to on–chip or on–board RAM, then to run and debug it. The following figure shows the functional block diagram for the DSP56651ADM.

2



DSP56651ADM Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56651 Applications Development System (continued)

Features

Hardware

- DSP56651 integrated cellular baseband processor
  - — RISC M•CORE MCU
    - — 32–bit load/store RISC architecture
    - — Fixed 16–bit instruction length
    - — 16–entry 32–bit general–purpose register file
    - — 32–bit internal address and data buses
    - — Efficient four–stage, fully interlocked execution pipeline
    - — Single–cycle execution for most instruction, two–cycle executing for branches and memory accesses
    - — Special branch, byte, and bit manipulation instructions
    - — Support for byte, half–word, and word memory accesses
    - — Fast interrupt support via vectoring/auto–vectoring and a 16–entry dedicated alternate register file
  - — High–performance DSP56600 core
    - — 1 x engine (e.g., 58.8 MHz = 58.8 MIPS)
    - — Fully pipelined 16 x 16–bit parallel multiplier–accumulator (MAC)
    - — Two 40–bit parallel barrel shifter
    - — Highly parallel instruction set with unique DSP addressing modes
    - — Position–independent code (PIC) support
    - — Nested hardware DO loops
    - — Fast auto–return interrupts
    - — On–chip support for software patching and enhancements
    - — Real–time trace capability via external address bus
  - — On–chip memories
    - — 4 K x 32–bit MCU ROM
    - — 512 x 32–bit MCU RAM
    - — 24 K x 24–bit DSP program RAM
    - — 24 K x 24–bit DSP program ROM
    - — 18 K x 16–bit DSP data ROM, split into 9 K x 16–bit X and 9 K x 16–bit Y data ROM spaces
    - — 16 K x 16–bit DSP data RAM, split into (7+1) K x 16–bit X and 8 K x 16–bit Y data RAM spaces
  - — On–chip peripherals
    - — Fully programmable phase–locked loop (PLL) for DSP clock generation
    - — External interface module (EIM) for glueless system integration
    - — External 22–bit address and 16–bit data MCU buses
    - — 32–source MCU interrupt controller
    - — Intelligent MCU/DSP interface (MDI) dual 1K x 16–bit RAM (shares 1K DSP X data RAM) with messaging status and control
    - — Serial audio codec port
    - — Serial baseband codec port
    - — Protocol timer frees the MCU from radio channel timing events
    - — Queued serial peripheral interface (QSPI)
    - — Keypad port capable of scanning up to an 8 x 8 matrix keypad
    - — General–purpose MCU and DSP timers
    - — Pulse width modulation (PWM) output
    - — Universal asynchronous receiver/transmitter (UART) with FIFO
    - — IEEE 1149.1–compliant boundary scan Joint Test Action Group (JTAG) test access port (TAP)
    - — Integrated DSP/M•CORE On–Chip Emulation (OnCE™) module
    - — DSP address bus visibility mode for system development
    - — ISO 7816–compatible Smart Card port
  - — Operating features
    - — Comprehensive static and dynamic power management
    - — M•CORE operating frequency: dc to 16.8–MHz at 2.4 V
    - — DSP operating frequency: dc to 58.8–MHz at 2.4 V
    - — Operating temperature:—40° to 85°C ambient
    - — Package: 17 x 17 mm, 196–lead PBGA
- 512 K x 16–bit flash memory
- Flash emulation bank 1 M x 16–bits
- 128 K x 16–bit or 256 K x 8–bit FSRAM
- Voice codec MC145483 with audio signal conditioning logic
- Interface connections
  - — EIM for memory (SRAM, flash, etc.) or peripherals (LCD, etc.)
  - — Keypad
  - — DSP56651 UART
  - — On–board dual UART
  - — Baseband codec serial port (BBP)
  - — Audio codec serial port (SAP)

DSP56651 Applications Development System (continued)

— QSPI
— Protocol timer
— SIM card interface
— Logic–analyzer interface
— Reset IN/OUT signals
— Power

- 14–pin ribbon target JTAG/OnCE™ debug connector
- 37–pin ribbon host computer interface cable
- 8–pin bottom connector
- UARTs
  — DSP56651 UART buffer with RS–232 compatible port
  — On–board UART buffer with RS–232 compatible port
- 16.8 MHz and 32.768 kHz clock sources
- 16–key, keypad daughter card with 128 x 64 pixel graphic/character LCD
- Power supply 7-12 V AC/DC 1AmA 2.1 mm (inside positive) power connector

Software

- DSP56600 Motorola Development Tools Software including the following:
  — Motorola 56600 GNU Compiler
  — Assembler
  — Linker
  — Hardware Debugger
  — Simulator
  — DSP56651/2 Drivers
  — Corresponding user's documentation
- Evaluation SDS CD–ROM containing M•CORE Singlestep™ debugger software
- Evaluation Diab CD–ROM containing M•CORE C compiler software

User Requirements

The user must provide the following:

- IBM–compatible PC (Pentium–90MHz) running Windows 95 or NT, 32Mbytes RAM, 3–1/2 inch diskette drive, CD–ROM drive, hard drive with 50Mbytes of free disk Space, open ISA slot for host card, and a mouse.

2

Supporting Documentation

The first three documents listed in the following table are required for a complete description of the DSP56651 chip and are necessary to design properly with the part. The fourth and fifth documents provide a description of the DSP56651ADM, including installation and use. These documents are provided with the DSP56651ADM. Additional copies are available from one of the following locations. (See back cover for detailed information.)

- A local Motorola distributor
- A Motorola semiconductor sales office
- Motorola literature distribution center
- The World Wide Web (WWW)

You can order DSP56651ADM literature by using the document order number provided in the table below.

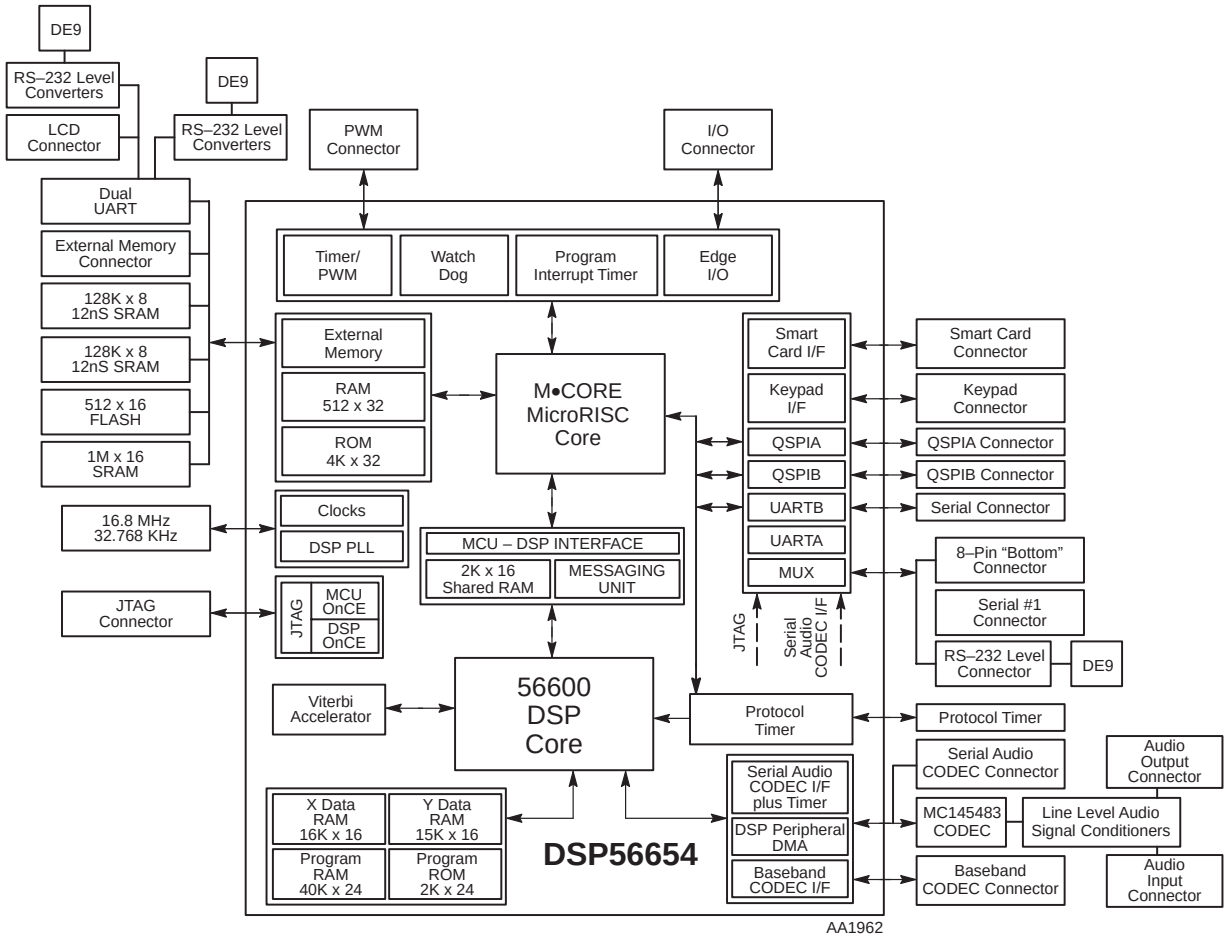
DSP56651 Documentation List

Document Name	Description	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family processor core and instruction set	DSP56600FM/AD
DSP56652 User's Manual	Detailed functional description of the DSP56652 memory configuration, operation, and register programming	DSP56652UM/D
DSP56651 Technical Data	DSP56651 features list and physical, electrical, timing, and package specifications.	DSP56651/D
DSP56651ADSA Product Brief	Overview description of the DSP56651ADS, including block diagram and list of features	DSP56651ADSAP/D
DSP56651ADM User's Manual	Detailed functional description of the DSP56651ADM, including requirements, installation, and general operating guidelines	DSP56651ADMUM/D
M•CORE Family Manual	Detailed description of the system interface, development support, the hardware accelerator unit, and on–chip peripherals for the microcontroller.	MCORERM/AD

DSP56654 Applications Development System

The DSP56654 applications development system (DSP56654ADS) is designed as a full–featured platform for developing real–time software and hardware products to support a new generation of applications in wireless and telecommunications products. The DSP56654 chip combines the power of Motorola's 32–bit M•CORE™ MicroRISC Engine (MCU) with a 24/16–bit DSP56600 digital signal processor (DSP) core, on–chip memory, protocol timers, and custom peripherals to provide a single–chip cellular base–band processor. The DSP56654ADS features on–board flash memory, two banks of SRAM, UARTs, and voice codec, as well as a daughter card with a 16–button keypad and 128 x 64 pixel graphic/character LCD display.

The ADS also includes the M•CORE C compiler, the DSP56600 C compiler, assembler, linker, debugger, and simulator, as well as all the necessary documentation. The user can connect hardware, such as external memories and analog–to–digital (A/D) or digital–to–analog (D/A) converters, thus making the DSP56654ADM ideal for developing products that will implement and demonstrate communications and audio processing algorithms. The DSP56654ADS is available for IBM–compatible PCs with a host interface card for industry standard architecture (ISA) interfaces, allowing the user to download software to on–chip or on–board RAM, then to run and debug it. The following figure shows the functional block diagram for the DSP56654ADM.



DSP56654ADS Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56654 Applications Development System (continued)

Features

Hardware

- DSP56654 integrated cellular baseband processor
  - — RISC M•CORE MCU
  - — 32–bit load/store RISC architecture
  - — Fixed 16–bit instruction length
  - — 16–entry 32–bit general–purpose register file
  - — 32–bit internal address and data buses
  - — Efficient four–stage, fully interlocked execution pipeline
  - — Special branch, byte, and bit manipulation instructions
  - — Support for byte, half–word, and word memory accesses
  - — Fast interrupt support via vectoring/ auto–vectoring and a 16–entry dedicated alternate register file
  - — High–performance DSP56600 core
    - — 1 x engine (e.g., 70 MHz = 70 MIPS)
    - — Fully pipelined 16 x 16–bit parallel multiplier–accumulator (MAC)
    - — Two 40–bit accumulators including extension bits
    - — 40–bit parallel barrel shifter
    - — Highly parallel instruction set with unique DSP addressing modes
    - — Position–independent code support
    - — Nested hardware DO loops
    - — Fast auto–return interrupts
    - — On–chip support for software patching and enhancements
    - — Real–time trace capability via external address bus
  - — On–chip memories
    - — 4 K x 32–bit MCU ROM
    - — 512 x 32–bit MCU RAM
    - — 40 K x 24–bit DSP Program RAM
    - — 2 K x 24–bit DSP Program ROM
    - — 31 K x 16–bit DSP data RAM, split into 16 K x 16–bit X data RAM and 15 K x 16–bit Y data RAM spaces
    - — 2 K x 16 DSP/MCU interface, dual port RAM (part of the 16 K x 16 X data RAM)
  - — On–chip peripherals
    - — Fully programmable phase–locked loop (PLL) for DSP clock generation
    - — External interface module (EIM) for glueless system integration
    - — External 22–bit address and 16–bit data MCU buses
    - — Thirty–two source MCU interrupt controller
    - — Intelligent MCU/DSP interface (MDI) dual 2 K x 16–bit dual port RAM (shares 2 K DSP X data RAM) with messaging status and control
    - — Serial audio codec port
    - — Serial baseband codec port
    - — Protocol timer frees the MCU from radio channel timing events
    - — Two queued serial peripheral interface (QSPI) communicate with external peripherals
    - — Keypad port capable of scanning up to an 8 x 8 matrix keypad
    - — Software watchdog timer, DSP timer, O/S programmable interrupt timer, and MCU general–purpose timers
    - — Pulse width modulation (PWM) output
    - — Two universal asynchronous receiver/transmitter (UARTs) with FIFO
    - — IEEE 1149.1–compliant boundary scan JTAG test access port (TAP)
    - — Integrated DSP/M•CORE On–Chip Emulation (OnCE™) module
    - — DSP address bus visibility and DSP data bus visibility modes for system development
    - — ISO 7816–compatible SmartCard port
  - — Operating features
    - — Comprehensive static and dynamic power management
    - — M•CORE operating frequency: dc to 16.8 MHz at 1.8 V
    - — DSP operating frequency: dc to 58.8 MHz at 1.8 V
    - — Internal operating voltage range: 1.8-2.5 V with 3.3 V–tolerant I/O
    - — Operating temperature: -40° to 85°C ambient
    - — 256–pin 17 x 17mm plastic ball grid array (PBGA) package
- 512 K x 16–bit flash memory
- Flash emulation bank 1 M x 16–bits
- 128 K x 16–bit or 256 K x 8–bit FSRAM
- Voice codec MC145483 with audio signal conditioning logic
- Interface connections
  - — EIM for memory (SRAM, flash, etc.) or peripherals (LCD, etc.)
  - — Keypad
  - — DSP56654 UART
  - — On–board dual UART
  - — Baseband codec serial port (BBP)

DSP56654 Applications Development System (continued)

  - — Audio codec serial port (SAP)
  - — QSPIA and QSPIB
  - — Protocol timer
  - — SIM card interface
  - — Logic–analyzer interface
  - — Reset IN/OUT signals
  - — Power
- 14–pin ribbon target JTAG/OnCE™ debug connector
- 37–pin ribbon host computer interface cable
- 8–pin bottom connector
- UARTs
  - — DSP56654 UART buffer with RS–232 compatible port
  - — On–board UART buffer with RS–232 compatible port
- 16.8 MHz and 32.768 kHz clock sources
- 16–key, keypad daughter card with 128 x 64 pixel graphic/character LCD
- Power Supply 12 V ac/dc 1 AMP with 2.1 mm receptacle (inside positive) power connector

Software

- DSP56600 Motorola Development Tools Software including the following:
  - — Motorola 56600 GNU Compiler
  - — Assembler
  - — Linker
  - — Hardware Debugger
  - — Simulator
  - — DSP56654 Drivers
  - — Corresponding user's documentation
- Evaluation SDS CD–ROM containing M•CORE Singlestep™ debugger software
- Evaluation Diab CD–ROM containing M•CORE C compiler software

User Requirements

The user must provide the following:

- Windows PC (Pentium® class processor or higher) running Windows® 95 operating system with 16 Mbytes of RAM or Windows NT® 4.0 (or higher) operating system with 32 Mbytes RAM, 3–1/2 inch diskette drive, CD–ROM drive, hard drive with 50 Mbytes of free disk space, open ISA slot for host card, and a mouse.

Supporting Documentation

The first four documents listed in the following table are required for a complete description of the DSP56654 chip and are necessary to design properly with the part. The fourth and fifth documents provide a description of the DSP56654ADM, including installation and use. These documents are provided with the DSP56654ADM. Additional copies of the first three are available from one of the following locations. (See back cover for detailed information.)

- A local Motorola distributor
- A Motorola semiconductor sales office
- Motorola literature distribution center
- The World Wide Web (WWW)

You will need the order number, listed in the following table, when ordering these documents.

You can order DSP56654ADM literature via the World Wide Web from URL:

http://www.mot.com/SPS/WIRELESS/dsptools.

Documentation List

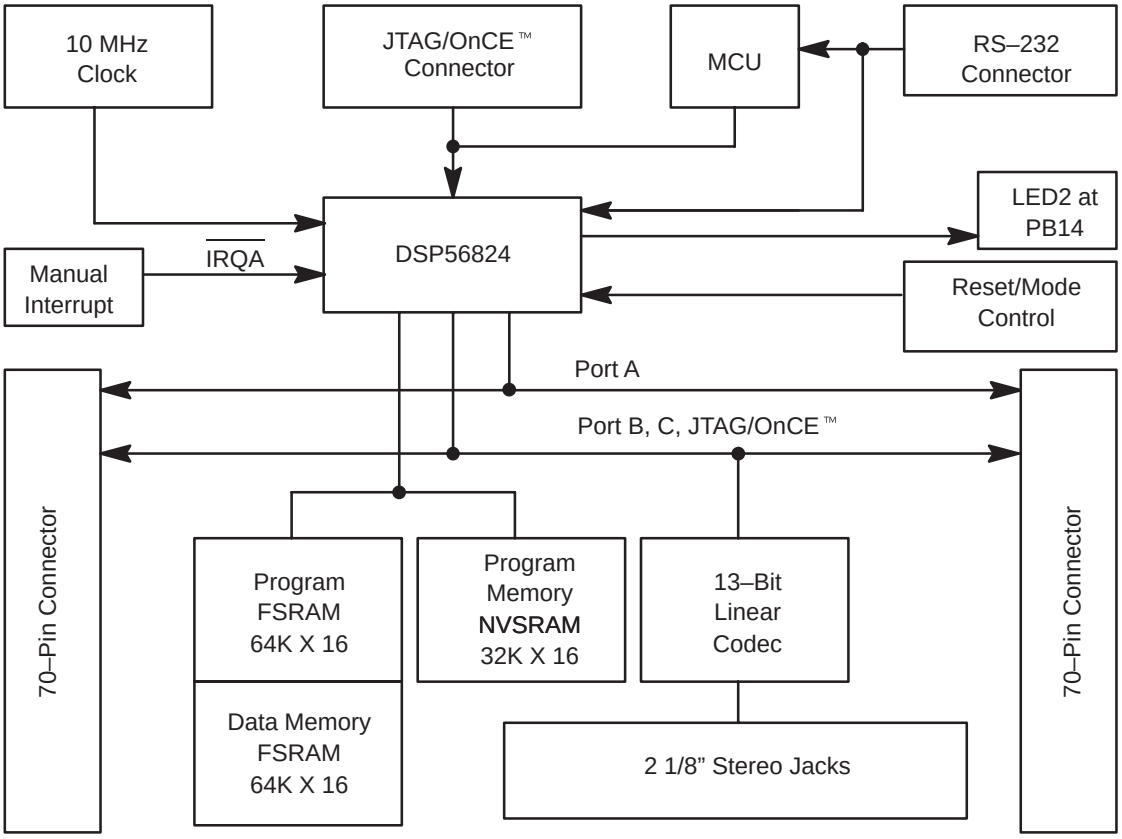
Document Name	Description	Order Number
DSP56600 Family Manual	Detailed description of the Family family processor core and instruction set	DSP56600FM/AD
DSP56654 User's Manual	Detailed functional description of the DSP56654 memory configuration, operation, and register programming	DSP56654UM/D
DSP56654 Technical Data	DSP56654 features list and physical, electrical, timing, and package specifications.	DSP56654/D
M•CORE Reference Manual	Detailed description of the system interface, development support, the hardware accelerator unit, and on–chip peripherals for the microcontroller.	MCORERM/AD
DSP56654ADS Product Brief	Overview description of the DSP56654ADS, including block diagram and list of features	DSP56654ADSAP/D
DSP56654ADM User's Manual	Detailed functional description of the DSP56654ADM, including requirements, installation, and general operating guidelines	DSP56654ADMUM/D

DSP56824 Applications Development System

The DSP56824 Applications Development System (ADS) is designed as a full–featured platform for developing realtime software and hardware products to support a new generation of applications in digital messaging, two–way radio, speech processing, and consumer electronics. The power of the 16–bit DSP56824 Digital Signal Processor (DSP) combined with the on–board 64K x 16–bit external program and static RAM (SRAM) 64K x 16–bit external data static RAM, 32K 16–bit external Non–Volatile Static RAM (NVSRAM) and Motorola's MC145483 13–bit linear voice audio codec makes the DSP56824ADS ideal for developing and implementing many messaging and audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56824 processor.

This system is available for IBM–PC–compatible and Sun hosts, with a host interface card for ISA or Sun S–bus interfaces, allowing the user to download software to on–chip or on–board RAM, then run and debug it. With the on–board expansion connectors, the user can connect hardware such as external memories and other devices, such as A/D or D/A converters, keypads, displays, and so forth. The following figure shows the functional block diagram for the DSP56824ADS.

2



DSP56824ADS Block Diagram

DSP56824 Features

Digital Signal Processing Core

- Efficient 16–bit DSP56800 family DSP engine
- As many as 20 Million Instructions Per Second (MIPS) at 40 MHz
- Instruction set supports both DSP and controller functions
- Software subroutine and interrupt stack with unlimited depth

Memory

- On–chip Harvard architecture
- 24 K x 16 program Flash memory
- 2 K x 16 data Flash memory
- 2 K x 16 Data RAM

DSP56824 Applications Development System (continued)

- Off–chip memory expandable to 64 K x 16 Data and 64 K x 16 program memory
- External memory expansion port programmable for 1 to 15 wait states

Peripheral Circuits

- External Memory Interface (Port A)
- Sixteen dedicated General Purpose Input/Output (GPIO) pins
- Serial Peripheral Interface (SPI) support: Two configurable 4–pin ports (SPI0 and SPI1)
- Synchronous Serial Interface (SSI) support: One 6–pin port (or six additional GPIO lines)
- Three programmable 16–bit timers
- Computer–Operating Properly (COP) and Realtime Interrupt (RTI) timers
- Two external interrupt/mode control pins and one external reset pin for hardware reset
- Software–programmable, Phase Lock Loop–based (PLL–based) frequency synthesizer

Energy Efficient Design

- Fully static, HCMOS design for 40 MHz to dc operating frequencies
- A single 2.7-3.6V power supply with 5 V–compatible I/O interface
- Power–saving Wait and multiple Stop modes available

DSP56824ADS Features

The DSP56824ADS kit contains the following components:

- DSP56824 Application Development Module (ADM) board
  - — DSP56824 processor
  - — All DSP signal lines accessible through top and bottom board connectors
  - — On–board codec with stereo input/output jacks
  - — User–replaceable oscillator clock chip for custom clocking requirements
- Command Converter card
- ISA Bus or Sun S–Bus Host Interface card
- Power supply and data connecting cables
- Motorola Development Tools software including the CLAS package
  - — Graphical User Interface (GUI) simplifies code development
  - — Compiler, Linker, and Assembler provide optimized code
- Supporting chip, software, and ADS documentation on CD–ROM

The DSP56824ADS is also available with a socketed DSP56824 processor (extra cost option).

Target Applications

The DSP56824ADS is intended as a full–featured platform for developing realtime software and hardware products to support a new generation of applications in digital messaging, two–way radio, speech processing, and consumer electronics.

System requirements

The Motorola Software Development Tools runs on PC–compatible, Sun and HP workstations with the following minimum configurations.

- PC–compatible computer (Pentium – 90 MHz or higher) running Windows™ 95 or Windows NT 4.0, 32 Mbytes RAM, CD–ROM drive, hard drive with 50 Mbytes of free disk space, and a mouse
- Sun SPARCstation running SunOS 4.1.3 or later or Solaris 2.5, CD–ROM drive, hard drive with 60 Mbytes of free disk space
- HP workstations, running HP–UX Version 9.x, CD–ROM drive, hard drive with 60 Mbytes of free disk space.

Ordering Information

The following table provides the ordering information for the DSP56824ADS.

DSP56824ADS Ordering Information

Description	Order Number
DSP56824ADS with ISA Host Interface adapter card for use with IBM–PC–compatible systems	DSP56824ADSA
DSP56824ADS with Sun S–Bus Host Interface adapter card for use with Sun S–Bus systems	DSP56824ADSF

Evaluation Modules

DSP56002EVM

The DSP56002EVM Evaluation Module is a low-cost platform designed to familiarize the user with Motorola's DSP56002 Digital Signal Processor (DSP). The 24-bit precision of the DSP combined with the on-board 32 K words of external SRAM and stereo CD-quality audio codec makes the Evaluation Module ideal for implementing and demonstrating many audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56002 processor. The user need only supply a 7–9 volt calculator-style power supply and an RS-232 serial cable.

The DSP56002EVM comes with Motorola's DSP56000 cross Assembler and Domain Technologies' debug software with windowed user interface. The software runs under MS-DOS on an IBM PC-compatible computer (386 class or higher) and communicates with the Evaluation Module over an RS-232 serial port.

Hardware Features

Fully assembled and tested Printed Circuit Board containing:

- 24-bit DSP56002 Digital Signal Processor operating at 40 MHz
  - — Up to 20 Million Instructions Per Second (MIPS)
    - 50 ns instruction cycle at 40 MHz
  - — Up to 120 Million Operations Per Second (MOPS) at 40 MHz
  - — Executes a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories
  - — 512 x 24-bit on-chip Program RAM with bootstrap ROM
  - — Two 256 x 24-bit on-chip data RAMs
  - — Two 256 x 24-bit on-chip data ROMs containing sine, A-law, and μ-law tables
  - — External memory expansion with 16-bit address and 24-bit data buses
  - — Byte-wide Host Interface (HI) with Direct Memory Access support
  - — Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
  - — Serial Communication Interface (SCI) for full-duplex asynchronous communications
  - — 24-bit Timer/Event Counter also generates and measures digital waveforms
  - — On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
  - — Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer
- 32 K x 24-bit zero-wait-state external Static RAM for expansion memory
  - — Option for 32 K x 8 bits of flash EEPROM for program bootstrapping and stand-alone operation
- Crystal Semiconductor's CS4215 stereo CD-quality sigma-delta Analog-to-Digital and Digital-to-Analog converter for high quality audio
  - — 24.576 MHz crystal for audio sampling rates of 48, 32, 16, 9.6, or 8 kHz
  - — 16-bit linear, 8-bit μ-law, 8-bit A-law, and 8-bit linear data formats
  - — Option for other crystals/frequencies for other sample rates, such as 44.1 kHz
- MC7805ACT voltage regulator
- RS-232 interface to OnCE™ controller and Serial Communications Interface (SCI)
  - — Option for a second RS-232 connector for access to the DSP56002 processor's serial communications port (SCI)
- MC68HC705K1 microcontroller performing RS-232-to-OnCE command conversion
- MC33078 pre-amp for analog buffering
- Strip connectors for external access to the DSP56002's memory expansion, Host Interface, and serial communications ports
- Jacks for stereo inputs, outputs, and headphones
- 2.1 mm jack and two screw terminals for power connection
- Documentation for the DSP56002, CS4215, Assembler, and debugger; plus board schematics

Software Features

- Motorola's DSP5600x Cross Assembler
  - — DSP56002 binary code from source code using labels, line numbers, definitions, and titles incorporating the architecture's complete instruction set and addressing modes, memory spaces, and parallel data transfers
  - — Macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - — Reports for cross-references, instruction cycle count, and memory use
  - — Extensive error checking and reporting

DSP56002EVM—Evaluation Modules (continued)

- — Six channels D/A audio quality conversion with 18-bit quality
- Domain Technologies' debug software with windowed user interface
  - — Symbolic debugging
  - — Four independent windows for data, disassembly, DSP registers, and commands
  - — Data and registers displayed as fractions, decimals, or hexadecimals
  - — Symbolic addressing and animated ASCII graphical display of memory segments
  - — Up to eight simultaneous breakpoints
  - — Built-in Assembler and disassembler
- Installation instructions and user notes on disk
- Demo software showing the advantages of 24 bits over 16 bits in audio processing
- Self-test files
  - — Executable and source code

2

DSP56007EVM

The DSP56007EVM Evaluation Module is a low-cost platform for multichannel digital audio applications development and prototyping. It demonstrates the capabilities and features of Motorola's DSP Symphony™ audio products which include the DSP56004, the DSP56004ROM, and the DSP56007. The DSP56007EVM features a DSP56007 with embedded software including FFTs, FIRs, and IIR filters useful in a variety of user developed audio software.

Special versions of the DSP56007EVM are available to authorized licensees of Dolby Laboratories and Lucasfilms Ltd. for supporting Dolby ProLogic®, Home THX™ Theater System, and Dolby AC-3® Surround (using a DSP56009).

The DSP56007EVM is a complete system with high quality stereo Analog-to-Digital conversion and Digital-to-Analog conversion. It also includes microcontroller, RS-232 to OnCE™ port debug interface, LCD display, memory, and digital audio I/O. The user need only supply a dual 8-to-12 volt power supply for analog circuits, an 8-to-15 volt power supply for digital circuits, and an RS-232 serial cable. The DSP56007EVM comes with Motorola's DSP56000 cross Assembler and Domain Technologies' debug software, which features a windowed user interface. This software runs under MS-DOS on an IBM PC-compatible computer (386 class or higher) and communicates with the Evaluation Module over an RS-232 serial port.

Hardware Features

Fully assembled and tested Printed Circuit Board containing:

- 24-bit DSP56007 Digital Signal Processor operating at 66 MHz
  - — Up to 33 Million Instructions Per Second (MIPS)
    - — 30.3 ns instruction cycle at 66 MHz
  - — Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories
  - — 2176 x 24-bit on-chip Y data RAM and 512 x 24 bit Y data ROM
  - — 1024 x 24-bit on-chip X data RAM and 512 x 24 bit X data ROM
  - — 6400 x 24-bit on-chip Program ROM of which 6348 words are available for the user code and the remaining 52 words include proprietary code for initilization and boot-straps
  - — 1024 x 24 bits of Y data RAM can be configured as Program RAM, replacing 1280 x 24 bits of Program ROM
  - — On-Chip Emulation (OnCE™) port for unobtrusive, processor speed-independent debugging
  - — Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer
- External DSP Memory
  - — 8192 bytes SRAM, 8192 bytes non-volatile RAM
  - — SRAM operates at zero wait states at 40 MHz DSP clock speed and with one wait state at 50 and 66 MHz
  - — Contents of SRAM may be block loaded into non-volatile RAM, enabling storage of bootstrap code in the lowest 3072 bytes
  - — Contents of non-volatile RAM may be block loaded into SRAM. This occurs automatically when DSP is bootstrapped in modes 1, 2, or 3
  - — 30-pin SIMM slot for easy DRAM expansion; addresses up to 4 M x 8, uses a standard Macintosh or PC SIMM
- Multichannel audio conversion
  - — Two channels (stereo) A/D audio quality conversion with 20-bit quality

DSP56007EVM—Evaluation Modules (continued)

- — Selectable 44.1 and 48 kHz sample frequencies for A/D and D/As
- — A/D may be clocked by selected sample frequency or by received SPDIF signal

- Convenient Signal I/O
  - — D/A outputs have programmable, analog-domain volume attenuators. These may be used for channel trim and master volume control to enable maximum use of D/A dynamic range at lower output levels
  - — RCA jacks for all analog audio input/output
  - — Optical and transformer-isolated electrical SPDIF/CP340 stereo digital audio inputs and outputs
  - — 50-pin expansion connector allows easy expansion and/or substitution of other input/output peripherals
- Complete User Interface
  - — MC68HC11E9 (52-pin CLCC package) allows the user to substitute user-programmed 68HC11 and prototype custom 68HC11 code
  - — 2 x 16 character Liquid Crystal Display and four soft switches for user interface
  - — Enables use of standard 4 x 4 keypad matrix
  - — Infrared remote control of user interface with optional remote
  - — MC68705 K1 microcontroller performing RS-232-to-OnCE™ port command conversions
- All technical information available for use as a reference design

Software Features

- Motorola's DSP5600x Cross Assembler
  - — DSP56007 binary code from source code using labels, sections, and macro definitions incorporating the DSP's complete instruction set, all addressing modes, and all memory spaces
  - — Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - — Reports for cross-references, instruction cycle count, and memory usage
  - — Extensive error checking and reporting
- Domain Technologies' debug software with windowed user interface
  - — Symbolic debugging
  - — Four main windows for data, code, DSP registers, and commands
  - — Data and registers displayed in fractional, decimal, or hexadecimal format
  - — Graphical display of memory segments
  - — Up to eight simultaneous software breakpoints
  - — Built-in in-line Assembler and disassembler
- Installation instructions and user notes on disk
- Demo software illustrating the advantage of 24 bits over 16 bits in audio processing
- I/O drivers and microcontroller interface software
- Microcontroller code for user interface and DSP control
- Sound field processing demo software
  - — executable and source code
- Self-test files
  - — executable and source code

2

DSP56009EVM

The DSP56009EVM Evaluation Module is a low-cost platform for multichannel digital audio applications development and prototyping. It demonstrates the capabilities and features of Motorola's DSP Symphony™ audio products, which include the DSP56004, the DSP56004ROM, the DSP56007, and the DSP56009. The DSP56009EVM features a DSP56009 with embedded software (including FFTs, FIR filters, and IIR filters) that is useful in a variety of user-developed audio software.

The DSP56009EVM is intended to provide a turnkey solution for digital audio decoding in audio/video applications, such as stereos and television sets. It provides full support for Dolby Pro Logic® and Dolby AC-3® Surround embedded in software. This on-board functionality is ready to use immediately.

This Evaluation Module is a complete system with high quality stereo Analog-to-Digital (A/D) conversion and six channels of Digital-to-Analog (D/A) conversion. The onboard circuitry includes a microcontroller, RS-232-to-On-Chip Emulation (OnCE™) port debug interface, LCD display, memory, and digital audio Input/Output (I/O). The user only needs to supply a dual 8-to-12 volt power supply for analog circuits, an 8-to-15 volt power supply for digital circuits, and an RS-232 serial cable.

DSP56009EVM—Evaluation Modules (continued)

The DSP56009EVM also includes Motorola's DSP56000 cross Assembler and Domain Technologies' Debug-56K debugging software, which runs under Microsoft® Windows™ 3.1 and Windows 95 on IBM PC-compatible computers (386 class or higher) and communicates with the evaluation module via an RS-232 serial port.

Hardware Features

The DSP56009EVM includes a fully assembled and tested Printed Circuit Board containing:

- 24-bit DSP56009 Digital Signal Processor operating at 81 MHz
  - — 40.5 Million Instructions Per Second (MIPS), 24.7 ns instruction cycle at 81 MHz
  - — Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories
  - — 4608 x 24-bit on-chip X data RAM and 3072 x 24-bit X data ROM
  - — 4352 x 24-bit on-chip Y data RAM and 1792 x 24-bit Y data ROM
  - — 512 x 24-bit Program RAM
  - — Additional 2304 x 24-bits X and Y data RAM configurable as Program RAM
  - — 10240 x 24-bit on-chip Program ROM
  - — OnCE port for unobtrusive, processor speed-independent debugging
  - — Software-programmable, Phase Lock Loop (PLL)-based frequency synthesizer
- External DSP memory
  - — 8192 bytes SRAM, 8192 bytes non-volatile RAM
  - — SRAM operates at zero wait states at 40 MHz, one wait state at 50, 66, and 81 MHz
  - — Contents of SRAM and non-volatile RAM block-loadable into non-volatile RAM
  - — Standard 30-pin SIMM slot addresses up to 4 M x 8 for easy DRAM expansion
- Complete user interface
  - — One-time-programmable MC68HC711E9 (socketed 52-pin CLCC package) allows user-programmed 68HC11 and prototyping custom 68HC11 code
  - — MC68705K1 performs RS-232-to-OnCE port command conversion
  - — 2 x 16 character LCD display, four soft switches, and optional 16-key keypad
  - — Infrared remote control of user interface with optional remote
- Convenient signal I/O
  - — D/A outputs with programmable, analog-domain attenuators for channel trim and master volume control give maximum dynamic range at lower output levels
  - — RCA jacks for all analog audio I/O
  - — Optical and transformer-isolated SPDIF/CP340 stereo digital audio I/O
  - — 50-pin expansion connector for expansion or substitution of other I/O peripherals
- Multi-channel audio conversion
  - — Two-channel (stereo) A/D audio-quality conversion with 20-bit quality
  - — Six-channel D/A audio-quality conversion with 18-bit quality
  - — Selectable 44.1 and 48 kHz sample frequencies for A/D and D/A conversion
  - — A/D clocked either by selected sample frequency or by received SPDIF signal
- Reference design information (including microcontroller code) provided on the Motorola DSP WWW site (http://www.motorola-dsp.com)

Software Features

Software included with the DSP56009EVM includes the following:

- Motorola's DSP5600x Cross Assembler
  - — Assembles binary code from source with labels, sections, and macro definitions using the full DSP instruction set, all addressing modes, and all memory spaces
  - — Allows using macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - — Generates reports for cross-references, instruction cycle count, and memory usage
  - — Provides extensive error checking and reporting
- Domain Technologies' Debug-56K debugging software with windowed user interface
  - — Provides four main windows for data, code, DSP registers, and commands
  - — Performs symbolic debugging with eight simultaneous software breakpoints
  - — Displays data and registers in fractional, decimal, or hexadecimal format
  - — Graphically displays memory segments
  - — Includes a built-in in-line Assembler and disassembler
- Installation instructions and user notes on disk
- Demo software and example pass-through code
- Interface software, drivers, and microcontroller code for user I/F and DSP control

DSP56303EVM

The DSP56303 Evaluation Module (DSP56303EVM) is designed as a low-cost platform for developing real-time software and hardware products to support a new generation of applications in wireless, telecommunications, and multimedia products using multi-line voice/data/fax processing, videoconferencing, audio applications, control, and general digital signal processing. The user can download software to on-chip or on-board RAM, then run and debug it. The user can also connect hardware, such as external memories and A/D or D/A converters, for product development. The 24-bit precision of the DSP56303 Digital Signal Processor (DSP) combined with the on-board 32 K of external SRAM and Crystal Semiconductor's CS4215 stereo, CD-quality, audio codec makes the DSP56303EVM ideal for implementing and demonstrating many communications and audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56303 processor.

Hardware Features

- 24-bit DSP56303 Digital Signal Processor
- High Performance DSP56300 core
  - — 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
  - — Object-code compatible with the DSP56000 core
  - — Highly parallel instruction set
  - — Fully pipelined 24 x 24-bit parallel multiplier-accumulator
  - — 56-bit parallel barrel shifter
  - — 24-bit or 16-bit arithmetic support under software control
  - — Position Independent Code (PIC) Support
  - — Unique DSP addressing modes
  - — On-chip memory-expandable hardware stack
  - — Nested hardware DO loops
  - — Fast auto-return interrupts
  - — On-chip concurrent six-channel DMA controller
  - — On-chip Phase Lock Loop (PLL)
  - — On-Chip Emulation (OnCE™) module
  - — JTAG port
  - — Address tracing mode reflects internal Program RAM accesses at external port

On-Chip Memories

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable
- 192 x 24-bit bootstrap ROM

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	4096 × 24-bit	0	2048 × 24-bit	2048 × 24-bit
enabled	disabled	3072 × 24-bit	1024 × 24-bit	2048 × 24-bit	2048 × 24-bit
disabled	enabled	2048 × 24-bit	0	3072 × 24-bit	3072 × 24-bit
enabled	enabled	1024 × 24-bit	1024 × 24-bit	3072 × 24-bit	3072 × 24-bit

- Off-Chip Memory Expansion
  - — Data memory expansion to two memory spaces of 256 K x 24-bit words
  - — Program memory expansion to one memory space of 256 K x 24-bit words
  - — External memory expansion port
  - — Four chip-select logic lines for glueless interface to SRAMs and SSRAMs
  - — On-chip DRAM controller for glueless interface to DRAMs
- On-Chip Peripherals
  - — Enhanced DSP56000-like 8-bit parallel Host Interface (HI08)
  - — Two Enhanced Synchronous Serial Interfaces (ESSI0 and ESSI1)
  - — Serial Communications Interface (SCI) with baud rate generator
  - — Triple timer module
  - — Up to thirty-four programmable General Purpose Input/Output (GPIO) pins, depending on which peripherals are enabled
- Reduced Power Dissipation
  - — Very low power CMOS design
  - — Wait and Stop low power standby modes
  - — Fully-static logic, operation from the device maximum frequency down to DC
- 32 K x 24-bit fast Static RAM for expansion memory
- 64 K x 8-bit Flash PEROM for stand-alone operation
- 16-bit CD-quality audio codec
  - — Two channels of 16-bit Analog-to-Digital (A/D) conversion

DSP56303EVM—Evaluation Modules (continued)

— Two channels of 16-bit Digital-to-Analog (D/A) conversion
— Software-selectable 8-bit and 16-bit data formats, including μ-law and A-law companding
— Stereo jacks for audio input, output, and headphones
- Command Converter
— DSP56002 for high-speed OnCE/JTAG command conversion software
— JTAG connector for use with the Application Development System (ADS) command converter card
- Connectors
— Host-to-ISA bus connector
— Port A connector
— ESSI0, ESSI1, and SCI connector

Software Features

- Motorola's DSP56xxx cross assembler
— Produces DSP56303 binary code from source code using labels, sections, and macro definitions incorporating the DSP's complete instruction set, all addressing modes, and all memory spaces
— Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
— Creates reports for cross-references, instruction cycle count, and memory usage
— Provides extensive error checking and reporting
- Domain Technologies debug software with Windows-based user interface
— Symbolic debugging
— Windows for data, code, DSP registers, commands, peripherals, etc.
— Data and registers displayed in fractional, decimal, or hexadecimal format
— Graphical display of memory segments
— Up to eight simultaneous software breakpoints
— Built-in-line assembler and disassembler
- Demonstration software and example pass-through code
- Self-test files
— executable and source code (Flash PEROM is preprogrammed with self-test and audio echo software.)

User Requirements

The user must provide the following:

- Power supply (7–9 V AC or DC with 2.1 mm power connector)
- RS–232 cable (DB9 male to DB9 female)
- Audio source, headphones, and a cable with 1/8–inch stereo plugs
- IBM PC compatible computer (386 class or higher) running Windows 3.1 (or higher) with an RS–232 serial port capable of 9,600–57,600 bit–per–second operation, 4 Mbytes RAM, 3–1/2 inch diskette drive, hard drive with 4 Mbyte of free disk space, and a mouse

Supporting Documentation

The first three documents listed in the following table are required for a complete description of the DSP56303 and are necessary to design properly with the part. The fourth and fifth documents provide a description of the DSP56303EVM, including installation and use. These documents are provided with the DSP56303EVM. Additional copies are available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

The DSP56303EVM can be ordered by the number listed below from the same locations.

DSP56303 Documentation List

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56303 User's Manual	Detailed functional description of the DSP56303 memory configuration, operation, and register programming	DSP56303UM/AD
DSP56303 Technical Data	DSP56303 features list and physical, electrical, timing, and package specifications	DSP56303/D
DSP56303EVM Product Information	Overview description of the DSP56303EVM, including block diagram and list of features	DSP56303EVMP/D
DSP56303EVM User's Manual	Detailed functional description of the DSP56303EVM, including requirements, installation, and general operating guidelines	DSP56303EVMUM/AD
DSP56303EVM	DSP56303 Evaluation Module kit with hardware, software, and documentation	DSP56303EVM

DSP56307EVM

DSP56307 Features

High Performance DSP56300 Core

- 100 Million Instructions Per Second (MIPS)* with a 100 MHz clock at 2.5 V (core) and 3.3 V (Input/Output)
- Object code compatible with the DSP56000 core
- Highly parallel instruction set
- Fully pipelined 24 x 24-bit parallel Multiplier-Accumulator (MAC)
- 56-bit parallel barrel shifter
- 24-bit or 16-bit arithmetic support under software control
- Position independent code support
- Addressing modes optimized for DSP applications
- On–chip instruction cache controller
- On–chip memory–expandable hardware stack
- Nested hardware DO loops
- Fast auto–return interrupts
- On–chip concurrent six–channel DMA controller
- On–chip Phase Lock Loop (PLL) and clock generator
- On–chip Emulation (OnCE™) module
- JTAG Test Access Port (TAP)
- Address Tracing mode reflects internal accesses at the external port

*170 Million Instructions Per Second using the EFCOP in filtering applications

2

On-Chip Memories

- 64 K on–chip RAM total
- Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable
- 192 x 24–bit bootstrap ROM

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache	Switch Mode	MSW1	MSW0
16 K x 24–bit	0	24 K x 24-bit	24 K x 24–bit	disabled	disabled	0/1	0/1
15 K x 24–bit	1024 x 24–bit	24 K x 24-bit	24 K x 24–bit	enabled	disabled	0/1	0/1
48 K x 24–bit	0	8 K x 24-bit	8 K x 24–bit	disabled	enabled	0	0
47 K x 24–bit	1024 x 24–bit	8 K x 24-bit	8 K x 24–bit	enabled	enabled	0	0
40 K x 24–bit	0	12 K x 24-bit	12 K x 24–bit	disabled	enabled	0	1
39 K x 24–bit	1024 x 24–bit	12 K x 24-bit	12 K x 24–bit	enabled	enabled	0	1
32 K x 24–bit	0	16 K x 24-bit	16 K x 24–bit	disabled	enabled	1	0
31 K x 24–bit	1024 x 24–bit	16 K x 24-bit	16 K x 24–bit	enabled	enabled	1	0
24 K x 24–bit	0	20 K x 24-bit	20 K x 24–bit	disabled	enabled	1	1
23 K x 24–bit	1024 x 24–bit	20 K x 24-bit	20 K x 24–bit	enabled	enabled	1	1

*Includes 4 K x 24–bit shared memory (i.e., memory shared by the core and the EFCOP)

- Off-Chip Memory Expansion
  - — Data memory expansion to two 256 K x 24-bit word memory spaces
  - — Program memory expansion to one 256 K x 24-bit word memory space
  - — External memory expansion port
  - — Chip Select Logic for glueless interface to SRAMs
  - — On-chip DRAM controller for glueless interface to DRAMs
- On-Chip Peripherals
  - — 3.0 through 3.6 V I/O interface
  - — General–purpose, fully programmable Enhanced Filter Coprocessor (EFCOP) performs filtering tasks concurrently with the DSP core with minimum core overhead
  - — 8–bit parallel Host Interface (HI08) supports a variety of buses (e.g., industry–standard architecture) and provides glueless connection to a number of industry–standard microcomputers, microprocessors, and DSPs
  - — Two Enhanced Synchronous Serial Interfaces (ESSI)
  - — Serial Communications Interface (SCI) with baud rate generator
  - — Triple timer module

DSP56307EVM—Evaluation Modules (continued)

- — Up to 34 programmable General–Purpose I/O pins (GPIO), depending on which peripherals are enabled
- Reduced Power Dissipation
  - — Very low–power CMOS design
  - — Wait and Stop low–power standby modes
  - — Fully–static logic, operation frequency down to DC
  - — Optimized power management circuitry

Target Applications

The DSP56307 is intended for wireless infrastructure applications with general filtering operations.

DSP56309EVM

2

Features

High Performance DSP56300 Core

- 80– and 100–million instructions per second (MIPS) with an 80– and 100–MHz clock at 3.0–3.6 V
- Object–code compatible with the DSP56000 core
- Highly parallel instruction set
- Data arithmetic logic unit (ALU)
  - — Fully pipelined 24 x 24–bit parallel multiplier–accumulator (MAC)
  - — 56–bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
  - — Conditional ALU instructions
  - — 24–bit or 16–bit arithmetic support under software control
- Program control unit (PCU)
  - — Position independent code (PIC) support
  - — Addressing modes optimized for DSP applications (including immediate offsets)
  - — On–chip instruction cache controller
  - — On–chip memory–expandable hardware stack
  - — Nested hardware DO loops
  - — Fast auto–return interrupts
- Direct memory access (DMA)
  - — Six DMA channels supporting internal and external accesses
  - — One–, two–, and three–dimensional transfers (including circular buffering)
  - — End–of–block–transfer interrupts
  - — Triggering from interrupt lines, all peripherals, and DMA channels
- Phase–locked loop (PLL)
  - — Allows change of low–power divide factor (DF) without loss of lock
  - — Output clock with skew elimination
- Hardware debugging support
  - — On–Chip Emulation (OnCE™) module
  - — Joint Test Action Group (JTAG) test access port (TAP)
  - — Address trace mode reflects internal program RAM accesses at the external port

On-Chip Memory

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size are programmable
- 192 x 24–bit bootstrap ROM

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	20480 × 24-bit	0	7168 × 24-bit	7168 × 24-bit
enabled	disabled	19456 x 24–bit	1024 × 24-bit	7168 × 24-bit	7168 × 24-bit
disabled	enabled	24576 × 24-bit	0	5120 × 24-bit	5120 × 24-bit
enabled	enabled	23552 × 24-bit	1024 × 24-bit	5120 × 24-bit	5120 × 24-bit

Off-Chip Memory Expansion

- External memory expansion port
- Data memory expansion to two 256 K x 24–bit word memory spaces (or up to two 4 M x 24–bit word memory spaces by using the address attribute AA0–AA3 signals)

DSP56309EVM—Evaluation Modules (continued)

- Program memory expansion to one 256 K x 24–bit words memory space (or up to one 4 M x 24–bit word memory space by using the address attribute AA0–AA3 signals)
- Simultaneous glueless interface to four blocks of either SRAM or DRAM through chip select logic
- Supports interleaved, non–interfering access to both types of memory without losing in–page DRAM access, including DMA–driven access

On–Chip Peripherals

- Enhanced DSP56000–like 8–bit parallel host interface (HI08) supports a variety of buses (e.g., industry standard architecture) and provides glueless connection to a number of industry standard microcomputers, microprocessors, and DSPs
- Two enhanced synchronous serial interfaces (ESSI0 and ESSI1), each with one receiver and three transmitters (allows six–channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to 34 programmable general purpose input/output (GPIO) pins, depending on which peripherals are enabled

Reduced Power Dissipation

- Very low–power CMOS design
- Fully–static logic, operation frequency down to 0 Hz (dc)
- Wait and stop low–power standby modes
- Optimized, cycle–by–cycle power management circuitry (instruction–dependent, peripheral–dependent, and mode–dependent)

Target Applications

The DSP56309 is intended for applications benefiting from high–performance and a large amount of on–chip memory, such as multi–channel telecommunications infrastructure.

2

DSP56824EVM

The DSP56824Evaluation Module (EVM) is used to demonstrate the abilities of the DSP56824 and provide a hardware tool allowing the development of applications that use the DSP56824.

The DSP56824EVM is an evaluation module board that includes a DSP56824 part, peripheral expansion connectors, external memory and a voice CODEC. The peripheral expansion connectors are used for signal monitoring and user feature expandability.

The DSP56824EVM is designed for the following purposes:

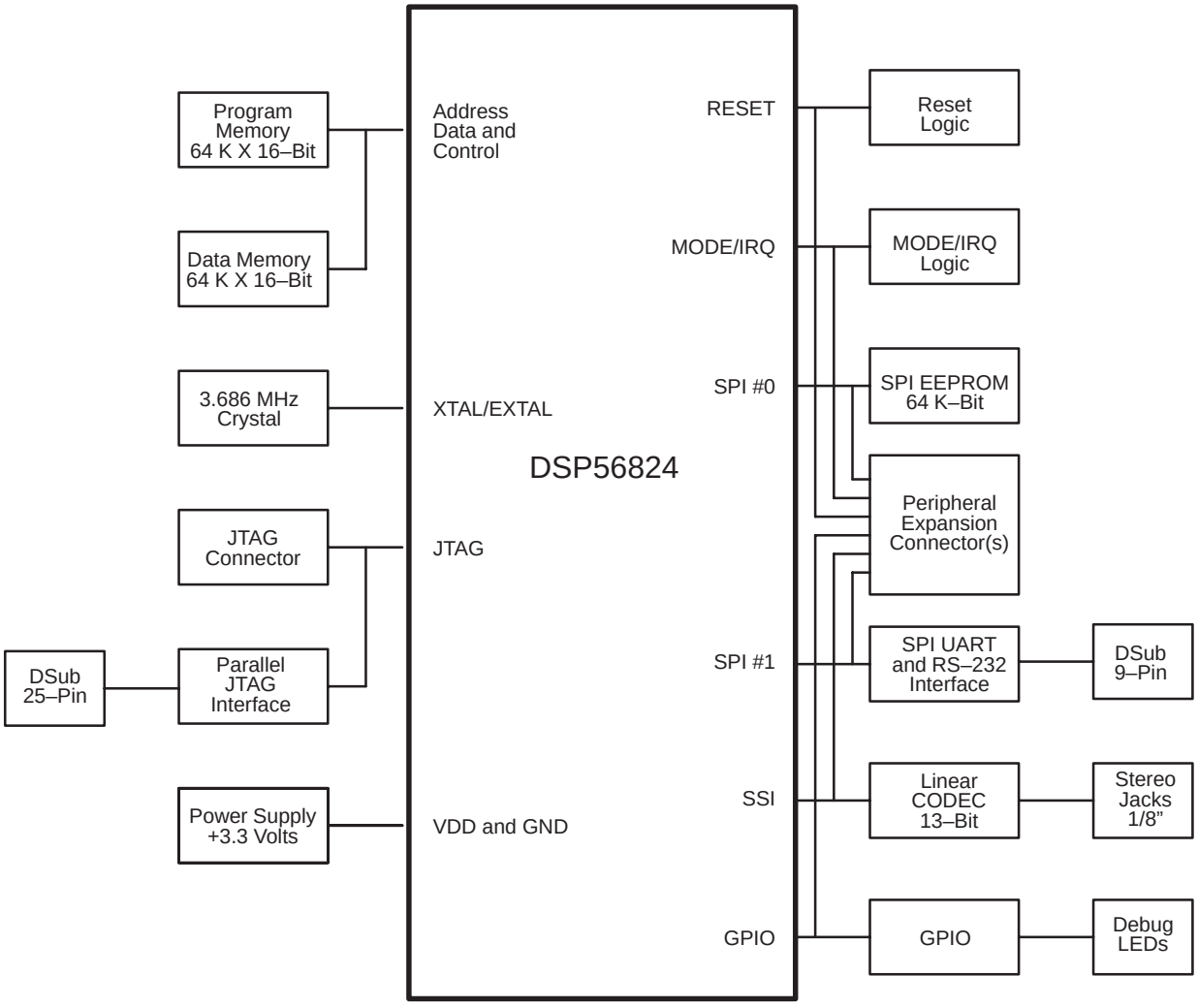
- To allow new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the DSP56824EVM facilitate evaluation of the feature set and the benefits of the family.
- To serve as a platform for real–time software development. The tool suite enables the user to develop and simulate routines then download the software to on–chip or on–board RAM, and then run and debug the software using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify break conditions and to execute user–developed software at full speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- To serve as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on–board peripherals can be disabled, providing the user with the ability to reassign any and all of the DSP's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the DSP chip is available to the user.

DSP56824EVM Architecture

The DSP56824EVM is used to facilitate the evaluation of various features of the DSP56824 part. The DSP56824EVM can be used to develop real–time software and hardware products based on the DSP56824. The DSP56824EVM provides the features necessary for a user to write and debug software, to demonstrate the functionality of that software, and to be able to interface with the customer's application specific device(s). The DSP56824EVM is flexible enough to allow the user to fully exploit the features of the DSP56824. (See Figure 0–1.)

DSP56824EVM—Evaluation Modules (continued)

2



DSP56824EVM Block Diagram

DSP56824 Evaluation Module Board

The DSP56824 Evaluation Module (EVM) demonstrates the capabilities and features of Motorola's DSP56824 Digital Signal Processor (DSP). The DSP56824EVM uses an on–board Parallel JTAG Interface command converter or can be interfaced with a external command converter via the JTAG/OnCE port. The DSP56824EVM is designed as a versatile card that can extend its peripheral expansion connectors for user defined debugging.

The main features of the DSP56824EVM include the following:

- DSP56824BU70 16–bit Digital Signal Processor @ 70 Mhz, and 3.3volts
- 64 K x 16–bit external Program Memory 0 wait state @ 70 MHz
- 64 K x 16–bit external Data Memory 0 wait state @ 70 MHz
- 64 K–bit SPI EEPROM memory for program and data storage
- Expansion connectors to allow the addition of external peripherals
- JTAG interface connector for external Command Converter Interface
- On–board Parallel Command Converter Interface, with a connector for PC printer port connections
- 13–bit linear Codec for voice applications with line–in and line–out jack connectors

DSP56824EVM—Evaluation Modules (continued)

- Low cost crystal oscillator for DSP frequency input
- SPI UART with RS–232 interface for easy connection to host processor
- On–board power regulation with external 7–12 V AC/DC supplied power input
- Three on–board real–time user debugging LEDs
- Two on–board switches to externally interrupt the DSP56824
- On–board power on reset with reset switch

Four Nylon Standoffs and Four Nylon Screws

Their function is to raise the board up to facilitate its use.

Power supply

12 V DC 500mA with 2.1 mm receptacle (inside positive) power connector.

Parallel Port Extender Cable DB25 male to DB25 female

Interface connection between the host and the evaluation board

Suite56 DSP56824EVM CD–ROM

Installation Software

This software shall allow the user to install the Suite56 SW Development Tools for the 800 Family, the technical documentation listed in paragraph 3.2.3, and the DSP56824EVM Example software. For detail information on the installation requirements, refer to paragraph 3.2.5

Software Components

DSP56800 Software Development Tools – shall be physically located in the CD. A link to the WWW shall be provided from installation to ensure the latest version of the software can be obtained. The tool set shall consist of:

- Debugger (able to support all Command Converters.)
- Software Simulator
- Assembler
- Linker/Librarian
- Various utilities

The DSP56824 is a general purpose DSP that combines processing power with configuration flexibility, making it an excellent cost–effective solution for signal processing and control functions. Because of its low cost, configuration flexibility, and compact program code, it is well–suited for cost–sensitive applications, such as digital wireless messaging, servo and motor control, digital answering machines, feature phones, modems and digital cameras.

The DSP56824 EVM kit is a low cost evaluation system (target cost to be $150.00) that is designed to demonstrate the capabilities and features of Motorola's newest derivative of the DSP56800 family of Digital Signal Processors (DSPs).

The main goal of this kit is to provide in one single place all of the necessary elements, such as hardware, software (assembler, linker, simulator, hardware debugger), accessories, and technical documentation

DSP56824EVM Example Software shall allow the user to become familiar with the features on the DSP56824EVM, programming the DSP56824EVM in C and Assembly language, using the Motorola ADS56800 Debug software and the Metrowerks CodeWarrior C Compiler.

The following example software is included in this product:

- Interrupt and LED software: when a hardware interrupt is enabled the debug LEDs shall turn on and off.
- Timer and LED software: the timer shall control how fast the LEDS blink.
- EEPROM software: memory shall transfer from SRAM to EEPROM.
- RS–232 Interface software: data shall be transferred from the DSP56824EVM to the computer via serial port.
- Audio Codec software: An analog signal shall be piped in to codec, codec to dsp, dsp to codec, codec to line out.

Technical Documentation

- Software Development Tools User's Manuals: The set of user's manual consists of the ADS Debugger, the Software Simulator, the Compiler, and the Assembly Tools User's manuals (Assembler, Linker, Librarian User's Manuals).
- DSP56800 Family User's Manual – Shall provide the user a detailed description of the DSP56800 family architecture, core, and its instruction set.
- DSP56824 User's Manual – Shall provide a detailed description of memory, peripherals and interfaces DSP56824
- DSP56824 Technical Data Sheet – Shall provide a detailed description of the pin and package descriptions, electrical and timing specifications

DSP56824EVM—Evaluation Modules (continued)

- Suite56 Parallel Port, Ethernet, and PCI Command Converter User's Manuals: Shall provide a detailed description of usability and set up. The Set shall include the Suite56 Parallel, Ethernet, PCI, and Universal Command Converter User's Manuals.
- DSP56824EVM Hardware Reference Manual: Shall provide a detailed description of memory, peripherals and interfaces DSP56824 board
- ADS User's Manual: Shall provide information about the four major components that make up a ADS(Host Card, Universal Command Converter, Software Development Tools (Control, Development, and Debugger SW)
- MC145483 13–Bit Linear Codec Data Sheet – Shall provide information about the 13–bit linear codec supplied on the EVM.

2

DSP56L811EVM

The DSP56L811 Evaluation Module (DSP56L811EVM) is designed as a low-cost platform for developing real-time software and hardware products to support a new generation of applications in digital messaging, two-way radio, speech processing, and consumer electronics. The user can download software to on-chip or on-board RAM, then run and debug it. The 16-bit precision of the DSP56L811 Digital Signal Processor (DSP) combined with the on-board 64 K x 16-bit external SRAM and Motorola's MC145483 13-bit linear voice audio codec makes the DSP56L811EVM ideal for developing and implementing many messaging and audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56L811 processor. The user can connect hardware, such as external memories and other devices, A/D or D/A converters, keypads, displays, and so forth via the expansion connectors.

Hardware Features

- 16-bit DSP56L811 Digital Signal Processor
- DSP56800 core
  - — Efficient 16-bit fixed point DSP56800 family DSP engine
  - — Up to 20 Million Instructions Per Second (MIPS) at 40 MHz
  - — Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
  - — Two 36-bit accumulators including extension bits
  - — 16-bit bidirectional barrel shifter
  - — Parallel instruction set with unique DSP addressing modes
  - — Hardware DO and REP loops
  - — DO loops nestable in software
  - — Address buses:
    - — One 16-bit internal memory address bus (XAB1)
    - — One 16-bit internal memory address bus (XAB2)
    - — One 19-bit internal Program Address Bus (PAB)
    - — One 16-bit External Address Bus (EAB)
  - — Data buses:
    - — One 16-bit bidirectional internal memory data bus (CGDB)
    - — One 16-bit unidirectional internal memory data bus (XDB2)
    - — One 16-bit bidirectional dedicated Peripheral Data Bus (PGDB)
    - — One 16-bit bidirectional internal Program Data Bus (PDB)
    - — One 16-bit bidirectional External Data Bus (EDB)
    - — Instruction set supports both DSP and controller functions
    - — Controller style addressing modes and instructions for compact code
    - — Efficient C Compiler and local variable support
    - — Software subroutine and interrupt stack with unlimited depth
    - — On-Chip Memories
    - — On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
    - — 1 K x 16 Program RAM
    - — 64 x 16 bootstrap ROM
    - — 2 K x 16 X data RAM
    - — Programs can run out of X data RAM
- Peripheral and Support Circuits
  - — External Memory Interface (EMI)

DSP56L811EVM—Evaluation Modules (continued)

- — Sixteen dedicated General Purpose Input/Output (GPIO) pins (eight pins programmable as interrupts)
- — Serial Peripheral Interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
- — Supports LCD drivers, A/D subsystems, and MCU systems
- — Supports inter-processor communications in a multiple master system
- — Demand-driven master or slave devices with high data rates
- — Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
- — Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
- — Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
- — Network mode using frame sync and up to 32 time slots
- — 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
- — Three programmable 16-bit timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
- — Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers
- — Two external interrupt/mode control pins
- — One external reset pin for hardware reset
- — JTAG/On-Chip Emulation (OnCE) 5-pin port for unobtrusive, processor speed-independent debugging
- — Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock

- Energy Efficient Design
  - — Power-saving Wait and multiple Stop modes available
  - — Fully static, HCMOS design for 40 MHz to DC operating frequencies
  - — 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
  - — 2.7 V–3.6 V power supply
- 32 K x 16-bit Fast Static RAM for expansion program memory
- 32 K x 16-bit Fast Static RAM for expansion data memory
- 13-bit linear audio codec
- Command Converter
  - — Motorola MC68HC705C4 for high-speed JTAG/OnCE command conversion
  - — JTAG connector for use with the Application Development System (ADS) Command Converter card
- Connectors
  - — RS-232 serial interface with local microcontroller support for JTAG/OnCE port
  - — Two 70-pin connectors that allow access to all DSP56L811 pins
  - — Software Features
- Motorola's DSP56xxx Cross Assembler
  - — Produces DSP56L811 binary code from source code using labels, sections, and macro definitions incorporating the DSP's complete instruction set, all addressing modes, and all memory spaces
  - — Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - — Creates reports for cross-references, instruction cycle count, and memory usage
  - — Provides extensive error checking and reporting
- Domain Technologies debug software with Windows-based user interface
  - — Symbolic debugging
  - — Windows for data, code, DSP registers, commands, peripherals, etc.
  - — Data and registers displayed in fractional, decimal, or hexadecimal format
  - — Graphical display of memory segments
  - — Up to eight simultaneous software breakpoints
  - — Built-in-line Assembler and disassembler

MC68175FDB FLEX™ DEVELOPMENT BOARD

The MC68175FDB FLEX Development Board is designed as a flexible platform for developing FLEX paging devices using the MC68175 FLEX™ chip decoder in conjunction with the Motorola FLEX™ 2-bit Analog-to-Digital (A/D) converter (or equivalent).

This two-chip solution simplifies the implementation of a FLEX™ paging device by accepting four-level audio signals from a wide range of readily-available paging receiver devices, and communicating via the Serial Peripheral Interface (SPI) port with a wide range of standard microcontrollers and microprocessors.

2

The Motorola FLEX™ 2-bit A/D converter accepts the four-level audio signal from the RF front end, and converts it to a 2-bit encoded symbol format. The symbols are passed directly to the MC68175 FLEX chip decoder, which handles the FLEX protocol, assembles the message packets, and communicates with the host microcontroller or microprocessor via the SPI connector.

MC68175FDB Features

MC68175 FLEX™ Chip Decoder IC

- FLEX paging protocol signal processor
  - — Sixteen programmable user address words
  - — Sixteen fixed temporary addresses
  - — 1600-, 3200-, and 6400-bits-per-second decoding
  - — Any-phase or single-phase decoding
  - — Uses standard Serial Peripheral Interface (SPI) in Slave mode
  - — Interrupt-driven communication allows low-current Stop mode operation of host processor
  - — Highly programmable receiver control
  - — Real-time clock time base and over-the-air update support
  - — FLEX software fragmentation and group messaging support
  - — Compatible with synthesized receivers
  - — Low Battery Indication (external detector)
  - — 1.8 to 3.3 V low power operation
  - — 32-pin Thin Quad Flat Pack (TQFP) package
- Motorola FLEX™ 2-bit A/D Converter
  - — 8-bit DAC peak and valley detectors
  - — Pin-selectable 1 kHz or 2 kHz 2-pole Butterworth low pass filter
  - — 2-bit A/D Converter
  - — 600 mVp-p input voltage range
  - — 30°C to + 85°C operating temperature range
  - — 100 mA typical operating current at VADD = 2.7 V
  - — Three modes of operation
    - — Fast Track mode-fast approximation to signal peak and valley in one cycle
    - — Slow Track mode-precise peak and valley acquisition in five more cycles
    - — Hold Acquisition
  - — Standby mode for low power consumption
  - — 2 V and 3 V operation, ± 10%, for both VDDD and AVADD
  - — 14-pin SOIC package
- FLEX Development Board Configuration Options
  - — BNC Connector for audio (encoder) input
  - — Receiver Interface Connector
  - — 38.4 kHz clock output for RF module
  - — SPI connector for host communications
  - — Battery Low emulation switch
  - — 2 V and 3 V operation with independent analog and digital supply circuitry
  - — Microprocessor/microcontroller interface buffered for 3 V or 5 V emulation support

Software

The Motorola FLEXstack™ software package is available for free download from the Motorola World-wide Web site at http://www.mot.com/FLEXstack. This package is available as C source, and is written in ANSI C to compile easily for a wide variety of host processors.

DSP Development Software

The Simulator/Macro-Assembler/Linker/Librarian software package is a development system support tool. The Simulator program imitates the operation of the DSP on a clock-cycle by clock-cycle basis and gives an accurate measurement of code execution time. All on-chip peripheral operations, memory and register updates, and exception processing activities may be functionally simulated.

User Friendly

- GUI works native to three operation systems:
  - — SunOS
  - — Windows 3.1
  - — HPUX
- Multiple overlapping windows for the display of debugging information, command input registers, memory, and programs

DSP Development Software (continued)

- Pull down menus for ease of use:
  - — Dialog boxes for selecting options of complex commands
  - — Tool bar will provide fast access to commonly performed actions
  - — Keyboard accelerators will be defined for commonly executed commands
  - — Help viewer will be provided for viewing pre-defined help on selected topics

Debugging Capabilities for C Language and Assembly

- Assembly language symbolic or C Language source code debugging capabilities

The full-featured Macro Cross Assembler translates one or more source files containing instruction mnemonics, operands, and assembler directives into a Common Object File Format (COFF) file, which is directly loadable by the Simulator. It supports the full instruction set, memory spaces, and parallel transfer fields of the DSP.

The Linker relocates and links relocatable COFF object modules from the Assembler to create an absolute load file, which can be loaded directly into the Simulator. The Librarian utility will merge separate, relocatable object modules into a single file, allowing frequently used modules to be grouped for convenient linking and storing.

The Assembler and Linker now provide support for assembly language source-level debugging via the Simulator. Global symbols, symbols local to sections, and even underscore labels may be referenced with all scoping constructs intact. In addition, the Assembler generates information about included files and macros. The Assembler and Linker also support numbered counters ranging from 0 to 65535.

C Compiler Packages

A full ANSI C compliant Compiler, based on GNU technology, provides higher efficiency and implements more than twenty major optimization techniques. It has improved in-line assembly capability and an ANSI C preprocessor. The package includes the C Compiler, a new COFF Assembler, Linker, complete ANSI C Libraries, and a new C source level debugger, as well as expanded user's reference manual. The software package is available for various host computers listed.

Overview

The Motorola Application Development System (ADS) is a tool used to design and test complex software applications and hardware products using a specific Motorola DSP chip. The related Application Development Modules (ADMs) contain the DSP chip and related hardware used for bench development and test. Detailed information about the content and use of the ADS is provided in the ADS User's Manual (order #DSPADSUM/AD). This manual provides specific information about the DSP56301 Application Development Module (DSP56301ADM). This section provides a summary description of the DSP56301ADM, additional requirements, and quick installation information. Detailed information about the DSP56301ADM design and operation is provided in the remaining sections of this manual.

Equipment

The following section gives a brief summary of the equipment required to use the DSP56301 Application Development Module (DSP56301ADM), some of which will be supplied with the module, and some of which must be supplied by the user.

What You Get with the DSP56301ADM

The following materials are provided with the DSP56301ADM:

- DSP56301 Application Development Module board
- DSP56301ADM Product Information
- DSP56301ADM User's Manual
- Motorola Digital Signal Processor Registration Form

DSP56301ADM Description and Features

The DSP56301ADM is designed as a versatile card that can be used not only as a stand–alone board, but can also be plugged into other cards. Four 50–pin connectors allow access to all the DSP signals, including V_{DD} and V_{SS}. This plug–in feature permits special configurations, including, among others, connection to a customized wire–wrapped or other application board to permit enhanced functionality. An overview description of the DSP56301ADM is also provided in the DSP56301ADM Product Information document (order number DSP56301ADMP/D) included with this kit.

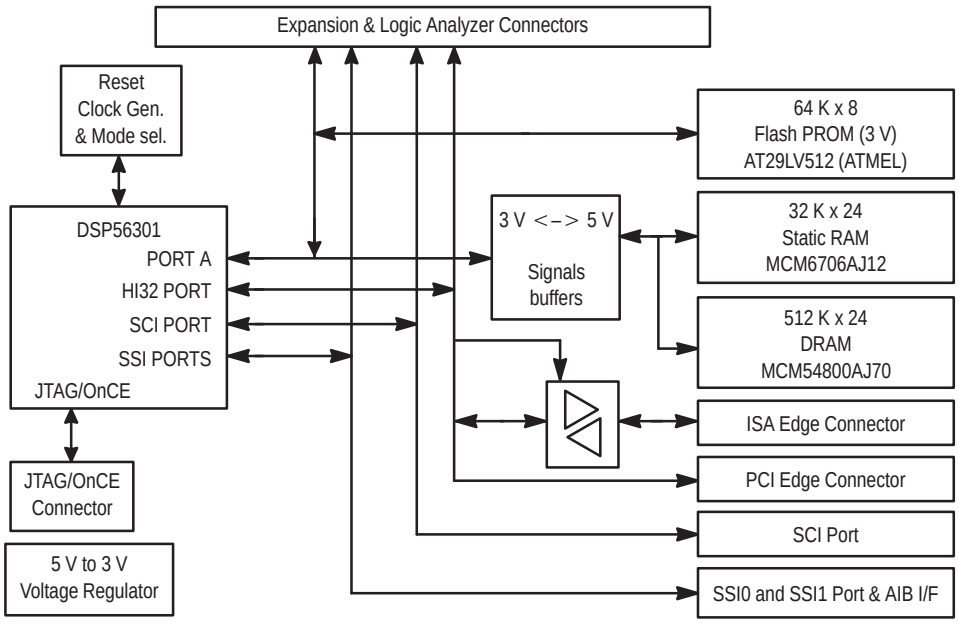
The main features of the DSP56301ADM include the following:

- DSP56301 24–bit Digital Signal Processor
- 32 K Word FSRAM with 12 ns access (5 V)
- 64 K Byte Flash PROM Memory, 200 ns access on–board (3 V) programmable
- 512 K Word DRAM, 70 ns access
- ISA bus compatible edge–connector (slave only operation)

DSP Development Software (continued)

- PCI bus compatible edge–connector (master and slave operation)
- Table mounted (stand–alone) operation, or computer plug–in card operation
- Integrated Expansion and Logic–Analyzer Connectors
- Dedicated SSI and SCI port connectors
- JTAG/OnCE port connector for easy hookup to Motorola command converter
- 5 V operation, with on board 3.3 V voltage regulation
- Power terminals and 8–pin clock socket for stand–alone operation

Note: Call your local Motorola sales office or distributor for additional information about the Motorola Application Development System (ADS) kit. The ADS kit includes two additional boards: a host interface card and an external universal command converter. The host interface card plugs in the host bus (on a PC–compatible, HP7xx workstation, or Sun/Sun–compatible system) inside the computer chassis. The external universal command converter card connects to the host card via a 37–pin ribbon cable. The command converter card connects to the JTAG connector on the DSP56301ADM via another short 14–pin ribbon cable. The ADS is only compatible with Motorola software tools.



DSP56301ADM Functional Block Diagram

Imaging Systems Division

In Brief . . .

The M680X0 Family

The M68000 Family continues to be the industry standard in computing and embedded control applications. Its' target markets include the low to mid–range computing industry, the laptop and handheld computing industry, telecommunication, office automation, network controllers, and consumer products.

The products in this family provide industry–standard architecture in an extremely cost–effective package/solution. Such inexpensive solutions are available at more than 100 MIPS with an excellent migration path.

The ColdFire Family

The ColdFire microprocessor architecture provides new levels of price and performance to the emerging cost–sensitive, high–volume, embedded markets, especially in the area of consumer products. Based on the concept of a variable–length RISC technology, ColdFire combines the architectural simplicity of conventional 32–bit RISC with a memory–saving, variable length instruction set. In defining the ColdFire architecture for embedded processing applications, Motorola has incorporated a RISC–based processor design for peak performance and a simplified version of the variable–length instruction set found in the M68000 Family for maximum code density. The result is a family of 32–bit microprocessors ideally suited to those embedded applications requiring high performance in a small core size.

68K Heritage Makes Moving to RISC Easy

The ColdFire instruction set is a subset of Motorola's 68K microprocessor family, so you can build on existing product designs, leverage your engineer's programming experience, and get your new product to market faster, with a smaller investment. It also means tool vendors can easily adapt their products, giving you access to familiar tools. An automated 68K–to–ColdFire processor assembly converter is available from MicroAPL Ltd.

2

MOTOROLA

Imaging Systems Division

2

The ColdFire Product Line

MCF5102

MCF5102, the first implementation of the ColdFire processor family, takes full advantage of the established 68K software base. Compatibility with existing MC68EC040 development tools gives developers access to a wide range of mature tool support.

MCF5202

The MCF5202 combines a ColdFire core with an integrated 2 KByte unified cache. A 32–bit multiplexed bus with dynamic bus sizing allows access to 8–, 16–, or 32–bit memory and peripherals in the same system. The debug module provides serial control and visibility of the processor and entire memory system, so developers can greatly reduce the product development cycle. Performance is 27 MIPS at 33 MHz.

MCF5204

The MCF5204 integrated processor integrates a 512–Byte instruction cache and 512–Byte SRAM with a UART, two timers and debug module. The MCF5204 offers a glueless interface to 8– and 16–bit RAM, ROM and peripherals. Performance is 13.5 MIPS at 33 MHz.

MCF5206

The MCF5206 highly integrated processor includes DRAM controller, chip selects, an interrupt controller, 2 timers, dual UARTs, parallel port and MBus interface. Its 512–Byte instruction cache and 512–Byte instruction and data SRAM provide a performance level of 17 MIPS at 33 MHz.

MCF5206e

The MCF5206e is a pin–compatible, 3.3V version of the MCF5206 with DMA and a MAC unit. On–chip memory sizes are increased to 4K I–cache and 8K SRAM, making for impressive performance of 50 MIPS at 54 MHz.

MCF5307

The MCF5307 is the first implementation of the Version 3 ColdFire core. Integration includes DMA, DRAM Controller, 2 UARTs, 2 Timers, 8 Chip Selects, 8 I/O, I2C–compatible bus (Mbus), SIM, Debug module. Memory sizes have been increased to 8K unified I/D cache and 4K SRAM. Performance is 70 MIPS at 45MHz (90 MHz clock–doubled internally).

Version 3 Core: While one of the goals of the original ColdFire microarchitecture was to minimize overall size, the driving factor in the Version 3 design was to better balance the logic delays associated with each pipeline stage to allow the operating frequency to be raised significantly. The Version 3 Instruction Fetch Pipeline is a 4–stage design with an optional instruction buffer stage, while the Operand Execution Pipeline retains its 2–stage structure.

MC68000 & Derivatives
(Including EC, SEC, and HC)

NOTE: Motorola no longer makes the MC68000, only derivatives.

- 32–Bit Data and Address Registers
- 16M Direct Addressing Range
- Program Counter
- 56 Powerful Instructions
- Operations on Five Main Data Types
- Memory–Mapped Input/Output
- 14 Addressing Modes

MC68020 & Derivatives
(Including the EC020)

The MC68020 is the first full 32–bit implementation of the M68000 family of microprocessors from Motorola. Using VLSI technology, the MC68020 is implemented with 32–bit registers and data paths, 32–bit addresses, a rich instruction set, and versatile addressing modes.

MC68030 & Derivatives
(Including the EC030)

The MC68030 is a second–generation full 32–bit enhanced microprocessor from Motorola. The MC68030 is a member of the M68000 Family of devices that combines a central processing unit (CPU) core, a data cache, an instruction cache, an enhanced bus controller, and a memory management unit (MMU) in a single VLSI device. The processor is designed to operate at clock speeds beyond 20 MHz. The MC68030 is implemented with 32–bit registers and data paths, 32–bit addresses, a rich instruction set, and versatile addressing modes.

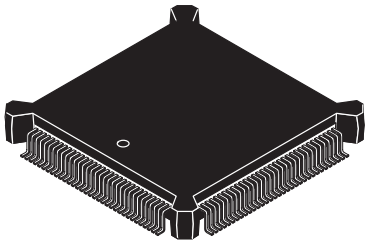
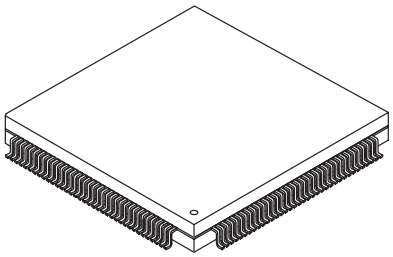
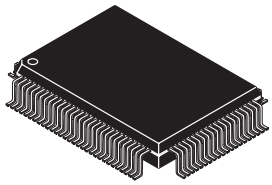
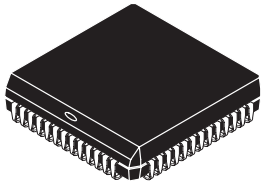
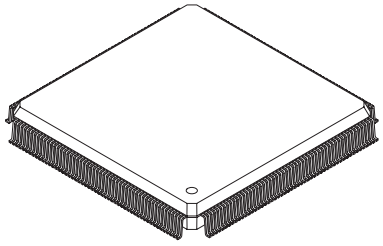
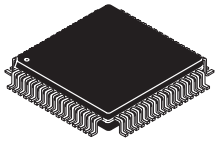
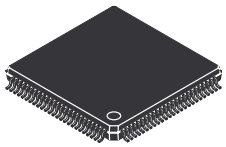
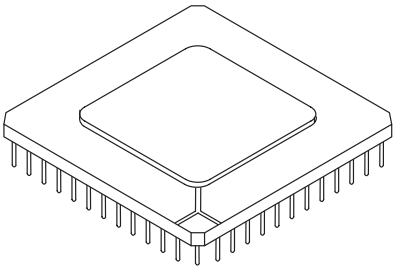
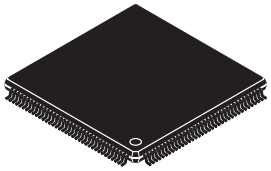
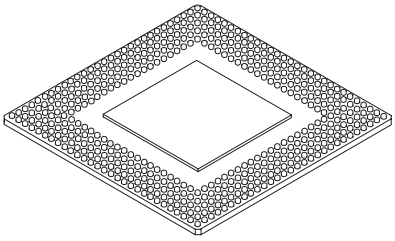
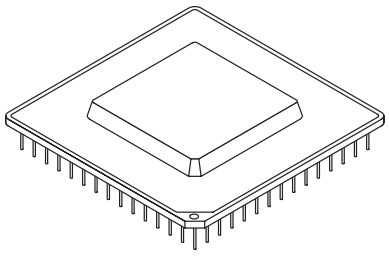
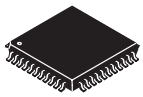
MC68040 & Derivatives
(Including EC, LC, and V)

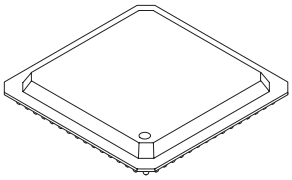
The MC68040, MC68040V, MC68LC040, MC68EC040, and MC68EC040V (collectively called M68040) are Motorola's third generation of M68000–compatible, high–performance, 32–bit microprocessors. All five devices are virtual memory microprocessors employing multiple concurrent execution units and a highly integrated architecture that provides very high performance in a monolithic HCMOS device. They integrate an MC68030–compatible integer unit (IU) and two independent caches. The MC68040, MC68040V, and MC68LC040 contain dual, independent, demand–paged memory management units (MMUs) for instruction and data stream accesses and independent, 4–Kbyte instruction cache. The MC68040 contains an MC68881/MC68882–compatible floating–point unit (FPU). The use of multiple independent execution pipelines, multiple internal buses, and a full internal Harvard architecture, including separate physical caches for both instruction and data accesses, achieves a high degree of instruction execution parallelism on all three processors. The on–chip bus snoop logic, which directly supports cache coherency in multimaster applications, enhances cache functionality.

MC68060 & Derivatives
(Including the LC060 and EC060)

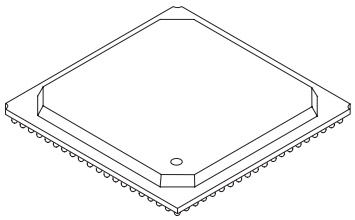
The superscalar MC68060 represents a new line of Motorola microprocessor products. The first generation of the M68060 product line consists of the MC68060, MC68LC060, and MC68EC060. All three microprocessors offer superscalar integer performance of over 100 MIPS at 66 MHz. The MC68060 comes fully equipped with both a floating–point unit (FPU) and a memory management unit (MMU) for high–performance embedded control and desk–top applications. For cost–sensitive embedded control and desktop applications where an MMU is required, but the additional cost of a FPU is not justified, the MC68LC060 offers high–performance at a lost cost. Specifically designed for low–cost embedded control applications, the MC68EC060 eliminates both the FPU and MMU, permitting designers to leverage MC68060 performance while avoiding the cost of unnecessary features. Throughout this product brief, all references to the MC68060 also refer to the MC68LC060 and the MC68EC060, unless otherwise noted.

68K/ColdFire Package Diagrams

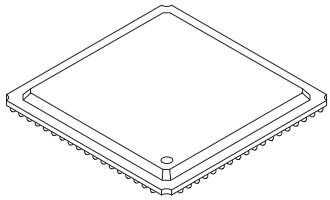
		
FC = Plastic Quad (Gull Wing)	FE = Ceramic Quad (Gull Wing)	FG = Plastic Quad Flat Pack (PQFP)
		
FN = Plastic Quad Pack (PLCC)	FT= Plastic Flat Pack (28 x 28 mm)	FU = Plastic Quad Flat Pack (14 x 14 mm)
		
PU = LQFP (14 x 14 mm) Plastic	RC = Pin Grid Array, Gold Lead Finish	PV = LQFP (20 x 20 mm) Plastic
		
ZU = Tape Ball Grid Array	RP = Plastic Pin Grid Array	PB = LQFP (10 x 10 mm) Plastic



ZT = 256 BGA



ZP = 272 BGA



ZP = 357 BGA

STAND–ALONE CPUs

Device No.	Package	Speeds	Rev	Device Name	Temp** (–40 to +85°C)	SOQ	MPQ	POQ	BRICK	Description
680X0										
MC68EC000	68–Lead FN 64–Lead FU	8, 10, 12, 16, 20 8, 10, 12, 16, 20		8–/16–/32–Bit HCMOS Embedded MPU		0 0	18 84	1008 252	 420	Low–cost embedded control MPU with 8–/16–bit selectable data bus.
						For FN, FU sample order—SPAKEC000FNXX, SPAKEC000FUXX				
MC68HC000	68–Lead FN, 68–Lead FC*, 68–Lead R*, RC*	8, 10, 12, 16, 20 8, 10, 12, 16 8, 10, 12, 16		HCMOS 16–/32–Bit MPU	CFN8, 10, 12, 16 CFC8, 10, 16 CRC8, 10, 12, 16	5 0 0 0	5 18 78 21	160 1008 780 210		Completely pin and timing MC68000–compatibility with a tenth of the power dissipation.
						For FC, FN, P, RC sample order—SPAKHC000FCXX, SPAKHC000FNXX, SPAKHC000PXX, SPAKH000RCXX*				
MC68HC001	68–Lead FN, 68–Lead RC	8, 10, 12, 16 8, 10, 12, 16		Statically Switchable 8–/16–Bit Data Bus	CFN8, 10 CRC8	0 0	18 21	1008 210		Functionally compatible with MC68000 and MC68008.
						For FN, RC sample order—SPAKHC001FNXX, SPAKHC001RCXX*				
MC68SEC000	64–Lead FU, 68–Lead PB	10, 16, 20 10, 16, 20		8–/16–/32–Bit Static HCMOS Embedded MPU	CFN8, 10 CRC8	0 1	84 1	252 1		Static version of the MC68EC000.
						For FU sample order—SPAKSEC000FUXX				
MC68020	114–Lead RC 132–Lead FE* 114–Lead RP 132–Lead FC	12*, 16, 20, 25, 33 16, 20, 25, 33 16, 20, 25 16, 20, 25, 33	E E E E	32–Bit MPU	CRC16, 20, 25 CRP16 CFC16, 25	1 0 1 0	1 36 1 36	14 180 13 144	 180	Complete 32–bit MPU. 5–Gbyte linear address space. Coprocessor interface. Instruction cache. Dynamic bus sizing. Excellent MPU for graphics control. On–chip cache speeds drawing algorithms. Bit field support for pixel manipulation.
						For FC, FE sample order—SPAK020FCXXE, SPAK020FEXXE				
MC68EC020	100–Lead FG 100–Lead RP	16, 25 16, 25		32–Bit Embedded MPU	CFG16 CRP25	0 1	66 1	264 13	330	32–bit data bus MPU with 24–bit address bus. Instruction cache. Dynamic bus sizing. Coprocessor interface. Low–cost packaging.
						For FG sample order—SPAKEC020FGXX				
MC68030	128–Lead RC 124–Lead RP 132–Lead FE	16, 20, 25, 33, 40, 50 16, 20, 25, 33 16, 20, 25, 33	C C C	Enhanced 32–Bit MPU	CRC25, 33 CRP16, 20, 25, 33	1 1 0	1 1 36	14 14 180		Complete 32–bit MPU with on–chip instruction and data caches, internal parallel buses, enhanced bus controller, and on–chip MMU.
						For FE sample order—SPAK030FEXXC				
MC68EC030	124–Lead RP 132–Lead FE 144–Lead PV	25, 40 25, 40 25	C C C	Embedded MPU	CRP25	1 1 0	1 36 60	14 180 240		32–bit MPU for embedded applications. On–chip instruction and data cache provide high–speed access for control routines and data. Utilizes low–cost DRAM bus interface.
						For FE, PV sample order—SPAKEC030FEXXC, SPAKEC030PVXXC				
MC68040	179–Lead RC 184–Lead FE	25, 33, 40 25, 33, 40		32–Bit MPU MMU FPU		1 0	1 24	10 96		Complete 32–bit MPU with on–chip instruction/data caches (4k bytes each). On–chip MMU. Full IEEE floating point, multiprocessing support with full M68000 Family compatibility.
						For FE sample order—SPAK040FEXX				

2

STAND–ALONE CPUs (continued)

Device No.	Package	Speeds	Rev	Device Name	Temp** (–40 to +85°C)	SOQ	MPQ	POQ	BRICK	Description
680X0										
MC68EC040	179–Lead RC 184–Lead FE	20, 25, 33, 40 20, 25, 33, 40		Embedded 32–Bit High Performance Processor		1 0	1 24	10 96	120	High–performance 32–bit MPU with on–chip instruction and data cache provides high–speed access for control routines and data. Utilizes low–cost DRAM bus interface.
						For FE sample order—SPAKEC040FEXX				
MC68LC040	179–Lead RC 184–Lead FE	20, 25, 33, 40 20, 25, 33, 40		High Performance 32–Bit Processor		1 0	1 24	10 96	120	68040–compatible integer unit and MMU. Ideal solution for cost–sensitive computer or sophisticated embedded applications.
						For FE sample order—SPAKLC040FEXX				
MC68040V	179–Lead RC 184–Lead FE	25, 33, 40 @ 3.3 V 25, 33 @ 3.3 V		32–Bit MPU MMU, FPU, Low– Voltage		1 0	1 24	0 96		Low–voltage complete 32–bit MPU with on–chip instruction/ data caches (4k bytes each). On–chip MMU. Full IEEE floating point, multiprocessing support.
						For FE sample order—SPAKEC040VFEXX, SPAKEC040VRCXX				
MC68060	206–Lead RC	50	A	Superscalar 32–Bit Processor		0	1	10		RISC hybrid superscalar MPU with full M68000 Family compatibility. Includes dual integer units, on–chip instruction/ data caches (8K bytes each), on–chip MMU, and full IEEE compliant FPU.
MC68EC060	206–Lead RC 304–Lead ZU	50 50, 66	E	Superscalar 32–Bit Processor		0 1	1 27	10 27		RISC hybrid superscalar MPU with full M68000 Family compatibility. Includes dual integer units, on–chip instruction/ data caches (8K bytes each). Ideal for high–performance embedded control applications.
MC68LC060	206–Lead RC 304–Lead ZU	50 50, 66	E	Superscalar 32–Bit Processor		0 1	1 27	10 27		RISC hybrid superscalar MPU with full M68000 Family compatibility. Includes dual integer units, on–chip instruction/ data caches (8K bytes each) and on–chip MMU.
MC68882	68–Lead RC 68–Lead FN	16, 20, 25, 33, 40, 50 16, 20, 25, 33, 40	A A	Enhanced Floating–Point Coprocessor (EFPCP)	CRC16, 20, 25, 33 CFN16, 20, 25, 33	1 1	1 1	21 18		Pin–to–pin timing and software compatibility with MC68881. Dual ported registers and increased pipelining allows 2–4 x performance of MC68881.

2

STAND–ALONE CPUs (continued)

Device No.	Package	Speeds	Rev	Device Name	Temp** (–40 to +85°C)	SOQ	MPQ	POQ	BRICK	Description
COLDFIRE										
MCF5102	144–Lead PV	16, 20, 25, 33	A	Embedded VL–RISC MPU		0	60	240		ColdFire variable–length RISC microprocessor designed for cost–sensitive embedded control applications. In addition to executing ColdFire code, this first family member is designed with additional capabilities that allow it to execute existing M680x0 code. Processor includes on–chip instruction/data caches (2K/1K respectively).
						For PV sample order—SPAK5102PVXXA				
MCF5202	100–Lead PU	16, 25	A	Embedded VL–RISC MPU		0	84	420		ColdFire variable–length RISC microprocessor designed for cost–sensitive embedded control applications. This member features a 2K unified cache.
						For PU sample order—SPAK5202PUXX				
MCF5204	100–Lead PU	16, 25, 33	A	Embedded VL–RISC MPU	CPU25A	0	84	84		ColdFire variable–length RISC microprocessor designed for cost–sensitive embedded control applications.
						For PU sample order—SPAK5203PUXX				
MCF5206	160–Lead FT	16, 25, 33	A	Embedded VL–RISC MPU	CFT16 CFT25	0	24	120		ColdFire variable–length RISC microprocessor designed for cost–sensitive embedded control applications.
						For FT sample order—SPAK5204FTXX				
XCF5307	208–Lead FT	66, 90		Embedded VL–RISC MPU		0	24	120		ColdFire Version 3 microprocessor with Multiply–Accumulate (MAC) unit, DRAM Controller, DMA Controller.
						For FT sample order—SPAK5307FTXX				

2

GENERAL–PURPOSE INTEGRATED PROCESSORS

Device No.	Package	Speeds	Rev	Device Name	Temp** (–40 to +85°C)	SOQ	MPQ	POQ	BRICK	Description
MC68306	132–Lead FC 144–Lead PV	16, 20 16, 20	A	Integrated EC000 Processor	CFC16	0 0	36 60	144 600	300	68000 CPU, 68681 DUART, DRAM control all in one chip.
						For FC, PV sample order—SPAK306FCXXA, SPAK306PVXXA				
XC68307* XC68307V*	100–Lead FG 100–Lead PU 100–Lead FG 100–Lead PU	16 16 8, 16 @ 3.3 V 8, 16 @ 3.3 V		Integrated Multiple Bus Processor	CFG16	0 0 0 0	66 84 66 84	264 420 264 420		Static EC000 Core Processor, UART, M–Bus Dual Timers, 8051 interface, dynamic 68000 bus.
						For FG, PU sample order—SPAK307FGXX, SPAK307FGXXV, SPAK307PUXX, SPAK307PUXXV				
MC68322	160–Lead FT	16, 20		Bandit–Integrated Printer Processor		0	24	96		Static EC000 Core Processor, RISC Graphics Processor, Print Engine Video Controller, DRAM Controller, and 1284 Parallel Port.
						For FT sample order—SPAK322FTXX				
MC68330* MC68330V*	144–Lead PV 144–Lead PV	16, 25 16 @ 3.3V	A A	Integrated CPU32 Processor	CPV16, CPV25	0 0	60 60	240 240		CPU32 core processor with integrated glue logic, clock chip select, and wait state. Power of 32–bit processor with inexpensive 16–bit data bus.
						For PV sample order—SPAK330PVXXA, SPAK330PVXXVA				
MC68340 MC68340V	144–Lead FE* 144–Lead PV 144–Lead FT 144–Lead FE* 144–Lead PV	16, 25 16, 25 16, 25 16 @ 3.3V 16 @ 3.3V	E E E E E	Integrated Processor with DMA	CFE16, CFE25 CPV16, CPV25 CFT16, CFT25	0 0 0 0 0	24 60 24 24 60	96 60 96 96 60	120 300 120	CPU32 core processor for data movement applications. Two channel DMA, two serial channels, two timers, chip selects, wait–state generation, and glue logic. MC68340V is the 3.3 volt version of the MC68340.
						For FE, FT, and PV sample order—SPAK340FEXXE, SPAK340FTXXVE, SPAK340PVXXVC				
XPC821	357–ball ZP	25, 50	A	Integrated PPC Microprocessor	CZP25	0	220	220	220	Integrates a high–performance embedded PowerPC core with communication processor module
XPC823	256–ball ZT 272–ball ZP	25, 50, 66, 75		Integrated PPC Microprocessor		0	40	40	400	Low–cost version of the MPC821.

* Not recommended for new designs.
** Extended temperature devices with minimum order requirements.

END OF LIFE

Device	Last Buy Date	Last Ship Date
MC68341FT	7/1/98	12/31/98
MC68349FT	7/1/98	12/31/98
MC68HC000P/FC/R	3/21/98	9/30/98
MC68HC681	2/25/98	8/31/98
XC68HC901	2/25/98	8/24/98
MC68EC030PV25C	7/1/98	12/31/98
MC68030PV25C	7/1/98	12/31/98

HARDWARE EVALUATION TOOLS

Device	Description
M68EC000IDP	M68EC000 Evaluation/Development System
M68EC020IDP	M68EC020 Evaluation/Development System
M68EC030IDP3	M68EC030 Evaluation/Development System
M68EC040IDP3	M68EC040 Evaluation/Development System
M68EC060IDP	M68EC060 Evaluation/Development System
M68306AN	MC68306 Development Board from Arnewsh
M68340EST	MC68340 Evaluation System
M5102EVM	MCF5102 Mezzanine Board (requires the M68EC040IDP or M68EC040CPU for development)
M5202EVM	MCF5202 Mezzanine Board (requires the M68EC040IDP or M68EC040CPU for development)
M5202GW	MCF5202 to MC68EC000 Microprocessor Bus Interface Card
M5204AN	MCF5204 Evaluation/Development System
M5206AN	MCF5206 Evaluation/Development System
M5307AN	MCF5307 Evaluation/Development System
MPC821ADS	MPC821 Application Development System
MPC823ADS	MPC823 Application Development System

2

Microcontroller Products

In Brief . . .

Motorola MCU's

Generation after generation Motorola continues to build on it's long tradition of superior microcontroller design. With Motorola you can choose from a diverse selection of devices with on–chip peripherals and memories to meet your specific design requirements.

Development tool support for the 68HCXX families comes from dozens of independent development tool suppliers with a variety of hardware and software development tools including: emulators, logic analyzers, programmers, evaluation boards, simulators, C compilers, real–time operating systems, assemblers, and debuggers. All allowing you to efficiently develop, monitor, test and debug your code to get your applications up and running fast.

68HC05

Motorola's 68HC05 family is the world's most popular microcontroller architecture. With so many standard 68HC05 microcontrollers from which to choose, you will easily find the right device for your application. This industry standard, 8–bit microcontroller architecture has numerous derivatives suitable for all types of applications, especially where low cost and solid 8–bit performance are required.

Motorola can offer you a large installed base of emulators, software tools and support are also available to customers. In addition Motorola can also boast a global capability with teamwork, in design, manufacturing, marketing and application support to ensure we help you meet your customer needs.

68HC08

Building on the success of the industry leading 68HC05, the higher performance 68HC08 family enhances the systems solution approach. It incorporates a flexible, modular design and a library of proven peripherals — to achieve even faster design cycle times, enhanced manufacturing quality and maximum cost efficiency. These devices are characterized by a high level of integration and offer a rich choice of features.

Motorola's 8–bit 68HC08 microcontroller features an expanded instruction set and a more powerful processor core. It's ideal for 8–bit applications that require more performance, but doesn't justify a major increase in cost. The 68HC08 creates more options and a full upward object–code compatibility which makes it easy to move up the performance curve when the application warrants.

68HC11

Our family of microcontrollers includes a true standout, the high performance 8–bit 68HC11 family. It offers a wide range of devices, each versatile in operation and covering a broad range of cost and performance combinations. Motorola's constant quest for improved quality and cycle time is why the 68HC11 holds it's premium position in the market place.

Our family was the first microcontroller to include EEPROM; setting the standard for its inclusion on most 68HC11 derivatives. The 68HC11 also offers a variety of on–chip peripherals and memories to meet specific design requirements along with versatile low–voltage operation.

The 68HC11 family offers architectural compatibility with the 68HC05 family of 8–bit microcontrollers. It is also source code compatible with the 68HC12 and 68HC16 families of microcontrollers for smooth upward migration.

68HC12

Motorola has enhanced it's lineup of advanced microcontrollers, with the 68HC12. This highly integrated, general purpose family is our 16–bit microcontroller architecture specifically designed for low power consumption. And it's completely source code compatible with Motorola's popular 68HC11 8–bit microcontroller family.

The 68HC12 is optimized for low power operations and features an enhanced CPU. It has 64 new instructions and a flexible modular design. Other key features include Background Debug mode for non–intrusive in–circuit programming and debugging, on–chip Flash EEPROM, fuzzy logic instruction and High Level Language support.

The 68HC12 is an exciting new option for Motorola's customers. The code efficient 68HC12 is ideal for today's portable, power thrifty applications that range from wireless communications and automotive to industrial controls and smaller than ever electronic products.

68HC16

The 16–bit 68HC16 modular microcontroller family offers Motorola customers an unsurpassed versatility. Its CPU features a faster multiply, divide, and integration of DSP functions, as well as speeds running eight times faster than standard 68HC11 microcontrollers. The 68HC16 family boasts an extensive list of standard features and modular peripherals that make this highly integrated family the perfect choice for a wide range of embedded control applications. the 68HC16 family is fully supported by a variety of hardware and software development tools, from Motorola and many independent suppliers.

68300

The 68300 is a powerful 32–bit modular microcontroller family with a CPU based on the 68000 instruction set. It combines high performance data manipulation capabilities with a group of peripheral subsystems. Flexibility combined with features like in–circuit debugging makes the 68300 ideal for a wide range of control — intensive applications. Because these microcontrollers use the same on–chip modules, external bus interface, and Motorola development systems as the 68HC16, upward migration is made easier.

MPC500

Motorola introduces the MPC500 family of RISC PowerPC™ microcontrollers, a development that not only raises embedded control performance levels but also the expectations of microcontroller customers around the world.

For the first time, embedded control designers can leverage the superior performance of a RISC processor based on the schedule PowerPC Architecture™. The MPC500 family also features the integration, functionality and modularity which have become trademarks of Motorola microcontrollers. In addition it offers the IMB peripheral from the HC16 and 68300 families.

The 500 family is derived from a revolutionary 32–bit RISC PowerPC microcontroller developed by Motorola specifically for an automotive application. With a challenging environmental conditions that range from voltage spikes to mechanical vibrations and electrical noise, automotive applications are excellent proving grounds for microcontroller quality and reliability. We pass with flying colors.

68HC05 MICROCONTROLLERS

All 68HC05 products have a standard operating voltage range from 3 V to 5.5 V unless noted in Comments.
All 68HC05 products have a standard operating temperature range from 0 to 70°C. Contact a Motorola Sales Office for availability of extended temperature versions.

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages	Emulation Version	Documentation
MC68HC05B6	6K	176	256	16-bit: (2IC, 2OC)	SCI+	8 ch (8-bit)	2 ch (8-bit)		24 i/o 8 i 2 o 32	✔	On-Chip Charge Pump EEPROM Write Protect	56 SDIP - B 52 PLCC - FN 64 QFP - FU	705B16 705B32	MC68HC05B6/D AN1120/D, AN434/D
MC68HC05B8	7.25K 7K	176	256	16-bit: (2IC, 2OC)	SCI+	8 ch (8-bit)	2 ch (8-bit)		24 i/o 8 i 2 o 32	✔	On-Chip Charge Pump EEPROM Write Protect	56 SDIP - B 52 PLCC - FN 64 QFP - FU	705B16 705B32	MC68HC05B6/D AN1058/D
MC68HC05B16	15K	352	256	16-bit: (2IC, 2OC)	SCI+	8 ch (8-bit)	2 ch (8-bit)		24 i/o 8 i 2 o 32	✔	On-Chip Charge Pump EEPROM Write Protect	56 SDIP - B 52 PLCC - FN 64 QFP - FU	705B16 705B32	MC68HC05B6/D AN1058/D
MC68HC05B32	32K	528	256	16-bit (2IC, 2OC):	SCI+	8 ch (8-bit)	2 ch (8-bit)		32 i/o	✔	On-Chip Charge Pump EEPROM Write Protect	52 PLCC - FN 56 SDIP - B 64 QFP - FU	705B32	MC68HC05B6/D AN1058/D
MC68HC05BD3	3.75K	128		MFT	I^2C		16 ch (8–bit)		24	✔	Horizontal and Vertical Sync Signal Processor	40 DIP - P 42 SDIP - B	705BD3	MC68HC05BD3D/H
MC68HC05BD5	7.75K	256		MFT	I^2C		16 ch (8–bit)		24	✔	Horizontal and Vertical Sync Signal Processor	40 DIP - P 42 SDIP - B	705BD3	MC68HC05BD3D/H
MC68HC05C8A	8K	176		16-bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i 31	✔	KBI (8 pins) 1 High Current Pin (20 mA sink) Mask Option Pullups High Speed Option (HSC05C8A) Low Power Option (HCL05C8A) (1.8 V minimum):	40 DIP - P 44 PLCC - FN 44 QFP - FB 42 SDIP - B	705C8A	HC05C8AGRS/D
MC68HC05C9A	16K	352		16-bit: (1IC, 1OC)	SPI SCI				24 i/o 7 i 31	✔	KBI (8 pins) 1 High Current Pin (10 mA sink) Mask Option Pullups High Speed Option (HSC05C9A) Low Power Option (HCL05C9A)	40 DIP - P 44 PLCC - FN 44 QFP - FB 42 SDIP - B	705C9A	HC05C9AGRS/D
MC68HC05D32	32K	352		16–bit (1IC, 1OC)	SCI		5 ch (6–bit)		31	✔	24 mA Port Driver	40 DIP - P 44 PLCC - FN	705D32	MC68HC05D9/D
MC68HC05J1A	1.2K	64		MFT, RTI					14 i/o	✔	KBI (4 pins) 4 High Current Pins (8 mA sink) Mask Option Pulldowns (14 pins) High Speed Version (HSC05J1A) Low Power Version (HCL05J1A): (1.8 V minimum)	20 DIP - P 20 SOIC - DW	705J1A	MC68HC05J1A/D MC68HC05J1AAD/D

68HC05 MICROCONTROLLERS (continued)

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages	Emulation Version	Documentation
MC68HC05J5A	2.5K	128		16–bit (1IC) MFT, RTI					14	✔	2 High–Current Pins (25 mA), LVR, RC Option Available	20 DIP – P 20 SOIC – DW 16 DIP – JP 16 SOIC – JDW	705J5A	HC05J5AGRS/H
MC68HC05JB3	2.5K	144		16-bit: (1IC, 1OC) MFT, RTI	USB				19	✔	1.5 Mbs USB with 3 Endpoints, LVR, KBI, 3.3 V Bandgap Reference	20 DIP – JP 20 SOIC – JDW 28 DIP – P 28 SOIC – DW	705JB3	HC05JB3GRS/H
MC68HC05JB4	3.5K	176		16 TIMER (1IC, 1OC) MFT, RTI	USB	6 ch (8-bit)			19 i/o	✔	Low Voltage Reset 3.3 V Regulator USB (1.5) MBS	28 DIP - P 28 SOIC - DW	705JB4	HC05JB4GRS/H
XC68HC05JJ6	6K	224		16-bit: (1IC, 1OC) MFT, RTI	SIOP	single slope 4 ch 12–bit			14 i/o	✔	Two Voltage Comparators used with timer to create A/D (12-bit resolution), KBI (4 pins), Programmable Pulldowns (14 pins), 6 High Current Pins (10 mA sink) EPROM Security Feature, LVI	20 DIP - P 20 SOIC - DW	705JJ7	HC05JJ6GRS/D
XC68HC05JP6	6K	224		16-bit: (1IC, 1OC) MFT, RTI	SIOP	4 ch 12–bit			22 i/o	✔	Two Voltage Comparators used with timer to create A/D (12-bit resolution), KBI (4 pins), Programmable Pulldowns (14 pins), 6 High Current Pins (10 mA sink) EPROM Security Feature, LVI	28 DIP - P 28 SOIC - DW	705JP7	HC05JJ6GRS/D
MC68HC05K0	0.5K	32		MFT, RTI					10 i/o	✔	4 High Current Pins (8 mA sink) Programmable Pulldowns (10 pins) Low Voltage Reset Mask Option Low Power version (HCL05K0): (1.8 V minimum)	16 DIP - P 16 SOIC - DW	705K1 805K3	MC68HC05K1/D AN463/D
MC68HC05K3	.9K	64	16 PEEP	MFT, RTI					10 i/o	✔	KBI (4 pins), Prog. Pulldowns (10 pins) 4 High Current Pins (8 mA sink) On-Chip Charge Pump 1.8 V Operating Voltage	16 DIP - P 16 SOIC - DW 20 SSOP – SD	805K3	HC05K3GRS/D
MC68HC05L5	8K	256		16-bit: (1IC, 1OC) RTI 8-bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1-4 x 27-39)	14 i/o 10 i 15 o 39		KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins), Open Drain (31 pins), 2.2 V	80 QFP - FU	705L16	HC05L5GRS/D

68HC05 MICROCONTROLLERS (continued)

Motorola Part Number	ROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages	Emulation Version	Documentation
MC68HC05L16	16K	512		16-bit: (1IC, 1OC) RTI 8-bit: (1IC, 1OC)	SIOP			156 Segment LCD: (1-4 x 27-39)	16 i/o 8 i 15 o 39		KBI (8 pins), Dual Oscillators 8 High Current Pins (10 mA sink) Programmable Pullups (24 pins) Open Drain (31 pins), 2.2 V Operation	80 QFP - FU	705L16	HC05L16GRS/D
MC68HC05L25	6K	176		16-bit Event, Timebase	SPI	2 ch (8–bit)		24 x 4 or 25 x 3	20	✔		52 LQFP – FU	705L26	HC05L25GRS/D
MC68HC05LJ5	1.2K	64		MFT, RTI					14	✔	RC Option Available	16 DIP – P	705J5A	HC05LJ5GRS/H
MC68HC05P1A	2K	128		16-bit: (1IC, 1OC)					20 i/o 1 i 21	✔	KBI (8 pins) Mask Option Pullups (8 pins) 2 High Current Pins (20 mA)	28 DIP - P 28 SOIC - DW	705P6A	HC05P1AGRS/D
MC68HC05P4A	4K	176		16-bit: (1IC, 1OC)	SIOP				20 i/o 1 i 21	✔	KBI (8 pins) 2 High Current Pins	28 DIP - P 28 SOIC - DW	705P6A	HC05P4AGRS/D
MC68HC05P6	4.5K	176		16-bit: (1IC, 1OC)	SIOP	4 ch (8-bit)			20 i/o 1 i 21	✔		28 DIP - P 28 SOIC - DW	705P6	MC68HC05P6/D AN1058/D ML68HC05P6AD/D
MC68HC05PL4/B	4K	256		16–bit (1IC, 1OC) 8–bit					23	✔	DTMF, 6–bit D/A, RC Option, KBI	28 DIP – P 28 SOIC – DW	705PL4/B	HC05PL4GRS/H
MC68HC05RC9	8K	352		IR Timer					20	✔	(See 705RC16)	28 DIP – P 28 SOIC – DW 44 PLCC – FN	705RC16	HC05RC18GRS/D
MC68HC05RC18	16K	352		IR Timer					20	✔	(See 705RC16)	28 DIP – P 28 SOIC – DW 44 PLCC – FN	705RC16	HC05RC18GRS/D
MC68HC05SR3	3.75K	192		8–bit		4–ch (8–bit)			32		LED Drive, LVR, KBI	40 DIP – P 44 QFP – FB 42 SDIP – B	705SR3	MC68HC05SR3D/H
MC68HC05SU3A	3.75K	192		8–bit					32		LED Drive, KBI	40 DIP – P	705SR3	MC68HC05SU3A/H
MC68HC05X4	4K	176		16-bit: (1IC, 1OC) MFT, RTI	CAN				16 i/o	✔	CAN (Controller Area Network) KBI (16 pins)	28 SOIC - DW	705X4	MC68HC05X4/D AN464/D
MC68HC05X32	32K	528	256	16-bit: (2IC, 2OC)	SCI+ CAN	8 ch (8-bit)	2 ch (8-bit)		32 i/o	✔	CAN (Controller Area Network), KBI (8 pins), EEPROM Write Protect, On-Chip Charge Pump	64 QFP - FU	705X32	MC68HC05X16/D AN1058/D

68HC05 ONE-TIME PROGRAMMABLE (OTP) / EMULATOR MCUs

All 68HC705 products have a standard operating voltage range from 3 V to 5.5 V unless noted in Comments.
All 68HC705 products have a standard operating temperature range from 0 to 70°C. Contact a Motorola Sales Office for availability of extended temperature versions.

Motorola Part Number	EPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages	Documentation
MC68HC705B16	15K	352	256	16-bit: (2IC, 2OC)	SCI+	8 ch (8-bit)	2 ch (8-bit)		32 i/o 2o	✔	On-Chip Charge Pump EEPROM Write Protect	52 PLCC - FN 64 QFP - FU	MC68HC05B6/D AN1058/D
XC68HC705B32	32K	528	256	16-bit, (21C, 2OC)	SCI+	8 ch (8-bit)	2 ch (8-bit)		32 i/o	✔	On-Chip Charge Pump EEPROM Write Protect	52 PLCC - FN 56 SDIP - B 64 QFP - FU	MC68HC05B6/D AN1058/D
MC68HC705BD3	7.75K	256		MFT	I^2C		16 ch (8-bit)		24	✔	Horizontal and Vertical Sync Signal Processor	40 DIP – P 42 SDIP – B	MC68HC05BD3D/H
MC68HC705BD7	11.5K	384		MFT	MBUS (DDC 1/2 B)	4 ch (8–bit)	16 ch (8-bit)		26	✔	Enhanced Sync Processor plus VESA DDC Block	40 DIP – P 42 SDIP – B	HC705BD7GRS/H
MC68HC705C8A	8K	304		16-bit: (1IC, 1OC)	SPI SCI				24 i/o 7i 31	✔	Mask Option Pullups (8 pins) KBI (8 pins) 1 High Current Pin (20 mA sink) High Speed Option (HSC705C8A) Superset of ROM C8A with more RAM EPROM Security	40 DIP - P 44 PLCC - FN 42 SDIP - B 44 QFP - FB	MC68HC705C8A/D
MC68HC705C9A	16K	352		16-bit: (1IC, 1OC)	SPI SCI				31 i/o	✔	Mask Option Pullups (8 pins) KBI (8 pins) 1 High Current Pin (20 mA sink) EPROM Security	40 DIP - P 44 PLCC - FN 42 SDIP - B 44 QFP - FB	HC705C9AGRS/D
XC68HC705D32A	32K	352		16-bit (1IC, 1OC)	SCI		5 ch (6–bit)		31	✔	24 mA Port Driver	40 DIP – P 44 PLCC – FN	MC68HC05D9/D
XC68HC705F32	32K	920	256	16-bit (41C, 40C) MFT, RTI	SCI SPI	8 ch (8–bit)	3 ch (8–bit)	4 x 40	up to 80	✔	DTMF, KBI (8 Pins)	100 LQFP – PU 80 QFP – FU	MC68HC05F32/D
MC68HC705J1A	1.2K	64		MFT, RTI					14 i/o	✔	KBI (4 pins), EPROM Security Feature 4 High-Current Pins (8 mA sink) Programmable Pulldowns (14 pins) RC osc version (68HRC705J1A) Hi-Speed Version (68HSC705J1A)	20 DIP - P 20 SOIC - DW	MC68HC705J1A/D
MC68HC705JB4	3.5K	176		16-bit: (ITC, 1OC, MFT, RTI)	USB	6 ch (8–bit)			39 I/0 19	✔	Low Voltage Reset 3.3 V Regulator USB (1.5) MBS	28 DIP, SOIC 28 SOIC - DW	HC05JB4GRS/H

68HC05 ONE–TIME PROGRAMMABLE (OTP) / EMULATOR MCUs (continued)

Motorola Part Number	EPROM (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM	Display Drive	I/O	COP	Comments	Packages	Documentation
XC68HC705JJ7	6K + 64-bit PEP	224		16-bit (1IC, 1OC) MFT, RTI	SIOP	single slope 4 ch (12–bit)			14 i/o	✔	Two voltage comparators used with timer to create A/D (12-bit resolution), KBI (4 pins), Programmable Pulldowns (14 pins), 6 High Current Pins (10 mA sink), EPROM security feature, LVI	20 DIP - P 20 SOIC - DW	HC705JJ7GRS/D
XC68HC705JP7	6K + 64-bit PEP	224		16-bit (1IC, 1OC) MFT, RTI	SIOP	single slope 4 ch (12–bit)			22 i/o	✔	Two voltage comparators used with timer to create A/D (12-bit resolution), KBI (4 pins), Programmable Pulldowns (14 pins), 6 High Current Pins (10 mA sink), EPROM security feature, LVI	28 DIP - P 28 SOIC - DW	HC705JJ7GRS/D
XC68HC805K3		64	920 16PEEP	MFT, RTI					10 i/o	✔	KBI (4 pins), Programmable Pulldowns (10 pins), 4 High Current Pins (8 mA sink), On-chip Charge Pump	16 DIP - P 16 SOIC - DW	MC68HC805K3/D
M68HC705KJ1	1.2K	64		MFT, RTI					10 i/o	✔	KBI (4 pins), Programmable Pulldowns (10 pins), 4 High Current Pins (8 mA sink), On-chip Charge Pump	16 DIP - P 16 SOIC - DW * 16 Cerdip -S	MC68HC705KJ1/D
MC68HC705L16	16K	512		16-bit (1IC, 1OC) 8-bit (1IC, 1OC) RTI	SIOP			4 x 39 Segments	39	✔	KBI (8 Pins), Dual Oscillators, 8 High–Current Pins, Programmable Pull–Ups, Open Drain	80 QFP – FU	HC05L16GRS/D
MC68HC705P6A	4.5K	176		16-bit (1IC, 1OC)	SIOP	4 ch (8 - bit)			20 i/o 21	✔	KBI (8 pins) 2 High Current Pins (15 mA sink)	28 DIP - P 28 SOIC - DW	HC705P6AGRS/D
MC68HC705PL4/B	4K	256		16-bit (1IC, 1OC) 8-bit					23	✔	DTMF, 6–Bit D/A, RC Option, KBI	28 DIP – P 28 SOIC – DW	HC05PL4GRS/H
XC68HC705RC16	16K	350		I.R. Timer					20	✔	Special Timer for Remote Control, Supports PLM, FSK Protocol. 705RC16 has different Pull–Ups than 05RC9/18	28 DIP – P 28 SOIC – DW	HC705RC16GRS/D
MC68HC705SR3	3.75K	192		8-bit Timer (7-bit prescaler)		4 ch (8-bit)			32 i/o		Programmable pullups (24 pins) KBI (8 pins), LED drive (8 pins) LVR	40 DIP- P 42 SDIP - B 44 QFP - FB	MC68HC05SR3D/H
MC68HC705X32	32K	528	256	16-bit, (21C, 2OC)	SCI+ CAN	8 ch (8-bit)	2 ch (8-bit)		32 i/o	✔	CAN (Controller Area Network)	64 QFP - FU	MC68HC05X16/D AN1058/D

* Windowed packages available only in sample quantities.

68HC08 MICROCONTROLLERS

Motorola Part Number	ROM/ EPROM Flash (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM (D/A)	Display Drive	I/O	COP	Additional Features	Packages	Emulation Version	Documentation
XC68HC08AZ32	32K	1K	512	4 ch & 2 ch 16-bit: (IC, OC, or PWM), PIT	SCI SPI	8 ch 8-bit	See Timer		50 i/o 48	✔	8 MHz Internal Bus (5 V) Controller Area Network 2.0B (MSCAN) Programmable PLL LVI/LVR KBI (5 pins)	64 QFP - FU 44 QFP – FB	908AZ60	HC08AZ32TS/D CPU08RM/AD TIM08RM/AD M68HC08RG/AD
XC68HC08AZ0		1K	512	4 ch & 2 ch 16-bit: (IC, OC, or PWM), PIT	SCI SPI	8 ch 8-bit	See Timer		50 i/o 48	✔	8 MHz Internal Bus (5 V) External Bus Interface Controller Area Network 2.0B (MSCAN) Programmable PLL LVI/LVR KBI (5 pins)	100 LQFP – PU	N/A	HC08AZ32TS/D CPU08RM/AD TIM08RM/AD M68HC08RG/AD
XC68HC08LN56	56K	1280 + 160 LCD		4 ch 16-bit: (IC, OC, or PWM), TBM	SCI Dual SPIs	4 ch 8-bit	See Timer	1280 Segment LCD; 40 x 32	42	✔	8 MHz Internal Bus (5 V) Programmable 32 kHz PLL LVI/LVR KBI (8 pins) Programmable pullups (8 pins)	144 LQFP - PV	708LN56 (Limited Qty)	HC08LN56GRS/D CPU08RM/AD TIM08RM/AD M68HC08RG/AD

68HC08 FLASH MCUs

Motorola Part Number	ROM/ EPROM Flash (Bytes)	RAM (Bytes)	EEPROM (Bytes)	Timer	Serial	A/D	PWM (D/A)	Display Drive	I/O	COP	Additional Features	Packages	Emulation Version	Documentation
XC68HC908AZ60	60K	2K	1K	6 ch & 2 ch 16-bit: (IC, OC, or PWM), PIT	SCI SPI	15 ch 8-bit	See Timer		48	✔	8 MHz Internal Bus (5 V) Controller Area Network 2.0B (MSCAN) Programmable PLL LVI/LVR KBI (5 pins)	64 QFP - FU	N/A	CPU08RM/AD TIM08RM/AD M68HC08RG/AD HC908AZ60GRS/D
XC68HC908GP20	20K	512		Dual 2 ch 16-bit (IC, OC, or PWM)	SCI SPI	8 ch 8-bit	See Timer		33 i/o	✔	32 KHZ PLL Low Voltage Reset Hi–Current Pins Time Base Module, KBI	40 DIP - P 44 QFP - FB	N/A	MC68HC908GP20/D CPU08RM/AD TIM08RM/AD

M68HC11 AND M68L11 DEVICES[1]

Motorola Part Number	ROM or *EPROM*	RAM	EEPROM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[2]	Operating Voltage	Package	Bus Types	Features	Development System	Documentation
68HC(L)11D0 68HC(L)11D3	0 4K	192 192	0 0	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	—	16 32	0–2.0 MHz 0–3.0 MHz 0–2.0 MHz	C, V, M C 0–70 °C	4.5–5.5 V 4.5–5.5 V 3.0–5.5 V	40 P 44 FN 44 FB	Mux	—	EVS/EM MMDS	BR777/D MC68HC11D3/D MC68HC11D3RG/AD
68HC711D3	*4K*	192	0	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG Pulse Accumulator	SPI, SCI	—	32	0–2.0 MHz 0–3.0 MHz	C, V, M C	4.5–5.5 V	40 P 44 FN 44 FS 44 FB	Mux	—	EVS/EM MMDS SPGMR	BR778/D MC68HC711D3/D MC68HC11D3RG/AD
68HC(L)11E0 68HC(L)11E1 68HC(L)11E9[4]	0 0 12K	512 512 512	0 512 512	16-bit Timer: 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	22 22 38	0–3.0 MHz 0–2.0 MHz	C, V, M 0–70 °C	4.5–5.5 V 3.0–5.5 V	52 FN 64 FU 52 PB 48 P	Mux	4 EEPROM Block Protects	EVS/EM MMDS SPGMR	MC68HC11E9TS/D MC68HC11E/D MC68HC11ERG/AD
68HC711E9[4]	*12K*	512	512	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	38	0–2.0 MHz 0–3.0 MHz	C, V, M C	4.5–5.5 V	52 FS 52 FN 64 FU	Mux	4 EEPROM Block Protects	EVB, EVS/EM MMDS SPGMR	BR775/D MC68HC11E/D MC68HC11ERG/AD
68HC11E20	20K	768	512	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	38	0–2.0 MHz 0–3.0 MHz	C, V, M	4.5–5.5 V	52 FN 64 FU	Mux	Expanded 11E9, Additional Baud Rates	EVS/EM MMDS SPGMR	MC68HC11E20TS/D MC68HC11E/D MC68HC11ERG/AD
68HC811E2[4]	0	256	2K	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	38	0–2.0 MHz	C, V, M	4.5–5.5 V	52 FN 48 P 52 PB	Mux	4 EEPROM Block Protects	EVB, EVBU EVS/EM MMDS SPGMR	BR780/D MC68HC11E/D MC68HC11ERG/AD
68HC711E20[4]	*20K*	768	512	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	38	0–2.0 MHz 0–3.0 MHz	C, V, M	4.5–5.5 V	52 FS 52 FN 64 FU	Mux	Expanded 11E9, Additional Baud Rates	EVS/EM MMDS SPGMR	MC68HC11E/D MC68HC11ERG/AD
68HC11FC0	0	1K	0	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	—	28	0–4.0 MHz 0–3.0 MHz 4 MHz 5 MHz 6 MHz	C C 0–70 °C C 0–70 °C	4.5–5.5 V 3.0-5.5 V 3.0-5.5 V 4.5-5.5 V 4.5-5.5 V	80 PU	Non-Mux	Chip-Selects	—	MC68HC11FTS/D

M68HC11 AND M68L11 DEVICES[1] (continued)

Motorola Part Number	ROM or *EPROM*	RAM	EEPROM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[2]	Operating Voltage	Package	Bus Types	Features	Development System	Documentation
68HC(L)11F1	0	1K	512	16-bit Timer 3 or 4 IC, 4 or 5 OC, RTI, WDOG, Pulse Accumulator	SPI, SCI	8 Bit	30	0–4.0 MHz 0–3.0 MHz 0-5.0 MHz	C, V, M C 0-70 °C	4.5–5.5 V 3.0–5.5 V 4.5-5.5 V	68 FN 80 PU	Non-Mux	Chip-Selects 4 EEPROM Block Protects	EVS/EM MMDS SPGMR	MC68HC11FTS/D MC68HC11F1/D MC68HC11F1RG/AD
68HC(L)11K0 68HC(L)11K1 68HC(L)11K3 68HC(L)11K4[4]	0 0 24K 24K	768 768 768 768	0 640 0 640	16-bit Timer 3 or 4 IC, 4 or 5 OC, 4 PWM, RTI, WDOG, Pulse Accumulator	SPI, SCI+	8 Bit	37 37 62 62	0–3.0 MHz 0–4.0 MHz 0–2.0 MHz	C, V, M C, V 0–70 °C	4.5–5.5 V 4.5–5.5 V 3.0–5.5 V	84 FN 80 FU	Non-Mux	Chip-Selects 5 EEPROM Block Protects	EVS/EM MMDS SPGMR	MC68HC11KTS/D MC68HC11K4/D MC68HC11K4RG/AD
68HC11KS2	32K	1K	640	16-bit Timer 3 or 4 IC, 4 or 5 OC, 4 PWM, RTI, WDOG, Pulse Accumulator	SPI, SCI+	8 Bit	51	0–4.0 MHz	C, V, M	4.5–5.5 V	68 FN 80 PU	Non-Mux	High Speed Enhanced Serial Interface Slow Mode	EVS/EM MMDS SPGMR	TBD
68HC711KS2	*32K*	1K	640	16-bit Timer 3 or 4 IC, 4 or 5 OC, 4 PWM, RTI, WDOG, Pulse Accumulator	SPI, SCI+	8 Bit	51	0–4.0 MHz	C, V, M	4.5–5.5 V	68 FN 68 FS 80 PU	Non-Mux	High-speed Enhanced Serial Interface Slow Mode	EVS/EM MMDS SPGMR	TBD
68HC11KW1	0	768	640	16-bit Timer 3 IC, 5 OC, 4 PWM, RTI, WDOG, Pulse Accumulator	SPI+, SCI+	10 Bit	80	0–4.0 MHz	C, V	4.5–5.5 V	100 PU	Non-Mux	4 Chip-Selects 10-ch, 10-bit ADC Enhanced Serial Interface 2 Additional Timers	MMDS EVS/EM	MC68HC11KW1/D
68HC11P2	32K	1K	640	16-bit Timer 3 or 4 IC, 4 or 5 OC, 4 PWM, RTI, WDOG, Pulse Accumulator	SPI, 3 SCI+	8 Bit	62	0–4.0 MHz	C	4.5–5.5 V	84 FN 80 FU	Non-Mux	PLL Clock 2 MI Bus Units	EVS/EM MMDS SPGMR	MC68HC11P2/D

Notes:
1. The HC midfix denotes 4.5–5.5 V operation. The L midfix denotes 3.0–5.5 V operation.
2. Temperature Ranges: C = (–40°C to 85°C), V = (–40°C to 105°C), M = (–40°C to 125°C).
4. A Secure ROM version of this device is available.

M68HC12 DEVICES

Motorola Part Number	ROM or *Flash*	RAM	EEPROM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[1]	Operating Voltage	Package	Bus Types	Features	Development System	Documentation
68C12A0 68C12A4	0 0	1K 1K	0 4K	16-bit Timer 8 IC/OC, RTI, COP, WDOG Pulse Accumulator	SPI, 2 SCI	8 Bit	91	5 MHz	0–70 °C	3.0 -3.6 V	112 PV	Non-Mux	16-Bit HC11 Fuzzy Logic Inst Background Debug™ Mode Low Power C Efficient	EVB SDI™ Interface	MC68HC812A4TS/D CPU12RM/AD
68HC12A0 68HC812A4	0 0	1K 1K	0 4K	16-bit Timer 8 IC/OC, RTI, COP, WDOG Pulse Accumulator	SPI, 2 SCI	8 Bit	91	8 MHz	C	4.5–5.5 V	112 PV	Non-Mux	16-Bit HC11 Fuzzy Logic Inst Background Debug™ Mode Low Power C Efficient	EVB SDI™ Interface	MC68HC812A4TS/D CPU12RM/AD
68HC912B32 68HC12BE32	*32K* 32K	1K	768	16-bit Timer 8 IC/OC, RTI, COP, WDOG Pulse Accumulator 4 PWM	SPI, SCI	8 Bit	63	8 MHz	C	4.5–5.5 V	80 FU	Mux	16-Bit HC11 Fuzzy Logic Inst Background Debug Mode C Efficient	EVB SDI Interface	MC68HC912B32TS/D CPU12RM/AD
68HC912BC32	*32K*	1K	768	16-bit Timer 8 IC/OC, RTI, COP, WDOG Pulse Accumulator 4 PWM	SPI, SCI	10 Bit	63	8 MHz	C	4.5–5.5 V	80 FU	Mux	16-Bit HC11 MSCAN Background Debug Mode C Efficient	EVB SDI Interface	MC68HC912BC32TS/D CPU12RM/AD

Notes:
1. Temperature Ranges: C = (–40°C to 85°C), V = (–40°C to 105°C), M = (–40°C to 125°C)
2. Minimum Package Quantity multiple to be used when ordering parts. Also available in sample and brick (QFP package) MPQ.

M68HC16 DEVICES

Motorola Part Number	ROM or *FLASH*	RAM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[1]	Operating Voltage	Package	Modes	Features	Modules	Develop–ment System	Development Software	Documentation
68HC16R1	48K	2K	Multichannel CTM7 PIT, WDOG	2 SCI, SPI	8/10 Bit	88	0–16.78 MHz	C	4.5–5.5 V	132 FC	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM2, 2K SRAM, ADC, MCCI, CTM7, 48K MRM	SDI, ICD, MEVB, MMDS	RTEK Kernel	MC68HC16R1PP/D MC68HC16R1/ 916R1UM/AD Module Reference Manuals
68HC916R1	*16K + 32K 2K BE*	2K	Multichannel CTM7 PIT, WDOG	2 SCI, SPI	8/10 Bit	88	0–16.78 MHz	C	4.5–5.5 V	132 FC	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM2, 2K SRAM, ADC, MCCI, CTM7, 16K + 32K FLASH, 2K BEFLASH	SDI, ICD, MEVB, MMDS	RTEK Kernel	MC68HC916R1PP/D MC68HC16R1/ 916R1UM/AD Module Reference Manuals
68HC916X1	*16K + 32K 2K BE*	2K	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, SCI	8 /10 Bit	70	0–16.78 MHz	C	4.5–5.5 V	120 TH	Expanded Bus Single-Chip Background Debug Mode	5 Chip Selects Synthesized Clock	CPU16, SCIM, 2K SRAM, ADC, QSM, GPT, 16K + 32K FLASH, 2K BEFLASH	SDI, ICD, MEVB, MMDS	RTEK Kernel	MC68HC916X1TS/D Module Reference Manuals
68HC16Y1[3]	48K	2K	16-channel TPU, 3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	SPI, 2 SCI	8/10 Bit	95	0–16.78 MHz	C, V, M	4.5–5.5 V	160 FT	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM, 2K SRAM, ADC, MCCI, GPT, TPU, 48K MRM	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit TPUMASM	MC68HC16Y1TS/D MC68HC16Y1UM/AD Module Reference Manuals
68HC916Y1[3]	*48K*	4K	16-channel TPU, 3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	SPI, 2 SCI	8/10 Bit	95	0–16.78 MHz	C	4.5–5.5 V	160 FT	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM, 2K SRAM, ADC, 2K TPURAM, MCCI, GPT, TPU, 48K FLASH	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit TPUMASM	MC68HC916Y1TS/D Module Reference Manuals
68HC16Y3	96K	4K	16-channel TPU2, 3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, 2 SCI	8/10 Bit	95	0–16.78 MHz	C,V	4.5–5.5 V	160 FT	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM2, 4K SRAM, ADC, MCCI, GPT, TPU2, 3 x 32K MRM	SDI, ICD, MEVB, MMDS	RTEK Kernel TPUMASM	—

M68HC16 DEVICES (continued)

Motorola Part Number	ROM or *FLASH*	RAM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[1]	Operating Voltage	Package	Modes	Features	Modules	Develop–ment System	Development Software	Documentation
68HC916Y3	*3 x 32K 4K TPU–FLASH*	4K	16-channel TPU2, 3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, 2 SCI	8/10 Bit	95	0–16.78 MHz	C	4.5–5.5 V	160 FT	Expanded Bus Single-Chip Background Debug Mode	9 Chip Selects Synthesized Clock	CPU16, SCIM2, 4K SRAM, ADC, MCCI, GPT, TPU2, 3 x 32K FLASH 4K TPUFLASH	SDI, ICD, MEVB, MMDS	RTEK Kernel TPUMASM	—
68CK16Z1	0	1K	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, SCI	8/10 Bit	46	0-16.78 MHz	C	2.7-3.6 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU16, SIM, 1K SRAM, ADC, GPT, QSM	SDI ICD	RTEK Kernel MCUinit	MC68HC16ZUM/AD Module Reference Manuals
68HC16Z1 68HC16Z3	0K 8K	1K 4K	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, SCI	8/10 Bit	46	0-16.78 MHz 0-20.97 MHz 0-25.17 MHz	C, V ,M C, V, M C	4.5-5.5 V 4.75-5.25 V 4.75-5.25 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU16, SIM, SRAM, MRM, ADC, GPT, QSM	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit	MC68HC16ZUM/AD Module Reference Manuals
68CK16Z4 68HC16Z4	0	1K	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	2 SCI, SPI	8/10 Bit	46	0-16.78 MHz	C	2.7-3.6 V 4.5-5.5 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU16, SIM, 1K SRAM, ADC, GPT, MCCI	SDI ICD	RTEK Kernel	MC68HC16ZUM/AD Module Reference Manuals

Notes:
1. Temperature Ranges: C = (–40°C to 85°C), V = (–40°C to 105°C), M = (–40°C to 125°C)
3. Available with either Enhanced TPU Function set (A) or Motion Control TPU Function Set (G).
4. Available in “ROMless” configure, with ROM array present, but not programmable.

M68300 DEVICES

Motorola Part Number	ROM or *FLASH*	RAM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[1]	Operating Voltage	Package	Modes	Features	Modules	Development System	Development Software	Documentation
68331	0	0	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse Accumulator PIT, WDOG	QSPI, SCI	—	43	0–16.78 MHz 0–20.97 MHz 0–25.17 MHz	C, V, M C, V, M C	4.5-5.5 V 4.75–5.25 V 4.75–5.25 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU32, SIM, QSM, GPT	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit	MC68331TS/D MC68331UM/AD MC68331/32EC/D Module Reference Manuals
68CK331	0	0	3 or 4 IC, 4 or 5 OC, 2 PWM, Pulse AccumulatorPIT, WDOG	QSPI, SCI	—	43	0–16.78 MHz	C	2.7–3.6 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU32, SIM, QSM, GPT	SDI	RTEK Kernel MCUinit	MC68CK331EC16/D MC68331UM/AD Module Reference Manuals
68332	0	2K	16-channel TPU PIT, WDOG	QSPI, SCI	—	31	0–16.78 MHz 0–20.97 MHz 0–25.17 MHz	C, V, M C, V, M C	4.5-5.5 V 4.75–5.25 V 4.75–5.25 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU32, SIM, QSM, TPU, 2K TPURAM	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit TPUMASM	MC68332TS/D MC68332UM/AD MC68331/32EC/D Module Reference Manuals
68LK332	0	2K	16-channel TPU PIT, WDOG	QSPI, SCI	—	31	0–16.78 MHz	C	3.0-3.6 V	132 FC 144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock	CPU32, SIM, QSM, TPU, 2K TPURAM	SDI	RTEK Kernel MCUinit TPUMASM	MC68LK332EC16/D MC68332UM/AD Module Reference Manuals
68336	0	7.5K	16-channel TPU, CTM4 PIT, WDOG	QSPI, SCI	10 Bit	55	0–20.97 MHz 0–25.17 MHz	C, V, M C, V	4.75–5.25 V	160 FT	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock Queued ADC	CPU32, SIM, TPU, 3.5K TPURAM, 4K SRAM, CTM4, QSM, QADC	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit TPUMASM	MC68336/376UM/AD Module Reference Manuals
68CK338	0	64	Multichannel CTM6 PIT, WDOG	QSPI, SCI	—	55	0–14.4 MHz	C	2.7–3.6 V	144 PV	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock Low Power CPU and SIM	CPU32, SIM, QSM, CTM6	SDI ICD	RTEK Kernel	MC68CK338TS/D Module Reference Manuals
68376	8K	7.5K	16-channel TPU, Multichannel CTM4 PIT, WDOG	QSPI, SCI	10 Bit	55	0–20.97 MHz 0–25.17 MHz	C, V, M C,V	4.75–5.25 V	160 FT	Expanded Bus Background Debug Mode	12 Chip Selects Synthesized Clock Queued ADC CAN 2.0B	CPU32, SIM, TPU, 3.5K TPURAM, 4K SRAM, CTM4, QSM, QADC, 8K MRM, TOUCAN	SDI, ICD, MEVB, MMDS	RTEK Kernel MCUinit TPUMASM	MC68336/376UM/AD Module Reference Manuals

Notes:
1. Temperature Ranges: C = (–40°C to 85°C), V = (–40°C to 105°C), M = (–40°C to 125°C)
3. Available with either Enhanced TPU Function set (A) or Motion Control TPU Function Set (G).

MPC500 DEVICES

Motorola Part Number	ROM or *EPROM*	RAM	EEPROM	Timer	Serial	ADC	I/O	Bus Speed	Temp Range[1]	Operating Voltage	Package	Modes	Features	Modules	Develop-ment System	Develop-ment Software	Documentation
MPC555	0	26K/ 6K	448K	2 TPU 3 MIOS 1– 8 PWM 10 DASM	TOUCAN QSMCM– SCI SCI BUFF QSPI IEEE 1149.1 JTAG	2Q ADC64	176	0–40 MHz	C,M	3.0–3.6 V, 5 V	277 PBGA	32–Bit Power PC™ RISC CPU FPU 8 Chip–Selects Background Debug Mode Available Q1/2000			EVB	3rd Party	RCPURM/AD MPC555PP/AD MPC555UM/WEB

Notes:
1. Temperature Ranges: C = (–40°C to 85°C), V = (–40°C to 105°C), M = (–40°C to 125°C)

PACKAGE OPTIONS (ACTUAL SIZE)

84-Lead PLCC/CLCC

50 mil (1.27 mm) Pitch
1.15 in x 1.15 in Body

68-Lead PLCC/CLCC

50 mil (1.27 mm) Pitch
0.950 in x 0.950 in Body

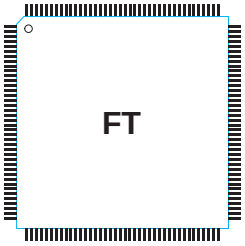
52-Lead PLCC/CLCC

50 mil (1.27 mm) Pitch
0.750 in x 0.750 in Body

44-Lead PLCC/CLCC

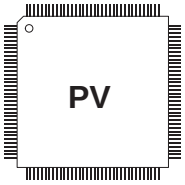
50 mil (1.27 mm) Pitch
0.650 in x 0.650 in Body

160-Lead QFP



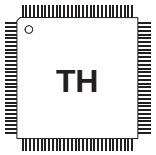
.65 mm Pitch
28 mm x 28 mm Body

144-Lead LQFP



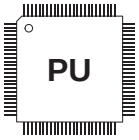
.5 mm Pitch
20 mm x 20 mm Body

120-Lead QFP/LQFP



.5 mm Pitch
16 mm x 16 mm Body

100-Lead LQFP



.5 mm Pitch
14 mm x 14 mm Body

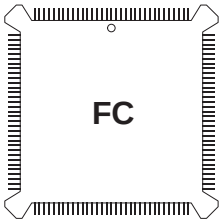
80-Lead QFP/LQFP

.65 mm Pitch
14 mm x 14 mm Body

52-Lead LQFP

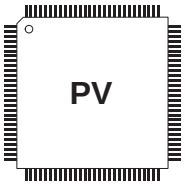
.65 mm Pitch
10 mm x 10 mm Body

132-Lead PQFP



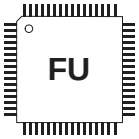
25 mil (0.635 mm) Pitch
0.950 in x 0.950 in Body
(Nominal, w/o Bumpers)

112-Lead LQFP



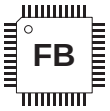
.65 mm Pitch
20 mm x 20 mm Body

64-Lead QFP



.8 mm Pitch
14 mm x 14 mm Body

44-Lead QFP



.8 mm Pitch
10 mm x 10 mm Body

48-Pin Plastic DIP

100 mil (2.54 mm) Pitch
2.45 in x .55 in Body
(100 mil x 600 mil pin centers)

40-Pin Plastic DIP

100 mil (2.54 mm) Pitch
2.05 in x .55 in Body
(100 mil x 600 mil pin centers)

28-Pin Plastic DIP

100 mil (2.54 mm) Pitch
1.45 in x .55 in Body
(100 mil x 600 mil pin centers)

24-Pin Plastic DIP

100 mil (2.54 mm) Pitch
1.25 in x .55 in Body
(100 mil x 600 mil pin centers)

56-Pin Plastic SDI InterfaceP

70 mil (1.778 mm) Pitch
2.05 in x .55 in Body
(70 mil x 600 mil pin centers)

2

TABLE DEFINITIONS

2

ADC — Analog to Digital Converter
BDM — Background Debug™ Mode
BCC — Business Card Computer
BE — Block Erasable FLASH Memory
CAN — Controller Area Network
CCTV — Closed Caption Television
CLCC — Ceramic Leaded Chip Carrier
COP — Computer Operating Properly (Watch Dog Timer)
CPU16 — 16-bit Central Processing Unit (HC11 Compatible)
CPU32 — 32-bit Central Processing Unit (68000 Compatible)
CTM — Configurable Timer Module (Various Hardware options)
DIP — Dual In-line Package
DTMF — Dual-Tone Multi-Frequency
EBI — External Bus Interface
EM — Emulation Module
EVB — Evaluation Board
EVBU — Universal Evaluation Board
EVK — Evaluation Kit
EVM — Evaluation Module
EVS — Evaluation System/Emulation Module
FPU — Floating Point Unit
GPT — General-Purpose Timer Module (4 IC, 5 OC, 2 PWM)
IC — Input Capture
I^2C — Inter-Integrated Circuit
IDE — Integrated Device Electronics (IBM PC/AT Type)
i/o — Bidirectional Input and Output Port Pins
i — Input Only Port Pins
ISPI — Internal Serial Peripheral Interface
KBI — Key Board Interrupt
LCD — Liquid Crystal Display
LVI — Low-Voltage Interrupt
LVPI — Low Voltage Program Inhibit
LVR — Low Voltage Reset
MCCI — Multichannel Communication Interface (2 SCI, SPI)
MDLC — Message Data Link Controller (J1850)
MEVB — Modular Evaluation Board
MFT — Multi Function Timer
MUX — Multiplexed
MMDS — Motorola Modular Development System
MRM — Masked ROM Module
o — Output Only Port Pins
OC — Output Compare
OSD — On-Screen Display
PEEP — Personality EEPROM
PEP — Personality EPROM
PGMR — Programmer
PIT — Programmable Interrupt Timer
PIO — Parallel Input Output (IBM PC/AT Type)
PLCC — Plastic Leaded Chip Carrier
PLL — Phase Locked Loop
POQ — Preferred Order Quantity
PQFP — Plastic Quad Flat Pack
PRU — Port Replacement Unit
PWM — Pulse Width Modulation
QADC — Queued Analog-to-Digital Converter (10-bit)
QFP — Quad Flat Pack
QSM — Queued Serial Module (SCI + QSPI)
QSPI — Queued SPI
RTC — Real-Time Clock
RTEK — Real-Time Executive Kernel
RTI — Real-Time Interrupt
SCI — Serial Communication Interface
SCI+ — Enhanced SCI
SCIM — Single-Chip Integration Module
SDI — Serial Debug Interface™
SDIP — Shrink Dual In-line Package
SIM — System Integration Module
SIO — Serial Input Output (IBM PC/AT Type)
SIOP — Simple Serial I/O Port
SPGMR — Serial Programmer
SPI — Serial Peripheral Interface
SPI+ — Enhanced SPI
SRAM — Standby RAM Module
TPU — Time Processing Unit (16 Programmable Channels)
TPURAM — Standby RAM Module with TPU Emulation Capability
TQFP — Thin Quad Flat Pack
UART — Universal Asynchronous Receiver/Transmitter
USB — Universal Serial Bus
VFD — Vacuum Flourescent Display
VREG — Voltage Regulator
WDOG — Watch Dog Timer
B — Shrink DIP (70 mil spacing)
DW — Small Outline (Wide-Body SOIC)
FA — 7 x 7 mm Quad Flat Pack (QFP)
FB — 10 x 10 mm Quad Flat Pack (QFP)
FE — CQFP (windowed) — Samples Only
FN — Plastic Quad (PLCC)
FS — CLCC (windowed) — Samples Only
FT — 28 x 28 mm Quad Flat Pack (QFP)
FU — 14 x 14 mm Quad Flat Pack (QFP)
FZ — CQFP (windowed) — Samples Only
K — Cersdip (windowed) — Samples Only
L — Ceramic Sidebraze
P — Dual-in-Line Plastic
PU — 14 x 14 Thin Quad Flat Pack (TQFP)
PV — 20 x 20 mm Thin Quad Flat Pack (TQFP)
S — Cerdip (windowed) — Samples Only

M•CORE™ microRISC Products

2

In Brief . . .

M•CORE technology provides a new level of performance for embedded control. The innovative microRISC core was developed specifically to efficiently implement embedded applications. The M•CORE architecture is one of the most compact full 32–bit implementations available, and is optimized for minimal power consumption.

The pipelined RISC execution unit uses 16–bit instructions to achieve maximum speed and code efficiency, while conserving on–chip memory resources. The instruction set is designed to support high–level language implementation. A non–intrusive, JTAG–compliant resident debugging system supports product development and in–situ testing. The M•CORE technology library also encompasses a full complement of on–chip peripheral modules designed specifically for embedded control applications.

The flagship M•CORE product, the MMC2001, includes 32 kbytes of fully static battery–backed RAM and up to 256 kbytes of on–chip ROM, UART and SPI communication interfaces, general–purpose and PWM timers, and a keypad interface. With a clock–speed of 33 MHz and a maximum run I_{DD} of 40 mA, the MMC2001 is ideal for the next generation of portable applications.

M•CORE Engine

The 32–bit M•CORE microRISC engine represents a new line of Motorola microprocessor core products. The processor architecture has been designed for high–performance and cost–sensitive embedded control applications, with particular emphasis on reduced system power consumption. This makes it suitable for a number of battery–operated, portable, and mobile products.

Total system power consumption is dictated by various components in addition to the processor core. In particular, memory power consumption (both on–chip and external) is expected to dominate overall power consumption of the core+memory subsystem. With this factor in mind, the instruction set architecture (ISA) for M•CORE makes the trade–off of absolute performance capability versus total energy consumption in favor of reducing the overall energy consumption. This is accomplished while maintaining an acceptably high level of performance at a given clock frequency.

By designing a streamlined execution engine, many of the same performance enhancements and implementation techniques used by desktop RISC designs are possible. By utilizing fixed–length instruction encoding and defining a strict load/store architecture, control complexity and overhead is minimized. The goal of minimizing the overhead memory system energy consumption is achieved by adopting a 16–bit instruction encoding. This choice significantly lowers the memory bandwidth needed to sustain a high rate of instruction execution. This careful selection of the instruction set for M•CORE allows the code density and overall memory footprint of the M•CORE architecture to approach and surpass the code density offered by CISC architectures.

M•CORE also minimizes power dissipation by using a fully–static design, dynamic clock management, and low–voltage operation. It automatically powers–down internal function blocks that are not needed on a clock–by–clock basis. Power conservation modes, which are invoked via three low–power mode instructions, provide for the absolute lowest power consumption.

The primary features of the M•CORE processor include the following:

- 32–bit load/store RISC architecture
- Fixed 16–bit instruction length
- 16 entry 32–bit general–purpose register file
- Efficient 4–stage execution pipeline, hidden from application software
- Single–cycle instruction execution for most instructions, two cycles for branches and memory access instructions
- Support for byte/halfword/word memory access
- Fast interrupt support with 16–entry user–controlled alternate register file
- Vectored and autovectored interrupt support
- On–chip emulation support
- Full static design for minimizing power consumption
- Fully supported by state of the art third–party development tools

Overview

Figure 1 is a block diagram of the M•CORE processor. The following paragraphs provide an overview of the M•CORE processor.

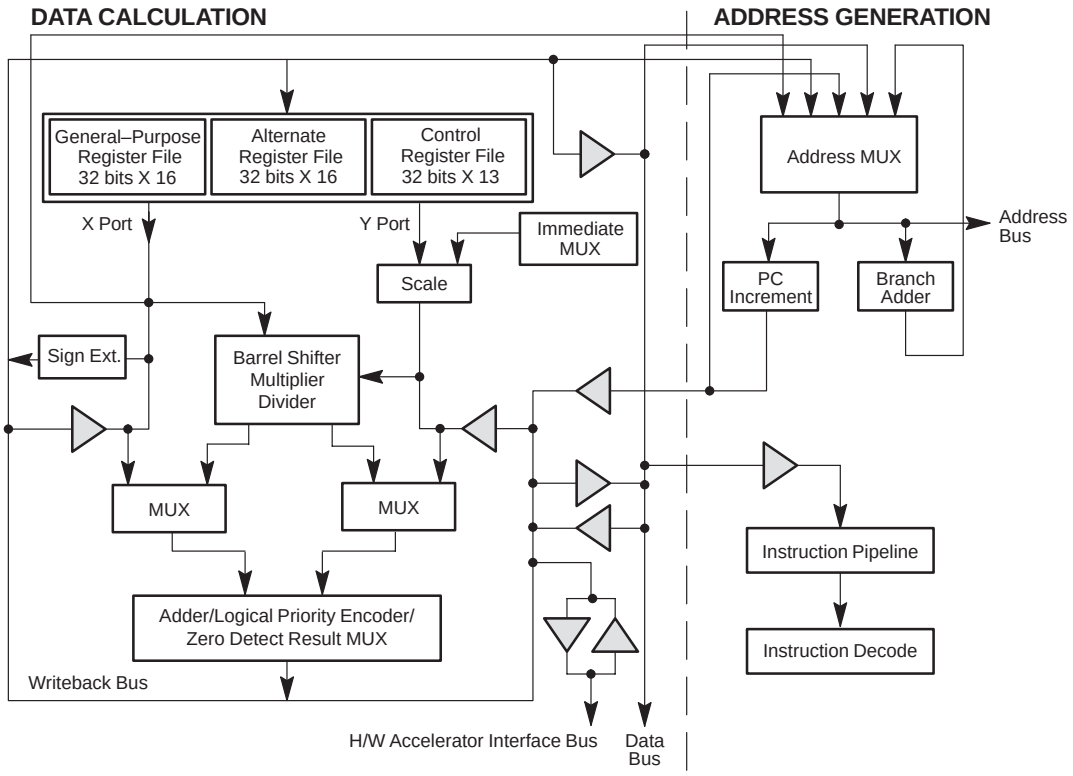


Figure 1. M•CORE Block Diagram

2

M•CORE Processor Core

The M•CORE utilizes a four–stage pipeline for instruction execution. The instruction fetch, instruction decode/register file read, execute, and register file write-back stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

16 general–purpose registers are provided for source operands and instruction results. Register R15 is used as the link register to hold the return address for subroutine calls. Register R0 is used as the current stack pointer by convention.

The execution unit consists of a 32–bit arithmetic/ logic unit (ALU), a 32–bit barrel shifter (Shifter), find–first–one unit (FFO), result feed–forward hardware, and miscellaneous support hardware for multiplication, division, and multiple register load and stores. Arithmetic and logical operations are executed in a single cycle with the exception of multiply and divide. Multiply is implemented with a 2–bit per clock, overlapped–scan, modified Booth algorithm with early–out capability to reduce execution time for operations with small multipliers. Divide is implemented with a 1–bit per clock early–in algorithm. The FFO unit operates in a single clock cycle.

The program counter unit has a PC incrementer and a dedicated branch address adder to minimize delays during change of flow operations. Branch target addresses are calculated in parallel with branch instruction decode, with a single pipeline bubble for taken branches and jumps, resulting in an execution time of two clocks. Conditional branches which are not taken execute in a single clock.

Memory load and store operations are provided for byte, halfword, and word (32–bit) data with automatic zero extension of byte and halfword load data. These instructions can execute in two clock cycles. Load and store multiple register instructions allow low overhead context save and restore operations. These instructions can execute in (N+1) clock cycles, where N is the number of registers to transfer.

A single condition/code carry (C) bit is provided for condition testing and for use in implementing arithmetic and logical operations greater than 32–bits. Typically, the C bit is set only by explicit test/comparison operations, not as a side–effect of normal instruction operation. Exceptions to this rule occur for specialized operations where it is desirable to combine condition setting with actual computation.

M•CORE Processor Core (continued)

A 16–entry alternate register file is provided to support low overhead interrupt exception processing, and both vectored and autovectored interrupts are supported by the CPU.

Power Management Features

M•CORE's industry–leading design maximizes power efficiency. The instruction set and the machine effectively access internal and external memory, which can consume a major portion of a chip and system's power. Being a 16–bit instruction machine, it can efficiently interface to external memory through a 16–bit interface.

Additionally, M•CORE 16–bit instruction mapping gives the user a compact memory image. This minimizes the number of accesses to both internal and external memory.

Both static and dynamic power–enhancing features are included in the architecture and implementation. In terms of the M•CORE architecture, three instructions — stop, doze, and wait, allow system designers to optimize their designs with these power–saving modes. The functionality of these modes is not dictated by the core but is configured by an external power management module. The M•CORE processor core provides output signals associated with the execution of each of these instructions that may be monitored by external logic to control operation of the core, as well as the rest of the system.

The M•CORE has a compact die area of 2.2 mm sq. in 0.36 (L effective) micron CMOS technology. The logic and routing capacitance have been minimized. Gated clocks played a major role in minimizing unnecessary or spurious bus transitions in the data path portion of the design.

Code Density

The M•CORE engine minimizes the overhead memory system by using (relatively) short 16–bit instruction encoding. This choice significantly lowers the memory bandwidth needed to sustain a high rate of instruction execution. The careful selection of instruction for M•CORE, allows for a compact data structure and a small overall memory footprint for the M•CORE architecture. M•CORE supports 8, 16 and 32–bit data, but is highly optimized for use out of 16–bit off–chip memory. This allows a design based around M•CORE to use less expensive and smaller memories, decreasing overall system cost, while also using less memory on–chip for more integrated solutions.

Hardware Accelerator Interface (HAI)

The M•CORE engine provides support for task acceleration by external hardware blocks which are optimized for specific application–related operations. Data is transferred between the core and an accelerator block by one or more of several mechanisms as appropriate for a particular implementation. These external hardware blocks may be as simple as a block for performing a population count, or a more complicated function such as a DSP acceleration block capable of high speed multiply/accumulate operation or data encryption.

Debug Interface

The M•CORE architecture supports on–chip emulation (OnCE™) circuitry through the JTAG interface, which provides a means of interacting with the M•CORE processor core and any peripherals. This allows a user to examine registers, memory, or on–chip peripherals, thus facilitating hardware/software development on the M•CORE processor core. Internal status and control registers are accessible via the serial scan chain during OnCE. To achieve this, special circuits and dedicated pins for the M•CORE processor core are provided to avoid sacrificing any user–accessible on–chip resources.

M•CORE Signal Groups

Figure 2 shows functional grouping of M•CORE signals.

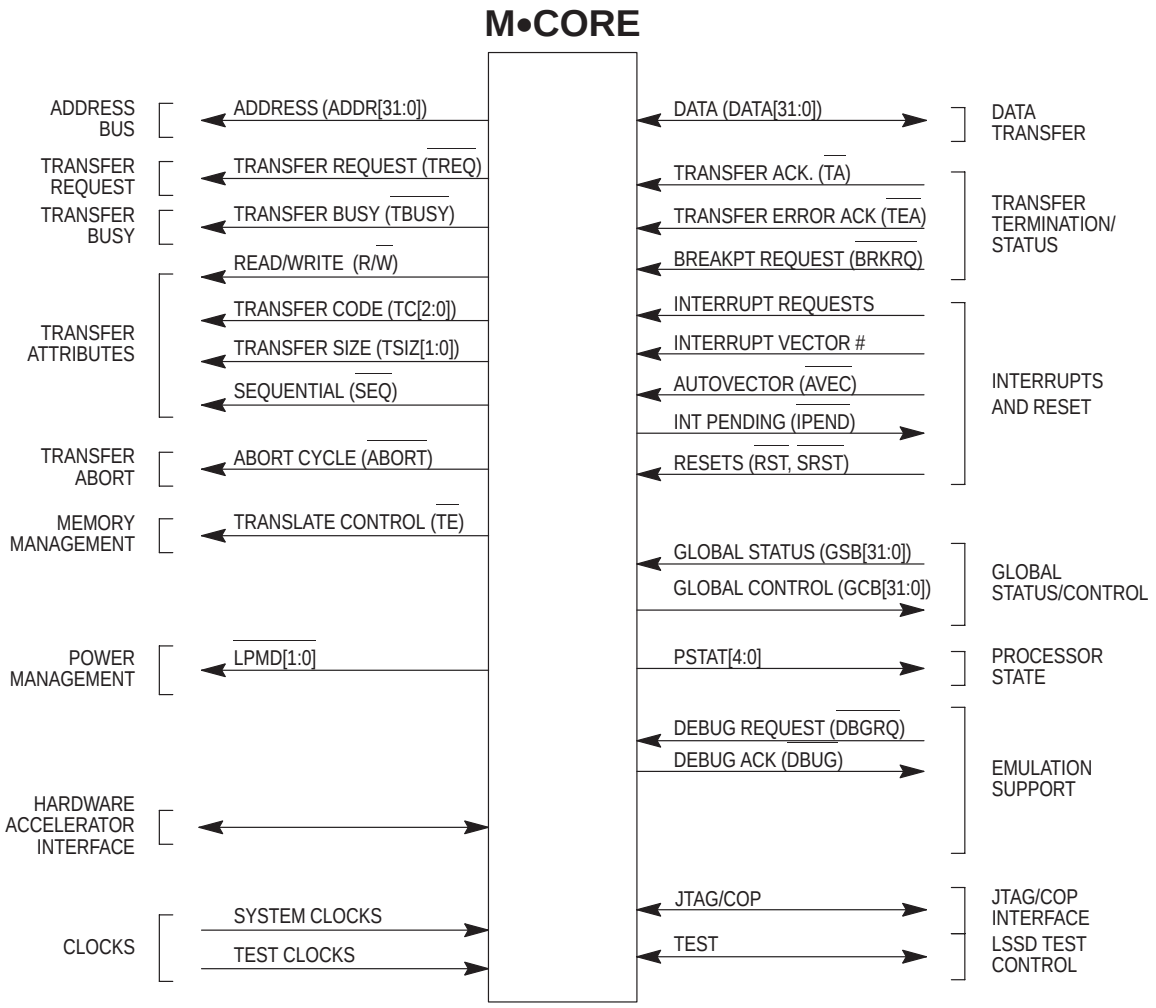


Figure 2. M•CORE Signal Function

Target Applications

The M•CORE architecture represents a new level of performance for embedded applications — an innovative, ultra–low power microRISC core designed to power a new generation of portable and mobile applications. Smaller in size and offering full 32–bit performance out of 16–bit memory, M•CORE delivers a high–performance, low–power solution ideally suited for battery–powered and wireless applications, including digital phones, pagers, electronic personal assistants, and for automotive safety products like anti–lock braking systems (ABS) and airbags, where system cost and high temperature rages are key variables. Combining performance and cost efficiencies in a compact, low–power design, M•CORE is the natural solution for any application where battery life and system costs are as important as MIPS.

Development Tools and Evaluation Systems

A solid selection of third–party development tools is available for the M•CORE processor, including highly optimized compilers, instruction–set simulators, debuggers, target monitors, software/hardware co–verification tools, real–time operating systems, and evaluation boards. Refer to Table 1 for a list of companies. The M•CORE architecture is also supported by an application binary interface (ABI) standard, that defines all the interfaces required by a compiler writer to create a toolchain for M•CORE. This standard allows interoperability between other ABI compliant M•CORE tools. To provide additional support and protection, M•CORE development tools are fully tested to ensure "customer–ready" validation before being released.

Table 1. Development Tool Companies

Company Name	Company Phone Number	Availability
Compilers/Debuggers		
Cosmic	www.std.com/cosmic	Porting
Diab Data	650–571–1700	now
Metrowerks	512–873–4740	Porting
Motorola GNU	www.motorola.com/mcore	now
SDS	630–368–0400	now
HIWARE	www.hiware.com	now
RTOS		
Embedded System Products	281–561–9990	now
Integrated Systems	408–542–1781	now
Microware	515–327–2337	Porting
Microtec	408–487–7336	now
Motorola RTEK	800–262–5486	now
Wind River Systems	510–748–4100	Porting
Instruction Set Simulators		
SDS	630–368–0400	now
Software/Hardware Verification		
Summit	512–343–3686	now
Mentor Graphics	503–685–1575	3Q98
ViewLogic/Eagle Design	503–520–2328	now
Logic Analyzers		
Hewlett–Packard (Processor Probe)	719–590–2558	now
Tektronix (Logic Analyzer)	503–627–6836	now
Development Boards		
MMCEVB1200	800–521–6274	now
MMCCMB1200	800–521–6274	now

MMC2001 M•CORE Integrated Microcontroller

The MMC2001 microcontroller is the first member of the M•CORE family of single–chip control systems. The M•CORE architecture is targeted for high–performance and cost–sensitive embedded control applications, with particular emphasis on reduced system power consumption, making the MMC2001 suitable for battery–operated products.

The MMC2001 incorporates the following functional units:

- M•CORE Integer Processor
  - — 32–bit RISC architecture, 16–bit instructions
  - — Low power, high performance
- OnCE Debug Module
- On–chip SRAM, 32 Kbytes with battery backup supply support
- On–chip ROM, 256 Kbytes
- Interrupt Controller
  - — Support for up to 32 interrupt sources
- External Interface Module
  - — External interface with 22 address lines and 16 data lines
  - — Chip select and wait state generation
  - — Bus watchdog timer
- Timer/Reset Module
  - — Crystal oscillator generates on–chip clock signal from a 32.768 kHz crystal
  - — Time–of–day timer provides real–time event information
  - — Watchdog timer resets the chip to recover from system failure
  - — Reset unit provides low voltage detection and backup power switching
  - — Periodic interrupt timer
- Serial Communication Port (UART)
  - — Two independent UART channels
  - — Asynchronous operation
  - — Baud rate generation
- 16–bit general–purpose I/O port with support for keyboard scan/encode
- 8–bit general–purpose I/O port with support for edge/level sensitive external interrupts
- Pulse Width Modulation Module (PWM)
  - — Six independent PWM channels
  - — Pins can also be configured for general–purpose I/O
- Interval Mode Serial Peripheral Interface (ISPI)
  - — Interval mode SPI operation
  - — Efficient communication with slower serial peripherals
  - — Designed for master/slave SPI operation
- DC to 33 MHz operation
- Low voltage — 1.8 to 3.6 volt operation with separate input/output and core supplies

Figure 3 is a block diagram of the MMC2001 microcontroller. The paragraphs that follow describe the functional components of the integrated control system.

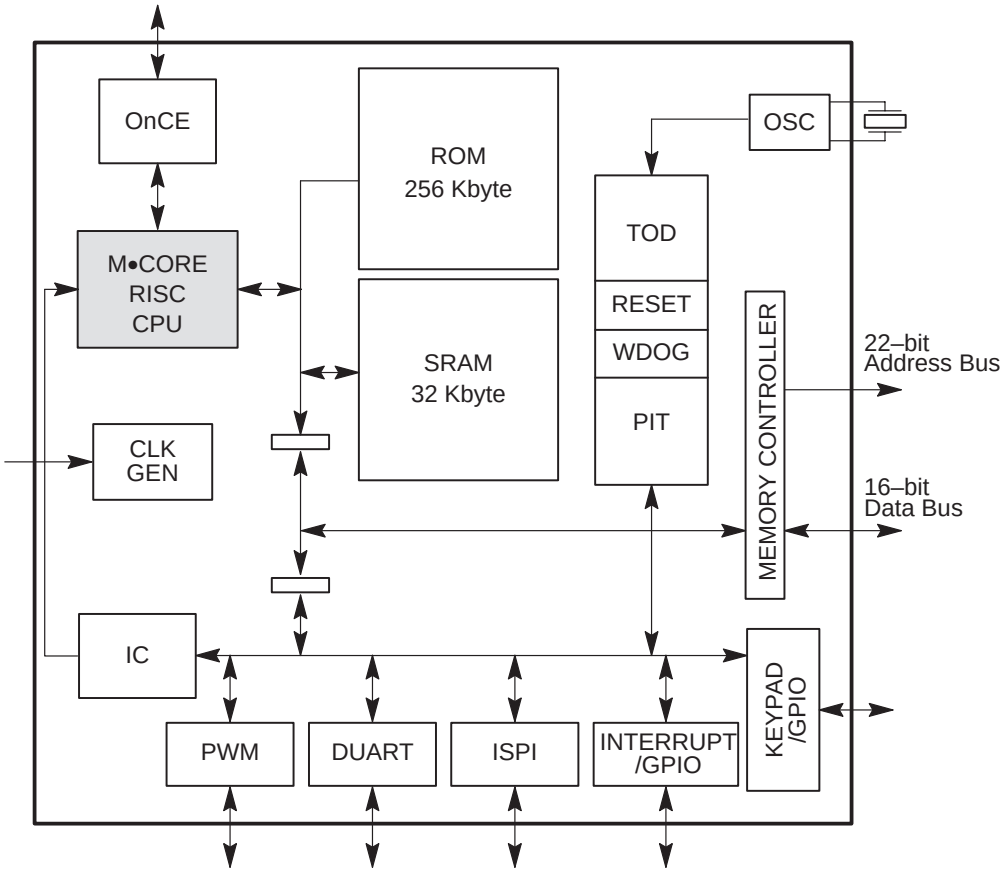


Figure 3. MMC2001 Block Diagram

M•CORE Processor Core

The 32–bit M•CORE microRISC engine is the first of a new line of Motorola microprocessor products designed expressly for embedded control applications. M•CORE is a streamlined execution engine that uses many of the same performance enhancements as mainstream RISC computer designs to minimize system complexity and overhead.

The M•CORE architecture includes on–chip emulation (OnCE) circuitry. A JTAG interface provides the means of interacting with the M•CORE processor and on–chip peripherals. A user can examine processor and on–chip peripheral registers, memory, and instruction execution to facilitate hardware/software development. Debug status and control registers are accessible during OnCE operation. Special circuitry and interface pins are provided to support non–intrusive debug and efficient use of on–chip resources.

Internal Standby RAM

The 32 Kbyte on–chip SRAM supports single–clock access by the M•CORE processor. SRAM supports byte, half word and word accesses. The RAM array is divided into two separate blocks that can be independently activated in order to conserve power.

On–Chip ROM

The 256 Kbyte ROM is pre–programmed with development support code, including:

- Floating point routines
  - — M•CORE ABI compliant routines to implement floating–point computation
- MBUG™ Motorola monitor debugger program with the following features:
  - — Assembly and disassembly of M•CORE instructions for modification and display of code
  - — Single–step trace and continued execution from a specified address

On–Chip ROM (continued)

— Modification, display, and movement of system memory
— Setting, displaying, and removing breakpoints
— Extensive on–line help
— Ability to execute user–assembled and/or downloaded software in a controlled environment
— Automatic decompression of compressed S–record files while downloading
— Logging function for generating a transcript of a debugging session

External Interface Module

The EIM provides 22 address lines and 16 data lines. It supports aligned byte, halfword, and word transfers via 8– and 16–bit ports. The upper or lower byte of the data bus can be used for 8–bit transfers. The EIM incorporates four chip–select circuits for external devices. Each chip select has a match address range of 16 Mbytes, a programmable wait state, selectable protection, and programmable data port size. Each unused chip–select pin can be programmed for use as a general–purpose output. The EIM also includes the logic for internal/external boot ROM select and a bus watchdog for all internal and external bus cycles. Show cycles are available for external visibility of internal bus cycles.

Clock Generation Module

This module controls system clock signals and implements low–power operation. There are two system clock signals. The HI_REFCLK signal for the processor is provided via an external clock input pin (CLKIN). The LOW_REFCLK signal is driven by an external crystal oscillator connected to the VOSC, XOSX, and EXOSC pins. On–chip peripherals can use LOW_REFCLK, HI_REFCLK, a prescaled LOW_REFCLK, or a combination of these, but must be properly synchronized when different clock sources are used.

On–chip peripherals can be shut down independently of the processor. The CLKOUT pin can be driven by either HI_REFCLK or LOW_REFCLK, or it can be de–activated.

There are four operating modes: run, wait, doze, and stop. Different output encodings on the low–power mode (LPMD) pins inform external devices which mode is in use. Run mode is for normal full operation, with all system clocks operating. The remaining modes are for power conservation. Each mode has an associated CPU instruction.

All low–power modes halt the CPU, which then must be awakened by an interrupt request or a reset. The TOD timer is unaffected by any low–power mode. In wait mode, only the CPU is halted, and it can be wakened by any interrupt request. Individual on–chip peripherals are pre–programmed for doze operation — some shut down, while some remain active. Peripherals that remain active can generate interrupt requests and wake up the CPU. In stop mode, most system clocks are halted, but the programmable interrupt and watchdog timers can be used to wake up the system (both can also be stopped). Most on–chip peripherals retain control register values during stop mode, but peripheral operations must be properly terminated before stop. This will ensure orderly re–activation when normal mode operation resumes.

Timer/Reset Module

The timer/reset module contains four timer submodules and the device reset control logic. The reset logic provides reset source status and controls the CLKOUT pin. There are four possible sources of system reset:

- A low–voltage monitor signal
- An external reset signal
- Power–on
- Watchdog timer

There is a status bit for each of the reset sources. The CLKOUT signal is disabled during reset to assure proper synchronization of external devices that use it as a clock reference. It must be re–enabled as a part of system initialization.

Timer functions include:

- Time–of–day with alarm (TOD)
  — Free–running, clocked at LOW_REFCLK/128.
  — Two 32–bit registers count seconds and fractions (1/256) of seconds
  — Unaffected by low–power modes
  — Alarm interrupt can be used to exit from any low–power state
- Periodic interrupt timer (PIT)
  — Clocked at LOW_REFCLK/4
  — Count down from modulus latch value (set–and–forget) or free–running
  — Polled or interrupt–driven operation
- Watch–dog timer (WD)
  — Clocked at LOW_REFCLK/16384
  — Time–out period determined by 6–bit count value
  — Count register re–loaded by each service sequence

Interrupt Controller Module

The IC module performs interrupt masking and priority support. Absolute priority of interrupt service requests is determined by the processor. The IC module manages requests from multiple sources and provides an interface to the processor. It can manage up to 32 interrupt sources, indicates pending interrupt requests, enables/disables interrupt sources, and determines whether an interrupt is a normal or fast–mode interrupt (fast–mode interrupts always have priority). The IC module also provides a mechanism for software to schedule interrupt requests.

Dual UART Module

This module provides two independent and nearly identical serial communications interfaces — UART0 and UART1. UART0 includes modem RTS and CTS support, UART1 does not. Both UARTs support standard serial communications at normal baud rates and are also compatible with the HPSIR/IrDA physical communication protocol. Each UART contains independent receivers and transmitters clocked by an independent clock generator. The generator can be clocked by system clock HI_REFCLK or by an external clock source on the DTR pin. A 12–bit programmable prescaler is used to generate the baud clock.

The UARTs support full duplex, auto–echo loopback, local loopback, and remote loopback modes. Data formats are 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits. 4–byte receive buffers and 2–byte transmit buffers minimize CPU service overhead. The module also provides error detection and maskable–interrupt capabilities. Each UART can generate an interrupt service request when operational or error condition events occur. Interrupts support wake up from low–power modes.

Interval Mode Serial Peripheral Interface

The ISPI supports a standard, multimaster serial peripheral interface bus, including interrupt–driven operation, and also supports transfers at programmable intervals to implement timed–event protocols.

The ISPI has three operating modes:

- Manual mode — typical SPI master mode operation
- Interval mode — manual mode plus the ability to exchange data at programmed periodic intervals.
- Slave mode — typical SPI slave mode operation

External Interrupt/GPIO Module

This module, also called the edge port, controls eight external interrupt request pins. Each pin is configurable for level–sensitive or edge (rising, falling, or both) detection. To enable external interrupts, this module must be configured to recognize the appropriate interrupt request signal, and the interrupt control module must be configured to enable the interrupt request to the processor. The eight pins can also be configured for use as general–purpose I/O pins.

Keypad/GPIO Module

The keypad module provides keypad matrix scanning functions. The module controls 16 pins, and can perform row and column monitoring functions for any keypad configuration up to eight rows by eight columns. Polled and interrupt–driven operation are supported, and there are interrupt request signals for both key depress and key release. If fewer than 64 keys are used, unused pins can be individually configured for use as general–purpose I/O. Pins [7:0] have internal pull–ups enabled when configured as inputs. Pins [15:8] can be configured as open–drain outputs, but normally have totem–pole style output drive. Pins [7:0] are always totem–pole driven when configured as outputs.

Pulse Width Modulator Module

The PWM module contains six identical PWM output channels. Each channel consists of a free–running counter, a period–compare register, a width–compare register, and an associated pin. Width and period registers are double buffered to allow for next cycle loading. All channels share a single prescaler that divides HI_REFCLK by eight predetermined values in the range 4 to 65536, but each channel can independently select a prescaler tap point. Each channel can make an independent maskable interrupt service request. Any unused pin can be used for general–purpose I/O. Channels can be configured as periodic interrupt sources, and the associated pin can be used for general–purpose I/O at the same time.

Device Availability

The MMC2001 is currently available in the package and operating frequency shown in Table 2.

Table 2. Device Availability

Package	Frequency
Plastic low–profile quad flat pack 144 lead	33 MHz

Technical Documentation

Table 3 shows the technical information which is available from Motorola literature distribution centers.

Table 3. Technical Documentation

Document Number	Document Title
MMC2001RM/D	MMC2001 Reference Manual
MCORERM/AD	M•CORE Reference Manual

2

Memory Products

2

In Brief . . .

Motorola has a broad portfolio of Fast Static RAM products from high–performance computing SRAMs (Late Write RAMs, Double Data Rate devices, and BurstRAMs) to a variety of communication memories (CAMs, ZBTE RAMs, NetRAMs, and Asynchronous).

Fast Static RAMs

SYNCHRONOUS

Late Write RAMs

Description	Organization	V_{DD}	Motorola Part Number	Pin Count	Packaging	Speed	Production	Comments
8M	512K x 18	2.5 – 3.3 V	MCM63L918A	119	(FC) FC-PBGA	3.8 / 4.0 / 4.2 / 4.5 ns Latency	Now	Register/Latch. Extended HSTL I/Os.
			MCM63R918	119	(RS) FC-CBGA (FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. HSTL I/Os.
			MCM63R918A	119	(FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. Extended HSTL I/Os.
	256K x 36	2.5 – 3.3 V	MCM63L836A	119	(FC) FC-PBGA	3.8 / 4.0 / 4.2 / 4.5 ns Latency	Now	Register/Latch. Extended HSTL I/Os.
			MCM63R836	119	(RS) FC-CBGA (FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. HSTL I/Os.
			MCM63R836A	119	(FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. Extended HSTL I/Os.
4M	256K x 18	2.5 – 3.3 V	MCM63R818	119	(FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. HSTL I/Os.
		3.3 V	MCM69R819A	119	(ZP) PBGA	5 / 6 / 7 / 8 ns	Now	Register/Register. LVTTL I/Os. Not recommended for new designs.
			MCM69L819A	119	(ZP) PBGA	8.5 / 9.0 / 9.5 ns Latency	Now	Register/Latch LVTTL I/Os. Not recommended for new designs.
			MCM69R818C	119	(ZP) PBGA	4 / 4.4 / 5 / 6 / 7 ns	Now	Register/Register. HSTL I/Os. Process shrink.
			MCM69L818C	119	(ZP) PBGA	5.5 / 6.5 / 7.5 / 8.5 ns Latency	Contact Factory	Register/Latch, HSTL I/Os. Not recommended for new designs.
			MCM69R820C	119	(ZP) PBGA	4 / 4.4 / 5 / 6 / 7 ns	Now	Register/Register. Process shrink. 2.5 V I/Os.
	128K x 36	2.5 – 3.3 V	MCM63R736	119	(FC) FC-PBGA	3.0 / 3.3 / 3.7 / 4.0 / 4.4 ns	Now	Register/Register. HSTL I/Os.
		3.3 V	MCM69R737A	119	(ZP) PBGA	5 / 6 / 7 / 8 ns	Now	Register/Register. LVTTL I/Os. Not recommended for new designs.
			MCM69L737A	119	(ZP) PBGA	8.5 / 9.0 / 9.5 ns Latency	Now	Register/Latch. LVTTL I/Os. Not recommended for new designs.
			MCM69R736C	119	(ZP) PBGA	4 / 4.4 / 5 / 6 / 7 ns	Now	Register/Register. HSTL I/Os. Process shrink.
			MCM69L736C	119	(ZP) PBGA	5.5 / 6.5 / 7.5 / 8.5 ns Latency	Contact Factory	Register/Latch, HSTL I/Os. Not recommended for new designs.
			MCM69R738C	119	(ZP) PBGA	4 / 4.4 / 5 / 6 / 7 ns	Now	Register/Register. Process shrink. 2.5 V I/Os.
1M	64K x 18	3.3 V	MCM69R618	119	(ZP) PBGA	4.4 / 5 / 6 / 7 ns	Now	Register/Register. HSTL I/Os. Not recommended for new designs.
	32K x 36	3.3 V	MCM69R536	119	(ZP) PBGA	4.4 / 5 / 6 / 7 ns	Now	Register/Register. HSTL I/Os. Not recommended for new designs.

Double Data Rate (DDR)

8M	512K x 18	2.5 V	MCM64E918	153	(FC) FC-PBGA	3.0 / 3.3 / 4.0 / 4.4 ns	Now	Data Rate 2x clock rate.
	256K x 36	2.5 V	MCM64E836	153	(FC) FC-PBGA	3.0 / 3.3 / 4.0 / 4.4 ns	Now	Data Rate 2x clock rate.

Shaded areas indicate Focused New Products.
NOTE: Package suffixes are enclosed by ( ) in packaging column.

SYNCHRONOUS

BurstRAMs

Description	Organization	V_{DD}	Motorola Part Number	Pin Count	Packaging	Speed	Production	Comments
8M	512K x 18	3.3 V	MCM63P919	100 119	(TQ) TQFP (ZP) PBGA	225 / 200 / 166 MHz	1Q00	2.5 V/3.3 V I/O pipelined.
			MCM63F919	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns	1Q00	2.5 V/3.3 V I/O flow–through.
	256K x 36	3.3 V	MCM63P837	100 119	(TQ) TQFP (ZP) PBGA	225 / 200 / 166 MHz	1Q00	2.5 V/3.3 V I/O pipelined.
			MCM63F837	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns	1Q00	2.5 V/3.3 V I/O flow–through.
4M	256K x 18	3.3 V	MCM69P819	100 119	(TQ) TQFP (ZP) PBGA	166 / 150 / 133 MHz	Now	2.5 V/3.3 V I/O pipelined. Being replaced by MCM63P819K.
			MCM69F819	100 119	(TQ) TQFP (ZP) PBGA	7.5 / 8 / 8.5 / 11 ns	Now	2.5 V/3.3 V I/O flow–through. Being replaced by MCM63F819K.
			MCM63P819K	100 119	(TQ) TQFP (ZP) PBGA	166 / 150 / 133 MHz	1Q00	2.5 V/3.3 V I/O pipelined. Replaces MCM69P819.
			MCM63F819K	100 119	(TQ) TQFP (ZP) PBGA	8.5 / 9 / 11 ns	1Q00	2.5 V/3.3 V I/O flow–through. Replaces MCM69F819.
			MCM63P819A	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	2.5 V/3.3 V I/O pipelined for higher performance applications.
			MCM63F819A	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	2.5 V/3.3 V I/O flow–through for higher performance applications.
		2.5 V	MCM64P819	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	2.5 V I/O pipelined for high speed low power applications.
			MCM64F819	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	2.5 V I/O flow–through for high speed low power applications.
		1.8 V	MCM65P819	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	1.8 V I/O pipelined for high speed low power applications.
			MCM65F819	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	1.8 V I/O flow–through for high speed low power applications.
	128K x 36	3.3 V	MCM69P737	100 119	(TQ) TQFP (ZP) PBGA	200 / 183 / 166 / 150 / 133 MHz	Now	2.5 V/3.3 V I/O pipelined. Being replaced by MCM63P737K.
			MCM69F737	100 119	(TQ) TQFP (ZP) PBGA	7.5 / 8 / 8.5 / 11 ns	Now	2.5 V/3.3 V I/O flow–through. Being replaced by MCM63F737K.
			MCM63P737K	100 119	(TQ) TQFP (ZP) PBGA	166 / 150 / 133 MHz	1Q00	2.5 V/3.3 V I/O pipelined. Replaces MCM63P737.
			MCM63F737K	100 119	(TQ) TQFP (ZP) PBGA	8.5 / 9 / 11 ns	1Q00	2.5 V/3.3 V I/O flow–through. Replaces MCM69F737.
			MCM63P737A	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	2.5 V/3.3 V I/O pipelined for higher performance applications.
			MCM63F737A	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	2.5 V/3.3 V I/O flow–through for higher performance applications.
		2.5 V	MCM64P737	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	2.5 V I/O pipelined for high speed low power applications.
			MCM64F737	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	2.5 V I/O flow–through for high speed low power applications.
		1.8 V	MCM65P737	100 119	(TQ) TQFP (ZP) PBGA	250 / 225 / 200 MHz	Now	1.8 V I/O pipelined for high speed low power applications.
			MCM65F737	100 119	(TQ) TQFP (ZP) PBGA	6.5 / 7 / 8 ns	Now	1.8 V I/O flow–through for high speed low power applications.
	128K x 32	3.3 V	MCM63P733A	100	(TQ) TQFP	150 / 133 / 117 / 100 / 90 MHz	Now	2.5 V/3.3 V I/O pipelined.
			MCM63F733A	100	(TQ) TQFP	8.5 / 9 / 10 / 11 ns	Now	2.5 V/3.3 V I/O flow–through.
			SCM63F733A	100	(TQ) TQFP	10 / 11 ns	Now	2.5 V/3.3 V I/O flow–through, –40 to 85˚C.
			MCM63P733B	100	(TQ) TQFP	250 / 225 / 200 MHz	Now	2.5 V/3.3 V I/O pipelined for higher performance applications.
			MCM63F733B	100	(TQ) TQFP	6.5 / 7 / 8 ns	Now	2.5 V/3.3 V I/O flow–through for higher performance applications.
		2.5 V	MCM64P733	100	(TQ) TQFP	250 / 225 / 200 MHz	Now	2.5 V I/O pipelined for high speed low power applications.
			MCM64F733	100	(TQ) TQFP	6.5 / 7 / 8 ns	Now	2.5 V I/O flow–through for high speed low power applications.
		1.8 V	MCM65P733	100	(TQ) TQFP	250 / 225 / 200 MHz	Now	1.8 V I/O pipelined for high speed low power applications.
			MCM65F733	100	(TQ) TQFP	6.5 / 7 / 8 ns	Now	1.8 V I/O flow–through for high speed low power applications.

2

SYNCHRONOUS

BurstRAMs

Description	Organization	V_{DD}	Motorola Part Number	Pin Count	Packaging	Speed	Production	Comments
1M	64K x 18	3.3 V	MCM69F618C	100	(TQ) TQFP	7.5 / 8 / 8.5 / 9 / 10 / 12 ns	Now	Flow–through BurstRAM, 5 V tolerant on all pins.
			MCM69P618C	100	(TQ) TQFP	133 / 125 / 100 / 83 / 75 MHz	Now	Pipelined BurstRAM, 5 V tolerant on all pins.
		5 V	MCM67B618A	52	(FN) PLCC	8.5 / 9 / 10 / 12 ns	Now	Not recommended for new designs. Use MCM67B618B.
			MCM67B618B	52	(FN) PLCC	9 ns	Now	Flow–through BurstRAM for Pentium™, MIPS.
			MCM67M618A	52	(FN) PLCC	9 / 10 / 12 ns	Now	Not recommended for new designs. Use MCM67M618B.
			MCM67M618B	52	(FN) PLCC	9 ns	Now	Flow–through BurstRAM for PowerPC™.
	32K x 36	3.3 V	MCM69F536C	100	(TQ) TQFP	7.5 / 8 / 8.5 / 9 / 10 / 12 ns	Now	Flow–through BurstRAM, 5 V tolerant on all pins.
			MCM69P536C	100	(TQ) TQFP	133 / 125 / 100 / 83 / 75 MHz	Now	Pipelined BurstRAM, 5 V tolerant on all pins.

2

ZBT® (Zero Bus Turnaround®) RAMs

8M	512K x 18	3.3 V	MCM63Z918	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
			MCM63Z916	100 119	(TQ) TQFP (ZP) PBGA	10 / 11 / 15 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
		2.5 V	MCM64Z918	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
			MCM64Z916	100 119	(TQ) TQFP (ZP) PBGA	10 / 11 / 15 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
	256K x 36	3.3 V	MCM63Z836	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
			MCM63Z834	100 119	(TQ) TQFP (ZP) PBGA	10 / 11 / 15 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
		2.5 V	MCM64Z836	100 119	(TQ) TQFP (ZP) PBGA	7 / 8 / 8.5 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
			MCM64Z834	100 119	(TQ) TQFP (ZP) PBGA	10 / 11 / 15 ns Latency	1Q00	Pipelined or flow–through with back–to–back read/write write/read cycles. Sampling 4Q99.
4M	256K x 18	3.3 V	MCM63Z818	100	(TQ) TQFP	143 / 133 / 100 MHz	Now	Pipelined with back–to–back read/write write/read cycles. Being replaced by MCM63Z818K.
			MCM63Z819	100	(TQ) TQFP	10 / 11 / 15 ns	Now	Flow–through with back–to–back read/write write/read cycles. Being replaced by MCM63Z819K.
			MCM63Z818K	100	(TQ) TQFP	143 / 133 / 100 MHz	1Q00	Pipelined with back–to–back read/write write/read cycles. Replaces MCM63Z818.
			MCM63Z819K	100	(TQ) TQFP	10 / 11 / 15 ns	1Q00	Flow–through with back–to–back read/write write/read cycles. Replaces MCM63Z819.
		2.5 V	MCM64Z818K	100	(TQ) TQFP	143 / 133 / 100 MHz	1Q00	Pipelined with back–to–back read/write write/read cycles. For low power applications.
			MCM64Z819K	100	(TQ) TQFP	10 / 11 / 15 ns	1Q00	Flow–through with back–to–back read/write write/read cycles. For low power applications.
	128K x 36	3.3 V	MCM63Z736	100	(TQ) TQFP	143 / 133 / 100 MHz	Now	Pipelined with back–to–back read/write write/read cycles. Being replaced by MCM63Z736K.
			MCM63Z737	100	(TQ) TQFP	10 / 11 / 15 ns	Now	Flow–through with back–to–back read/write write/read cycles. Being replaced by MCM63Z737K.
			MCM63Z736K	100	(TQ) TQFP	143 / 133 / 100 MHz	1Q00	Pipelined with back–to–back read/write write/read cycles. Replaces MCM63Z736.
			MCM63Z737K	100	(TQ) TQFP	10 / 11 / 15 ns	1Q00	Flow–through with back–to–back read/write write/read cycles. Replaces MCM63Z737.
		2.5 V	MCM64Z736K	100	(TQ) TQFP	143 / 133 / 100 MHz	1Q00	Pipelined with back–to–back read/write write/read cycles. For low power applications.
			MCM64Z737K	100	(TQ) TQFP	10 / 11 / 15 ns	1Q00	Flow–through with back–to–back read/write write/read cycles. For low power applications.

CAMs (Content Addressable Memory)

CAMs	16K x 64	3.3 V	MCM69C432	100	(TQ) TQFP	180 ns Match Time	Now	Content addressable memory for communication applications. 16K connections.
	4K x 64	3.3 V	MCM69C232	100	(TQ) TQFP	160 ns Match Time	Now	Content addressable memory for communication applications. 4K connections.

Tag RAMs

Tag RAMs	64K x 18	3.3 V	MCM69T618	100	(TQ) TQFP	5 ns	Now	100 MHz Data/Tag RAM. For MIPS R5000, Pentium Pro, and graphics accelerators applications. Not recommended for new designs.

SYNCHRONOUS

Integrated Cache Solutions

Description	Organization	V_{DD}	Motorola Part Number	Pin Count	Packaging	Speed	Production	Comments
Integrated Cache Solutions	32K x 72	3.3 V	MPC2605	241	(ZP) PBGA	83 / 66 MHz	Now	Integrated L2 cache for PowerPC processors. One component for 256KB, two for 512KB, and four for 1MB L2 cache solution.

Separate and Dual I/O Devices

4M	512K x 9	5 V	MCM67Q909	86	(ZP) PBGA	10 / 12 ns	Now	General synchronous separate I/O with write pass through. 3.3 V output levels. Not recommended for new designs.
	128K x 36	3.3 V	MCM63D736	176	(TQ) TQFP	100 / 133 MHz	1Q00	Dual address, Dual I/O NetRAM pipelined per port chip enable.
1M	128K x 9	5 V	MCM67Q709A	86	(ZP) PBGA	10 ns	Now	General synchronous separate I/O with write pass through. 3.3 V output levels. Not recommended for new designs.
	32K x 36	3.3 V	MCM69D536	176	(TQ) TQFP	6/8 ns	Now	Dual address, dual I/O. NetRAM.
	64K x 18	3.3 V	MCM69D618	100	(TQ) TQFP	6/8 ns	Now	Dual address, dual I/O. NetRAM.

2

ASYNCHRONOUS

Description	Organization	V_{DD}	Motorola Part Number	Pin Count	Packaging Package width in mils	Speed	Production	Comments
4M	512K x 8	3.3 V	MCM6946	36 44	400 (YJ) SOJ (TS) TSOP	10 / 12 / 15 ns	Now	Not recommended for new designs. EOL pending.
	256K x 16	3.3 V	MCM6343	44	400 (YJ) SOJ (TS) TSOP	11 / 12 / 15 ns	Now	Not recommended for new designs.
	1M x 4	3.3 V	MCM6949	32	400 (YJ) SOJ	10 / 12 /15 ns	Now	Not recommended for new designs. EOL pending.
3M	128K x 24	3.3 V	MCM6341	119	(ZP) PBGA	10 / 11 / 12 /15 ns	Now	DSP applications for base stations and other communication applications. Industrial temperature available.
1M	64K x 18	5 V	MCM67A618A	52	(FN) PLCC	10 / 12 / 15 ns	Now	Not recommended for new designs. Use MCM67A618B.
			MCM67A618B	52	(FN) PLCC	TBD	Now	General asynchronous, latched address and data.
	128K x 8	3.3 V	MCM6926A	32	400 (WJ) SOJ	8 / 10 / 12 /15 ns	Now	EOL Status – Last Purchase January 2000.
	256K x 4	3.3 V	MCM6929A	32	400 (WJ) SOJ	8 / 10 / 12 /15 ns	Now	EOL Status – Last Purchase January 2000.

APPLICATION NOTES

Description	Document Number
Using Motorola's Dual Port NetRAMs for Interprocessor Communication in a Datacomm Application	AN1807
Using the MCM69D536/MCM69D618 NetRAMs with Different Speed Computing Elements	AN1779
MPC8xx to BurstRAM Interfacing	AN1777
ZBT Primer	AN1773
BurstRAM to ZBT RAM	AN1729
Configuring the MPC2605 Integrated L2 Cache with the MPC106	AN1265
Switch Fabric Implementation Using Shared Memory	AN1704
Using Motorola's Fast Static RAM CAMs on a Media Independent Interface	AN1726
Using the MCM69C232/MCM69C432 Content–Addressable Memory on an ATM Line Card	AN1296
Dual Port Memory for Multiprocessor Applications	AN1707
Plastic Ball Grid Array (PBGA)	AN1231
DSP5630x FSRAM Interfacing	AN1268
DSP5630x FSRAM Module Interfacing	AN1289
Output Loading Effects on Fast Static RAMs	AN1243
Thermal Performance of Plastic Ball Grid Array (PBGA) Packages for Next Generation FSRAM Devices	AN1232
The Motorola BurstRAM	AN1209

For additional information on FSRAM products: http://motorola.com/fastsrams

2

ATM

In Brief . . .

Asynchronous Transfer Mode (ATM) is the communications protocol for the new broadband, full–service network. It can transmit voice, video, and data simultaneously to enable the deployment of broadband services such as high–speed Internet access, LAN interconnect for telecommuters, and video–on–demand.

Today's end–users, information technology, and telecommunication managers are searching for ways to save on network deployment and usage costs while meeting efficiency and quality requirements. In addition, they want to have cost–effective access to broadband resources when they need them, regardless of traffic type.

Operators, who are being asked to maximize their usage of resources, want to avoid congestion while sharing network resources. Further, they need a way to fulfill differing customer needs with cost–effective, selectable cost/performance levels. Motorola's 92500 Family of ATM cell processors was designed with the needs of these groups in mind.

The 92500 ATMC Family offers advanced ATM functionality for a variety of applications such as DSLAMS (Digital Subscriber Line Access Multiplexes), WAN and Enterprise Switches, and Multi–Service Platforms.

ATM Network

ATM Network Description

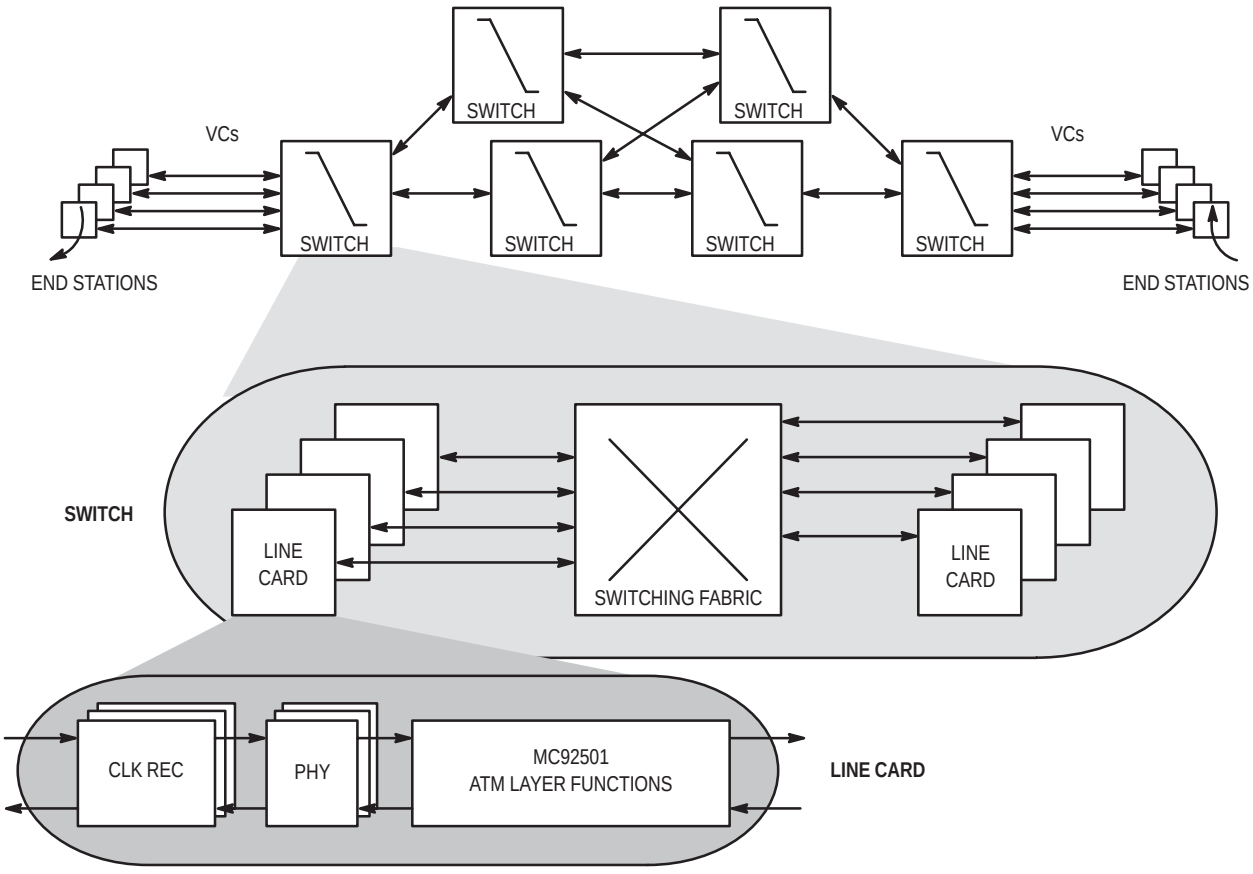
A typical ATM network consists of user end stations that transmit and receive 53–byte data cells on virtual connections (see figure below). Physical links and switching systems interconnect the virtual connections. A virtual connection's path is established at the beginning of the data transfer, maintained while the end–stations are communicating, and torn down after the transfer is complete. This transmission method increases the transfer speed because the determination of the path the data will take is done only at the beginning of the data transfer instead of when each data sub–block or packet is transferred.

On a given physical link, each connection is assigned a unique connection identifier. The connection identifier is placed in the header of each cell by the transmitting equipment and is used by the receiving equipment to route the cell to the next physical link on the connection path. All cells belonging to a specific virtual connection follow the identical path from the transmitting end station through the switching systems to the receiving end station.

An ATM switch contains a high–speed switching fabric that connects multiple line cards. The switching fabric connects the input port to the output port based on the switch's routing table. The line card interfaces between the physical medium and the switching fabric by recovering incoming cells from the arriving bit stream or converting outgoing cells into a bit stream for transmission. An ATM swtich partitioned in this fashion can efficiently handle multiple physical links by independently transferring each incoming ATM cell from its source port to its destination port, based on the switch's routing table.

ATM standards divide the tasks to be performed on each side of the switch fabric into PHY layer and ATM layer tasks. The PHY layer tasks are dependent on the physical medium that connects ATM switches. The ATM layer tasks operate at the cell level and are independent of the physical medium.

MC92501 IN AN ATM NETWORK APPLICATION



ATM Cell Processor

MC92501
Case 1208

The MC92501 is an ATM layer device composed of dedicated high–performance ingress and egress cell processors combined with UTOPIA Level 2–compliant physical (PHY) and switch interface ports (see Block Diagram). The MC92501 is a second generation ATM cell processor in Motorola's 92500 series.

Features of the MC92501

The MC92501 integrates address translation, UPC/NPC, OAM, and statistical functions into a single semiconductor device. By incorporating the standardized functions of the switch, the ATMC can reduce the switch's design cycle time, while allowing the customer to differentiate the product.

General Features

- Full–Duplex Operation at Data Rates up to 155 Mbit/sec
- Implements ATM Layer Functions for Broadband ISDN According to ATM Forum UNI 4.0 and TM 4.0 Specifications, ITU Recommendations, and Bellcore Recommendations

OAM (Operations, Administration, and Management)

- Performance Monitoring Block Test on All 64K Connections
- Fault Management Functions (AIS, RDI, CC, and Loopback)
- OAM Functionality Operates in Both the Ingress and Egress Directions

UPC/NPC (Usage/Network Parameter Control)

- Supports Partial Packet Discard (PPD), Early Packet Discard (EPD), and Limited EPD
- Change ABR RM Cell Priority
- Bidirectional UPC or NPC Design with up to Four Leaky Buckets Per Connection
- Selective Discard CLP = 1 (or CLP = 0 + 1) Flow on Selected Connections
- Support for CLP Transparency

ATM Interfaces

- UTOPIA Level 2 PHY Interface and UTOPIA ATM Layer Interface
- Supports a Programmable Number (up to 11 bytes) of Additional Switch Overhead Routing Header
- Each Physical Link Can Be Configured as Either a UNI or NNI Port
- Programmable 32–Bit Microprocessor Interface Supporting Big–Endian or Little–Endian Bus Formats

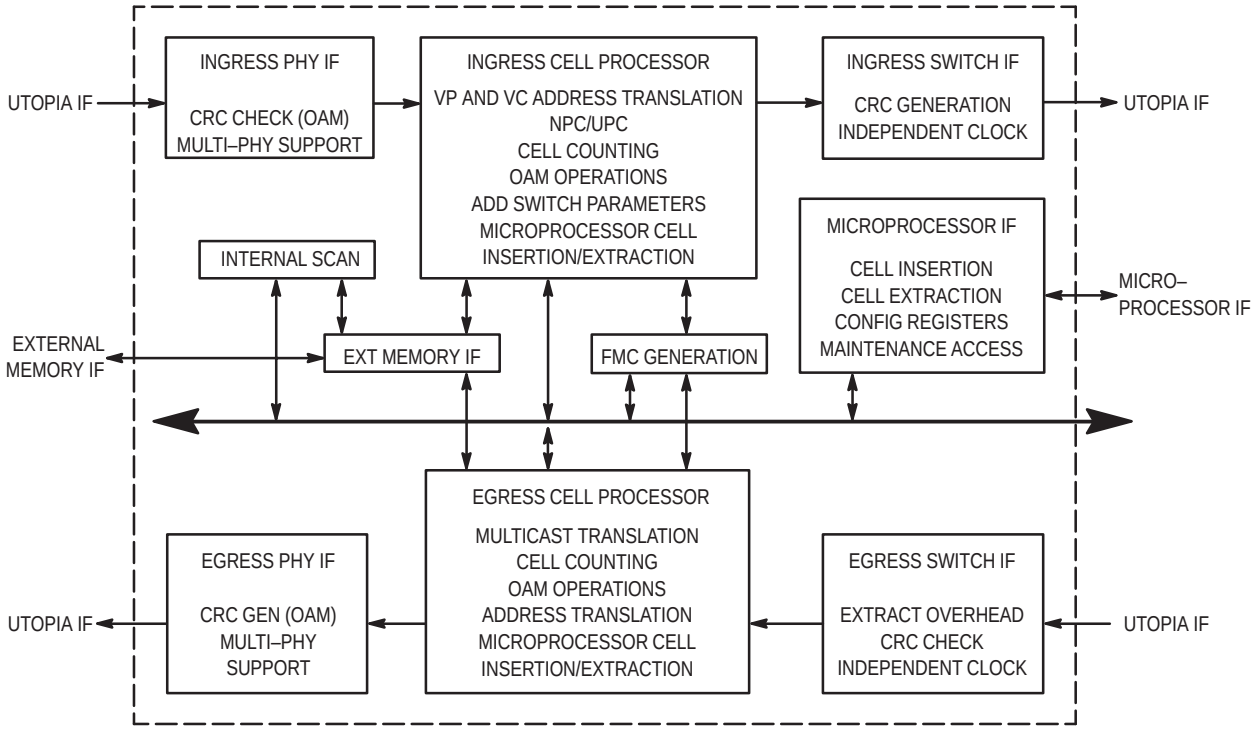
Statistics

- Per VC Counters
- Per PHY Counters

Address Translation

- Performs Internal VPI and VCI Address Compression for up to 64K VCs
- Supports Multicast, Multiport Address Translation

REPRESENTATIVE BLOCK DIAGRAM



2

ATMC Evaluation Board

MC92501EVB

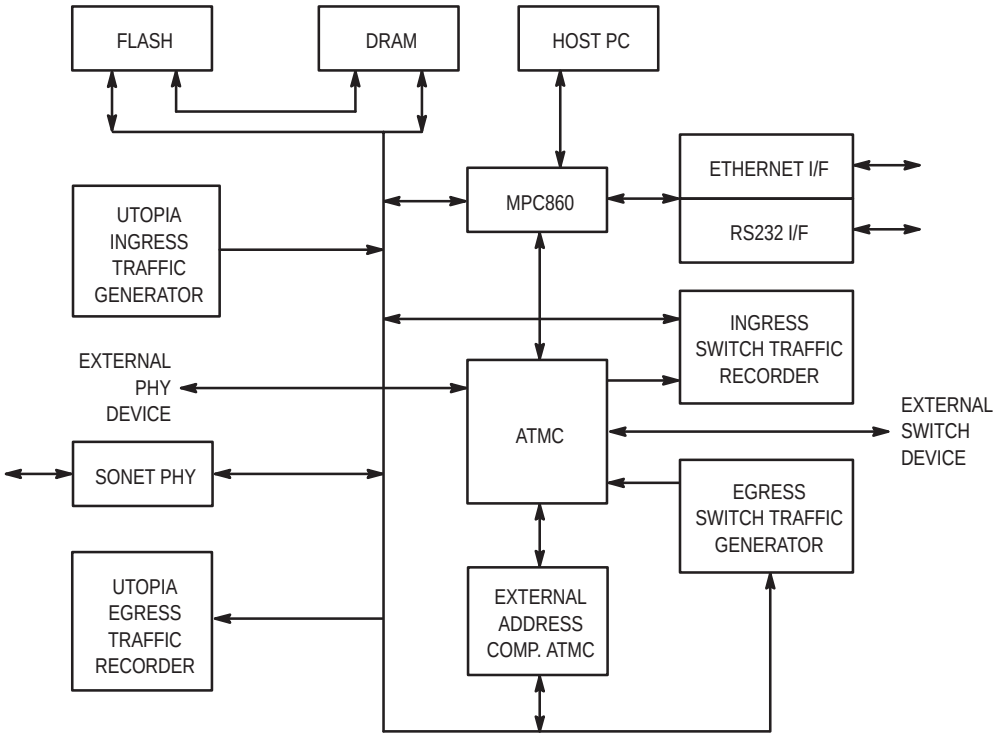
Motorola's ATMC Evaluation Board (MC92501EVB) is a powerful tool designed to help reduce time to market for ATM switching products. The MC92501EVB includes the functions on a typical ATM line card, allowing switch designers to begin software development before their hardware has been completed. The evaluation board contains traffic generators and receivers, as well as standard ATM interfaces, so that external data path devices can be connected. In addition, the board contains a host port interface for board configuration. This combination of features enables designers to evaluate their products and perform testing.

General Features

- SONET PHY
- UTOPIA Ingress Traffic Generator
- Ingress Switch Traffic Controller
- Egress Switch Traffic Generator
- UTOPIA Egress Traffic Recorder
- External Switch Device
- ATMC External Address Compression

2

FUNCTIONAL BLOCK DIAGRAM



2

Communication and Interface Circuits

In Brief . . .

COMMUNICATION CIRCUITS
Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems: telecommunications and data communications. Each had its individual hardware components complement, and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coaxial cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and use a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola Semiconductor serves a wide range of requirements for the voice/data marketplace. We offer both CMOS and Analog technologies, each to its best advantage, to upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid–state single–chip crosspoint switch, the more recent monolithic Subscriber–Loop–Interface Circuit (SLIC), a single–chip Codec/Filter (Mono–Circuit), the Universal Digital Loop Transceivers (UDLT), basic rate ISDN (Integrated Services Digital Network), Asymmetric Digital Subscriber Line (ADSL), and single–chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

INTERFACE CIRCUITS

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing with microprocessor or digital systems and the external world, or to other systems.

The line drivers, receivers, and transceivers permit communication between systems over cables of several thousand feet in length, and at data rates of up to several megahertz.

Telecommunications

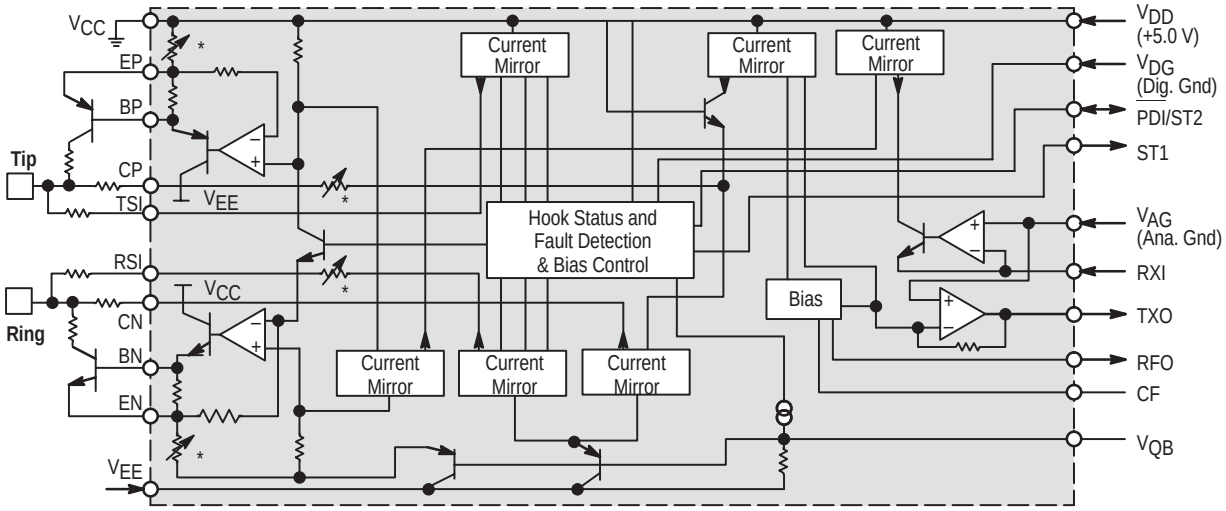
Subscriber Loop Interface Circuit (SLIC)

MC33121P, FN
T_A = –40° to +85°C, Case 738, 776

With a guaranteed minimum longitudinal balance of 58 dB, the MC33121 is ideally suited for Central Office applications, as well as PBXs, and other related equipment. Protection and sensing components on the two–wire side can be non–precision while achieving required system performance. Most BORSHT functions are provided while maintaining low power consumption, and a cost effective design. Size and weight reduction over conventional transformer designs permit a higher density system.

- All Key Parameters Externally Programmable with Resistors:
  - Transmit and Receive Gains
  - Transhybrid Loss
  - Return Loss
  - DC Loop Current Limit and Battery Feed Resistance
  - Longitudinal Impedance
- Single and Double Fault Sensing and Protection
- Minimum 58 dB Longitudinal Balance (2–wire and 4–wire) Guaranteed
- Digital Hook Status and Fault Outputs
- Power Down Input
- Loop Start or Ground Start Operation
- Size & Weight Reduction Over Conventional Approaches
- Available in 20 Pin DIP and 28 Pin PLCC Packages
- Battery Voltage: –21.6 to –42 V

3



*Indicates Trimmed Resistor

Short Loop Dual PCM Codec–Filter/SLIC Chipset with GCI

MS140131KT (Includes MC1420232 and MC1430132)
Case 751F, 824D

The MS140131KT chipset provides all the functions necessary to connect analog telephone sets or other analog terminals (telefax, answering machines, modems, etc.) into digital communication systems. It provides an economical solution for the traditional "BORSHT'' functions found in central–office exchanges, but is optimized for short–range communication (e.g., up to 500 m with four RENs attached). Virtually all system–dependent parameters can be set under software control, giving a hitherto unprecedented flexibility to the system integrator, as well as optimizing the system cost. The digital interface to the SH POTS chipset uses the industry–standard "GCI'' interface.* The system architecture has been designed to offer the most cost–effective solution for short–haul systems, yet offers the full flexibility required to meet world–wide analog telephony standards. Suitable for Q.552 applications.

The MS140131KT chipset comprises three devices (see the Block Diagram): a pair of high–voltage devices, the Short–Haul Line Interface Circuit (SH LIC) which provides the signal and power interface to the analog lines (one per line) and a low–voltage CMOS, DSP–based dual codec/control device (CODSP) which provides all signal processing and control functions for up to two lines.

Key Features

- Digitally Programmed Transmission and Signalling Characteristics Meets World–Wide Specification Requirements
- Integrated Ringing: Sine or Trapezoid
- Metering Injection
- Battery Reversal
- Tone Generators for Signalling and Test
- Minimal External Components
- Codec and SLIC Functions for Two Lines
- Low–Cost POTS Interface for Short Range
- Standard GCI Interface

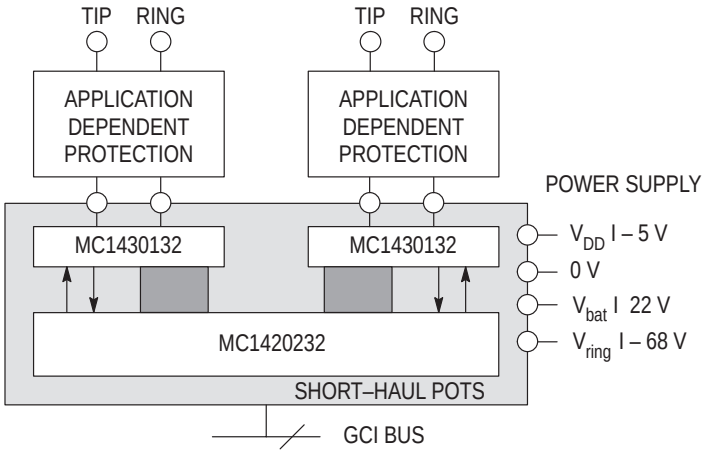
Applications

- Advanced ISDN NT (NTplus)
- Analog/Digital PABX
- Cable Telephone Systems (Set–Top Box)
- Remote Telephone Access Systems
- Fibre to the Curb
- Radio in the Loop
- Internet Telephones

*The General Circuit Interface (GCI) is an interface specification developed jointly by Alcatel, Italtel, GPT and Siemens; date March 1989; issue 1.0.

3

BLOCK DIAGRAM



PBX Architecture (Analog Transmission)

PCM Monocircuits Codec–Filters (CMOS LSI)

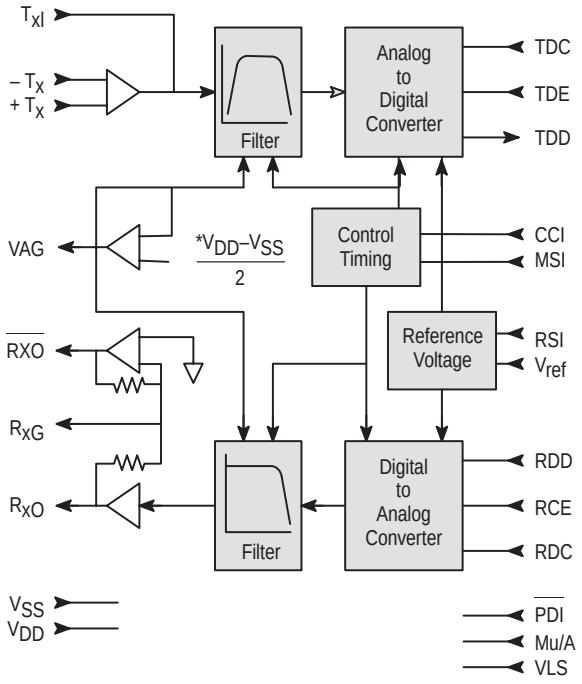
MC145500 Series

Case 648, 708, 751G, 776

The Monocircuits perform the digitizing and restoration of the analog signals. In addition to these important functions, Motorola's family of pulse–code modulation monocircuits also provides the band–limiting filter functions – all on a single monolithic CMOS chip with extremely low power dissipation.

The Monocircuits require no external components. They incorporate the bandpass filter required for antialiasing and 60 Hz rejection, the A/D–D/A conversion functions for either U.S. Mu–Law or European A–Law companding formats, the low–pass filter required for reconstruction smoothing, an on–board precision voltage reference, and a variety of options that lend flexibility to circuit implementations. Unique features of Motorola's monocircuit family include wide power supply range (6.0 to 13 V), selectable on–board voltage reference (2.5, 3.1, or 3.8 V), and TTL or CMOS I/O interface.

Motorola supplies three versions in this series. The MC145503 and MC145505 are general–purpose devices in 16 pin packages designed to operate in digital telephone or line card applications. The MC145502 is the full–feature device that presents all of the options available on the chip. This device is packaged in a 22 pin DIP and 28 pin chip carrier package.



MC145506

Case 708, 736

The MC145506 is a per channel codec–filter PCM mono–circuit. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. It has HCMOS compatible digital outputs and otherwise supplements the MC145500 – MC145505 series of PCM Codec–Filters. The MC145506 is functionally similar to the MC145502. It is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage. The MC145506 is offered in a 22–pin package and has the capability of selecting from three peak overload voltages (2.5, 3.15, and 3.78 V). Most of the features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

The MC145506 maintains compatibility with Motorola's family of TSACs and MC3419/MC33120 SLIC products.

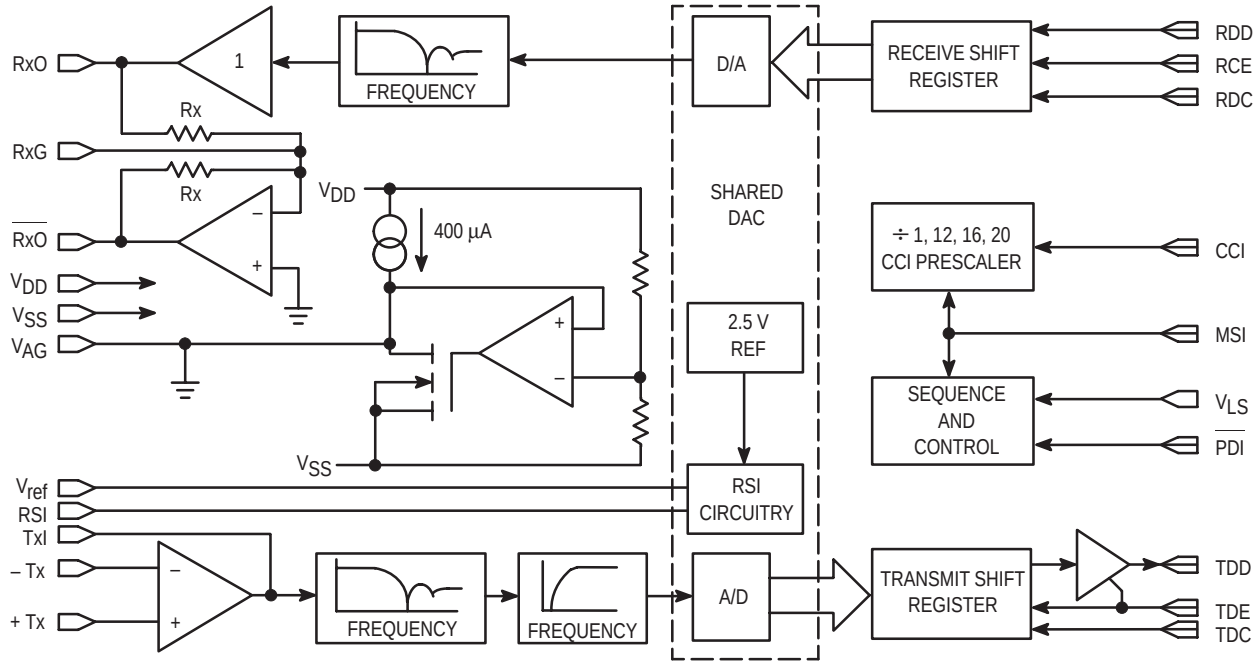
The MC145500 family of PCM Codec–Filter mono–circuits utilize CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

MC145506 (22–Pin Package, HCMOS Output Version of MC145502)

- Selectable Peak Overload Voltages (2.5, 3.15, 3.78 V)
- Push–Pull Analog Output with Gain Adjust
- 64 kHz to 4.1 MHz Transmit and/or Receive Data Clock Rate
- Transmit Bandpass and Receive Low–Pass Filters on Chip
- Pin Selectable Mu/A Law Companding with Corresponding Data Format
- On–Chip Precision Reference Voltage (3.15 V)
- Power Dissipation of 50 mW, Power Down of 0.1 mW at ± 5 V
- Three Terminal Transmit Input Operational Amplifier
- Automatic Prescaler Accepts 128 kHz, 1.536, 1.544, 2.048, and 2.56 MHz for Internal Sequencing
- Separate Transmit and Receive Data Clocks

PBX Architecture (continued)

MC145506 PCM CODEC–FILTER MONO–CIRCUIT BLOCK DIAGRAM



NOTES: ⊲ Controlled by V_{LS}
Rx ≈ 100 kΩ (internal resistors)

MC145554/57/64/67

Case 648, 751D, 751G, 738

These per channel PCM Codec–Filters perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision voltage reference. The MC145554 (Mu–Law) and MC145557 (A–Law) are general purpose devices that are offered in 16 pin packages. The MC145564 (Mu–Law) and MC145567 (A–Law), offered in 20 pin packages, add the capability of analog loop–back and push–pull power amplifiers with adjustable gain.

All four devices include the transmit bandpass and receive lowpass filters on–chip, as well as active RC pre–filtering and post–filtering. Fully differential analog circuit design assures lowest noise. Performance is specified over the extended temperature range of –40° to +85°C.

These PCM Codec–Filters accept both industry standard clock formats. They also maintain compatibility with Motorola's family of MC3419/MC33120 SLIC products.

MC14LC5480 Series

All devices in the MC14LC5480 series (including MC14LC5480, MC145481, MC145482, MC145483 and MC145484) are general purpose per channel PCM Codec–Filters. The MC14LC5480, MC145481 and MC145484 are pin–selectable Mu–Law or A–Law companding. The MC145482 and MC145483 are 13–bit linear PCM Codec–Filters. These devices offered in 20–pin DIP, SOIC, and SSOP packages. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. These devices are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision reference voltage.

These devices have an input operational amplifier whose output is the input to the encoder sections. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal.

3

PBX Architecture (continued)

From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by the single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of the differential design is that noise injected via the power supplies is a common–mode signal that is canceled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

The MC14LC5480EVK is the primary tool for evaluation and demonstration of the MC14LC5480 series.

MC14LC5480DW, SD

Case 751D, 940C–02

This 5.0 V PCM Codec–Filter offers the following features:

- Single 5.0 V Power Supply
- Typical Power Dissipation of 15 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage (1.575 V)
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

MC145481DW, SD

Case 751D, 940C–02

This 3.0 V PCM Codec–Filter offers the following features:

- Single 2.7 V to 5.25 V Power Supply
- Typical Power Dissipation of 8.0 mW at 3.0 V, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage of 0.886 V for a –5.0 dBm TLP at 600 Ω
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

MC145482DW, SD

Case 751D, 940C–02

This 5.0 V 13–bit linear PCM Codec–Filter offers the following features:

- Single 5.0 V Power Supply
- 13–Bit Linear ADC/DAC Conversions with 2s Complement Data Format
- Typical Power Dissipation of 25 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Trasmit High–Pass Filter May be Bypassed by Pin Selection
- Active R–C Pre–Filtering and Post–Filtering
- On–Chip Precision Reference Voltage of 1.575 V for a 0 dBm TLP at 600 Ω
- Full–Duplex Sample Rates from 7.0 to 16 k Samples/s
- 3–Terminal Input Op Amp Can Be Used, or a 2–Channel Input Multiplexer
- Receive Gain Control from 0 to –21 dB in 3.0 dB Steps in Synchronous Operation
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

MC145483DW, SD

Case 751D, 940C–02

This 3.0 V 13–bit linear PCM Codec–Filter offers the following features:

- Single 3.0 V Power Supply
- 13–Bit Linear ADC/DAC Conversions with 2s Complement Data Format
- Typical Power Dissipation of 8.0 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Trasmit High–Pass Filter May be Bypassed by Pin Selection
- Active R–C Pre–Filtering and Post–Filtering
- On–Chip Precision Reference Voltage of 0.886 V for a –5.0 dBm TLP at 600 Ω
- 3–Terminal Input Op Amp Can Be Used, or a 2–Channel Input Multiplexer
- Receive Gain Control from 0 to –21 dB in 3.0 dB Steps in Synchronous Operation
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

PBX Architecture (continued)

The MC145483 is ideal as a DSP front end. In fact, the MC145483 is used in the evaluation platform for Motorola's DSP56L811. The MC145483 makes the DSP56L811EVM evaluation platform ideal for developing and implementing many messaging and audio processing algorithms.

MC145484DW, SD

Case 751D, 940C–02

This 5.0 V PCM Codec–Filter offers the following features:

- Single 5.0 V Power Supply
- Typical Power Dissipation of 15 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage of 1.575 V for a 0 dBm TLP at 600 Ω
- Push–Pull 300 Ω Power Drivers with External Gain Adjust

PBX Architecture (continued)

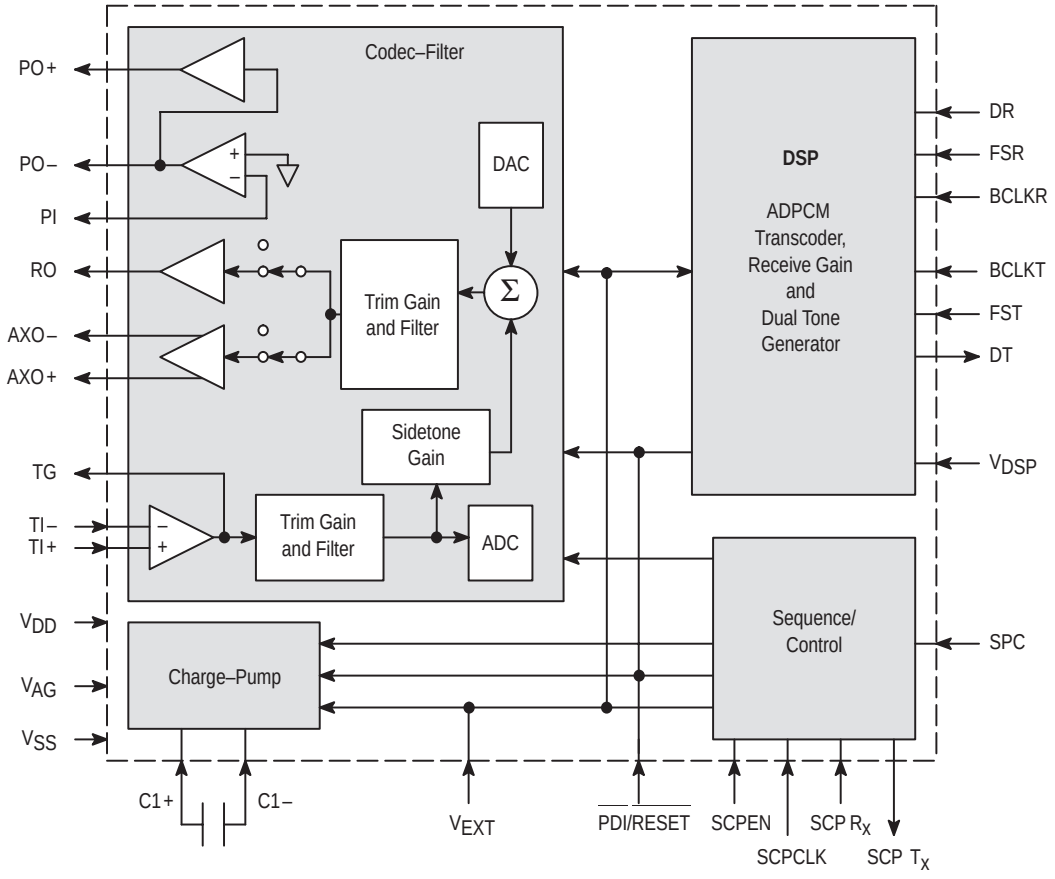
MC14LC5540P, DW, FU

Case 710, 751F, 873

The MC14LC5540 ADPCM Codec is a single chip implementation of a PCM Codec–Filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 V to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC14LC5540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 (1988) and ANSI T1.301 (1987). It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

Figure 1. MC14LC5540 ADPCM Codec Block Diagram



PBX Architecture (continued)

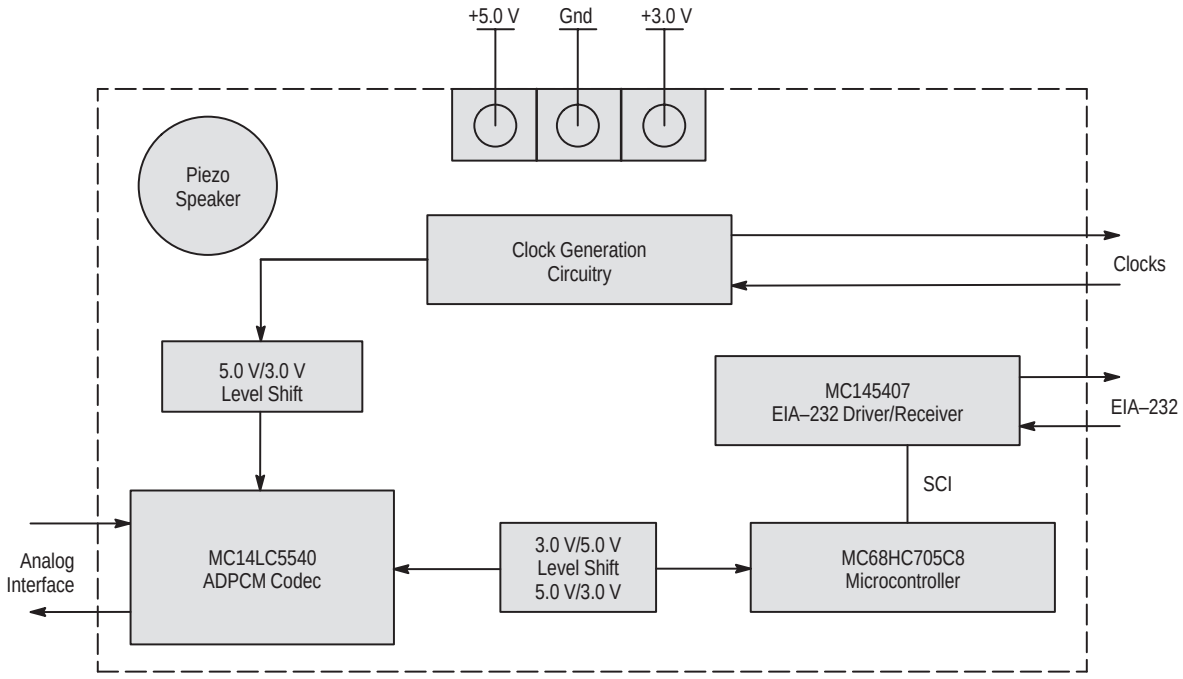
MC145537EVK

ADPCM Codec Evaluation Kit

The MC145537EVK is the primary tool for evaluation and demonstration of the MC14LC5540 ADPCM Codec. It provides the necessary hardware and software interface to access the many features and operational modes of the MC14LC5540 ADPCM Codec.

- Provides Stand Alone Evaluation on Single Board
- The kit provides Analog–to–Analog, Analog–to–Digital or Digital–to–Analog Connections – with Digital Connections being 64 kbps PCM, 32 or 24 kbps ADPCM, or 16 kbps CCITT G.726 or Motorola Proprietary ADPCM
- +5.0 V Only Power Supply, or 5.0 V Plus 2.7 to 5.25 V Supply
- Easily Interfaced to Test Equipment, Customer System, Second MC145537EVK or MC145536EVK (5.0 V Only) for Full Duplex Operation
- Convenient Access to Key Signals
- Piezo Loudspeaker
- EIA–232 Serial Computer Terminal Interface for Control of the MC14LC5540 ADPCM Codec Features
- Compatible Handset Provided
- Schematics, Data Sheets, and User's Manual Included

Figure 2. MC145537EVK Block Diagram



3

PBX Architecture (continued)

MC14LC5480EVK

PCM Codec–Filter Evaluation Kit

The MC14LC5480EVK is the primary tool for evaluation and demonstration of the following PCM and linear codec–filters.

Table 1. Mu/A–Law and Linear PCM Codec–Filters

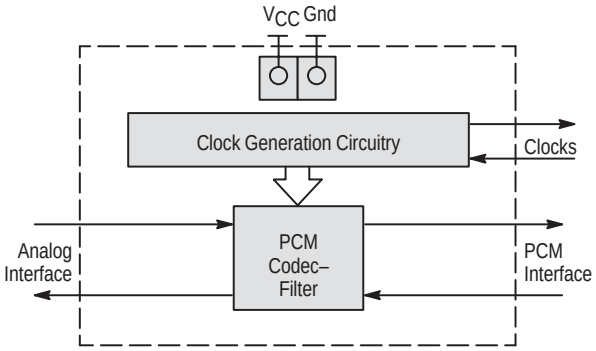
Part Number	V_{CC}	Description
MC14LC5480	5.0 V	Mu/A–Law Companding
MC145481	3.0 V	Mu/A–Law Companding
MC145482	5.0 V	13–Bit Linear
MC145483	3.0 V	13–Bit Linear
MC145484	5.0 V	Mu/A–Law Companding

Figure 3. is a functional block diagram of the MC14LC5480EVK. The MC14LC5480EVK is comprised of two functional blocks — the clocking circuitry, and one of the PCM Codec–Filters listed in Table 1.

User I/O to the board is provided via a number of convenient connectors. First, an industry standard 4–pin RJ11 handset jack (P1) is provided to connect the handset included with the kit. Next, a 2x20 pin header (P13) is provided for access to key analog and digital signals for connection to external test equipment, a user defined system, or a second MC14LC5480EVK. And finally, two male BNC connectors (P6 and P14) provide convenient access to the codec's analog transmit and receive paths for connection to external test equipment.

The MC14LC5480EVK requires either a 5.0 V or 3.0 V supply provided through P2 at the top of the circuit board.

Figure 3. MC14LC5480EVK Functional Block Diagram



- Provides Standalone Evaluation on a Single Board
- Single 5.0 V or 3.0 V Power Supply
- Easily Interfaced to Test Equipment, Customer System, or Second MC14LC5480EVK
- Convenient Access to Key Signals
- Generous Wire Wrap Area for Application Development
- Kit Provides Analog–to–Analog, Analog–to–Digital, and Digital–to–Analog
- Compatible Handset Provided
- Kit Includes: Schematics, Data Sheets, User's Manual, and Samples of Each PCM Codec–Filter

Dual Tone Multiple Frequency Line Interface

MC145740F

Case 751J

The MC145740 is a silicon gate HCMOS LSI designed for general purpose Dual Tone Multiple Frequency (DTMF) communications, and contains a DTMF signal generator and a receiver for all 16 standard digits.

The generator block has a differential line driver which drives a 600 Ω load with 0 dBm level. The transmit signal level is adjusted in 1 dB steps by the programmable attenuator.

The receiver block has an Auto Gain Control (AGC) amplifier to demodulate 50 dB (typ) dynamic range of DTMF signals to the hexadecimal codes.

The device also includes a serial control interface that permits a CPU to exercise the following built–in features.

- Single Power Supply: 3.6 to 5.5 V
- DTMF Generator and Receiver for All 16 Standard Digits
- 0 dBm Line Driver Into 600 Ω Load
- AGC Amplifier
- Programmable Transmit Attenuator
- Serial Control Interface
- Power Down Mode, Less Than 1 μA

ISDN Voice/Data Circuits

Integrated Services Digital Network

ISDN is the revolutionary concept of converting the present analog telephone networks to an end–to–end global digital network. ISDN standards make possible a wide variety of services and capabilities that are revolutionizing communications in virtually every industry.

Motorola's ISDN product family includes the MC145572 U–Interface Transceivers, MC145574 S/T–Interface Transceivers, MC145576 ISDN Single–Chip NT1, and the MC68302 Integrated Multi–Protocol Processor family. These are supported by a host of related devices including the MC14LC5480 +5.0 V PCM Codec–Filter, MC14LC5540 ADPCM Codec, MC145500 family of single–chip codec/filters, MC145745 V.21/V.23 single–chip modem with DTMF generator and receiver, MC34129 Switching Power Supply Controller, and the MC145406/07 CMOS EIA 232–E Driver/ Receiver family.

Motorola's key ISDN devices fit into four ISDN network applications: a digital subscriber line card, an NT1 network termination, an ISDN terminal adapter, and an ISDN terminal. Digital subscriber line cards are used in central offices, remote concentrators, channel banks, T1 multiplexers, and other switching equipment. The NT1 network termination block illustrates the simplicity of remote U– to S/T–interface conversion. The ISDN terminal adapter and ISDN terminal block show how Motorola ICs are used to combine voice and data in PC compatible boards, digital telephones, and other terminal equipment. Expanded applications such as a PBX may include these and other Motorola ISDN circuits. Many "non–ISDN" uses, such as pairgain applications, are appropriate for Motorola's ISDN devices as well.

Second Generation U–Interface Transceivers

MC145572PB
Case 824D

MC145572FN
Case 777

The MC145572 fully conforms to ANSI T1.601–1992, the North American standard and ETSi ETR080, the European standard for ISDN Basic Access on a single twisted–wire pair. The transceiver achieves a remarkable 10^{-7} bit error rate performance on all ANSI and ETSi specified test loops with worst–case impairments present. The state–of–the–art 0.65 micron single–chip solution uses advanced design techniques to combine precision analog signal processing elements with three digital signal coprocessors to build an adaptively equalized echo cancelling receiver.

Two modes of handling U–interface maintenance functions are provided on the MC145572. In the automatic maintenance mode the U–interface transceiver handles all ANSI specified maintenance and channel procedures internally to minimize your software development effort. Automatic procedures include generating and monitoring the cyclic redundancy check, reporting and counting far end block errors (near end block errors too), handling the ACT and DEA bits, as well as monitoring and appropriately responding to embedded operations channel messages.

The MC145572 has 275 mW maximum power dissipation. It also has an enhanced TDM interface that supports an on–chip timeslot assigner, GCI and IDL modes of operation.

The optional manual maintenance mode lets you choose an inexpensive microcontroller, such as a member of Motorola's MC68HC05 family, to control and augment the standard maintenance channel functions. This flexible feature also allows for easy implementation of proprietary maintenance functions.

Second Generation S/T–Interface Transceivers

MC145574PB
Case 873A

MC145574DW
Case 751F

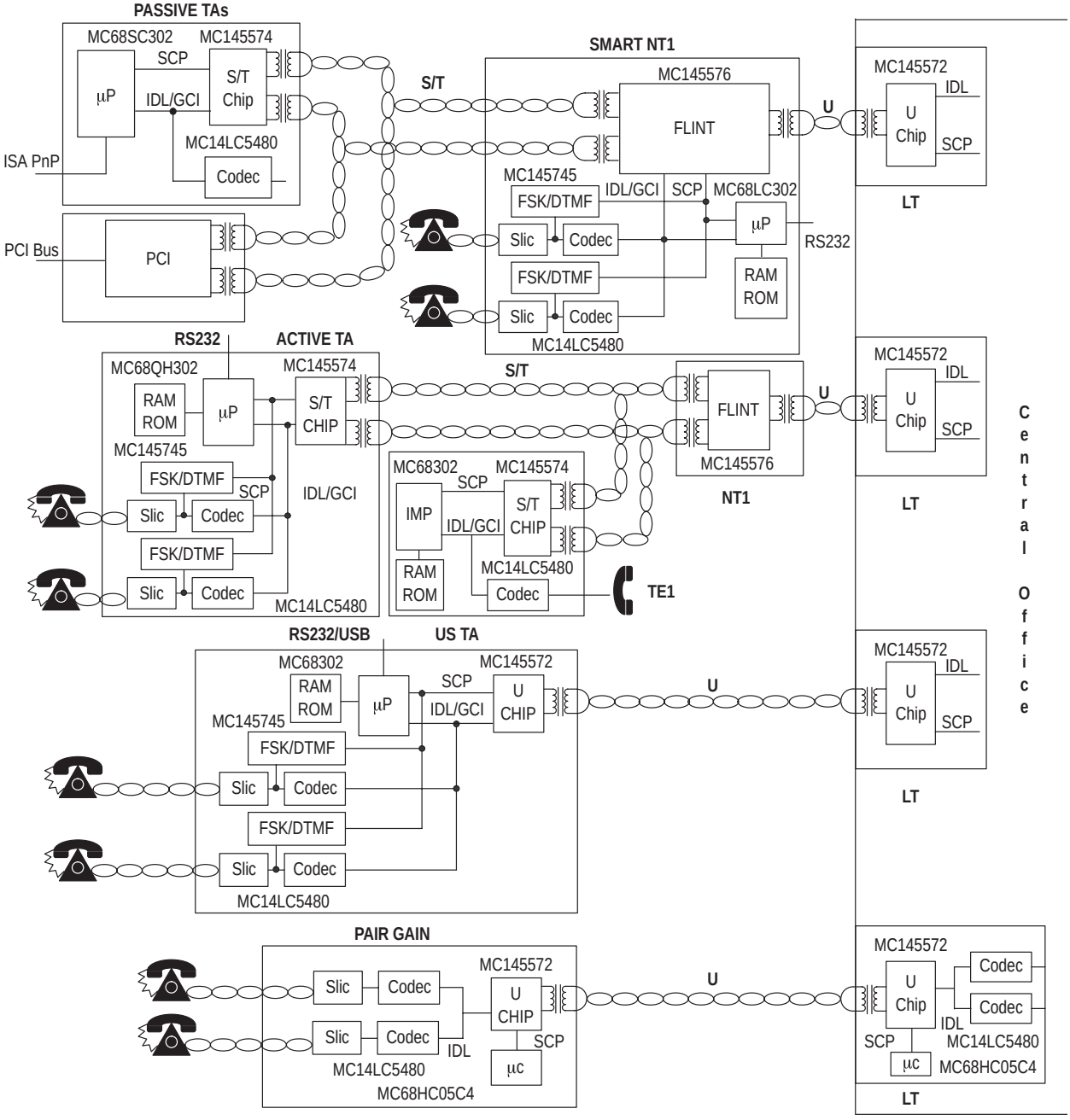
The MC145574 S/T–Interface Transceivers provide a CCITT I.430 compatible interface for use in line card, network termination, and ISDN terminal equipment applications. Manufactured with Motorola's advanced 0.65 micron CMOS mixed analog and digital process technology, the MC145574 is a physical layer device capable of operating in point–to–point or point–to–multipoint passive bus arrangements. In addition, the MC145574 implements the optional NT1 Star topology, NT terminal mode and TE slave mode.

ISDN Voice/Data Circuits (continued)

This device features outstanding transmission performance. It reliably transmits over 1 kilometer in a point–to–point application. Comparable performance is achieved in all other topologies as well. Other features include pin selectable terminal or network operating modes, industry standard microprocessor serial control port, full support of the multiframing S and Q channels, a full range of loopbacks, and low power CMOS operation, with a maximum power consumption of 90 mW.

The MC145574 has an enhanced TDM interface that supports GCI, IDL and an on–chip timeslot assigner.

The Motorola ISDN Solution



ISDN Voice/Data Circuits (continued)

ISDN Single–Chip NT1

MC145576PB

Case 824D

The ISDN Single–Chip NT1 offers the most cost–effective solution for the design of Network Termination Equipment. It has a flexible interface, making it compatible with other Motorola ISDN components. When combined with Motorola's controller family, the MC145576 becomes the heart of a powerful and cost–effective Smart NT1 solution.

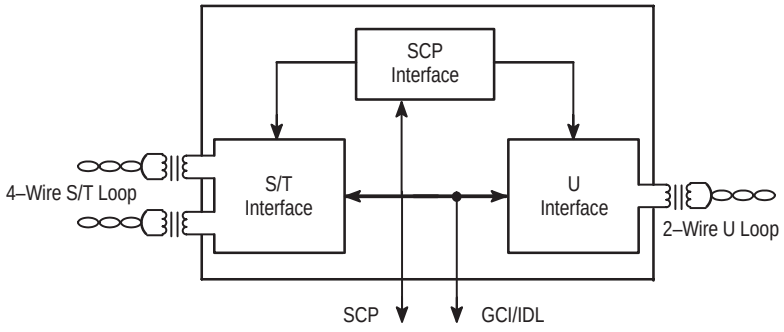
The MC145576 integrated NT1 fully complies with the appropriate USA and European recommendations for the U–interface — ANSI T1.601 1992, ETSI ETR 080, FT CS3211 in NT mode — and the S/T–interface — ITU I.430, ANSI T1.605, ETSI ETS 300 012 in NT mode.

The U–interface uses 2B1Q line coding. The device offers both GCI and IDL/SCP interfaces for compatibility with previous designs based upon the MC145574 S/T–Interface Transceiver and the MC145572 U–Interface Transceiver chip set. The SCP serial interface allows connection to the extensive family of Motorola controllers.

When combined with a member of the MC68302 family of multiprotocol controllers, MC145484 PCM codec, and an analog line interface (SLIC), the MC145576 enables optimal design of a Smart NT1 or a Smart Terminal Adapter (U–interface based TA with an S/T bus access). The same architecture can be used with a second codec and SLIC to allow for a dual analog interface design.

3

Block Diagram



Features

- Fully–conformant U– and S/T–interfaces, meets and exceeds all loop performance requirements according to U.S. and European standards
  - U–interface: ANSI T1.601 1992, ETSI ETR 080, FT CS3211
  - S/T–interface: ITU I.430, ANSI T1.605, ETSI ETS 300 012
- Supports micro–linebreaks per ETSI standard
- Flexible system interface, pin–selectable (IDL + SCP) or GCI interface
- NT terminal interface
- Fully–automatic activation in GCI mode
- Automatic handling of basic maintenance functions
- Warm start capability
- NT synchronizes to and operates with 80 kHz+/–32 ppm received signal from LT
- Automatic internal compliance with Embedded Operation Channel (EOC) Protocol, as specified in ANSI and ETSI standards
- Dedicated pins for
  - Pulse test signal generation
  - Power Mode Select PS 1/2
  - Fixed/adaptive timing selection for S bus
  - Loopback active
  - LED activation
- Complete set of loopbacks
- Low power consumption (250 mW typical)
- Single 5 V power supply
- S and Q multiframe capability via external microcontroller connection
- High–performance CMOS process technology
- Compatible with 3 V devices

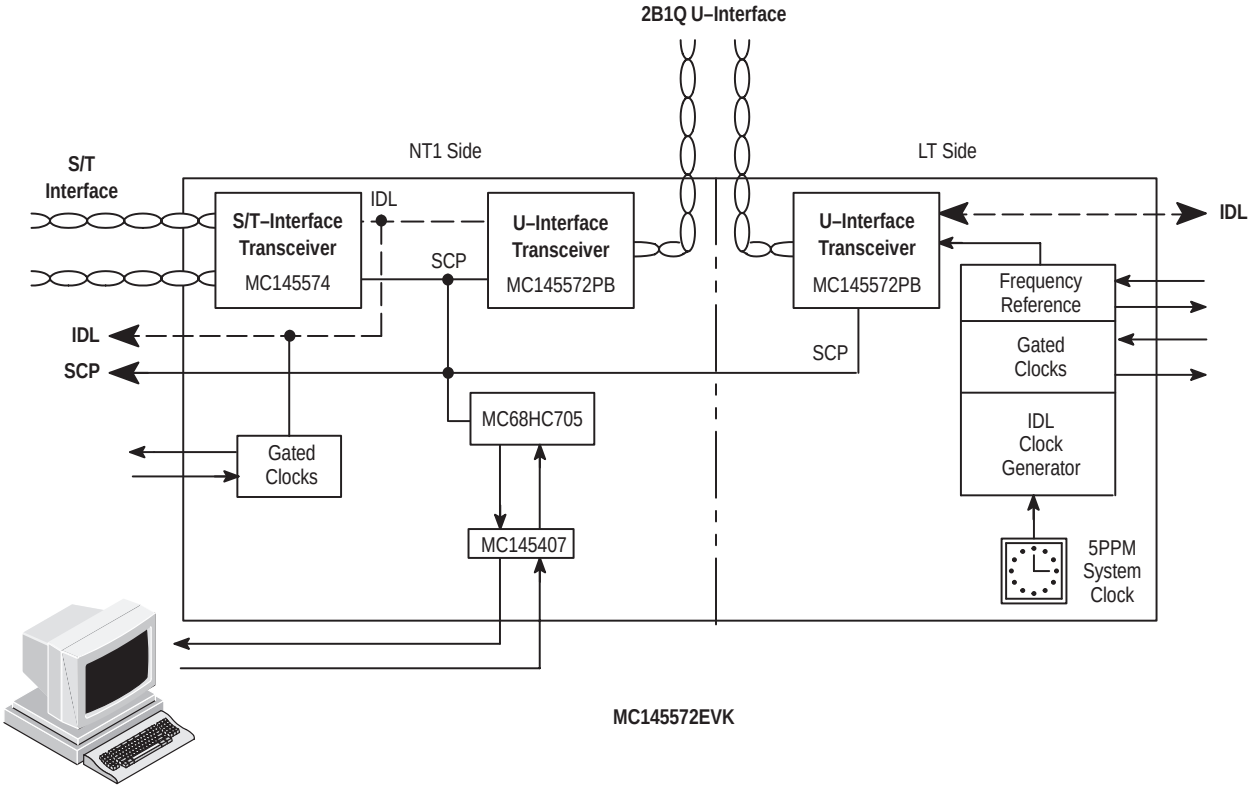
ISDN Voice/Data Circuits (continued)

U–Interface Transceiver Evaluation Kit

MC145572EVK

This kit provides the hardware and software to evaluate the many configurations under which the MC145572EVK is able to operate. Used as a whole, it operates as both ends of the two–wire U interface that extends from the customer premises (NT1) to the switch line card (LT). The board can be functionally separated, providing independent NT1 and LT evaluation capability.

The kit provides the ability to interactively manipulate status registers in the MC145572EVK U–Interface transceiver or in the MC1455574S/T–Interface transceiver with the aid of an external terminal. The device can also be controlled using the MC68302 Integrated Multiprotocol Processor application development system to complete a total Basic Rate ISDN evaluation solution.



MC145572EVK

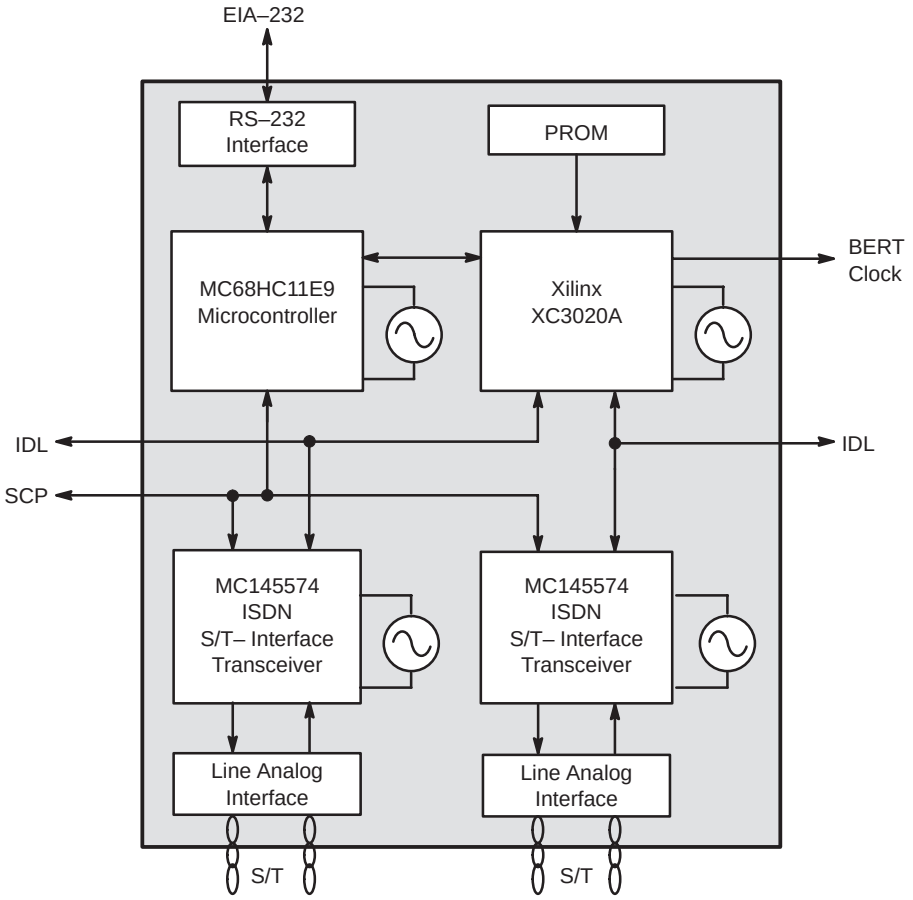
ISDN Voice/Data Circuits (continued)

ISDN S/T–Interface Evaluation Kit

MC145574EVK

The MC145574EVK S/T–Interface Transceiver Evaluation Kit provides a convenient and efficient vehicle for evaluation of the MC145574 ISDN S/T–Interface Transceiver. The Kit consists of two complete S/T–interfaces, either of which is programmable as the TE (Terminal Equipment) or NT (Network Termination) side. The EVK does not terminate ISDN call control messages.

The on–board controller and firmware enables the interactive manipulation of status registers in the transceivers with the aid of an external terminal.



MC145574EVK Features:

General

- On–board Microcontroller with resident Monitor software
- Convenient access to key signals
- NT and TE Software Development Platform

Hardware

- Gated data clocks provided for Bit Error Rate testing
- Supports S/T–Interface Terminal development
- EIA–232 (V.28) serial port for Terminal interface
- Single 5 V supply

Software

- Resident Firmware Monitor for user control
- Activation and Deactivation menus
- MC68HC11 Assembly Language Source Code available

ISDN Voice/Data Circuits (continued)

ISDN Single Chip NT1 Evaluation Kit

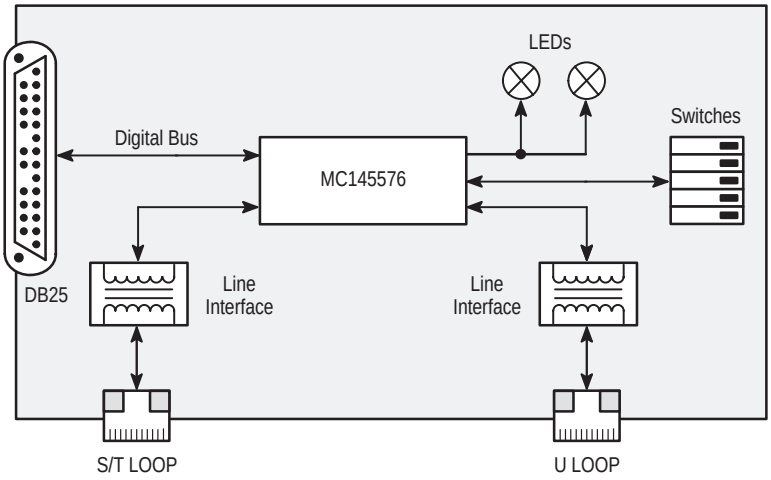
MC145576EVK

This evaluation board has been designed to demonstrate the MC145576 Single Chip NT1.

The device on the board may be configured in Basic NT1 mode, or as a Smart NT1, which provides terminal access to the MC145576 via IDL/SCP or GCI interfaces.

The MC145576EVK is powered by an external 5 V power supply. A separate connector can be used to provide +40 V to the TE through the S/T line (separate grounds are provided).

MC145576EVK Block Diagram



MC145576EVK Features:

- Configurable as Basic or Smart NT1
- IDL/SCP or GCI access in Smart NT1 mode
- Test pulses available
- Status LEDs

ISDN Voice/Data Circuits (continued)

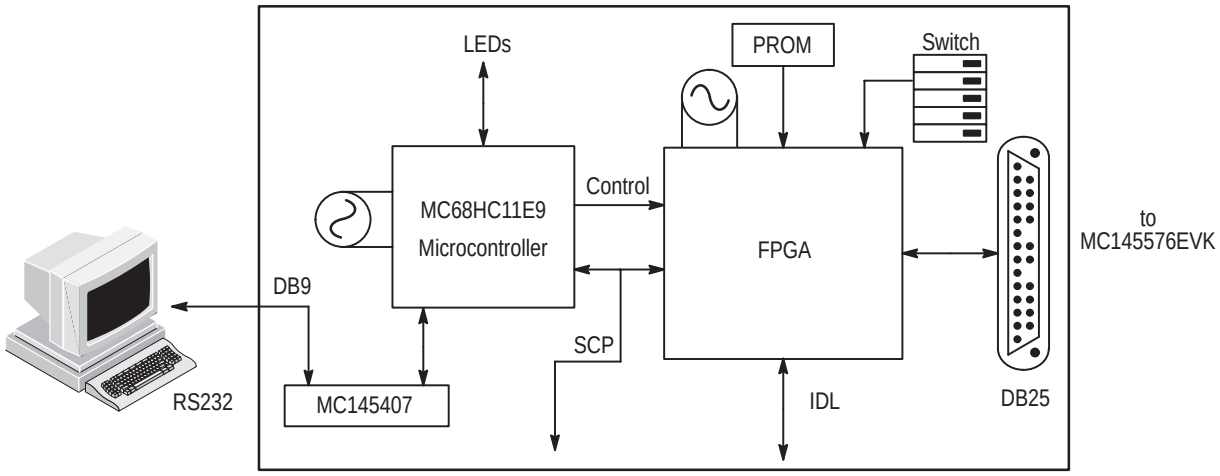
Driving Board for the MC145576EVK

MC145576DRV

This driving board is a convenient and efficient vehicle for evaluation of the MC145576 Single Chip NT1 configured for Smart NT1 applications. It should be directly connected to the MC145576EVK board, and configured in the IDL/SCP mode.

The MC145576DRV provides the ability to interactively manipulate status registers in the MC145576 with the aid of an external terminal. It provides also some gated clocks for BER testing.

MC145576DRV Block Diagram



MC145576DRV Features:

- Computer Operation
- Resident Firmware Monitor for User Control of Board
- Smart NT1 Activation and Deactivation Software
- MC68HC11 Assembly Language Source Code Available
- On–Board 68HC11 Microcontroller with Resident Monitor Software
- Convenient Access to Key Signals
- Only +5 Volt Power Supply (the board is powered by the MC145576EVK board)
- Gated Data Clocks Provided for Bit Error Rate Testing
- Can be used as a MC145576 Development Tool
- EIA–232 (V.28) Serial Port for Terminal Interface

3

Asymmetric Digital Subscriber Line

ADSL (Asymmetric Digital Subscriber Line) is an exciting new telecommunications technology that dramatically increases the functionality of the existing copper infrastructure.

ADSL delivers more than 6 Mbps from the central office to the home, in addition to a 640 kbps upstream transmission for interactive communications. And ADSL does this on the existing telephone lines reaching up to 12,000 feet. With rates as low as 256 kbps, ADSL can provide serivce beyond 20 kft.

Motorola's CopperGold™ ADSL Transceiver is a highly integrated single chip solution, designed for high speed broadband access. The flexible DMT–based transceiver is engineered to achieve low cost, while maintaining high performance. The high integration of the transceiver offers significant power and board–space savings while providing superior performance at a low cost.

Designed to be compliant with both categories one and two of the ANSI TI.413 standard, the CopperGold Solution utilizes echo cancellation and trellis coding for a high performance, future–proof product capable of 8 Mbps simplex and up to 1 Mbps bi–directional.

Motorola's CopperGold Family includes the highly–integrated transceiver (MC145650), and a wide array of complementary components tailored for specific applications such as Ethernet transceivers (MC68160), ATM Cell Processors (MC92501), and many host control options (MPC860, MPC860SAR, MPC850, MPC850SAR.) The CopperGold Family of ADSL Solutions is fully supported with evaluation boards, APIs, a system analyzer and Motorola's world–class applications support.

3

CopperGold™ Asymmetric Digital Subscriber Line (ADSL) Transceiver

MC145650

The MC145650 is a single integrated circuit transceiver device for ANSI (American National Standard Institute) T1.413 category 2 ADSL modems(1), based on the Discrete Multi–tone (DMT) line code. The category 2 specification requires payload rates of (6.144 Mbps + 640 kbps) downstream and 640 kbps upstream, with crosstalk, over carrier serving area (CSA) range loops, and to achieve (1.544 Mbps + 176 kbps) downstream and 176 kbps upstream with crosstalk, over selected ANSI integrated services digital network (ISDN) loops. The payload makeup is flexible thereby allowing multiple data streams to be multiplexed and demultiplexed.

The MC145650 is capable of data rates up to 8 Mbps downstream and 1 Mbps bi–directionally, however actual rates obtained in any system are dependent on loop length, impairments, and transmitted power. The ADSL and DMT techniques are adaptive, changing system parameters based on loop characteristics in order to optimize the data rate.

This device combined with a microcontroller and a line interface may be configured as either a central office ADSL transceiver unit (ATU–C) or as a remote terminal ADSL transceiver unit (ATU–R).

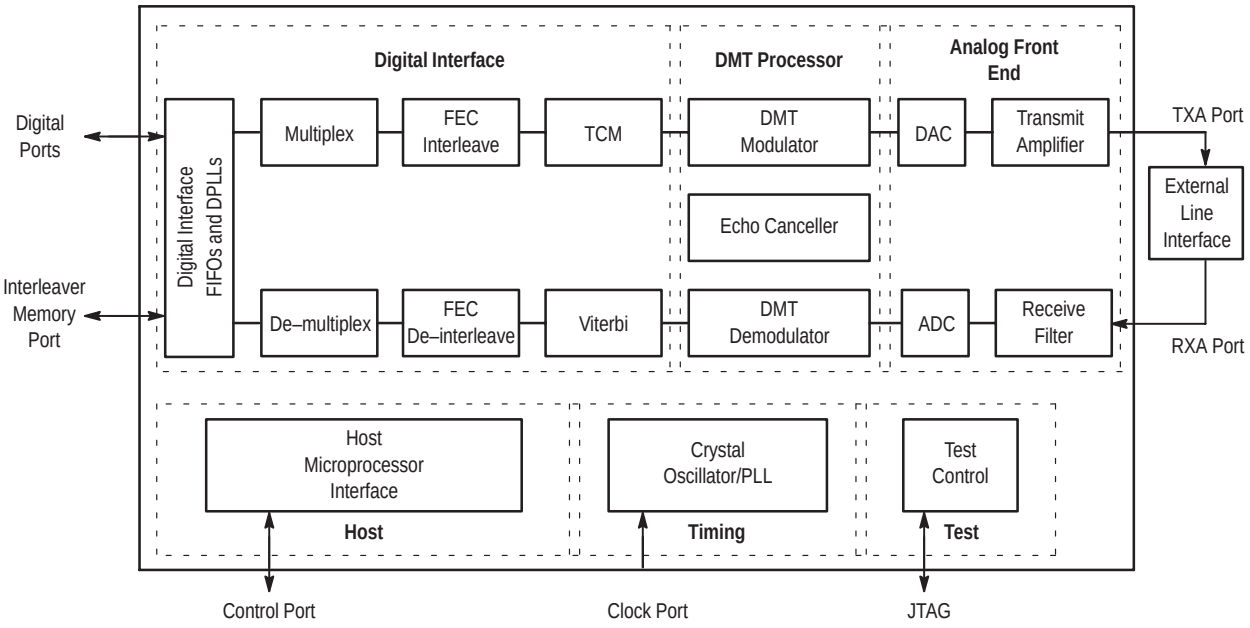
An ADSL system could be configured to provide the user with high speed Internet access with POTS, or two 3 Mbps MPEG2 (or four 1.5 Mbps MPEG1) video channels, a 640 kbps bi–directional data channel, along with POTS (Plain Old Telephone Service), all over existing copper telephone wire.

All of the basic functions required to perform both the transmit and the receive operations in a category 2 ADSL modem are contained within the MC145650. These functions include those that make up the transmit and receive data processing as well as the control, timing and test functions that are outside the data path. A detailed functional block diagram of the MC145650 is shown below.

Note (1): Without 26 dBm transmit power boost.

Asymmetric Digital Subscriber Line (continued)

MC145650 BLOCK DIAGRAM



CopperGold™ V.90/G.lite Modem Chip Set

MC143462SK

Motorola's CopperGold Lite chip set, MC143462SK, is designed to allow modem manufacturers to build the next generation of consumer modems. The CopperGold Lite supports the operation of traditional V.90 analog data, fax, and voice (D/F/V) services, or digital subscriber line (G.Lite) services in a cost–effective modem platform. Created for PC network interface card (NIC) applications, the chip set is bundled with the software required to build a PC NIC. A comprehensive design kit (MC143462RDK) which includes a reference modem, the bill of materials, certification reports, gerber files, and documentation is also available.

The CopperGold Lite integrates Motorola's proven V.90 modem technology with its high–performance, standards–compliant MC143410 24–bit Digital Signal Processor (DSP). This Discrete Multi–Tone based DSP is designed for compliance with the G.992.2 standard. The DSP is designed to squeeze the highest performance over the longest loops, which translates into more customers, higher connection rates, and fewer customer service calls.

Designed with the flexibility of an embedded 24–bit DSP, this upgradable chip set is designed to support the new ITU series of ADSL standards: G.992.2 (G.Lite) and G.994.1 (G.hs). The DSP's ability to support multiple ITU standards enables a manufacturer to ship a "universal'' modem that is designed to connect with the wide variety of ADSL configurations being deployed in different regions in the world — splitterless or splittered, 256 or 128 subcarriers for frequency division multiplexing, and DSL over POTS.

PC drivers and hardware included with the CopperGold Lite are compliant to the PC99 System Design Guide specifications for modem and network devices. In addition, these drivers implement the protocol stacks required for connectivity with DSL service.

Asymmetric Digital Subscriber Line (continued)

Components

- MC143418 DSL AFE
- MC143410 24–Bit DSP with PCI Interface
- All Software Required for V.90/G.lite Functionality

Customer Benefits

- Low–cost, Integrated Design
- High Performance Consumer Communications Solution for PC
- Designed for Upgradability to Future Standards

Features

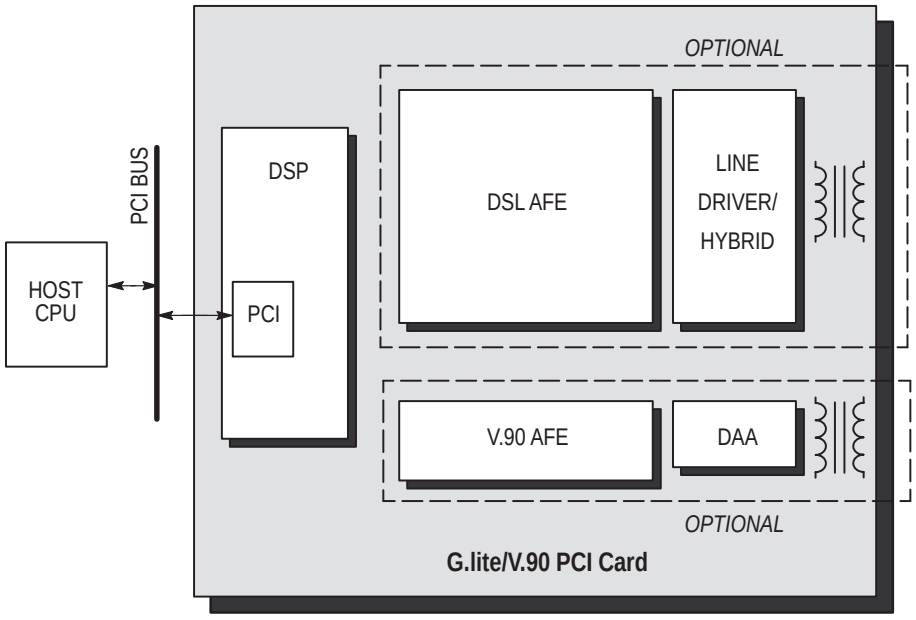
- V.90 and G.lite Compliant
- Compatible with the ADSL DMT: T1.413i2 Category I and II
- PC99 Compliant, Supports Windows® 98, Windows 2000
- RFC2364: PPP Over AAL5
- RFC1483: Ethernet Over AAL5
- ACPI D3Cold Support
- PCI 2.2 Compliant
- Upgradable to Future Standards
- Backed by Motorola's V.34 and DSL IP Portfolio

Typical Applications

- NIC Card Hybrid Solutions (V.90 and G.lite)
- PC OEMs, Remote Modem Manufacturers

3

BLOCK DIAGRAM



Asymmetric Digital Subscriber Line (continued)

CopperGold™ Control Software

MC145650CSW1

The CopperGold Control Software provides complete control and monitoring of the MC145650 CopperGold Transceiver and the ADSL link.

The control software is written in ANSI C and is independent of host processor and operating system. The customer's application software controls and monitors the CopperGold Transceiver via the CopperGold API (Application Programming Interface). The API consists of multiple C functions that provide access to the control software. Based on the ANSI T1.413 standard, the API is intended for use by programmers who are developing software for the control of the ADSL transceiver. The control software and API are delivered with comprehensive documentation and provide the following advantages and benefits:

- Decreases product development costs, time to market, and project risk.
- Eliminates a layer of complexity and risk associated with controlling the CopperGold Transceiver.
- Enables customers to focus software resources on embedded applications where product differentiation may be incorporated.
- Portable to customer's operating system and host processor.
- Control software updates, if necessary, are provided with new releases of silicon, rendering changes to the silicon transparent to the application software.

The CopperGold Control Software provides the following capabilities:

- ADSL Link Initialization and Control
- Transceiver Initialization
- Application Programmable Link Parameters
- Embedded Operations Channel (eoc) Message Interface
- ADSL Overhead Control (aoc) Channel Operations
- Extensive Error Reporting
- Accumulation of Link Statistics

CopperGold™ Evaluation System

MC145650EVS

The CopperGold Evaluation System provides Motorola customers with a complete and convenient evaluation platform for CopperGold Asymmetric Digital Subscriber Line (ADSL) applications. The Evaluation System includes 2 evaluation boards (ATU–C, ATU–R) and all necessary software and cabling.

Motorola created the CopperGold Evaluation System to help customers reduce their product development costs, time to market, and project risk. This system can be used to evaluate the CopperGold Transceiver and Line Driver, as well as the CopperGold Control Software.

The Evaluation System offers the following advantages and benefits:

- Provides complete bit error rate testing of an ADSL link.
- Shows the current status of the ADSL link via an on–board display.
- Provides a performance baseline for the entire CopperGold system.

The Evaluation System also includes the CopperGold System Analyzer, a PC–based (Windows NT™) graphical user interface (GUI) application. The System Analyzer controls and monitors the system and offers the following advantages and benefits:

- Enables complete control of the CopperGold Evaluation System via the CopperGold API.
- Allows customization for the user's needs.
- Provides an interface to control an external line simulator.
- Provides scripting which can be used to automate system tests.
- Provides application software downloading capabilities.

The CopperGold Evaluation System consists of the following hardware and software:

Hardware

- 2 CopperGold Evaluation Boards
  - CopperGold Transceiver
  - M68302 Processor
  - On–board Bit Error Rate Tester (BERT)
  - LCD Character Display
- Line Driver Daughter Cards
- RS232/422 Cables

Software

- CopperGold System Analyzer
- CopperGold Control Software (pre–loaded on the evaluation board)

Asymmetric Digital Subscriber Line (continued)

CopperGold™ System Development Kit

MC145650RDK5

Dedicated to providing our customers with the tools they need to be successful in the ADSL marketplace, Motorola introduces the CopperGold System Development Kit (SDK). Jointly developed by Motorola and ATLAS Communication Engines, the CopperGold SDK provides an ATU–R hardware reference design and an ATU–C modular platform for the support of multiple transceivers by one host controller.

The CopperGold SDK was designed to help Motorola customers reduce their time–to–market and focus on product functionality and differentiation, reaping the competitive advantages that come with a shortened development cycle. The end result is the manufacturer is free to focus on value–added features and differentiation, while still providing an interoperable solution to service providers and end users.

The ATU–R portion of the CopperGold SDK is designed as an ADSL Transmission Unit for the Remote End, allowing for standards–based, cost–competitive, and interoperable implementations. By using the reference design, which includes all aspects of the ATU–R, equipment providers can address interoperability issues while optimizing for product cost and time–to–market — without incurring heavy development expenditures.

Components

- ATU–R Hardware Reference Design
- ATU–C Modular Platform

Benefits

- Rapid Time–to–Market
- Cost Reduction
- Enables Product Differentiation
- Interoperability
- Standards–Based
- Accelerated Deployment

Voice/Data Communication (Digital Transmission)

2–Wire Universal Digital Loop Transceiver (UDLT)

MC145422P, DW Master Station
Case 708, 751E

MC145426P, DW Slave Station
Case 708, 751E

The UDLT family of transceivers allows the use of existing twisted–pair telephone lines (between conventional telephones and a PBX) for the transmission of digital data. With the UDLT, every voice–only telephone station in a PBX system can be upgraded to a digital telephone station that handles the complex voice/data communications with no increase in cabling costs.

In implementing a UDLT–based system the A/D to D/A conversion function associated with each telset is relocated from the PBX directly to the telset. The SLIC (or its equivalent circuit) is eliminated since its signaling information is transmitted digitally between two UDLTs.

The UDLT master–slave system incorporates the modulation/demodulation functions that permit data communications over a distance up to 2 kilometers. It also provides the sequence control that governs the exchange of information between master and slave. Specifically, the master resides on the PBX line card where it transmits and receives data over the wire pair to the telset. The slave is located in the telset and interfaces the monocircuit to the wire pair. Data transfer occurs in 10–bit bursts (8 bits of data and 2 signaling bits), with the master transmitting first, and the slave responding in a synchronized half–duplex transmission format.

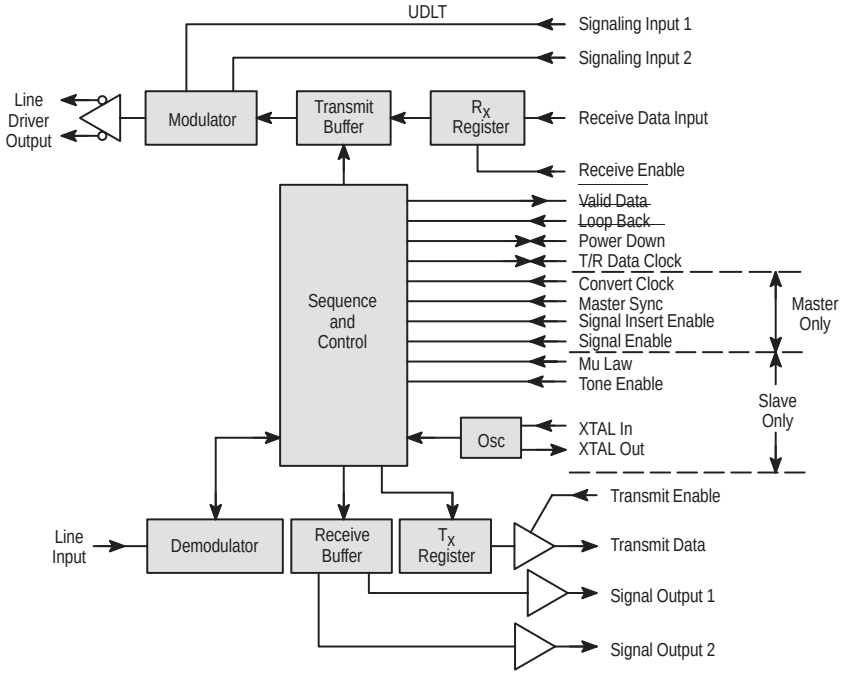
UDLTs utilize a 256 kilobaud Modified Differential Phase Shift Keyed (MDPSK) burst modulation technique for transmission to minimize radio frequency, electromagnetic, and crosstalk interference. Implementation through CMOS technology takes advantage of low–power operation, increased reliability, and the proven capabilities to perform complex telecommunications functions.

Functional Features
- Provides Synchronous Duplex 64 kbits/Second Voice/Data Channel and Two 8 kbits/Second Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5.0 V to 8.0 V Power Supply

MC145422 Master UDLT
- 2.048 MHz Master Clock
- Pin Controlled Power–Down and Loop–Back Features
- Variable Data Clock – 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbits/Seconds Channel into LSB of 64 kbits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT
- Compatible with MC145500 Series and Later PCM Codec–Filters
- Automatic Power–Up/Down Feature
- On–Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

Voice/Data Communication (Digital Transmission) (continued)



3

2–Wire ISDN Universal Digital Loop Transceiver II (UDLT II)

MC145421P, DW Master

Case 709, 751E

MC145425P, DW Slave

Case 709, 751E

Similar to the MC145422/26 UDLT, but provide synchronous full duplex 160 kbps voice and data communication in a 2B + 2D format for ISDN compatibility on a single twisted pair up to 1 km. Single 5.0 V power supply, protocol independent.

Analog Modem Chip Sets

The Motorola family of analog modem systems is a complete line of software upgradable modem solutions for a wide variety of PC, multimedia, and embedded applications. Each family member includes the basic data, fax, and voice modem features such as V.90 capability, as well as K56flex™ compatibility. When ordering these modems, all major integrated circuits and requisite software are included under one part number. Depending on the requirements of their system application, developers can choose between a controller–less or external/embedded modem chip set. The controller–less solution is the MS143455SK PCI modem chip set. The MS143450SK External/Embedded Modem chip set does not require special host software and can be implemented as a standalone device.

The analog modem systems family also features reference design kits (RDKs) for rapid system implementation. Reference design kits are not intended for detailed system evaluation and software development. RDKs will demonstrate lowest cost implementation, be certified for electrical emissions and electrical safety, and be homologated for target countries. RDKs also allow for customers to evaluate modem/fax and voice performance.

Analog Modem Systems Family Chip Sets and Software

Series	Host Controller	Host Data Pump
MS143450SK	No	No
MS143455SK	Yes	No

Series	DSP Controller	DSP Data Pump	ISDN–Capable
MS143450SK	Yes	Yes	No
MS143455SK	No	Yes	No

3

Analog Modem Chip Sets (continued)

External/Embedded Modem Chip Set and Software

MS143450SK

The Motorola MS143450SK is a complete analog modem chip set and software for retail and embedded modem applications. The MS143450SK DSP–based modem controller and data pump are upgradable via software download. This ensures that Motorola upgrades or improvements of modem software can rapidly be incorporated into any end product. The MS143450SK's modem and voice functions utilize a Motorola DSP56300–based core. The DSP56300 core offers a single instruction per cycle, 24–bit DSP architecture, and is well–suited for modem and audio DSP applications. The MC143416 Dual 16–Bit Linear Codec–Filter offers a single–chip implementation of the data conversion interface required to design high–speed modems, and features a telephony and acoustic codec, clock generation, conditioning, and sample rate conversion of signals to and from the data interface.

Included with the MS143450SK is Motorola's complete suite of modem software. With the Motorola software, developers can rapidly incorporate an upgradable high–performance communications solution into their system.

The MC143450RDK Reference Design Kit is a turn–key design for the Motorola external/embedded modem. The MC143450RDK is designed with minimum cost and rapid implementation in mind. It allows the developer to evaluate modem and voice feature performance and to perform a detailed system cost analysis. An evaluation software license is included along with schematics, complete Bill of Materials (BOM), layout recommendations, and Gerber files for PCB fabrication. The MC143450RDK is also designed to pass all electrical and safety certifications required by national certification bodies worldwide. This includes regulations such as FCC Part 68 and FCC Part 15 in the United States.

Integrated Circuits Included

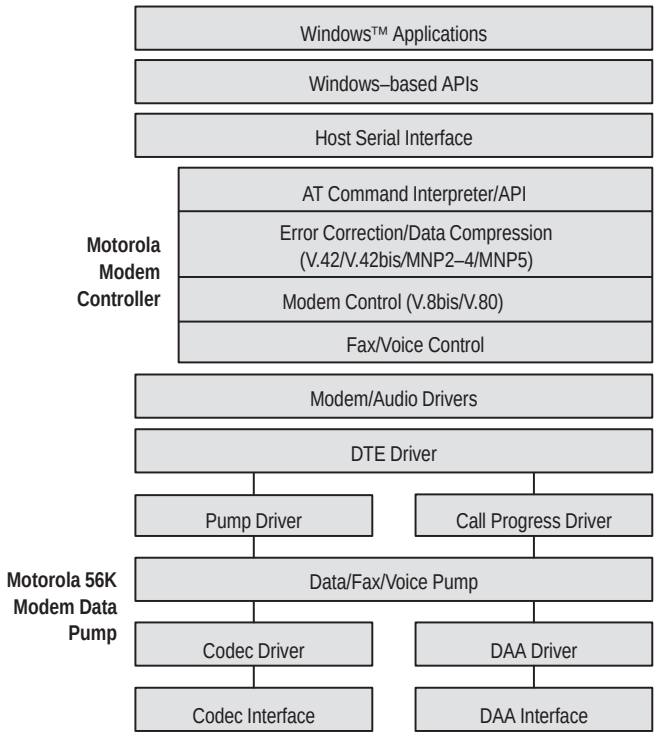
- DSP56300 Core 24–Bit Modem DSP
- MC143416 Dual 16–Bit Linear Codec–Filter

Software Included

- External/Embedded Modem Controller and Data Pump Software

Features

- High Performance 24–Bit DSP
- High Quality Dual Integrated Codec
- ITU–T V.80 (Video Ready), Enhanced Caller ID, Plug and Play Support, and Distinctive Ring
- Data/Fax/Voice Features



Analog Modem Chip Sets (continued)

PCI Controller–less Modem Chip Set and Software

MS143455SK

The MS143455SK is a controller–less modem, developed using Motorola's DSP56300–based 24–bit DSP architecture. It is implemented with the control code running on the host PC and the data pump code running on the DSP. The main features of the MS143455SK are: a V.34/V.90 data modem using V.42/MNP®4 error correction and a V.42bis/MNP5 data compression, a V.17 fax modem using a TIA/EIA 578 Class I fax, and a voice modem supporting a full–duplex speakerphone with telephone answering machine. The MS143455SK is a complete modem chip set with a Windows™ 95 and Windows NT™ device driver and a PCI interface.

The modem system is shown in the block diagram. The application software uses the PCI interface to send and receive data/control information to and from the MS143455SK. The control code includes error correction, data compression, and Hayes™ AT command sets implemented on the host computer. The MS143455SK utilizes a single 24–bit modem DSP performing data pump operations. The DSP56300 core offers a single instruction per cycle, 24–bit DSP architecture, and is well–suited for modem and audio DSP applications.

Motorola's PCI Controller–less Modem Chip Set and Software is the industry's first desktop power managed modem that supports full ACPI "Wake–On–Ring" technology. This capability allows PCs that have been put into low power, suspended state to automatically turn themselves on upon receiving a phone call. This modem feature allows the PCs to receive incoming messages such as faxes and voice mails that would otherwise be missed.

The MC143416 Dual 16–Bit Linear Codec–Filter offers a single–chip implementation of the data conversion interface required to design high–speed modems, and features a telephony and acoustic codec, clock generation, conditioning, and sample rate conversion of signals to and from the data interface. The MC143421 PCI Bus Interface is a low cost and highly integrated PCI interface solution that includes Advanced Configuration Power Interface (ACPI) features. It is designed to enable the addition of a PCI interface to PC peripherals such as DSP–based analog modems.

The MC143455RDK is the reference design kit for the MS143455SK chip set, and is designed with minimum cost and rapid implementation in mind. It allows the developer to evaluate modem and voice feature performance and to perform a detailed system cost analysis. An evaluation software license is included along with schematics, complete Bill of Materials (BOM), layout recommendations, and Gerber files for PCB fabrication. The MC143455RDK is also designed to pass all electrical and safety certifications required by national certification bodies worldwide. This includes regulations such as FCC Part 68 and FCC Part 15 in the United States.

Integrated Circuits Included

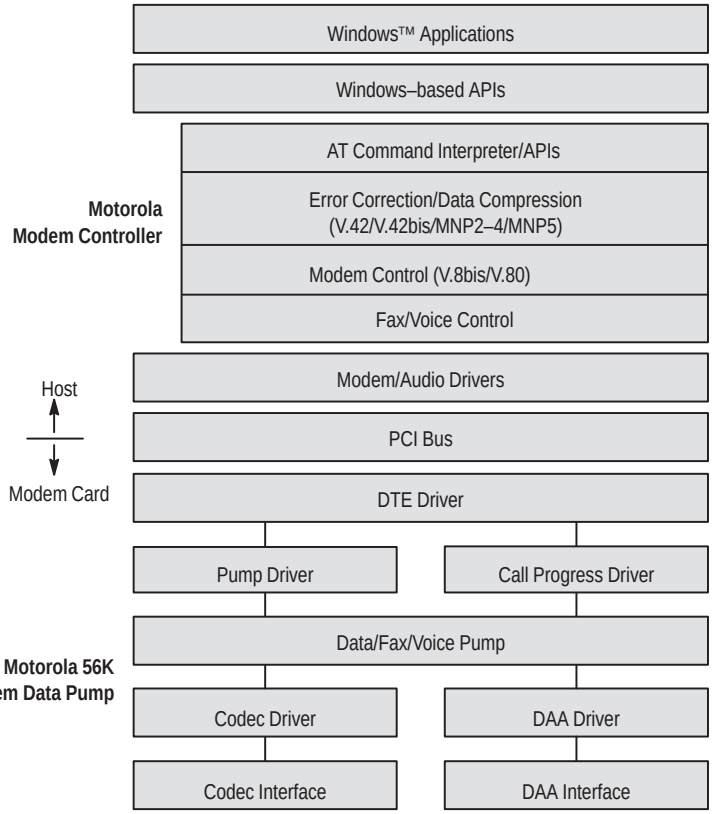
- DSP56300 Core 24–Bit Modem DSP
- MC143416 Dual 16–Bit Linear Codec–Filter (COder/DECoder)
- MC143421 PCI Bus Interface

Software Included

- PCI Controller–less Modem Controller and Data Pump Software

Features

- High–Performance K56flex™ Data, Voice, and Fax Modem Which Interfaces Popular Communications Applications
- Controller–Less (Host–Based Controller) for Lowest Cost and Minimum Utilization of Host CPU Resources
- Operating System Support Device Drivers Included: Windows 95 and Windows NT Device Drivers
- High–Performance 24–Bit DSP with Adjustable Control Features for Market Differentiation
- High Quality Dual Integrated Codec–Filter Analog Front End (AFE)
- Common Device Driver Software for ISA and PCI Controller Code


Windows™ Applications
Windows–based APIs
AT Command Interpreter/APIs
Error Correction/Data Compression
(V.42/V.42bis/MNP2–4/MNP5)
Modem Control (V.8bis/V.80)
Fax/Voice Control
Motorola
Modem Controller
Modem/Audio Drivers
Host
PCI Bus
Modem Card
DTE Driver
Pump Driver
Call Progress Driver
Data/Fax/Voice Pump
Motorola 56K
Modem Data Pump
Codec Driver
DAA Driver
Codec Interface
DAA Interface

Analog Modem Chip Sets (continued)

External/Embedded Modem Reference Design Kit

MC143450RDK

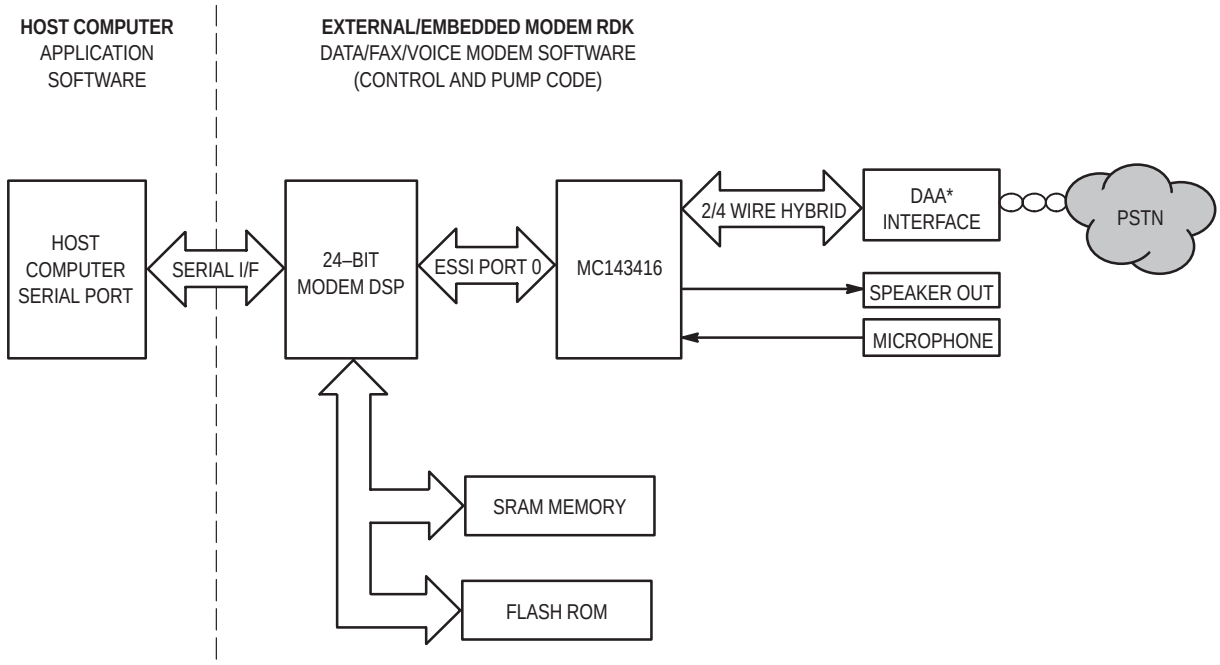
The External/Embedded Modem Reference Design Kit (RDK) was developed to facilitate the creation of unique Public Switched Telephone Network (PSTN) communication products using Motorola's DSP56300–based 24–bit DSP architecture. The critical component of this kit is an external modem which provides a means of testing and evaluating Motorola's V.34/V.90 data/fax/voice modem supporting the Hayes™ AT Command Set, Data Compression/Error Compression (V.42bis/V.42), Class 1 Fax, Telephone Answering Machine, and Full–Duplex Speakerphone.

The application software uses the host computer's serial port to communicate with the 24–bit modem DSP to perform all the control and data pump operations for data/fax/voice. All modem firmware is executed from the DSP's volatile memory system so that new features can be easily upgraded. The DSP makes use of its built–in peripherals to interface directly with the serial port of the host computer and to interface with the data (telephony) and voice (acoustic) codecs (COder/DECoder) which provide Analog–to–Digital (A/D) and Digital–to–Analog (D/A) conversions between the modem and the analog interfaces. The MC143416 Dual 16–Bit Linear Codec–Filter offers a single–chip implementation of the data conversion interface required to design high–speed modems, and features a telephony and acoustic codec, clock generation, conditioning, and sample rate conversion of signals to and from the data interface.

Features

- Complete External/Embedded Modem Turn–Key Design
- Programmable DSP and Memory System Consisting of SRAM and Flash ROM for Software Upgradability
- Turn–Key Internationalization Support
- ITU–T V.80 (Video Ready), Enhanced Caller ID, Plug and Play Support, and Distinctive Ring

BLOCK DIAGRAM



* DAA = Data Access Arrangement

Analog Modem Chip Sets (continued)

PCI Controller–less Modem Reference Design Kit

MC143455RDK

The MC143455RDK PCI Controller–less Modem Reference Design Kit (RDK) was developed to facilitate the creation of unique Public Switched Telephone Network (PSTN) communication products using Motorola's DSP56300–based 24–bit DSP architecture and Motorola's MC143416 Dual 16–Bit Linear Codec–Filter*. The critical component of this kit is an internal modem platform which provides a means of testing and evaluation of Motorola's V.34/V.90 data/fax/voice modem.

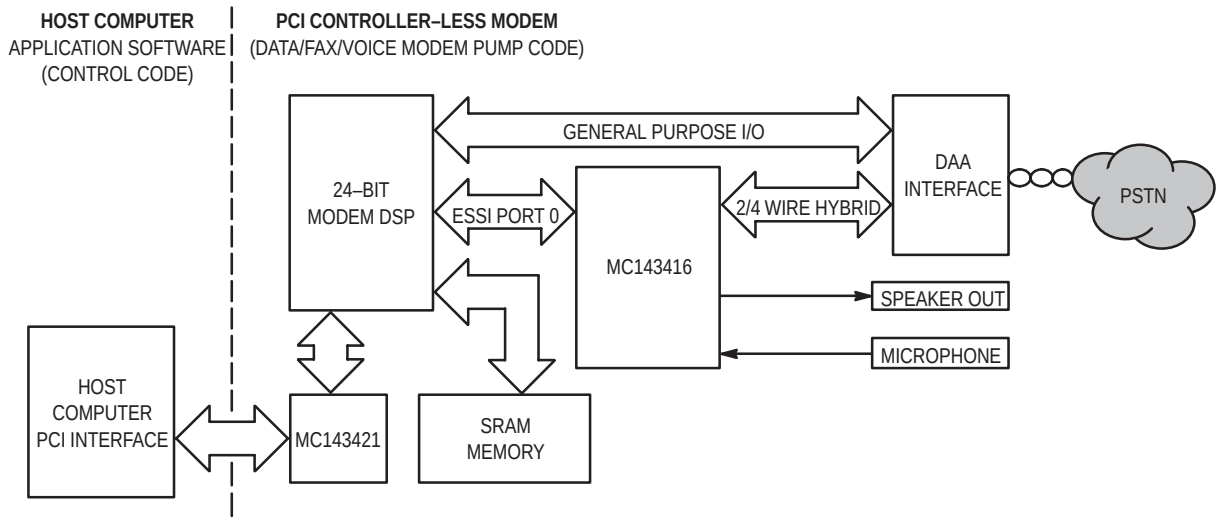
Motorola's PCI Controller–less Modem is the industry's first desktop power managed modem that supports full ACPI "Wake–On–Ring" technology. This capability allows PCs that have been put into low power, suspended state to automatically turn themselves on upon receiving a phone call. This modem feature allows the PCs to receive incoming messages such as faxes and voice mails that would otherwise be missed.

In the controller–less modem design, modem control code operations are performed by the host computer, while the modem pump code for data/fax/voice applications are executed by the 24–bit modem DSP. The application software uses the PCI interface to transmit/receive data to or from the DSP. All modem software is installed into the host computer and downloaded to the DSP's system memory through the MC143421 PCI Bus Interface so that new modem features can be added. The DSP makes use of its built–in host port interface together with a PCI bus interface device to communicate directly with the host computer. Enhanced Synchronous Serial Interface (ESSI) communicates with the MC143416, which provides Analog–to–Digital (A/D) and Digital–to–Analog (D/A) conversions. The MC143416 is a single–chip implementation of the data/voice converters required for high–speed modems and features a telephony and acoustic codec, clock generation, signal conditioning, programmable sampling rates, built–in analog mixer, and speaker driver. The MC143421 PCI Bus Interface is a low cost and highly integrated PCI interface solution that includes Advanced Configuration Power Interface (ACPI) features. It is designed to enable the addition of a PCI interface to PC peripherals such as DSP–based analog modems.

Features

- Complete Controller–less Modem Turn–Key Design
- Programmable DSP and Memory System Consisting of SRAM for Software Upgradability
- Turn–Key Internationalization Support
- ITU–T V.80 (Video Ready), Enhanced Caller ID, PCI Bus Interface, and Distinctive Ring
- Data/Fax/Voice Modem with Host–Based Controller
- Operation System Support: Windows™ 95 and Windows NT™

BLOCK DIAGRAM



* Codec = COder/DECoder

Analog Modem Chip Sets (continued)

Multichannel Infrastructure Modem Evaluation Kit

MC143457EVK

The Motorola MC143457EVK is a complete modem solution for infrastructure modem applications. This DSP–based Multichannel Infrastructure Modem (MIM) is completely upgradable via software, which ensures that the MIM Evaluation Kit is ready to receive the latest in field upgrades and infrastructure applications such as vocoders for voice over internet protocol, and gateway hosting. The MC143457EVK offers an enabling evaluation system to address the infrastructure modem market. Combining the controller functionality of the PowerPC™ MPC860 product family with the high performance DSP56300 family and glueless, low power FSRAM devices allows Motorola to provide a total system solution.

The MC143457EVK comes complete with all the hardware and software needed to evaluate an analog modem "head end," or modem termination system. The data pump software provides a direct digital, 8 kHz sampled, PCM data interface. This allows a seamless digital TDM connection onto an E1/T1 interface, eliminating the need for codecs and other costly glue hardware. Another key benefit of this solution is the memory efficiency of the re–entrant modem software, allowing a highly scalable and upgradable architecture.

The MC143457EVK is designed to enable the evaluation of the performance and functionality of the entire Motorola solution. The board consists of three main parts: the main MEP board, an additional network interface daughter card, and an optional SIMM–style daughter card, which consists of an additional five DSP56303s with associated 128K x 24 FSRAM devices.

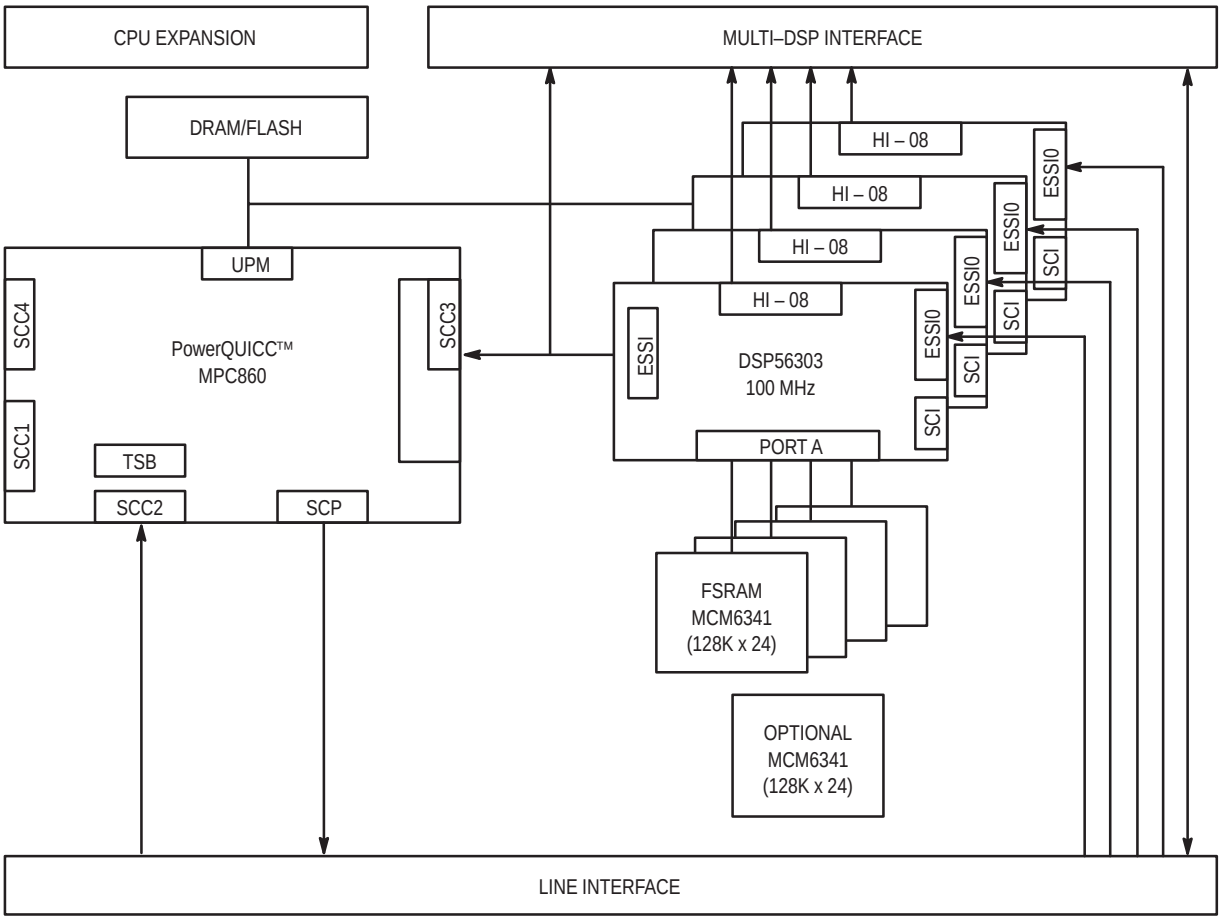
The MEP board consists of four DSP56303s. The first three DSP56303s each have a single 128K x 24 asynchronous FSRAM (MCM6341). In addition, the final DSP56303 has 256K x 24 assigned to it in the form of two 128K x 24 devices, to enable more software flexibility if required. These are all controlled by an MPC860 PowerPC controller. Each of the DSP56303s can handle up to three full–duplex V.90/V.34 (1996) modem channels simultaneously.

The MC143457EVK offers a cost effective solution that enables multiple modem channels to run on a single DSP56303, while enabling a concentrated low power consuming design, which is adaptable to suit the needs of both telecom equipment providers and remote access systems manufacturers.

Features

- Motorola system solution includes: MPC860MH, DSP56303, and MCM6341 (128K x 24).
- Support for up to 12 modem channels on the motherboard, with option to expand up to 27 channels with the inclusion of the SIMM–style daughter card.
- Provides a full–time slot–selectable TDM link — suitable for multiple T1 or E1 connections.
- Parallel communications/data path and capabilities for future 2 Mbps serial data link between MPC860 and DSP56303s.
- SIMM–style daughter card module available offering five DSP56303s and 128K x 24 single wait state FSRAMs. Motherboard has SDRAM SIMM module for added system flexibility.
- Evaluation board design enables accurate measurement of DSP56303 and MPC860 power consumption.

HARDWARE BLOCK DIAGRAM



3

Analog Front End ICs

Dual 16–Bit Linear Codec–Filter

MC143416PB

Case 824D

The MC143416 Dual 16–Bit Linear Codec–Filter is a single–chip implementation of the data conversion interface required to design high–speed modems meeting a wide range of standards such as ITU–T V.34 and V.90. It includes two high performance Analog–to–Digital (A/D) and Digital–to–Analog (D/A) data converters. The device performs all filtering operations related to the conditioning and sample rate conversion of signals to and from the data interface. Output from both codecs (COder/DECoder) is in 16–bit 2s complement format.

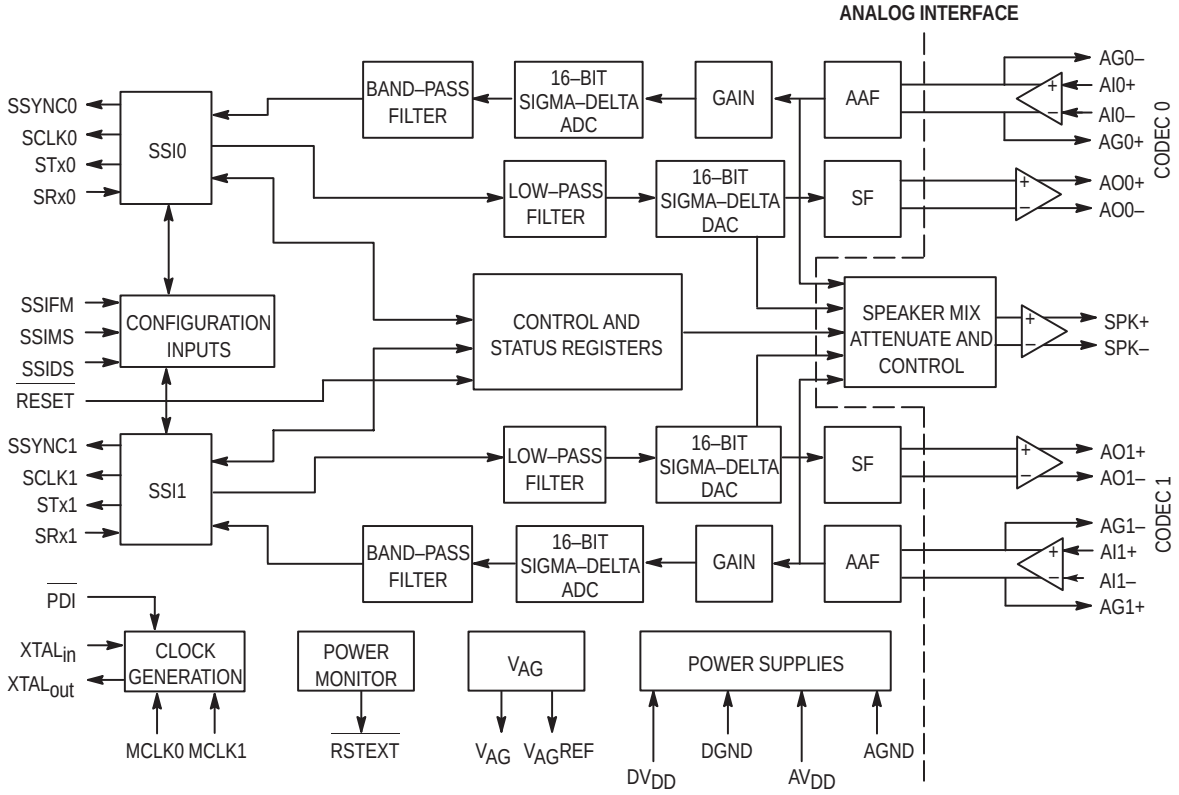
The MC143416 includes the necessary logic needed to generate all clocks (oversampling, intermediate frequency, and baud rate) required to perform the data processing operations involved in the oversampling conversion of voice and data signals. Sample rates are fully programmable in the range of 8 kilosamples/second (ks/s) to 16 ks/s. The bandwidth of the MC143416 is 0.425 * Sample Frequency (FS).

The MC143416 includes two Synchronous Serial Interfaces (SSIs) through which an external Digital Signal Processor (DSP) can configure and monitor the operation of the device. Digital sample data is transferred to and from the codecs through the serial ports. In addition, information can be written and read to the control and status registers of the device via the serial port, transparent to the flow of sample data. When used in a high–speed modem application, the MC143416 provides the analog front end interface required to support modem and voice features.

MC143416 Features:

- Fully–Differential Analog Circuit Design for Lowest Noise
- Two High Performance Sigma–Delta A/D and D/A Converters
- Band–Pass and Low–Pass Filtering for Both Codecs is Performed On–Chip
- Power Monitor Circuit
- Single 5.0 V ± 5% Power Supply
- Two Configurable Serial Ports
- On–Chip Precision Reference Voltage
- On–Chip Speaker Driver and Mixer with Programmable Gain — Capable of Delivering 15 mW of Power into a Small Speaker (32 Ω)
- Bandwidth is 0.425 * FS
- No External Filtering Required Because of Flat Response Over Passband
- Capable of Providing the Analog Front End for Wide Range of Modem Standards

Figure 4. MC143416 Block Diagram



3

Line Drivers

Table 2. EIA–232–E/V.28 CMOS Drivers/Receivers

Device	Suffix/ Package	Pins	Drivers	Receivers	Power Supplies (V)	Features
MC145403	P/738, DW/751D	20	3	5	±5.0 to ±12	
MC145404			4	4		
MC145405			5	3		
MC145406	P/648, DW/751G, SD/940B	16	3			
MC145407	P/738, DW/751D	20			+5.0	Charge Pump
MC145408	P/724, DW/751E, SD/940B	24	5	5	±5.0 to ±12	
MC145583	DW/751F, VF/940J	28	3	5	+3.3 to +5.0	On–board ring monitor circuit; charge pump, power down

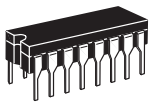
Bus Interface

3

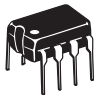
Table 3. 8–Bit PCI Bus Interface

Device	Power Supply	Comments	T_A (°C)	Suffix/ Package
MC143421	5.0 V	• Fully Compliant 32–Bit PCI 2.1 Interface • Four Address Lines and Byte–Wide Data • Eight General Purpose I/O Lines • ACPI Power Management and OnNow™ Support • Single Digital 100–Pin QFP VLSI Implementation	– 25 to 75	FU/842D

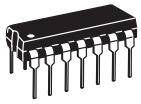
Communications Circuits Package Overview



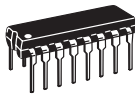
CASE 620
L SUFFIX



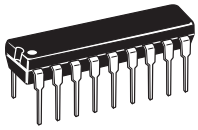
CASE 626
P SUFFIX



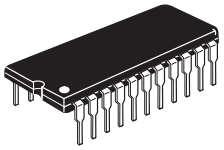
CASE 646
P SUFFIX



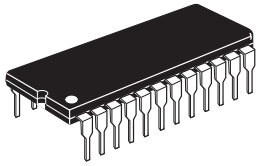
CASE 648
P SUFFIX



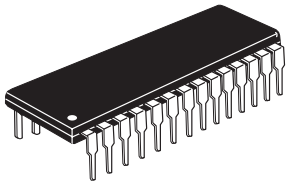
CASE 707
P SUFFIX



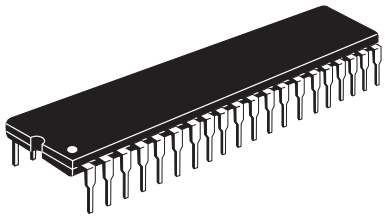
CASE 708
P SUFFIX



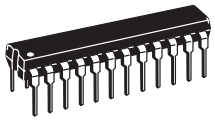
CASE 709
P SUFFIX



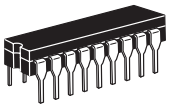
CASE 710
P SUFFIX



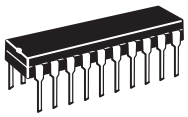
CASE 711
P SUFFIX



CASE 724
P SUFFIX



CASE 726
L SUFFIX

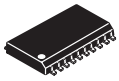


CASE 738
DP, P SUFFIX

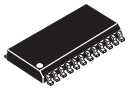
CASE 751
D SUFFIX

CASE 751A
D SUFFIX

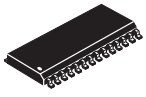
CASE 751B
D SUFFIX



CASE 751D
DW, FP SUFFIX

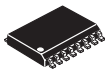


CASE 751E
DW SUFFIX

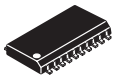


CASE 751F
DW SUFFIX

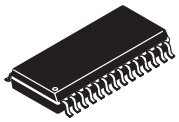
Communications Circuits Package Overview (continued)



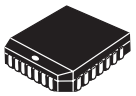
CASE 751G
DW SUFFIX



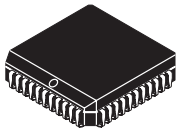
CASE 751J
F SUFFIX



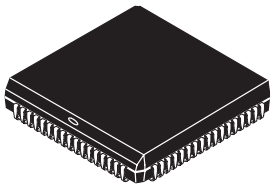
CASE 751M
FW SUFFIX



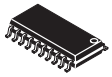
CASE 776
FN SUFFIX



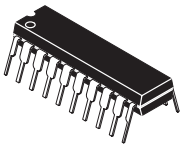
CASE 777
FN SUFFIX



CASE 779
FN SUFFIX

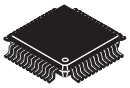


CASE 803C
F SUFFIX

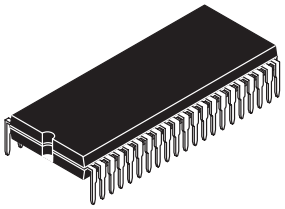


CASE 804
H SUFFIX

CASE 824D
PB SUFFIX



CASE 848B
FB SUFFIX



CASE 858
B SUFFIX

CASE 873
FB, FTB, FU SUFFIX

CASE 873A
PB SUFFIX

CASE 873C
FTA SUFFIX

CASE 932
FTA SUFFIX

CASE 940C
SD SUFFIX

CASE 948C
DT SUFFIX

CASE 948D
DT SUFFIX

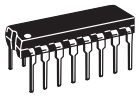
CASE 948F
DTB SUFFIX

CASE 976
FTB SUFFIX

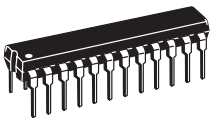
CASE 977
FTA SUFFIX

3

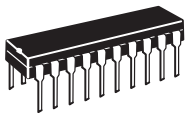
Interface Circuits Package Overview



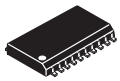
CASE 648
P, PC SUFFIX



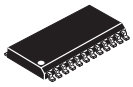
CASE 724
P SUFFIX



CASE 738
P SUFFIX

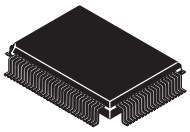


CASE 751D
DW SUFFIX



CASE 751E
DW SUFFIX

CASE 751G
DW SUFFIX



CASE 842D
FU SUFFIX

CASE 940B
SD SUFFIX

CASE 940J
VF SUFFIX

3

Sensors and Smoke Integrated Circuits (ICs)

In Brief . . .

Motorola's sensor products feature three product families, smoke and alarm ICs, acceleration, and pressure sensors. These devices combine silicon micromachining with high volume semiconductor manufacturing technology and processes for highly accurate, reliable, repeatable, cost–effective devices.

Pressure Sensors

Combining integrated circuit and micromachining technology, this diverse family of pressure sensing products offers performance, reliability and design adaptability in a single monolithic device. The versatile, cost–effective MPX series of pressure transducers are available in a number of versions:

- Fully integrated signal conditioned sensors for high–level output;
- Temperature compensated and calibrated, for simplified circuits
- Uncompensated for unlimited adaptability and;
- Multiple packaging and porting options

Target applications: Medical products, systems and diagnostic devices, industrial process control, automotive engine, safety, and body electronics.

Smoke ICs

Motorola's Smoke Integrated Circuits (ICs) are low power, CMOS devices designed to meet a wide range of smoke detector applications at a very competitive price. Motorola has been producing both photoelectric and ionization smoke ICs for more than 15 years. Found in consumer and commercial applications worldwide, these integrated circuits can be operated using a battery or AC power. In addition, these devices are designed to be used in stand alone units or as an interconnected system of up to 40 units. All of Motorola's smoke ICs have component recognition from Underwriter's Laboratories and the newest devices meet the NFPA's new "temporal three'' horn pattern.

Target applications: Residential and industrial smoke detectors and systems.

Alarm ICs

The MC14600 Alarm IC is designed to simplify the process of interfacing an alarm level voltage condition to a piezoelectric horn and/or LED. With an extremely low average current requirement and an integrated low battery detect feature, the part is ideally suited to battery operated applications. The MC14600 is easily configured, with a minimum of passives, to serve a wide range of applications and circuit configurations. Typical applications include intrusion alarms, moisture or water ingress alarms, and personal safety devices.

- High impedance, FET input comparator
- Comparator outputs for low battery and alarm signal output
- Alarm detect threshold easily established with 2 resistor
- Integrated oscillator and piezoelectric horn driver
- Low battery trip point set internally (altered externally)
- Horn "chirp'' during low battery condition
- Pulsed LED drive output
- Reverse battery protection
- Input protection diodes on the detect input
- Average supply current: 9 μa

Pressure Sensors

Introduction

Motorola pressure sensors combine advanced piezoresistive sensor architecture with integrated circuit technology to offer a wide range of pressure sensing devices for automotive, medical, consumer and industrial applications. Selection versatility includes choice of:

Pressure Ranges in PSI

0 to 0.58, 0 to 1.45, 0 to 6, 0 to 7.3, 0 to 14.5, 0 to 29, 0 to 75, 0 to 100, 0 to 150 psi.

Sensing Options

Uncompensated, Temperature Compensated/Calibrated, and Integrated (Signal Conditioned with on–chip amplifiers).

Application Measurements

Absolute, Differential, Gauge

Package Options

- Surface mount and through–hole with several porting options

4

Linearity

Linearity refers to how well a transducer's output follows the equation: $V_{out} = V_{off} + \text{sensitivity} \times P$ over the operating pressure range. There are two basic methods for calculating nonlinearity: (1) end point straight line fit (see Figure 1) or (2) a least squares best line fit. While a least squares fit gives the "best case" linearity error (lower numerical value), the calculations required are burdensome.

Conversely, an end point fit will give the "worst case" error (often more desirable in error budget calculations) and the calculations are more straightforward for the user. Motorola's specified pressure sensor linearities are based on the end point straight line method measured at the midrange pressure.

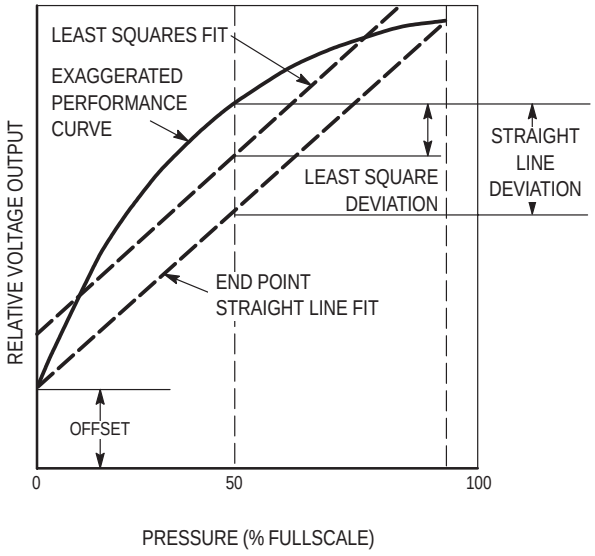


Figure 1. Linearity Specification Comparison

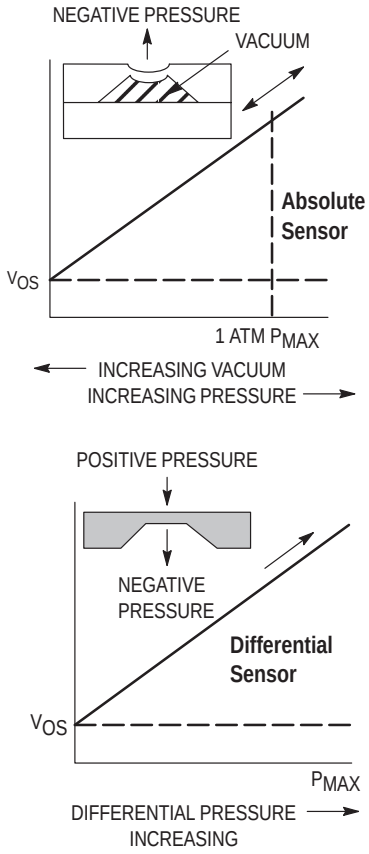
Operation

Motorola pressure sensors provide three types of pressure measurement: Absolute Pressure, Differential Pressure and Gauge Pressure.

Absolute Pressure Sensors measure an external pressure relative to a zero–pressure reference (vacuum) sealed inside the reference chamber of the die during manufacture. This corresponds to a deflection of the diaphragm equal to approximately 14.5 psi (one atmosphere), generating a quiescent full–scale output for the MPX2102A (14.5 psi) sensor, and a half–scale output for the MPX2202A (29 psi) device. Measurement of external pressure is accomplished by applying a relative negative pressure to the "Pressure" side of the sensor.

Differential Pressure Sensors measure the difference between pressures applied simultaneously to opposite sides of the diaphragm. A positive pressure applied to the "Pressure" side generates the same (positive) output as an equal negative pressure applied to the "Vacuum" side.

Gauge Pressure readings are a special case of differential measurements in which the pressure applied to the "Pressure" side is measured against the ambient atmospheric pressure applied to the "Vacuum" side through the vent hole in the chip of the differential pressure sensor elements.



Motorola sensing elements can withstand pressure inputs as high as four times their rated capacity, although accuracy at pressures exceeding the rated pressure will be reduced. When excessive pressure is reduced, the previous linearity is immediately restored.

Figure 2. Pressure Measurements

4

Typical Electrical Characteristic Curves

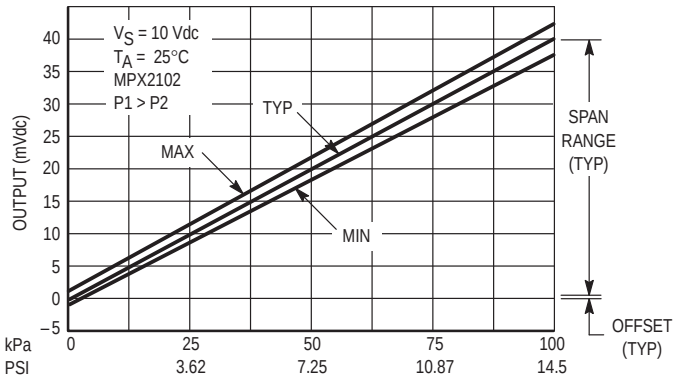


Figure 3. Output versus Pressure Differential

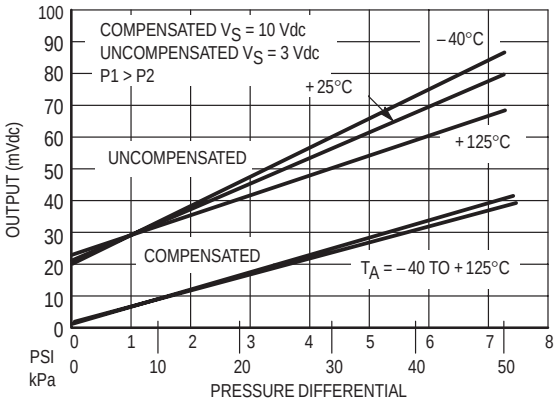


Figure 4. Typical–Output Voltage versus Pressure and Temperature for Compensated and Uncompensated Devices

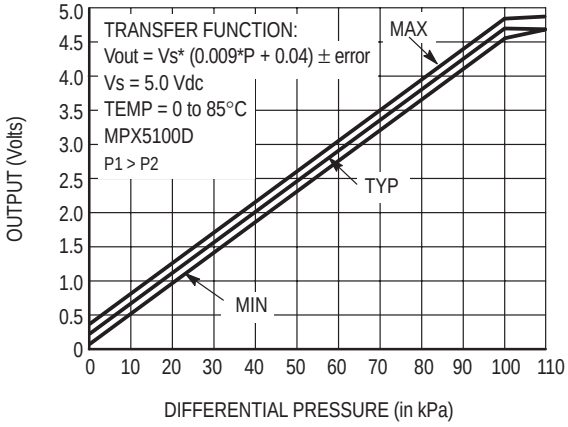


Figure 5. Signal Conditioned MPX5100

Cross–sectional Drawings

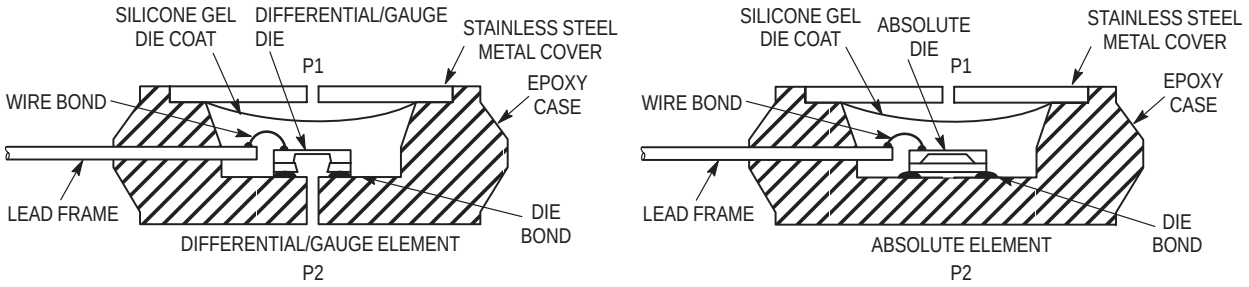


Figure 6. Cross–Sectional Diagrams (not to scale)

Figure 6 illustrates the absolute sensing configuration (right) and the differential or gauge configuration in the basic chip carrier (Case 344). A silicone gel isolates the die surface and wire bonds from harsh environments, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPX series pressure sensor operating characteristics and internal reliability and qualification tests are based on use of dry air as the pressure media. Media other than dry air may have adverse effects on sensor performance and long term stability. Contact the factory for information regarding media compatibility in your application.

4

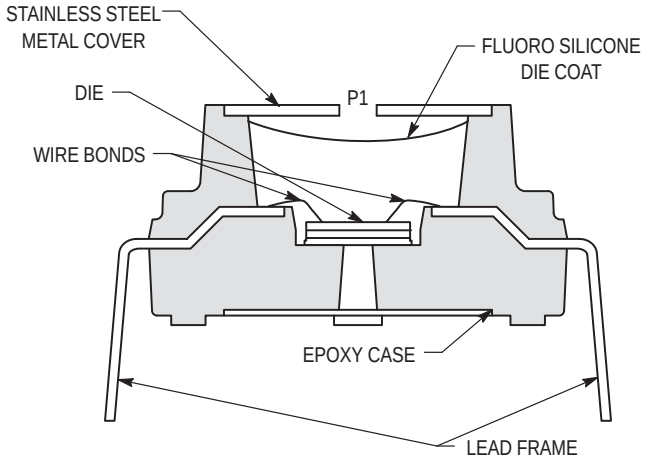


Figure 7. Cross–Sectional Diagram (not to scale)

Figure 7 illustrates the differential/gauge die in the basic chip carrier (Case 473). A silicone gel isolates the die surface and wirebonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

PRESSURE SENSOR PRODUCTS

Table 1. Uncompensated

Device Series	Max Pressure Rating		Over Pressure (kPa)	Offset mV (Typ)	Full Scale Span mV (Typ)	Sensitivity (mV/kPa)	Linearity % of FSS(1)	
	psi	kPa					(Min)	(Max)
MPX10	1.45	10	75	20	35	3.5	–1.0	1.0
MPXV10	1.45	10	75	20	35	3.5	–1.0	1.0
MPX12	1.45	10	75	20	55	3.5	–1.0	1.0
MPX53	7.3	50	200	20	60	1.2	–0.6	0.4
MPXV53	7.3	50	200	20	60	1.2	–0.6	0.4

Table 2. Compensated and Calibrated (On–Chip)

MPX2010	1.45	10	75	±1.0	25	2.5	–1.0	1.0
MPX2050	7.3	50	200	±1.0	40	0.8	–0.25	0.25
MPX2100	14.5	100	400	±1.0	40	0.4	–0.25	0.25
MPX2100A	14.5	100	400	±2.0	40	0.4	–1.0	1.0
MPX2200	29	200	400	±1.0	40	0.2	–0.25	0.25
MPX2200A	29	200	400	±1.0	40	0.2	–1.0	1.0

Table 3. Compensated and Calibrated (On–Chip) Medical Grade

Device Series	Max Pressure Rating		Supply Voltage (Vdc)	Offset mV (Max)	Sensitivity (μV/V/mmHg)	Output Impedance Ohms (Max)	Linearity % of FSS(1)	
	psi	kPa					(Min)	(Max)
MPX2300DT1	5.8	40	6.0	0.75	5.0	330	–3.0	3.0

4

Table 4. Signal Conditioned (On–Chip)

Device Series	Max Pressure Rating		Over Pressure (kPa)	Full Scale Span V (Typ)	Sensitivity (mV/kPa)	Accuracy (0–85°C) % of V_{FSS}
	psi	kPa				
MPX4100A	15.2	105	400	4.59	54	±1.8
MPXA4100A	15.2	105	400	4.59	54	±1.8
MPX4101A	14.8	102	400	4.59	54	±1.8
MPX4105A	15.2	105	400	4.59	54	±1.8
MPX4115A	16.7	115	400	4.59	45.9	±1.5
MPXA4115A	16.7	115	400	4.59	45.9	±1.5
MPX4200A	29	200	400	4.59	25.5	±1.5
MPX4250A	36.3	250	400	4.6	20	±1.5
MPXV4006	0.87	6	10	4.6	750	±5.0
MPXV5004	0.57	3.9	10	3.9	1000	±2.5 (10–60°C)
MPX5010	1.45	10	75	4.5	450	±5.0
MPXV5010	1.45	10	75	4.5	450	±5.0
MPX5050	7.3	50	200	4.5	90	±2.5
MPX5100	14.5	100	400	4.5	45	±2.5
MPX5500	72.5	500	2000	4.5	9.0	±2.5
MPX5700A	100	700	2800	4.5	6.4	±2.5
MPX5999	150	1000	4000	4.5	4.5	±2.5

(1) Based on end point straight line fit method. Best fit straight line linearity error is approximately 1/2 of listed value.

Table 5. Pressure Sensors by Pressure Range

Device Series	Maximum Pressure Rating		Device Type
	psi	kPa	
MPXV4006G	.87	6	Signal Conditioned (On–chip)
MPXV5004G	.57	3.9	Signal Conditioned (On–chip)
MPX10D	1.45	10	Uncompensated
MPXV10G	1.45	10	Uncompensated — Next Gen., Low Profile Package
MPX12D	1.45	10	Uncompensated
MPX2010D	1.45	10	Compensated and Calibrated (On–chip)
MPX5010D	1.45	10	Signal Conditioning (On–chip)
MPXV5010G	1.45	10	Signal Conditioning (On–chip) — Small Outline Package
MPX2300D	5.80	40	Compensated and Calibrated — Medical Grade
MPX53D	7.30	50	Uncompensated
MPXV53G	7.30	50	Uncompensated — Small Outline Package
MPX2050D	7.30	50	Compensated and Calibrated (On–chip)
MPX5050D	7.30	50	Signal Conditioned (On–chip)
MPX2100A,D	14.50	100	Compensated and Calibrated (On–chip)
MPX4101A	14.80	102	Signal Conditioned (On–chip)
MPXA4100A	15.20	105	Signal Conditioned (On–chip) — Small Outline Package
MPX4105A	15.20	105	Signal Conditioned (On–chip)
MPX4115A	16.70	115	Signal Conditioned (On–chip)
MPXA4115A	16.70	115	Signal Conditioned (On–chip) — Small Outline Package
MPXS4115A	16.70	115	Signal Conditioned (On–chip) — Next Gen., Surface Mount Package
MPX5100A,D	16.70	115	Signal Conditioned (On–chip)
MPX2200A,D	29.00	200	Compensated and Calibrated (On–chip)
MPX4200A	29.00	200	Signal Conditioned (On–chip)
MPX4250A,D	36.30	250	Signal Conditioned (On–chip)
MPX5500D	72.5	500	Signal Conditioned (On–chip)
MPX5700A,D	1015	700	Signal Conditioned (On–chip)
MPX5999D	150	1000	Signal Conditioned (On–chip)

4

Table 6. MPX10/53 Series (Uncompensated)

Device Type	Measurement/Porting Options	Package Options	Pressure Range	
			0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)
4–Pin Basic Elements	Differential	Case 344–15	MPX10D, MPX12D	MPX53D
Ported Elements	Differential Port	Case 344C–01	MPX10DP, MPX12DP	—
	Gauge	Case 344B–01	MPX10GP, MPX12GP	MPX53GP
	Gauge Stovepipe	Case 344E–01	MPX10GS	—
8–Pin Ported Elements	Gauge (Small Outline)	Case 482A–01	MPXV10G	MPXV53G

Table 7. MPX2000 Series (Temperature Compensated and Calibrated On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range			
			0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	0 to 29 PSI (0 to 200 kPa)
4–Pin Basic Elements	Absolute	Case 344–15	—	—	MPX2100A	MPX2200A
	Differential	Case 344–15	MPX2010D	MPX2050D	MPX2100D	MPX2200D
Ported Elements	Absolute Port	Case 344B–01	—	—	MPX2100	MPX2200
	Differential Port	Case 344C–01	MPX2010DP	MPX2050DP	MPX2100	MPX2200
	Gauge	Case 344B–01	MPX2010GP	MPX2053GP	MPX2100	MPX2200
	Gauge Stovepipe	Case 344E–01	MPX2010GS	—	—	—
	Gauge Axial	Case 344F–01	MPX2010GSX	—	—	—

Table 8. MPX4000 Series (Signal Conditioned On–Chip)

Device Type	Measurement Options	Package Options	Pressure Range				
			0 to 0.87 PSI (0 to 6 kPa)	3 to 15 PSI (20 to 105 kPa)	2.3 to 14.7 PSI (15 to 102 kPa)	2.3 to 16.6 PSI (15 to 115 kPa)	3 to 36.2 PSI (20 to 250 kPa)
6–Pin Basic Elements	Absolute	Case 867–08	—	MPX4100A, MPX4105A	MPX4101A	MPX4115A	MPX4200A, MPX4250A MPX4250D
Ported Elements	Absolute Port	Case 867B–04	—	MPX4100AP	—	MPX4115AP	MPX4250AP MPX4250DP MPX4250GP
	Absolute Stovepipe	Case 867E–03	—	MPX4100AS	—	MPX4115AS	—
8–Pin Basic Elements	Absolute (Small Outline)	Case 482–01	—	MPXA4100A	—	MPXA4115A	—
	Gauge (Small Outline)	Case 482–01	MPXV4006G	—	—	—	—
Ported Elements	Absolute (Small Outline)	Case 482A–01	—	—	—	MPXA4115A	—
	Gauge (Small Outline)	Case 482A–01	MPXV4006GC	—	—	—	—

Table 9. MPX5000 Series (Signal Conditioned On–Chip)

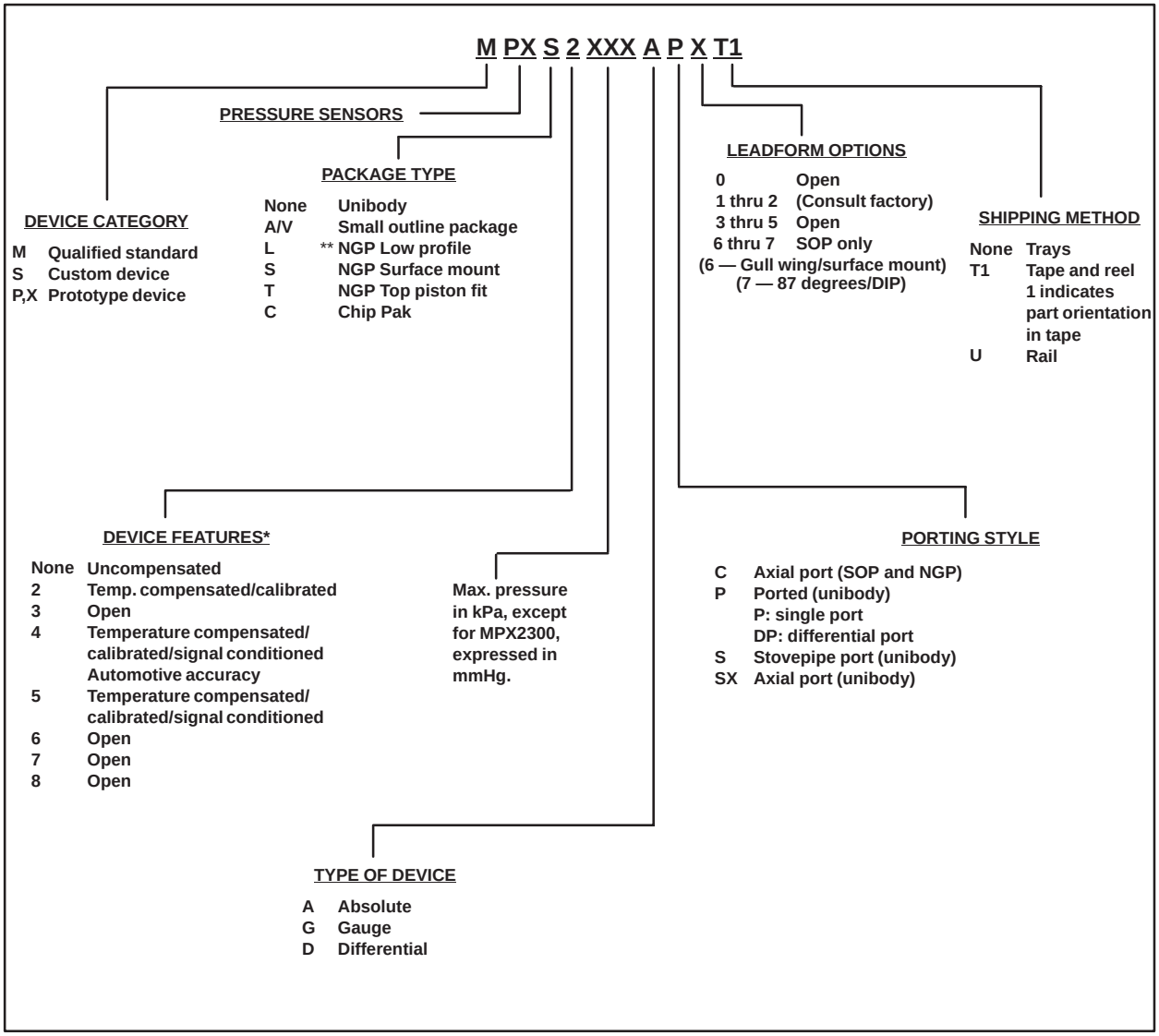
Device Type	Measure–ment Options	Package Options	Pressure Range				
			0 to 0.57 PSI (0 to 3.9 kPa)	0 to 1.45 PSI (0 to 10 kPa)	0 to 7.3 PSI (0 to 50 kPa)	0 to 14.5 PSI (0 to 100 kPa)	2.3 to 16.6 PSI (15 to 115 kPa)
6–Pin Basic Element	Absolute	Case 867–08	—	—	—	—	MPX5100A
	Differential	Case 867–08	—	MPX5010D	MPX5050D	MPX5100D	—
Ported Element	Absolute Port	Case 867B–04	—	—	—	—	MPX5100AP
	Differential Port	Case 867C–05	—	MPX5010DP	MPX5050DP	MPX5100DP	—
	Gauge	Case 867B–04	—	MPX5010GP	MPX5050GP	MPX5100GP	—
	Gauge Stovepipe	Case 867E–03	—	MPX5010GS	—	—	—
	Gauge Axial	Case 867F–03	—	MPX5010GSX	—	—	—
8–Pin Small Outline	Gauge	Case 482–01	MPXV5004G	MPXV5010G	MPXV5004G	MPXV4006G	—
	Gauge Axial	Case 482A–01	MPXV5004GC	MPXV5010GC	MPXV5004GC	MPXV4006GC	—

Table 10. MPX5000 Series (Signal Conditioned On–Chip) (continued)

Device Type	Measurement Options	Package Options	Pressure Range		
			0 to 75 PSI (0 to 500 kPa)	0 to 100 PSI (0 to 700 kPa)	0 to 150 PSI (0 to 1000 kPa)
6–Pin Basic Element	Absolute	Case 867–08	—	—	—
	Differential	Case 867–08	MPX5500D	MPX5700D	MPX5999D
Ported Element	Absolute Port	Case 867B–04	—	MPX5700DA	—
	Differential Port	Case 867C–05	MPX5500DP	MPX5700DP	—
	Gauge	Case 867B–04	—	MPX5700GP	—

4

Device Numbering System for Pressure Sensors



Note: Actual device marking may be abbreviated due to space constraints but packaging label will reflect full part number.

*Only applies to qualified and prototype devices. This does not apply to custom devices.

Examples: MPX10DP 10 kPa uncompensated, differential device in minibody package, ported, no leadform, shipped in trays.

MPXA4115A6T1 115 kPa automotive temp. compensated and calibrated device with signal conditioning, SOP surface mount with gull wing leadform, shipped in tape and reel.

4

Table 11. Smoke Integrated Circuits (CMOS Analog)

Type	Operating Voltage	Horn Modulation	Primary Power Source	Package Options	Interconnectable	Description
MC14467P1	6–12 V	4/6	DC	DIP	No	Ion
MC14468P	6–12 V	4/6	AC	DIP	Yes	Ion
MC14578P	3.5–14 V	No Horn Driver	DC	DIP	No	Smoke Comparator
MC145010DW	6–12 V	4/6	AC/DC	DIP/SOIC	Yes	Photo
MC145010DWR2	6–12 V	4/6	AC/DC	DIP/SOIC	Yes	Photo
MC145010P	6–12 V	4/6	AC/DC	DIP/SOIC	Yes	Photo
MC145011P	6–12 V	4/6	AC	DIP/SOIC	Yes	Photo
MC145012DW	6–12 V	NFPA *(new tone)*	AC/DC	DIP/SOIC	Yes	Photo
MC145012DWR2	6–12 V	NFPA *(new tone)*	AC/DC	DIP/SOIC	Yes	Photo
MC145012P	6–12 V	NFPA *(new tone)*	AC/DC	DIP/SOIC	Yes	Photo
MC145017P	6–12 V	NFPA *(new tone)*	DC	DIP	No	Ion
MC145018P	6–12 V	NFPA *(new tone)*	AC	DIP	Yes	Ion

Table 12. Alarm Integrated Circuits (CMOS Analog) *NEW PRODUCTS*

Type	Operating Voltage Min. Max.	Horn Modulation	Primary Power Source	Package Options	Description
MC14600P	6.0 V–12 V	4/6	DC	Plastic DIP (16 Pin)	• Alarm Detection • Horn Driver • Low Battery Detection • LED Driver
MC14600DW	6.0 V–12 V	4/6	DC	SOIC (Wide Body)	
MC14600DWR2	6.0 V–12 V	4/6	DC	SOIC/Tape & Reel (Wide Body)	

EVALUATION TOOLS

Table 13. Literature

Tool Set	Description
ASB200	**Motorola Sensor Development Board**
ASB201	**Uncompensated Series Sensor Module**
ASB202	**MPX2000 Series Sensor Module**
ASB205	**MPX5000 Series Sensor Module**
ASB210	**10″ H_2O Sensor Module**
KIT14600/D	**Alarm IC Sample Kit**
Marketing Literature	**Description**
DL200/D	Sensor Device Data Book, Rev 4
HB218/D	Pressure Sensor Distributor Handbook
SG162/D	SPD Selector Guide, Current Rev 30
Application Notes	**Description**
AN1516/D	Liquid Level Control Using a Motorola Pressure Sensor
AN1551/D	Low Pressure Sensing with the MPX2010 Pressure Sensor
AN1556/D	Designing Sensor Performance Specifications for MCS–Based Systems
AN1557/D	A Cookbook Approach to Designing a Differential–Signal Amplifier for Sensor Applications
AN1559/D	Application Considerations for a Switched Capacitor Accelerometer
AN1571/D	Digital Blood Pressure Meter
AN1573/D	Understanding Pressure and Pressure Measurement
AN1583/D	Motorola's Next Generation Piston Fit Pressure Sensor Packages
AN1584/D	"Very Low–Pressure'' Smart Sensing Solution with Serial Communications Interface
AN1585/D	High–Performance, Dynamically–Compensated Smart Sensor System
AN1586/D	Designing a Homemade Digital Output for Analog Voltage Output Sensors
AN1611/D	Impact and Tilt Measurement
AN1612/D	Shock and Mute Pager Applications Using Accelerometer
AN1620/D	Monolithic Integrated Solution for MAP Sensors
AN1621/D	Integrated Silicon Bulk Micromachined Barometric Pressure Sensor for Control Unit and External Mount
AN1622/D	EMC Considerations for Automotive Sensors
AN1636/D	Implementing Auto Zero for Integrated Pressure Sensors
AN1638/D	Offset Calibration of Gauge Pressure Sensors Using Parallel I/O Ports
AN1640/D	Reducing Accelerometer Susceptibility to BCI
AN1645/D	Micromachined Electromechanical Sensors for Automotive Applications
AN1646/D	Noise Considerations for Integrated Pressure Sensors
AN1651/D	Uncompensated Series Sensor Module
AN1652/D	MPX2000 Series Sensor Module
AN1653/D	MPX5000 Series Sensor Module
AN1654/D	10″ H_2O Sensor Module
AN1655/D	ASB200 Motorola Sensor Development Controller Board (MC68HC705JP7)
AN1660/D	Compound Coefficient Pressure Sensor PSPICE Models
AN1668/D	Washing Machine Sensor Selection
AN1690/D	Alarm IC General Applications Overview
AN4004/D	+2g Acceleration Sensing Module Based on a +40g Integrated Accelerometer

4

REFERENCE TABLE

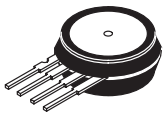
Table 14. Pressure Unit Conversion Constants (Most Commonly Used — Per International Conventions)

	PSI(1)	in. H_2O(2)	in. Hg(3)	K Pascal	millibar	cm H_2O(4)	mm Hg(5)
PSI(1)	1.000	27.681	2.036	6.8948	68.948	70.309	51.715
in. H_2O(2)	3.6126×10^{-2}	1.000	7.3554×10^{-2}	0.2491	2.491	2.5400	1.8683
in. Hg(3)	0.4912	13.595	1.000	3.3864	33.864	34.532	25.400
K Pascal	0.14504	4.0147	0.2953	1.000	10.000	10.1973	7.5006
millibar	0.01450	0.40147	0.02953	0.100	1.000	1.01973	0.75006
cm H_2O(4)	1.4223×10^{-2}	0.3937	2.8958×10^{-2}	0.09806	0.9806	1.000	0.7355
mm Hg(5)	1.9337×10^{-2}	0.53525	3.9370×10^{-2}	0.13332	1.3332	1.3595	1.000

NOTES: 1. PSI — pounds per square inch; 2. at 39°F; 3. at 32°F; 4. at 4°C; 5. at 0°C

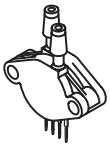
PRESSURE PACKAGING OPTIONS (Sizes not to scale)

4–PIN

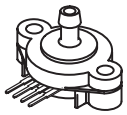


BASIC ELEMENT*
CASE 344–15
SUFFIX A / D

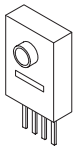
GAUGE PORT*
CASE 344B–01
SUFFIX AP / GP



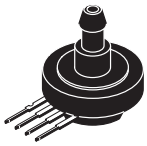
DUAL PORT*
CASE 344C–01
SUFFIX DP



AXIAL PORT
CASE 344F–01
SUFFIX ASX / GSX

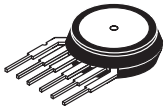


MEDICAL CHIP PAK*
CASE 423A–03



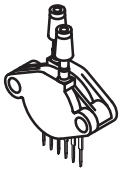
STOVEPIPE PORT
CASE 344E–01
SUFFIX AS/GS

6–PIN

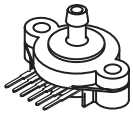


BASIC ELEMENT*
CASE 867–08
SUFFIX A / D

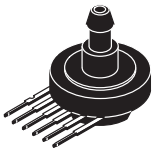
GAUGE PORT*
CASE 867B–04
SUFFIX AP / GP



DUAL PORT*
CASE 867C–05
SUFFIX DP

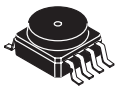


AXIAL PORT
CASE 867F–03
SUFFIX ASX / GSX

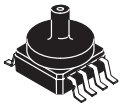


STOVEPIPE PORT
CASE 867E–03
SUFFIX AS / GS

8–PIN

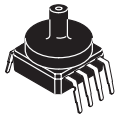


SMALL OUTLINE
(SURFACE MOUNT)*
CASE 482–01



SMALL OUTLINE
(PORTED/SURFACE MOUNT)*
CASE 482A–01

SMALL OUTLINE
(DIP)*
CASE 482B–03



SMALL OUTLINE
(PORTED/DIP)*
CASE 482C–03

*Indicates preferred packaging options

4

4

RF and IF Products

In Brief . . .

While Motorola is a worldwide leader in semiconductor products, there is not a category in which the selection is more diverse, or more complete, than in products designed for RF system applications. From MOS, bipolar power and signal transistors to integrated circuits, Motorola's RF components cover the entire spectrum from HF to microwave to personal communications. Yet, product expansion continues — not only to keep pace with the progressive needs of the industry, but to better serve the needs of designers for a reliable and comprehensive source of supply.

How to Use This Selector Guide

The RF Monolithic Integrated Circuits and the RF/IF Integrated Circuits products in this guide are divided into three major functional categories: RF Front End ICs, RF/IF Subsystem ICs and Frequency Synthesis. Each of these categories is further subdivided based on circuit functionality. This structure differentiates highly integrated subsystem ICs from fundamental circuit building blocks and discrete transistors.

The Small Signal Transistors, Medium Power Transistors, Power MOSFETs, Power Bipolar Transistors, Power Amplifier Modules and CATV Distribution Amplifiers are FIRST divided into major categories by power level. SECOND, within each category parts are listed by frequency band, except for small signal and medium power transistors, which are divided by application. Small signal transistor applications are low noise, linear amplifiers, switches, and oscillators. THIRD, within a frequency band, transistors are further grouped by operating voltage and, finally, output power.

To Replace Devices in an Existing Design

Call your local Motorola Sales Office or Distributor to determine Motorola's closest replacement device.

Applications Assistance

Applications assistance is only a phone call away — call the nearest Semiconductor Sales office or 1-800-521-6274.

Access Data On–Line!

Use the Motorola SPS World Marketing Internet Server to access Motorola Semiconductor Product data at http://motorola.com/sps/ or http://motorola.com/sps/rf/. The SPS World Marketing Server provides you with instant access to data sheets, selector guide information, package outlines, on–line technical support and much more.

Table of Contents

5

RF and IF Products

Table of Contents – continued

5

Design Tools and Data Available On–Line for Your Design–in Process at: http://motorola.com/sps/rf/designtds/designtd.html

Access LDMOS Models, Test Fixtures and Reference Designs On–line!

Visit our web pages for distribution of our NEW electro–thermal models for RF LDMOS transistors.

The url is: **http://sps.motorola.com/models/ldmos/ldmosmodels.html**

The new Motorola Electro Thermal (MET) model for RF LDMOS transistors is a nonlinear model that for the first time examines both electrical and thermal phenomena and can account for dynamic self–heating effects of device performance. It is specifically tailored to model high power RF LDMOS transistors used in base station, HDTV digital broadcast, and land mobile radio applications. Implemented in the HP–EEsof's® Libra® (V6.1 and V6.6) and Advanced Design System (ADS V1.1) harmonic balance simulators, the MET LDMOS model is capable of performing small–signal, large–signal, harmonic–balance, noise and transient simulations. Because of its ability to simulate self–heating effects, the MET model is more accurate than existing models, enabling circuit designers to predict prototype performance more accurately and reduce cycle time.

The model is available as a compiled code for all major computer platforms including Microsoft® Windows® 95, 98 and Windows NT® 4.0, Solaris® 2.6 and HP–UX® 10.2. The object code can easily be linked with HP–EEsof's Libra and ADS harmonic balance simulators.

Subscribe to our LDMOS Models mail list to get the latest news on the availability of newly released RF LDMOS Transistor Models. To subscribe, just fill out the RF LDMOS Transistor Model Subscription form on–line at http://sps.motorola.com/models/ldmos/ldmosmodels.html and you will receive notification of new models as they are posted.

AND, visit our web pages for distribution of Test Fixtures and Reference Designs.

The url is: **http://motorola.com/sps/rf/designtds/designtd.html**

The Test Fixture Library contains application specific solutions for select Motorola parts. Access the Test Fixture Library to determine which test fixture is most suitable for your application.

The Reference Design Library contains easy–to–copy, fully functional amplifier designs. They consist of "no tune" distributed element matching circuits designed to be as small as possible, include temperature compensated bias circuitry, and are designed to be used as "building blocks" for our customers.

5

You can use the Test Fixture Library Application and Loan Agreement to check out Test Fixture(s) from the Test Fixture Library as well as using the Test Fixture Library Application to request development of a new application specific solution. Use the Reference Design Library Application and Loan Agreement from the Reference Design Library to check out Reference Design(s).

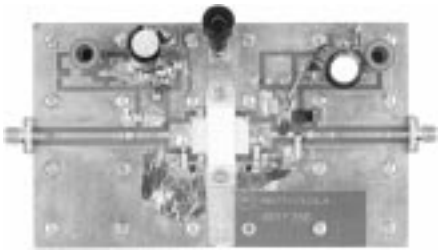


Figure 1. Test Fixture Example

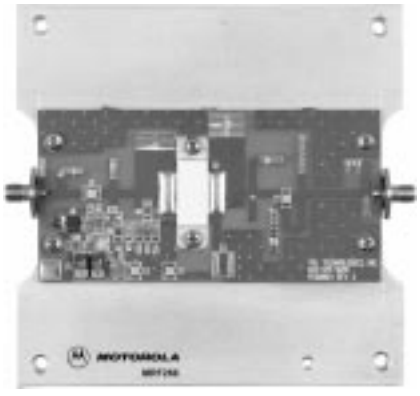


Figure 2. Reference Design Example

5

RF Front End ICs

Motorola's RF Front End integrated circuit devices provide an integrated solution for the personal communications market. These devices are available in plastic SO–8, SO–16, SOT–143, TSSOP–16, TSSOP–16EP, Micro–8, TSSOP–20EP, LQFP–48 or PFP–16 packages.

Evaluation Boards

Evaluation boards are available for RF Front End Integrated Circuits. For a complete list of currently available boards and ones in development for newly introduced product, please contact your local Motorola Distributor or Sales Office.

Table of Contents

RF Front End ICs

RFICs

Downconverters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	LNA Gain dB (Typ)	LNA NF dB (Typ)	Mixer Conv. Gain dB (Typ)	Mixer NF dB (Typ)	Case No./ Package	System Applicability
MC13142[18b]	DC to 1800	2.7 to 6.5	13.5	17	1.8	–3.0	12	751B/ SO–16	ISM, Cellular, PCS
MRFIC1814[18b]	1800 to 2000	2.7 to 4.5	10	17	2.5	8.0	10	948C/ TSSOP–16	DCS1800, PCS, PHS

Upconverters/Exciters

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current mA (Typ)	Conv. Gain dB (Typ)	Output IP3 dBm (Typ)	Case No./ Package	System Applicability
MRFIC0954[18b]★	800 to 1000	2.7 to 5.0	65	5.0	31	28	948M/ TSSOP–20EP	CDMA, TDMA, ISM
MRFIC1813[18b]	1700 to 2000	2.7 to 4.5	25	0.1	15	11	948C/ TSSOP–16	DCS1800, PCS
MRFIC1854[18b]★	1700 to 2000	2.7 to 5.0	70	5.0	31	23	948M/ TSSOP–20EP	CDMA, TDMA, PCS

Power Amplifiers

5

Device	Freq. Range MHz	Supply Volt. Range Vdc	Saturated P_{out} dBm (Typ)	PAE % (Typ)	Gain P_{out}/P_{in} dB (Typ)	Case No./ Package	System Applicability
MRFIC0917[18e]	800 to 1000	2.7 to 5.5	34.5	45	22.5	978/PFP–16	GSM
MRFIC0919[18b,46a]	800 to 1000	3.0 to 5.5	35.3	48	32.3	948L/ TSSOP–16EP	GSM
MRFIC1817[18e]	1700 to 2000	2.7 to 5.0	33.5	42	30.5	978/PFP–16	DCS1800, PCS
MRFIC1818[18e]	1700 to 2000	2.7 to 6.0	34.5	42	31.5	978/PFP–16	DCS1800, PCS
MRFIC1819[18b,46a]	1700 to 2000	3.0 to 5.0	33	40	27	948L/ TSSOP–16EP	DCS1800, PCS
MRFIC1856[18b,46a]	800 to 1000	3.0 to 5.6	32	50	32	948M/ TSSOP–20EP	TDMA, CDMA, AMPS
	1700 to 2000		30	35	30		TDMA, CDMA, PCS
MRFIC2006[18b]	500 to 1000	1.8 to 4.0	15.5	25	23	751/SO–8	Cellular, ISM, CT2

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

[46]To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

RF Front End ICs (continued)

RF Building Blocks

Amplifiers

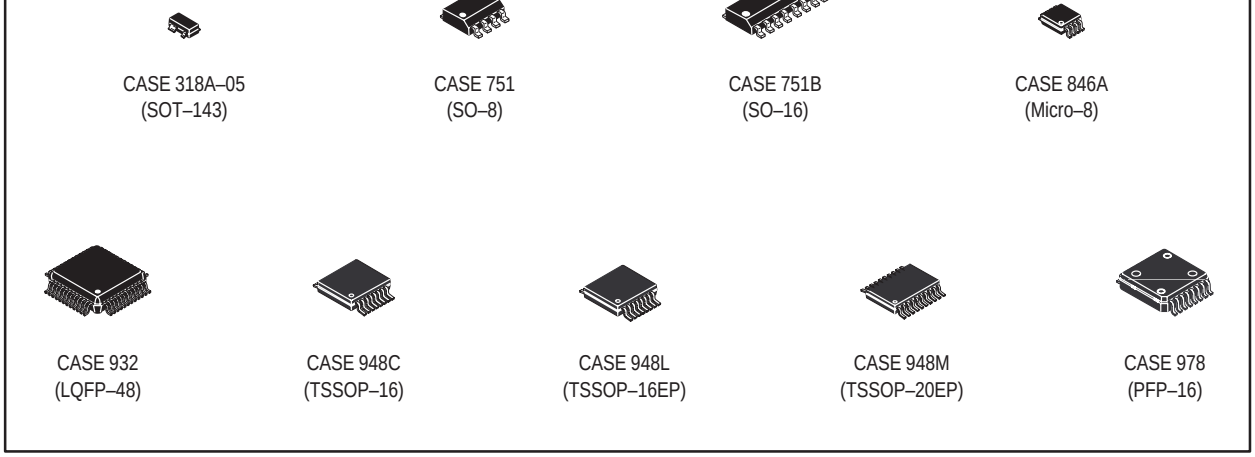
Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Small Signal Gain dB (Typ)	Output IP3 dBm (Typ)	NF dB (Typ)	Case No./ Package	System Applicability
MC13144[18b]	100 to 2000	1.8 to 6.0	8.5	1	17	12	1.4	751/SO–8	ISM, PCS, Cellular
MRFIC0915[18c]	100 to 2500	2.7 to 5.0	2.0	–	16.2	4.0	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0916[18c]	100 to 2500	2.7 to 5.0	4.7	–	18.5	11	1.9	318A/ SOT–143	ISM, PCS, Cellular
MRFIC0930DM[18b]	800 to 1000	2.7 to 4.5	8.5	20	19	10	1.7	846A/ Micro–8	GSM, AMPS, ISM
MRFIC1501[18b]	1000 to 2000	3.0 to 5.0	5.9	–	18	10	1.1	751/SO–8	GPS
MRFIC1808DM[18b]	1700 to 2100	2.7 to 4.5	5.0	8.0	18	13	1.6	846A/ Micro–8	DCS1800, PCS
MRFIC1830DM[18b]	1700 to 2100	2.7 to 4.5	9.0	20	18.5	8.5	2.1	846A/ Micro–8	DCS1800, PCS

Mixers

Device	RF Freq. Range MHz	Supply Volt. Range Vdc	Supply Current mA (Typ)	Standby Current μA (Typ)	Conv. Gain dB (Typ)	Input IP3 dBm (Typ)	Case No./ Package	System Applicability
MC13143[18b]	DC to 2400	1.8 to 6.0	4.1	–	–2.6	16	751/SO–8	ISM, PCS, Cellular

[18]Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

RF Front End Integrated Circuit Packages



5

RF/IF Subsystems

Table of Contents

5

RF/IF Subsystems

Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC} (Typ)	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	CVSD Compatible	Low Battery Detect	Notes	Suffix/ Package
MC13109A	2.0 to 5.5 V	Active Mode 6.7 mA Inactive Mode 40 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13110A MC13110B	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13111A MC13111B	2.7 to 5.5 V	Active Mode 8.5 mA Inactive Mode 15 µA	✓	✓	✓	–	✓	CT–0	FB/848B, FTA/932
MC13145	2.7 to 6.5 V	Active Mode 27 mA Inactive Mode 10 µA	✓	–	–	✓	–	Receiver with coilless demod CT–900	FTA/932
MC13146	2.7 to 6.5 V	Active Mode 18 mA Inactive Mode 10 µA	–	–	–	✓	–	Transmitter with VCO CT–900	FTA/977
MC33410	2.7 to 5.5 V	Active Mode 13 mA Inactive Mode 10 µA	✓	✓	–	✓	✓	Digital Baseband CT–900	FTA/932
MC33411A MC33411B	2.7 to 5.5 V	Active Mode 15 mA Inactive Mode 10 µA	✓	✓	✓	–	✓	Analog Baseband CT–900	FTA/932

5

GPS Subsystem ICs

Device	RF Freq (MHz)	IF Freq (MHz)	V_{CC} (V)	I_{CC} (mA) (Typ)	Dual Conversion Receiver	Dual Loop PLL	Limiting Amplifier	Variable Gain IF Amplifier	Case No.
MRFIC1502	1575	9.5	4.5 to 5.5	52	✓	✓	–	–	932
MRFIC1504★	1575	4.1	2.7 to 3.3	28	✓	✓	✓	✓	932

★New Product

Receivers

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC2800	1.1 to 3.0 V	1.5 mA	–110 dBm	75 MHz	455 kHz	–	✓	>1.2 kb	Pager Applications	FTA/873C
MC3356	3.0 to 9.0 V	20 mA	30 µV	150 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	DW/751D
MC3361B	2.0 to 8.0 V	3.9 mA	2.6 µV	60 MHz	455 kHz	✓	–	>4.8 kb	Squelch and Scan	D/751B
MC3361C	2.0 to 8.0 V	2.8 mA								D/751B
MC3371	2.0 to 9.0 V	6.0 mA	1.0 µV	100 MHz			✓ 60 dB		RSSI	D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC3374	1.1 to 3.0 V	1.5 mA	0.5 µV	75 MHz		–	–		Low Battery Detect	FTB/873
MC13135	2.0 to 6.0 V	4.0 mA	1.0 µV	200 MHz	10.7 MHz/ 455 kHz	–	✓ 70 dB	>4.8 kb	Voltage Buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136									Voltage Buffered RSSI, Ceramic Quad Detector	DW/751E
MC13150	2.5 to 6.0 V	1.7 mA	1.0 µV	500 MHz		✓	✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977
MC13156	2.0 to 6.0 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–	✓ 80 dB	500 kb	CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2.0 to 6.0 V	6.0 mA		950 MHz				>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873

IFs

Device	V_{CC}	I_{CC} (Typ)	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC13055	3.0 to 12 V	25 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	D/751B
MC13155	3.0 to 6.0 V	7.0 mA	100 µV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

5

Transmitters

Device	V_{CC}	I_{CC} (Typ)	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Package
MC13176	2.0 to 5.0 V	40 mA	80 dBm	1.0 GHz	5.0 MHz	$f_{out} = 32 \times f_{ref}$, includes power down function	D/751B

Miscellaneous Functions

ADCs/DACs

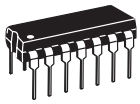
Device	Function	I/O Format	Resolution	Number of Analog Channels	On–Chip Oscillator	Other Features	Suffix/ Package
MC144110	DAC	Serial	6 Bits	6	–	Emitter–Follower Outputs	DW/751D
MC144111				4			DW/751G
MC145050	ADC		10 Bits	11	–	Successive Approximation	P/738, DW/751D
MC145051					✓		
MC145053				5			P/646, D/751A

Encoders/Decoders

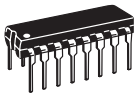
Device	Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Suffix/ Package
MC145026	Encoder	Depends on Decoder	Depends on Decoder	Depends on Decoder	Simplex	P/648, D/751B
MC145027	Decoder	5	243	4	Simplex	P/648, DW/751G
MC145028		9	19,683	0	Simplex	

5

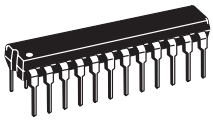
RF/IF Subsystems Packages



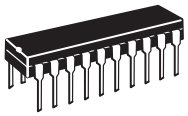
CASE 646
P SUFFIX
(DIP–14)



CASE 648
P SUFFIX
(DIP–16)



CASE 724
P SUFFIX
(DIP–24)

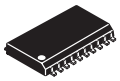


CASE 738
P SUFFIX
(DIP–20)

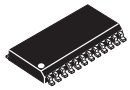
CASE 751
D SUFFIX
(SO–8)

CASE 751A
D SUFFIX
(SO–14)

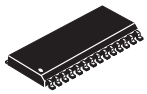
CASE 751B
D SUFFIX
(SO–16)



CASE 751D
DW SUFFIX
(SO–20L)

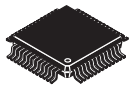


CASE 751E
DW SUFFIX
(SO–24L)



CASE 751F
DW SUFFIX
(SO–28L)

CASE 751G
DW SUFFIX
(SO–16W)



CASE 848B
FB SUFFIX
(QFP–52)

CASE 873
FB, FTB SUFFIX
(LQFP–32)

CASE 873C
FTA SUFFIX
(LQFP–32)

CASE 932
FTA SUFFIX
(LQFP–48)

CASE 948D
DT SUFFIX
(TSSOP–20)

CASE 948F
DTB SUFFIX
(TSSOP–16)

CASE 977
FTA SUFFIX
(LQFP–24)

5

5

Frequency Synthesis

Table of Contents

5

Frequency Synthesis

Single PLL Synthesizers

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Features	Device	Suffix/ Case
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface	MC145151–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Parallel Interface, Uses External Dual–Modulus Prescaler	MC145152–2	DW/751F
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface	MC145157–2	DW/751G
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5 V	Serial Interface, Uses External Dual–Modulus Prescaler	MC145158–2	DW/751G
100 @ 3.0 V 185 @ 4.5 V	2.7 to 5.5	2 @ 3 V 6 @ 5 V	Serial Interface, Auxiliary Reference Divider, Evaluation Kit – MC145170EVK	MC145170–2	P/648, D/751B, DT/948C
1000	2.7 to 5.5	4.25	4–Line Parallel Interface	MC12181	D/751B
1100	2.7 to 5.5	7 @ 5 V	Serial Interface, Standby, Auxiliary Reference Divider, Evaluation Kit – MC145191EVK	MC145193(46a)	F/751J, DT/948D
2000	2.7 to 5.5	4 @ 3 V	Serial Interface, Standby, Auxiliary Reference Device, Evaluation Kit – MC145202EVK	MC145202–2(46a)	F/751J, DT/948D
2500	2.7 to 5.5	9.5	Serial Interface	MC12210	D/751B, DT/948E
2800	4.5 to 5.5	3.5	Fixed Divider	MC12179	D/751

(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

Dual PLL Synthesizers

5

Maximum Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Device	Suffix/ Case
60 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162	P/648, D/751B
85 @ 3.0 V both loops	2.5 to 5.5	3 @ 3 V	Serial Interface, Standby	MC145162–1	D/751B
550, 60	1.8 to 3.6	3	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145181	FTA/873C
1100 both loops	2.7 to 5.5	12	Serial Interface, Standby, Evaluation Kit – MC145220EVK	MC145220	F/803C, DT/948D
1200, 550	1.8 to 3.6	4	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145225	FTA/873C
2200, 550	1.8 to 3.6	5	10 MHz Serial Interface, Multiple Standby Modes, Dual 8–Bit DACs, Voltage Multiplier for Phase Detectors (See Note).	MC145230	FTA/873C

NOTE: The MC145230EVK development system may be used with the MC145181, MC145225, or MC145230. The MC145230 is soldered to a tested board; MC145181, MC145225 and MC145230 device samples are included. The user must supply the VCOs for the MC145181.

PLL Building Blocks

Prescalers

Frequency (MHz)	Divide Ratios	Single or Dual Modulus	Supply Voltage (V)	Supply Current (mA)	Features	Device	Suffix/ Case
225	32/33	Dual	4.5 to 5.5, 5.5 to 9.5	7.8 max		MC12015	D/751
225	40/41	Dual	4.5 to 5.5, 5.5 to 9.5	7.8 max		MC12016	D/751
225	64/65	Dual	4.5 to 5.5, 5.5 to 9.5	7.8 max		MC12017	D/751
225	20/21	Dual	4.5 to 5.5	7.5 max		MC12019	D/751
1100	8/9, 16/17	Dual	4.5 to 5.5	5.3 max (unloaded)		MC12026A	D/751
1100	127/128, 255/256	Dual	4.5 to 5.5	6.5 max (at 5.0 V)		MC12038A	D/751
1100	64/65, 128/129	Dual	2.7 to 5.5	2.0 max	Low Power	MC12052A	D/751
1100	64/65, 128/129	Dual	2.7 to 5.5	2.5 max	Low Power, Standby	MC12053A	D/751
1100	126/128, 254/256	Dual	2.7 to 5.5	2.0 max	Low Power	MC12058	D/751
1100	10,20,40,80	Single	4.5 to 5.5	5.0 max		MC12080	D/751
1100	2, 4, 8	Single	2.7 to 5.5	4.5 max	Standby	MC12093	D/751
2000	32/33, 64/65	Dual	4.5 to 5.5	12 max		MC12034A	D/751
2000	64/65, 128/129	Dual	2.7 to 5.5	2.6 max	Low Power	MC12054A	D/751
2500	2, 4	Single	2.7 to 5.5	14 max	Standby	MC12095	D/751
2800	64, 128, 256	Single	4.5 to 5.5	11.5 max		MC12079	D/751
2800	64, 128	Single	4.5 to 5.5	14.5 max		MC12089	D/751

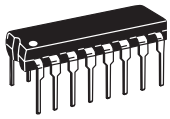
Voltage Control Oscillators

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
1300	2.7 to 5.5	Two high drive open collector outputs (Q, QB), Adjustable output amplitude	MC12147	D/751
1100	5.0	Single load ECL type output	MC12148	D/751
1300	2.7 to 5.5	Two high drive open collector outputs (Q, QB), Adjustable output amplitude, Low drive output for prescaler	MC12149	D/751

Phase–Frequency Detectors

Frequency (MHz)	Supply Voltage (V)	Features	Device	Suffix/ Case
800 (Typ)	4.75 to 5.5	MECL10H compatible	MCH12140	D/751
800 (Typ)	4.2 to 5.5	100K ECL compatible	MCK12140	D/751

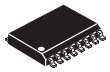
RF/IF Integrated Circuits Packages



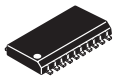
CASE 648
P SUFFIX
(DIP–16)

CASE 751
D SUFFIX
(SO–8)

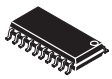
CASE 751B
D SUFFIX
(SO–16)



CASE 751G
DW SUFFIX
(SO–16W)



CASE 751J
F SUFFIX
(SO–20)

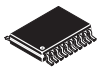


CASE 803C
F SUFFIX
(SO–20)

CASE 873C
FTA SUFFIX
(LQFP–32)

CASE 948C
DT SUFFIX
(TSSOP–16)

CASE 948D
DT SUFFIX
(TSSOP–20)



CASE 948E
DT SUFFIX
(TSSOP–20)

5

Motorola RF Discrete Transistors

Motorola offers the most extensive group of RF Discrete Transistors offered by any semiconductor manufacturer anywhere in the world today.

From Bipolar to FET, from Low Power to High Power, the user can choose from a variety of packages. They include plastic and ceramic that are microstrip circuit compatible or surface mountable. Many are designed for automated assembly equipment.

Major sub–headings are Small Signal, Medium Power, Power MOSFETs and Bipolar Transistors.

Table of Contents

5

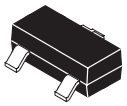
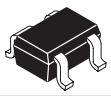
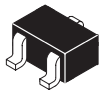
Motorola RF Small Signal Transistors

Motorola's broad line of RF Small Signal Transistors includes NPN Silicon Bipolar Transistors characterized for low noise amplifiers, mixers, oscillators, multipliers, non–saturated switches and low–power drivers.

These devices are available in a wide variety of package types. Most of these transistors are fully characterized with s–parameters.

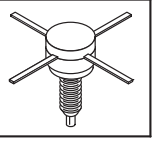
Plastic Packages

Table 1. Plastic

Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	NF_{min} @ f Typ dB	NF_{min} @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 318–08/6 — SOT–23									
MMBR941LT1(18c)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941LT3(18d)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR941BLT1(18c)	8.0	15	2.1	2000	8.5	2000	10	50	
MMBR951LT1(18c)	8.0	30	2.1	2000	7.5	2000	10	100	
Case 318M — SOT–343									
MBC13904T1(18c,46b)	11	15	1.2	1000	15	1000	5.0	15	
Case 419 — SC–70/SOT–323									
MRF947T1(18c,d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947T3(18d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947AT1(18c)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF947BT1(18c,d)	8.0	15	2.1	2000	10.5	1500	10	50	
MRF957T1(18c)	9.0	30	2.0	2000	9.0	1500	10	100	
MRF1047T1(18c)	12	15	1.0	1000	13	1000	5.0	45	
Case 463/1 — SC–90/SC–75									
MRF949T1(18c)	9.0	15	1.5	1000	14	1000	–	50	
MRF959T1(18c)	9.0	30	1.6	1000	8.0	1000	–	100	

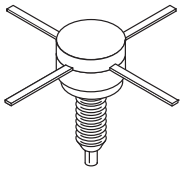
Ceramic SOE Case

Table 2. Ceramic SOE Case

Device	Gain–Bandwidth @ f_T Typ GHz	Gain–Bandwidth @ I_C mA	NF @ f Typ dB	NF @ f MHz	Gain @ f Typ dB	Gain @ f MHz	Maximum Ratings $V_{(BR)CEO}$ Volts	Maximum Ratings I_C mA	Package
Case 244A/1									
MRF587	5.5	90	3.0	500	13	500	15	200	

(17)PNP
(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.
(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

RF Small Signal Transistors Packages



CASE 244A
STYLE 1

CASE 318–08
STYLE 6
(SOT–23)

CASE 318M
(SOT–343)

CASE 419
(SC–70/SOT–323)

CASE 463
STYLE 1
(SC–90/SC–75)

5

Motorola RF Medium Power Transistors

RF Medium Power Transistors are used in portable transmitter applications and low voltage drivers for higher power devices. They can be used for analog cellular, GSM and the newer digital handheld cellular phones. GaAs, LDMOS and Bipolar devices are available. RF Medium Power Transistors are supplied in Motorola's high performance PLD line of surface mount power RF packages. Other applications include talkback pagers, wireless modems and LANs, cable modems, highspeed drivers and instrumentation.

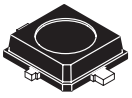
Discrete Wireless Transmitter Devices

Device	Freq. MHz	V_{DD} V	Typical Output Power dBm	Typical Drain Eff. %	Typical Gain dB	Semiconductor Technology	Case. No./ Package
MRF9382T1 (18f, 46a)	900	6.0	36.5	65	10.5	LDMOS	449/ PLD–1
MRF9482T1 (18f, 46a)	900	4.8	36.0	65	10	LDMOS	449/ PLD–1

(18) Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units.

(46) To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

RF Medium Power Transistors Packages



CASE 449
(PLD–1)

Motorola RF High Power Transistors

RF Power MOSFETs

Motorola RF Power MOSFETs are constructed using a planar process to enhance manufacturing repeatability. They are *N–channel field effect transistors* with an oxide insulated gate which controls vertical current flow.

Compared with bipolar transistors, RF Power FETs exhibit higher gain, higher input impedance, enhanced thermal stability and lower noise. The FETs listed in this section are specified for operation in RF Power Amplifiers and are grouped by frequency range of operation and type of application. Arrangement within each group is first by order of voltage then by increasing output power.

Table 1. To 150 MHz HF/SSB – Vertical MOSFETs

For military and commercial HF/SSB fixed, mobile and marine transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} Typical Gain dB @ 30 MHz	Typical IMD d_3 dB	Typical IMD d_{11} dB	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB							
MRF171A★	30	0.45	20	–32	—	1.52	211–07/2
V_{DD} = 50 Volts, Class AB							
MRF148A	30	0.5	18	–35	–60	1.5	211–07/2
MRF150	150	3	17	–32	–60	0.6	211–11/2
MRF154	600	12	17	–25	—	0.13	368/2
MRF157	600	6	20	–25	—	0.13	368/2

Table 2. To 225 MHz VHF AM/FM – Vertical MOSFETs

For VHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Efficiency Typical %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB						
MRF134	5	0.2	14/150	55	10	211–07/2
MRF136	15	0.38	16/150	60	3.2	211–07/2
MRF171A★	45	0.56	19.5/150	65	1.52	211–07/2
MRF173	80	4	13/150	65	0.8	211–11/2
MRF174	125	8.3	11.8/150	60	0.65	211–11/2
MRF141	150	15	10/175	55	0.6	211–11/2
MRF141G	300	15	13/175	55	0.35	375/2
V_{DD} = 50 Volts, Class AB						
MRF151	150	7.5	13/175	45	0.6	211–11/2
MRF151G	300	7.5	16/175	55	0.35	375/2

★New Product

5

RF Power MOSFETs (continued)

Table 3. To 500 MHz VHF/UHF AM/FM

For VHF/UHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
V_{DD} = 28 Volts, Class AB – Vertical MOSFETs						
MRF158	2	0.035	17.5/500	52	13.2	305A/2
MRF160	4	0.08	17/500	55	7.2	249/3
MRF166C	20	0.62	16/500	55	2.5	319/3
MRF166W	40	1	16/500	55	1.0	412/1
MRF177	100	6.4	12/400	60	0.65	744A/2
MRF275L★	100	13.2	8.8/500	55	0.65	333/2
MRF275G	150	10.7	11.2/500	55	0.44	375/2

Table 4. To 520 MHz

Designed for broadband VHF & UHF commercial and industrial applications. The high gain and broadband performance of these devices make them ideal for large–signal, common–source amplifier applications in 12.5/7.5 volt mobile, portable and base station operation.

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
VHF & UHF, V_{DD} = 7.5 Volts, Class AB, Land Mobile Radio – LDMOS Die						
MRF1517T1(18f,46a)	8	0.6	11/520	55	2.0	466/1
VHF & UHF, V_{DD} = 7.5/12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die						
MRF1513T1(18f,46a)	3	0.3	11/520	55	2.0	466/1
MRF1511T1(18f,46a)	8	0.6	11.5/175	55	2.0	466/1
VHF & UHF, V_{DD} = 12.5 Volts, Class AB, Land Mobile Radio – LDMOS Die						
MRF1518T1(18f,46a)	8	0.6	11/520	55	2.0	466/1

5

Table 5. To 1.0 GHz – Lateral MOSFETs

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	IMD dBc	Package/Style
470 – 1000 MHz, V_{DD} = 28 Volts, Class AB – LDMOS Die							
MRF373★	60	2.7	14.7/860	56	1.0	—	360B/1
MRF373S★	60	2.7	14.7/860	56	0.75	—	360C/1
MRF372(9)	180 (PEP)	7.2	14.0/860	35	0.4	–30	375B/2
MRF374(46a)	100 (PEP)	5.5	13.5/860	36	0.5	–31	375F/1
470 – 1000 MHz, V_{DD} = 50 Volts, Class AB – LDMOS Die							
MRF376(9)	240	9.6	14/860	55	0.3	—	TBD

(9)In development.

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

RF Power MOSFETs (continued)

Table 5. To 1.0 GHz – Lateral MOSFETs (continued)

Device	P_{out} Output Power Watts	P_{in} Input Power Typical Watts	G_{ps} (Typ)/Freq. dB/MHz	η Eff., Typ %	θ_{JC} °C/W	Package/Style
800 – 1.0 GHz, V_{DD} = 26 Volts, Class AB – LDMOS Die						
MRF6522–5R1(18a,46a)	5	0.06	18/960	53	15	458A/1
MRF6522–10R1(18a,46a)	10	0.16	17.5/960	55	6.0	458A/1
MRF9045(25,46a)	45	0.9	17/900	38	1.3	360B/1
MRF9045S(25,46a)	45	0.9	17/900	38	1.3	360C/1
MRF9045M(25,46b)	45	1.13	16/900	50	1.2	1265/—
MRF6522–70(18i)★	70	1.8	16/921–960	58	1.1	465D/1
MRF187(25)★	85	4.3	13/880	33	0.7	465/1
MRF187S(25)★	85	4.3	13/880	33	0.7	465A/1
MRF9085(25,46a)	90	1.8	17/900	38	0.6	465/1
MRF9085S(25,46a)	90	1.8	17/900	38	0.6	465A/1
MRF9180(46a)	180	3.6	17/900	38	0.4	375D/2
800 – 1.0 GHz, V_{DD} = 28 Volts, Class AB – LDMOS Die						
MRF181SR1(18a,25,46a)	8	0.16	17/945	35	3.6	458/1
MRF181ZR1(18a,25,46a)	8	0.16	17/945	35	3.6	458A/1
MRF182	30	1.2	14/945	58	1.75	360B/1
MRF182S(18a)	30	1.2	14/945	58	1.75	360C/1
MRF183(25)	45	2.3	13.5/945	38	1.5	360B/1
MRF183S(18a,25)	45	2.3	13.5/945	38	1.5	360C/1
MRF184	60	1.9	13.5/945	60	1.1	360B/1
MRF184S(18a)	60	1.9	13.5/945	60	1.1	360C/1
MRF6522–60★	60	2.0	14/960	60	1.1	360B/1
MRF185(3)	85	3.4	14/960	53	0.7	375B/2
MRF186(3,25)★	120	7.6	12/945	53	0.6	375B/2

Table 6. To 2.1 GHz – Lateral MOSFETs

Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
1805 – 1990 MHz, V_{DD} = 26 Volts – LDMOS Die (GSM1800, GSM1900 and PCS TDMA)						
MRF18060A★	60	AB	26/500	13/1805–1880	0.97	465/1
MRF18060AS★	60	AB	26/500	13/1805–1880	0.97	465A/1
MRF18060B(46a)	60	AB	26/500	14/1930–1990	0.97	465/1
MRF18060BS(46a)	60	AB	26/500	14/1930–1990	0.97	465A/1
MRF18090A(46a)	90	AB	26/750	14/1805–1880	0.7	465B/1
MRF18090B(46a)	90	AB	26/750	13.5/1930–1990	0.7	465B/1

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(25)Two–tone Performance, Power is PEP

(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

5

RF Power MOSFETs (continued)

Table 6. To 2.1 GHz – Lateral MOSFETs (continued)

Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
1.9 GHz, V_{DD} = 26 Volts – LDMOS Die (PCS CDMA)						
MRF19030(25,46a)	30	AB	26/250	13/1990	2.0	465E/1
MRF19030S(25,46a)	30	AB	26/250	13/1990	2.0	465F/1
MRF19045(25,46b)	45	AB	26/450	14/1990	0.84	465E/1
MRF19045S(25,46b)	45	AB	26/450	14/1990	0.84	465F/1
MRF19060(25)★	60	AB	26/500	12.5/1990	0.97	465/1
MRF19060S(25)★	60	AB	26/500	12.5/1990	0.97	465A/1
MRF19090(25)★	90	AB	26/750	11.5/1990	0.65	465B/1
MRF19090S(18a,25)★	90	AB	26/750	11.5/1990	0.65	465C/1
MRF19085(25,46b)	90	AB	26/750	12.5/1990	0.64	465/1
MRF19085S(25,46b)	90	AB	26/750	12.5/1990	0.64	465A/1
MRF19120(3,25,46a)	120	AB	26/1000	11.9/1990	0.45	375D/2
MRF19120S(3,25,46a)	120	AB	26/1000	11.9/1990	0.45	375E/2
MRF19125(25,46b)	125	AB	26/1200	12.5/1990	0.53	465B/1
MRF19125S(25,46b)	125	AB	26/1200	12.5/1990	0.53	465C/1
2.0 GHz, V_{DD} = 26 Volts – LDMOS Die						
MRF281SR1(18a,25,46a)	4	A, AB	26/25	13.6/2000	8.75	458/1
MRF281ZR1(18a,25,46a)	4	A, AB	26/25	13.6/2000	8.75	458A/1
MRF282SR1(18a,25,46a)	10	A, AB	26/75	12.5/2000	2.9	458/1
MRF282ZR1(18a,25,46a)	10	A, AB	26/75	12.5/2000	2.9	458A/1
MRF284(25)	30	A, AB	26/200	10.5/2000	2.0	360B/1
MRF284SR1(18a,25)	30	A, AB	26/200	10.5/2000	2.0	360C/1
MRF286(25,46a)	60	A, AB	26/500	10.6/2000	0.73	465/1
MRF286S(25,46a)	60	A, AB	26/500	10.6/2000	0.73	465A/1
2.1 GHz, V_{DD} = 28 Volts – LDMOS Die (W–CDMA, UMTS)						
MRF21030(25,46a)	30	AB	28/250	13.5/2170	2.0	465E/1
MRF21030S(25,46a)	30	AB	28/250	13.5/2170	2.0	465F/1
MRF21060(25)★	60	AB	28/500	12.5/2170	1.02	465/1
MRF21060S(25)★	60	AB	28/500	12.5/2170	1.02	465A/1
MRF21090(25,46a)	90	AB	28/750	11.7/2170	0.65	465B/1
MRF21090S(25,46a)	90	AB	28/750	11.7/2170	0.65	465C/1
MRF21120(3,25,46a)	120	AB	28/1000	11.6/2170	0.45	375D/2
MRF21120S(3,25,46a)	120	AB	28/1000	11.6/2170	0.45	375E/2
MRF21125(25,46a)	125	AB	28/1300	12.5/2170	0.53	465B/1
MRF21125S(25,46a)	125	AB	28/1300	12.5/2170	0.53	465C/1
MRF21180(3,25,46a)	160	AB	28/1700	11.3/2170	0.39	375D/2
MRF21180S(3,25,46a)	160	AB	28/1700	11.3/2170	0.39	375E/2

(3)Internal Impedance Matched Push-Pull Transistors

(18)Tape and Reel Packaging Option Available by adding suffix: a) R1 = 500 units; b) R2 = 2,500 units; c) T1 = 3,000 units; d) T3 = 10,000 units; e) R2 = 1,500 units; f) T1 = 1,000 units; g) R2 = 4,000 units; h) R1 = 1,000 units; i) R3 = 250 units.

(25)Two–tone Performance, Power is PEP

(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

RF Power Bipolar Transistors

Motorola's broad line of bipolar RF power transistors are characterized for operation in RF power amplifiers. Typical applications are in base stations, military and commercial landmobile, avionics and marine radio transmitters. Groupings are by frequency band and type of application. Within each group, the arrangement of devices is by major supply voltage rating, then in the order of increasing output power. All devices are NPN polarity except where otherwise noted.

UHF Transistors

Table 1. 100 – 500 MHz Band

Designed for UHF military and commercial aircraft radio transmitters.

Device	P_{out} Output Power Watts	P_{in} (Max) Input Power Watts	G_{PE} (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class C					
MRF392(3)	125	19.8	8/400	0.7	744A/1
MRF393(3)	100	18	7.5/500	0.7	744A/1

900 MHz Transistors

Table 2. 900 – 960 MHz Band

Designed specifically for the 900 MHz mobile radio band, these devices offer superior gain, ruggedness, stability and broadband operation. Devices are for mobile and base station applications.

Device	P_{out} Output Power Watts	Class	P_{in}(Max) Input Power Watts	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 24 Volts — Si Bipolar						
MRF858S	3.6 (CW)	A	0.29	11/900	6.9	319A/2
MRF897(3)	30	AB	3	10/900	1.7	395B/1
MRF897R(3)	30	AB	3	10.5/900	1.7	395E/1
MRF898(2)	60 (CW)	C	12	7/900	1	333A/1
V_{CC} = 26 Volts — Si Bipolar						
MRF6409	20	AB	26/50	10/960	3.8	319/2
MRF6414	50	AB	26/200	8.5/960	1.3	333A/2
MRF899(3)	150	AB	24	8/900	0.8	375A/1

1.5 GHz Transistors

Table 3. 1600 – 1640 MHz Band

Device	P_{out} Output Power Watts	Class	η Eff. (Min) %	Gp (Min)/Freq. Power Gain dB/MHz	θ_{JC} °C/W	Package/Style
MRF16006	6	C	40	7.4/1600	6.8	395C/2
MRF16030	30	C	40	7.5/1600	1.7	395C/2

(2)Internal Impedance Matched

(3)Internal Impedance Matched Push-Pull Transistors

5

Microwave Transistors

Table 4. L–Band Long Pulse Power

These products are designed for pulse power amplifier applications in the 960–1215 MHz frequency range. They are capable of handling up to 10 μs pulses in long pulse trains resulting in up to a 50% duty cycle over a 3.5 millisecond interval. Overall duty cycle is limited to 25% maximum. The primary applications for devices of this type are military systems, specifically JTIDS and commercial systems, specifically Mode S. Package types are hermetic.

Device	P_{out} Output Power Watts	P_{in}(Max) Input Power Watts	G_{PB} (Min) Gain @ 1215 MHz dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts — Class C Common Base					
MRF10005	5	0.71	8.5	8	336E/1
V_{CC} = 36 Volts — Class C Common Base					
MRF10031	30	3	10	3	376B/1
MRF10120	120	19	8	0.6	355C/1
V_{CC} = 50 Volts					
MRF10150	150	15	10(7)	0.25	376B/1
MRF10350	350	44	9(7)	0.11	355E/1
MRF10502★	500	63	9(7)	0.12	355J/1

Linear Transistors

The following sections describe a wide variety of devices specifically characterized for linear amplification. Included are medium power and high power parts covering frequencies to 2.0 GHz.

Table 5. UHF Ultra Linear For TV Applications

The following device has been characterized for ultra–linear applications such as low–power TV transmitters in Band IV and Band V and features diffused ballast resistors and an all–gold metal system to provide enhanced reliability and ruggedness.

Device	P_{ref} (Min) Watts	Gp (Min)/Freq. Small Signal Gain dB/MHz	3 Tone IMD(8) dB	θ_{JC} °C/W	Package/Style
V_{CC} = 28 Volts, Class AB					
TPV8100B	100(11)	8.5/860	—	0.7	398/1

Table 6. Microwave Linear for PCN Applications

The following devices have been developed for linear amplifiers in the 1.5–2 GHz region and have characteristics particularly suitable for PDC, PCS or DCS1800 base station applications.

Device	P_{out} Watts	Class	Bias Point Vdc/mA	Gain (Typ)/Freq dB/MHz	θ_{JC} °C/W	Package/Style
V_{CC} = 26 Volts–Bipolar Die						
MRF6404(16)	30	AB	26/150	8.2/1880	1.4	395C/1
MRF6420(46a)	60	AB	26/200	10/1880	0.7	451/1
MRF15090	90	A, AB	26/250	8.3/1490	0.7	375A/1
MRF20030R	30	AB	26/120	11/2000	1.4	395C/1
MRF20060R	60	AB	26/200	9.8/2000	0.7	451/1
MRF20060RS	60	AB	26/200	9.8/2000	0.7	451A/1

(7)Typical @ 1090 MHz

(8)Vision Carrier: – 8 dB; Sound Carrier: – 7 dB; Sideband Carrier: – 16 dB

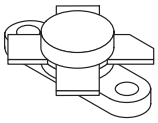
(11)Output power at 1 dB compression in Class AB

(16)Formerly known as "TP4035"

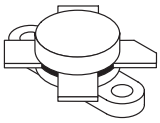
(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

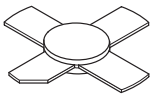
RF Power MOSFETs and Bipolar Transistors Packages



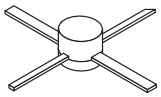
CASE 211–07
STYLE 1, 2
(.380″ FLANGE)



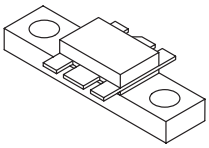
CASE 211–11
STYLE 1, 2
(.500″ FLANGE)



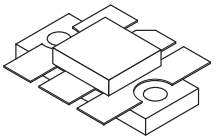
CASE 249–06
STYLE 3



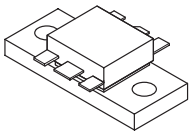
CASE 305A
STYLE 1, 2
(.204″ PILL)



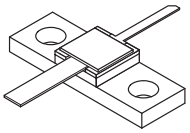
CASE 319
STYLE 1, 2, 3
(CS–12)



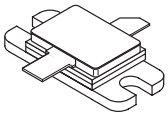
CASE 333
STYLE 1, 2



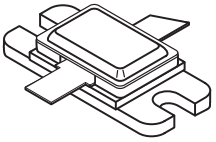
CASE 333A
STYLE 1, 2
(MAAC PAC)



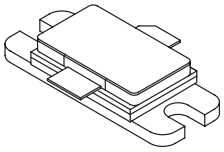
CASE 336E
STYLE 1



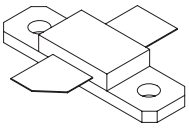
CASE 355C
STYLE 1



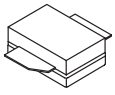
CASE 355E
STYLE 1



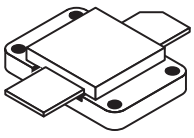
CASE 355J–02
STYLE 1



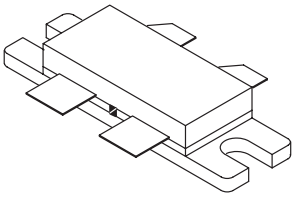
CASE 360B
STYLE 1
(Micro 250)



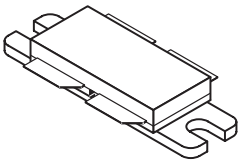
CASE 360C
STYLE 1
(Micro 250S)



CASE 368
STYLE 2
(HOG PAC)

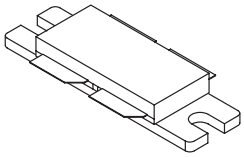


CASE 375
STYLE 2

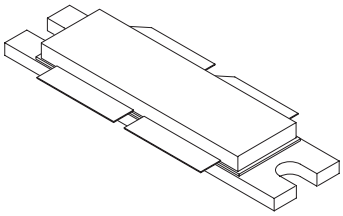


CASE 375A
STYLE 1

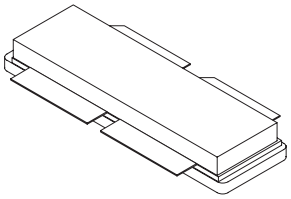
5



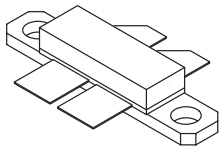
CASE 375B
STYLE 2
(Micro 860)



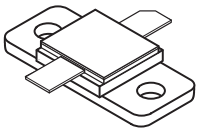
CASE 375D
STYLE 2



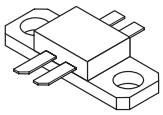
CASE 375E
STYLE 2



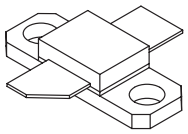
CASE 375F
STYLE 1



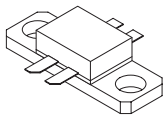
CASE 376B
STYLE 1



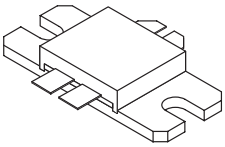
CASE 395B
STYLE 1



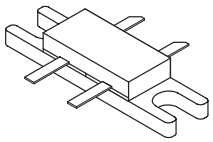
CASE 395C
STYLE 1, 2



CASE 395E
STYLE 1

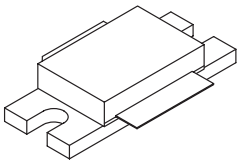


CASE 398
STYLE 1

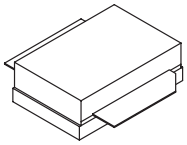


CASE 412
STYLE 1

CASE 449
STYLE 1
PLASTIC
(PLD 1)



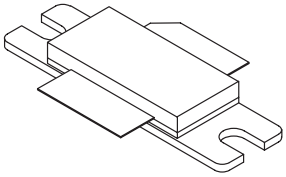
CASE 451
STYLE 1



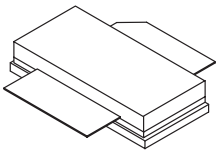
CASE 451A
STYLE 1

CASE 458
STYLE 1
(Micro 200S)

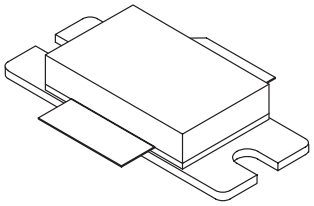
CASE 458A
STYLE 1
(Micro 200Z)



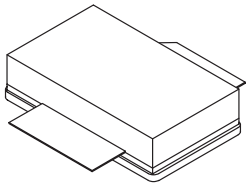
CASE 465
STYLE 1



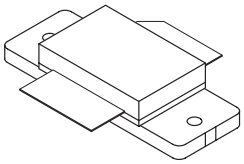
CASE 465A
STYLE 1



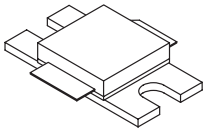
CASE 465B
STYLE 1



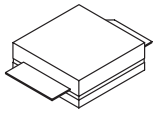
CASE 465C
STYLE 1



CASE 465D
STYLE 1

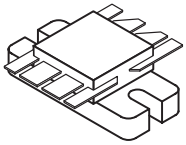


CASE 465E
STYLE 1

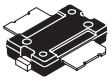


CASE 465F
STYLE 1

CASE 466
STYLE 1
PLASTIC
(PLD 1.5)



CASE 744A
STYLE 1, 2



CASE 1265
PLASTIC
(PRFP–1)

5

Motorola RF Amplifier Modules

Motorola's RF portfolio includes many hybrid designs optimized to perform either in narrowband base station transmitter applications, or in broadband linear amplifiers. Motorola modules feature two or more active transistors (LDMOS, GaAs, or Bipolar die technology) and their associated 50 ohm matching networks. Circuit substrate and metallization have been selected for optimum performance and reliability. For PA designers, hybrid modules offer the benefits of small and less complex system designs, in less time and at a lower overall cost.

Table of Contents

5

Motorola RF Amplifier Modules/ICs

Complete amplifiers with 50 ohm input and output impedances are available for all popular base station transmitter systems, including GSM and CDMA, covering frequencies from 800 MHz up to 2.2 GHz.

Base Stations

Designed for applications such as macrocell drivers and microcell output stage, these class AB amplifiers are ideal for GSM base station systems at 900, 1800 and 1900 MHz, with power requirements up to 16 watts.

Table 1. Base Stations

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/ Style
880–960 MHz (for GSM900) — Class AB (LDMOS Die) – Lateral MOSFETs						
MHVIC910L[46b]	10	0.050	921–960	22	26	978/–
1805–1880 MHz (for GSM1800) — Class AB (LDMOS Die) – Lateral MOSFETs						
MHW1810–1★	10	0.040	1805–1880	24	26	301AW/1
MHW1810–2★	10	0.008	1805–1880	32	26	301AW/1

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/ Style
1805–1880 MHz (for GSM1800) — Class AB (Silicon Bipolar Die)						
MHW1815	15	0.015	1805–1880	30	26	301AK/1

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{DD} Supply Voltage Volts	Package/ Style
1930–1990 MHz (for GSM1900) — Class AB (LDMOS Die) – Lateral MOSFETs						
MHW1910–1★	10	0.040	1930–1990	24	26	301AW/1

Device	P_{out} Output Power Watts	P_{in} Input Power Watts	f Frequency MHz	G_P Power Gain, Min dB	V_{CC} Supply Voltage Volts	Package/ Style
1930–1990 MHz (for PCS1900) — Class AB (Silicon Bipolar Die)						
MHW1915	15	0.019	1930–1990	29	26	301AK/1

Table 2. Base Station Drivers

These 50 ohm amplifiers are recommended for modern multi–tone CDMA, TDMA and UMTS base station pre–driver applications. Their high third–order intercept point, tight phase and gain control, and excellent group delay characteristics make these devices ideal for use in high–power feedforward loops.

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (Silicon Bipolar Die)

Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9125	800–960	15	400	20	0.5	31	43	7.5	448/2
MHL9128	800–960	28	400	20	0.5	31	43	7.5	448/1

[46]To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

★New Product

Base Stations (continued)

Table 2. Base Station Drivers (continued)

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A (LDMOS Die) – Lateral MOSFETs

Device	BW MHz	V_{DD} (Nom.) Volts	I_{DD} (Nom.) mA	Gain (Nom.) dB	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept (Typ) dBm	NF (Typ) dB	Case/ Style
MHL9838★	800–925	28	770	31	.1	39	50	3.7	301AP/1
MHL9236★	800–960	26	550	30.5	.1	34	47	3.5	301AP/1
MHL9236M★	800–960	26	550	30.5	.1	34	47	3.5	301AP/2
MHL9318(46a)	860–900	28	500	17.5	.1	35.5	49	3.0	301AS/1
MHL19338★	1900–2000	28	500	30	.1	36	46	4.2	301AP/1
MHL19936(46b)	1900–2000	28	1400	30	.2	41	51	4.2	301AY/1
MHL21336(46b)	2100–2200	26	500	30	.15	35	45	4.5	301AP/1

Ultra–Linear (for CDMA, W–CDMA, TDMA, Analog) – Class A – GaAs FET

MHL9025(46b)	790–920	15	330	21.5	.25	31.5	48	2.5	438F/1

Wideband Linear Amplifiers

Table 1. Standard 50 Ohm Linear Hybrid

This series of RF linear hybrid amplifier has been optimized for wideband, 50 ohm applications. These amplifiers were designed for multi–purpose RF applications where linearity, dynamic range and wide bandwidth are of primary concern. Each amplifier is available in various package options. The MHL series utilizes a new case style that provides microstrip input and output connections.

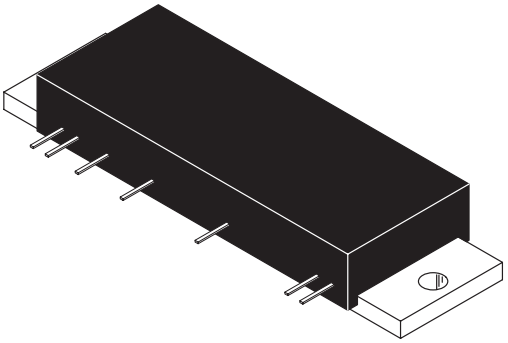
Device	BW MHz	V_{CC} (Nom.) Volts	I_{CC} (Nom.) mA	Gain/Freq. (Typ) dB/MHz	Gain Flatness (Typ) ±dB	P_{1dB} (Typ) dBm	3rd Order Intercept Point/Freq. (Typ) dBm/MHz	NF/Freq. (Typ) dB/MHz	Case/ Style
MHL8018	40–1000	28	210	18.5/900	1	26	38/1000	7.5/1000	448/1
MHL8118	40–1000	28	400	17.5/900	1	30	41.5/1000	8.5/1000	448/1

(46)To be introduced: a) 4Q99; b) 1Q00; c) 2Q00

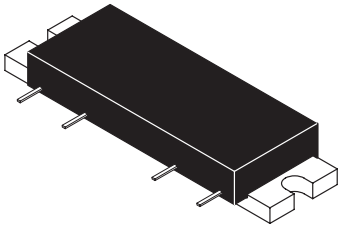
★New Product

5

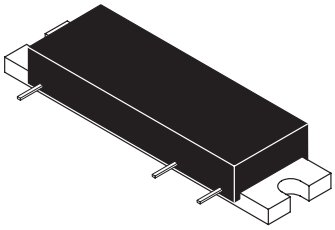
RF Amplifier Modules Packages



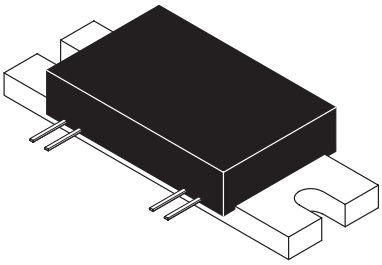
CASE 301AK
STYLE 1



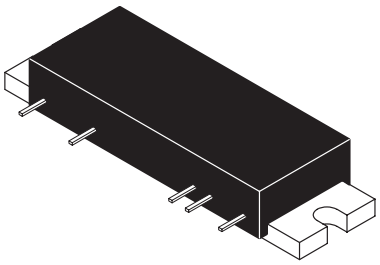
CASE 301AP
STYLE 1, 2



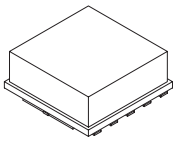
CASE 301AS
STYLE 1



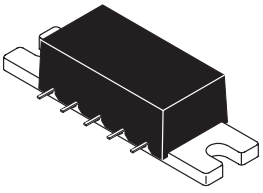
CASE 301AW
STYLE 1



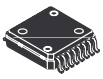
CASE 301AY
STYLE 1



CASE 438F
STYLE 1



CASE 448
STYLE 1, 2



CASE 978

5

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Table of Contents

5

Motorola RF CATV Distribution Amplifiers

Motorola Hybrids are manufactured using the latest generation technology which has set new standards for CATV system performance and reliability. These hybrids have been optimized to provide premium performance in all CATV systems up to 152 channels.

Forward Amplifiers

40–1000 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 152 CH	Cross Modulation dB 152 CH	Noise Figure @ 1000 MHz dB Max	Package/ Style
MHW9182B★	18.5	152	+38	–63(40)	–61	–61	7.5	714Y/1
MHW9242A(46a)	24.2	152	+38	–61(40)	–62	–60	8.0	714Y/1

40–860 MHz Hybrids

Device	Gain dB Typ @ 50 MHz	Frequency MHz	V_{CC} Volts	2nd Order IMD @ V_{out} = 50 dBmV/ch Max	DIN45004B @ f=860 MHz dBμV Min	Noise Figure @ 860 MHz dB Max	Package/ Style
CA901	17	40 – 860	24	–60	120	8.0	714P/2
CA901A	17	40 – 860	24	–64	120	8.0	714P/2
Power Doubling Hybrids							
CA922	17	40 – 860	24	–63	123	9.5	714P/2
CA922A	17	40 – 860	24	–67	123	9.5	714P/2

5

40–860 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
MHW8182B★	18.5	128	+38	–64(40)	– 66	– 65	7.5	714Y/1
MHW8222B(46c)	21.9	128	+38	–60(40)	– 64	– 63	7.0	714Y/1
MHW8242B★	24	128	+38	–62(40)	– 64	– 60	7.5	714Y/1
MHW8272A	27.2	128	+38	–64(40)	– 64	– 62	7.0	714Y/1
MHW8292	29	128	+38	–56(40)	– 60	– 60	7.0	714Y/1

(40)Composite 2nd Order; V_{out} = +38 dBmV/ch

(46)To be introduced: a) 4Q99; b) 1Q00 c) 2Q00

★New Product

CATV Distribution: Forward Amplifiers (continued)

40 – 860 MHz Hybrids, V_{CC} = 24 Vdc, Class A (continued)

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 128 CH	Cross Modulation FM = 55.25 MHz dB 128 CH	Noise Figure @ 860 MHz dB Max	Package/ Style
Power Doubling Hybrids								
MHW8185L(21)★	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/1
MHW8185LR(28)★	18.5	128	+40	–62(39)	– 63	– 64	8.5*	714Y/2
MHW8185	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/1
MHW8185R(14)	18.8	128	+40	–62(39)	– 64	– 64	8.0	714Y/2
MHW8205L(22)★	19.5	128	+40	–60(39)	– 63	– 64	8.5*	714Y/1
MHW8205	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/1
MHW8205R(24)★	19.8	128	+40	–60(39)	– 63	– 64	8.0	714Y/2
MHW8205LR(29,46b)	19.8	128	+40	–60(39)	– 63	– 64	8.5*	714Y/2

*@ 870 MHz

40 – 750 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 110 CH	Cross Modulation FM = 55.25 MHz dB 110 CH	Noise Figure @ 750 MHz dB Max	Package/ Style
MHW7182B★	18.5	110	+40	–63(39)	– 66	– 64	6.5	714Y/1
MHW7222A	21.5	110	+40	–57(39)	– 60	– 60	7.0	714Y/1
MHW7222B(46c)	21.9	110	+40	–60(39)	– 61	– 60	6.5	714Y/1
MHW7242B★	24	110	+40	–62(39)	– 63	– 58	7.0	714Y/1
MHW7272A	27.2	110	+40	–64(39)	– 64	– 60	6.5	714Y/1
MHW7292	29	110	+40	–60(39)	– 60	– 60	6.5	714Y/1
Power Doubling Hybrids								
MHW7185CL(23)★	18.5	110	+44	–64(36)	–61	–63	7.5	714Y/1
MHW7185CLR(33,46a)	18.5	110	+44	–64(36)	–61	–63	7.5	714Y/2
MHW7185C	18.8	110	+44	–64(36)	–62	–63	7.5	714Y/1
MHW7185CR(15)	18.8	110	+44	–64(36)	–62	–63	7.5	714Y/2
MHW7205CL(27)★	19.5	110	+44	–63(36)	–61	–62	7.5	714Y/1
MHW7205C	19.8	110	+44	–63(36)	–61	–62	7.5	714Y/1
MHW7205CLR(34,46b)	19.5	110	+44	–63(36)	–61	–62	7.5	714Y/2
MHW7205CR(26)★	19.8	110	+44	–63(36)	–61	–62	7.5	714Y/2

(14)Mirror Amplifier Version of MHW8185
(15)Mirror Amplifier Version of MHW7185C
(21)Low DC Current Version of MHW8185; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(22)Low DC Current Version of MHW8205; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(23)Low I_{CC} Version of MHW7185C
(24)Mirror Amplifier Version of MHW8205
(26)Mirror Amplifier Version of MHW7205C
(27)Low I_{CC} Version of MHW7205C
(28)Mirror Amplifier Version of MHW8185L
(29)Mirror Amplifier Version of MHW8205L
(33)Mirror Amplifier Version of MHW7185CL; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(34)Mirror Amplifier Version of MHW7205CL; Typical I_{CC} @ Vdc = 24 V is 365 mA.
(36)Composite 2nd order; V_{out} = +44 dBmV/ch
(39)Composite 2nd order; V_{out} = +40 dBmV/ch
(46)To be introduced: a) 4Q99; b) 1Q00 c) 2Q00
★New Product

5

CATV Distribution: Forward Amplifiers (continued)

40–550 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 550 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 77 CH	Cross Modulation dB 77 CH		
MHW6182	18.2	77	+44	–72(35)	–58	–62	7.0	714Y/1
MHW6222	22	77	+44	–66(35)	–57	–57	6.0	714Y/1
MHW6272	27	77	+44	–64(35)	–57	–57	6.5	714Y/1
MHW6342T	34.5	77	+44	–64(35)	–57	–57	6.5	714AA/1

40–450 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) @ 50 MHz dB	Channel Loading Capacity	Maximum Distortion Specifications				Noise Figure @ 450 MHz dB Max	Package/ Style
			Output Level dBmV	2nd Order Test dB	Composite Triple Beat dB 60 CH	Cross Modulation dB 60 CH		
MHW5182A	18.2	60	+46	–72(31)	–61	–59	6.5	714Y/1
MHW5222A	22	60	+46	–72(31)	–60	–59	5.5	714Y/1

(31)Channels 2 and M13 @ M22
(35)Channels 2 and M30 @ M39

5

Reverse Amplifiers

5–200 MHz Hybrids, V_{CC} = 24 Vdc, Class A

Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB: 22 CH	Composite Triple Beat dB: 26 CH	Cross Modulation dB: 22 CH	Cross Modulation dB: 26 CH	Noise Figure @ 175 MHz dB Max	Package/ Style
MHW1224	22	22	+50	–72	–69	–68.5(19)	–62	–62(19)	5.5	714Y/1
MHW1244	24	22	+50	–72	–68	–67.5(19)	–61	–61(19)	5.0	714Y/1

Low Current Amplifiers — 5–50 MHz Hybrids, V_{CC} = 24 Vdc, Class A

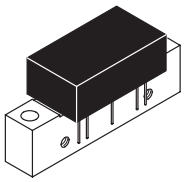
Device	Hybrid Gain (Nom.) dB	Channel Loading Capacity	I_{DC} mA Max	Maximum Distortion Specifications: Output Level dBmV	2nd Order Test(30) dB	Composite Triple Beat dB: 4 CH	Cross Modulation dB: 4 CH	Noise Figure @ 50 MHz dB Max	Package/ Style
MHW1254L	25	4	135	+50	–70	–70	–62	4.5	714Y/1
MHW1304L	30	4	135	+50	–70	–66	–57	4.5	714Y/1

(19)Typical

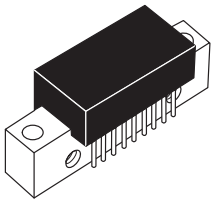
(30)Channels 2 and A @ 7

5

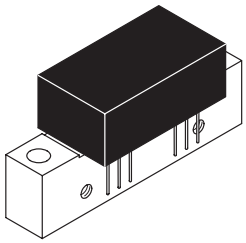
RF CATV Distribution Amplifiers



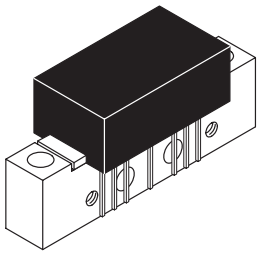
CASE 714AA
STYLE 1



CASE 714P
STYLE 2



CASE 714V



CASE 714Y
STYLE 1, 2

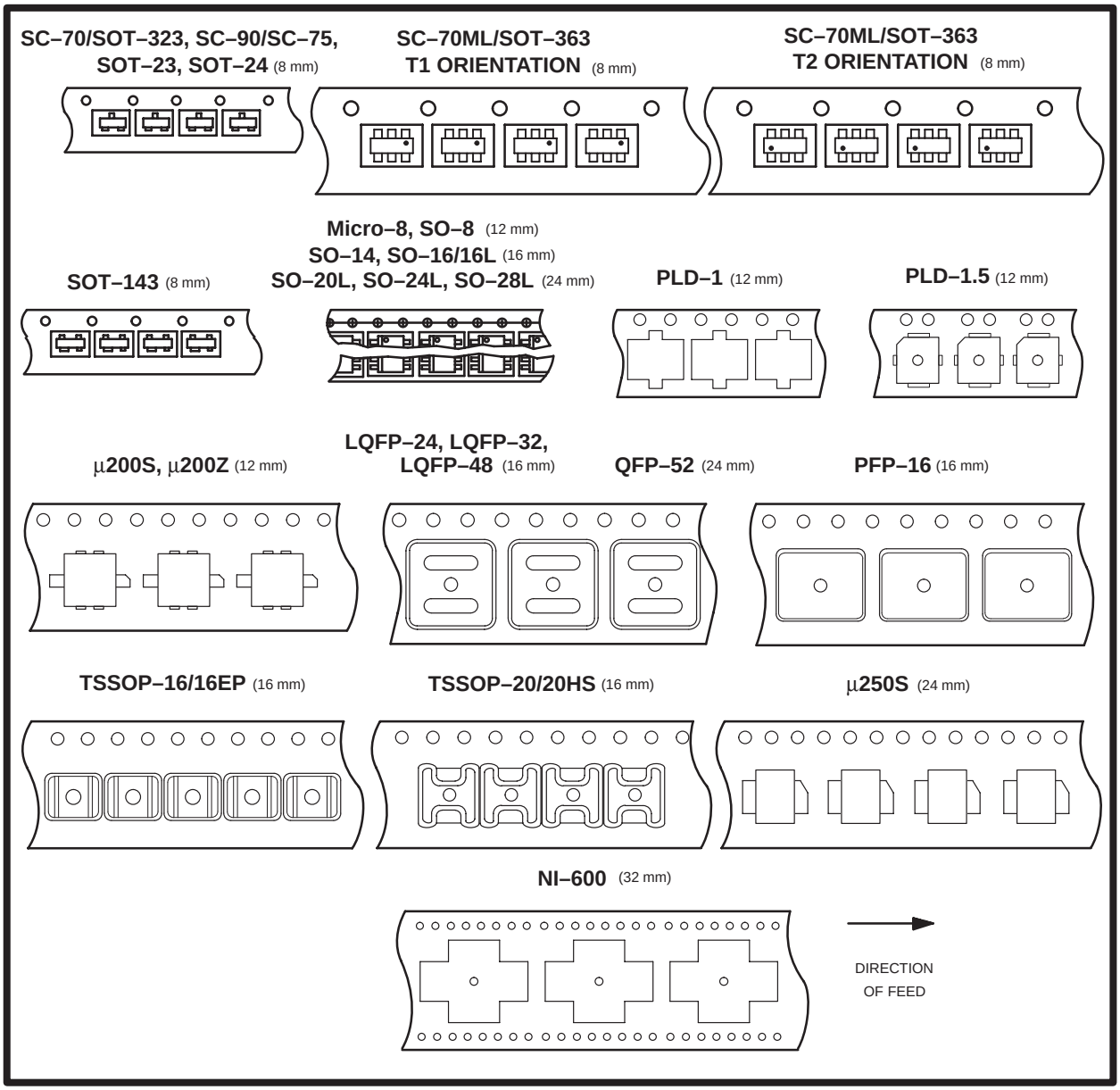
5

RF and IF Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel–back” cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- SC–70/SOT–323, SC–70ML/SOT–363, SC–90/SC–75, SOT–23, SOT–24, SOT–143 in 8 mm Tape
- Micro–8, PLD–1, PLD–1.5, SO–8, µ200S, µ200Z in 12 mm Tape
- SO–14, SO–16/16L, LQFP24, LQFP–32, LQFP–48, TSSOP–16/16EP, TSSOP–20/20HS in 16 mm Tape
- QFP–52, SO–20L, SO–24L, SO–28L, µ250S in 24 mm Tape
- NI–600 in 32 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.


SC–70/SOT–323, SC–90/SC–75, SOT–23, SOT–24 (8 mm)
SC–70ML/SOT–363 T1 ORIENTATION (8 mm)
SC–70ML/SOT–363 T2 ORIENTATION (8 mm)
Micro–8, SO–8 (12 mm)
SO–14, SO–16/16L (16 mm)
SO–20L, SO–24L, SO–28L (24 mm)
SOT–143 (8 mm)
PLD–1 (12 mm)
PLD–1.5 (12 mm)
µ200S, µ200Z (12 mm)
LQFP–24, LQFP–32, LQFP–48 (16 mm)
QFP–52 (24 mm)
PFP–16 (16 mm)
TSSOP–16/16EP (16 mm)
TSSOP–20/20HS (16 mm)
µ250S (24 mm)
NI–600 (32 mm)
DIRECTION OF FEED

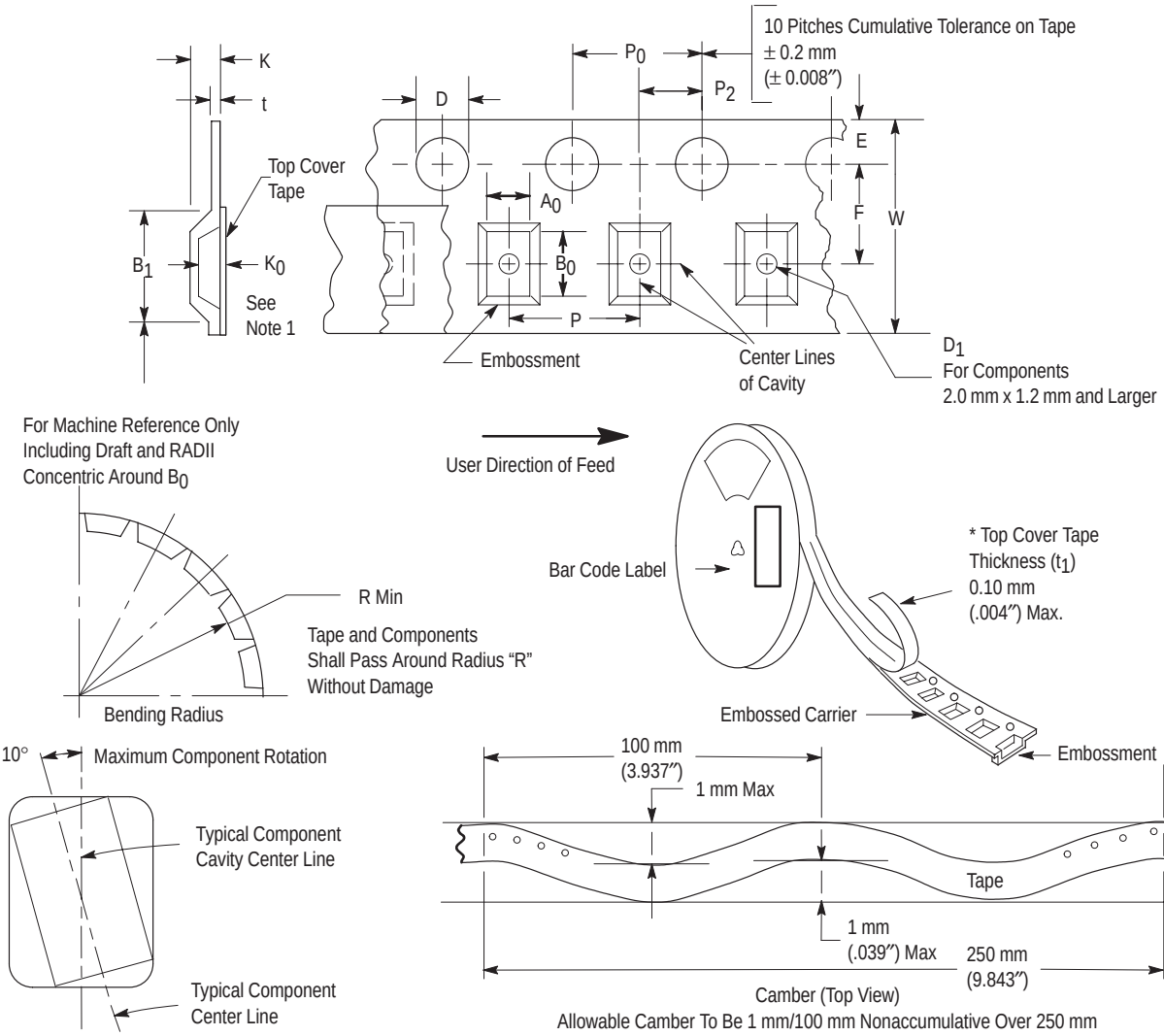
5

EMBOSSED TAPE AND REEL ORDERING INFORMATION

Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
SC–70/SOT–323	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SC–70ML/SOT–363	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000 3,000	T1 T2
SC–90/SC–75	8	4.0 ± 0.1 (.157 ± .004)	178 (7)	3,000	T1
Micro–8	12	8.0 ± 0.1 (.315 ± .003)	330 (13)	2,500	R2
PLD–1	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PLD–1.5	12	8.0 ± 0.1 (.315 ± .004)	178 (7)	1,000	T1
PFP–16	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,500	R2
LQFP–24	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	2,000	R2
LQFP–32	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,800	R2
LQFP–48	16	12.0 ± 0.1 (.472 ± .004)	330 (13)	2,000	R2
QFP–52	24	24.0 ± 0.1 (.945 ± .004)	330 (13)	1,500	R2
SO–8	12	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–14	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–16/16L	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
SO–20L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO–24L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SO–28L	24	12.0 ± 0.1 (.472 ± .004)	330 (13)	1,000	R2
SOT–23, SOT–24	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
SOT–143	8 8	4.0 ± 0.1 (.157 ± .004)	178 (7) 330 (13)	3,000 10,000	T1 T3
TSSOP–16/16EP	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
TSSOP–20/20HS	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	R2
µ200S (458)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
µ200Z (458A)	12	12.0 ± 0.1 (.471 ± .004)	178 (7)	500	R1
µ250S (360C)	24	16.0 ± 0.1 (.631 ± .004)	330 (13)	500	R1
NI–600 (465D)	32	32.0 ± 0.1 (1.26 ± .004)	330 (13)	250	R3

EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS



DIMENSIONS

Tape Size	B_1 Max	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
8 mm	4.55 mm (.179″)	1.5 + 0.1 mm −0.0 (.059 + .004″ −0.0)	1.0 Min (.039″)	1.75 ± 0.1 mm (.069 ± .004″)	3.5 ± 0.05 mm (.138 ± .002″)	2.4 mm Max (.094″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	25 mm (.98″)	0.6 mm (.024″)	8.3 mm (.327″)
12 mm	8.2 mm (.323″)		1.5 mm Min (.060″)		5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)			30 mm (1.18″)		12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5 ± 0.1 mm (.453 ± .004″)	11.9 mm Max (.468″)					24.3 mm (.957″)
32 mm	23.0 mm (.906″)	1.5 + 0.1 mm −0.0 (.059 + .004″ −0.0)	1.5 mm Min (.059″)	1.75 ± 0.1 mm (.069 ± .004″)	14.2 ± 0.1 mm (.559 ± .004″)	—	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .004″)	50 mm (1.969″)	0.6 mm (.024″)	32.2 mm (1.272″)

Metric dimensions govern — English are in parentheses for reference only.

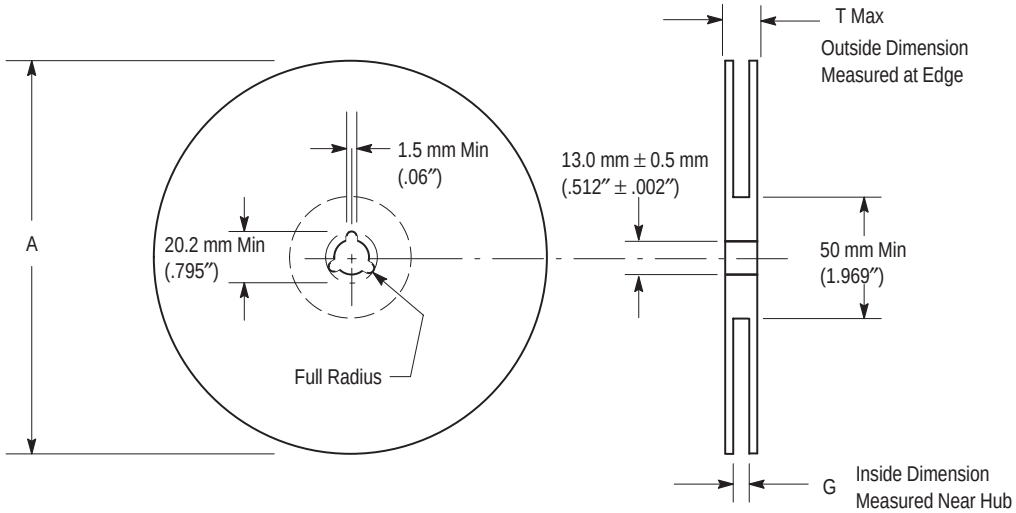
NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: If B_1 exceeds 4.2 mm (.165) for 8 mm embossed tape, the tape may not feed through all tape feeders.

NOTE 3: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 5.1–43.

5

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
8 mm	330 mm (12.992″)	8.4 mm + 1.5 mm, –0.0 (.33″ + .059″, –0.00)	14.4 mm (.56″)
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, –0.0 (.961″ + .070″, –0.00)	30.4 mm (1.197″)
32 mm	360 mm (14.163″)	32.4 mm + 2.0 mm, –0.0 (1.276″+ 0.79″, –0.00)	—

Reel Dimensions

Metric Dimensions Govern — English are in parentheses for reference only

5

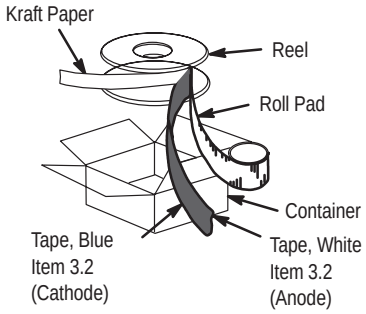


Figure 1. Reel Packing

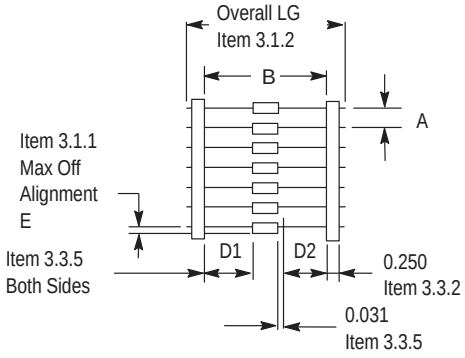


Figure 2. Component Spacing

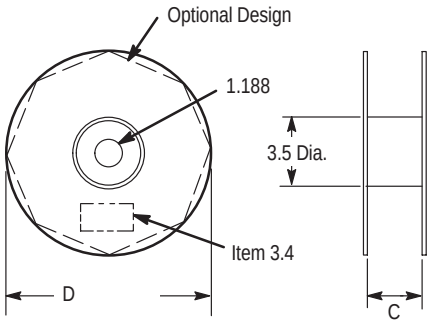


Figure 3. Reel Dimensions

5

Product Literature and Technical Training

In Brief . . .

With the pace of new semiconductor product introductions, the task of providing an effective and up–to–date perspective of available components is beyond the means of any single document. Hence, a comprehensive Motorola Literature System has been put in place to keep semiconductor users totally informed of all aspects of the Motorola product lines — from new product introductions, to applications, to major changes in directions.

The Motorola technical literature library and associated services consist of the following:

- An extensive library of Data Books, each containing a complete selection of data sheets associated with a particular product line.
- A series of User's Manuals and Design Manuals dealing with the application of highly complex products.
- A wide range of Application Notes and Article Reprints detailing the utilization of new and significant products.
- Instructor–led Training for:
  Digital Signal Processing (DSP) Family — DSP56K, DSP563xx/6xx
  High End MPUs — PowerPC, MPC60x, MPC7xx M68000 Family and ColdFire — MC68xxx, MCF51xx, MCF52xx
  Microcontrollers (MCU) MC68HC05, 08, 11, 12, 16, MC6833x
  Netcomm Products — MC68302, MC68360, MPC860, MPC8260

These products and services are described on the following pages. However, because of different conditions and standards, some of these may not be available outside the USA.

6

6

Technical Data Services

Motorola Semiconductor Master Product Selection Guide

For the identification and preliminary selection of components for circuit and system designs

For the design engineer, the Motorola Master Product Selection Guide is perhaps the most important single document for the identification and preliminary selection of components for circuit and system designs. Within its pages is a complete listing and description of Motorola semiconductor devices currently in general use, and those recommended for new designs. It serves two purposes:

1. It lists all standard products in the vast Motorola semiconductor inventory for rapid identification.
2. It divides this total product offering into a variety of major product categories, with sufficient technical information to permit an intelligent first–order evaluation as to the most suitable devices for a specific application.

M*fax* — Touch–Tone Fax

M*fax* offers access to over 40,000 Motorola documents for faxing to customers worldwide. With menus and voice instruction, customers can request the documents needed using their own touch–tone telephones from any location 7 days a week and 24 hours a day.

A number of features are offered within the **M*fax*** system, including special documents (4–digit code identifiers for currently referenced promotional or advertising material), product data sheets, application notes, engineering bulletins, selector guides, Literature Order Forms, and Technical Training Information.

How to reach us:
MFAX: RMFAX0@email.sps.mot.com
or (602) 244–6609
or 1–800–774–1848 (U.S. and Canada)

Motorola SPS Internet Server

Technical data such as the complete Master Product Selection Guide along with the OEM North American price book are available on the Internet server with full search capabilities. Other data on the server include abstracts of data books, application notes, selector guides, and textbooks. All have easy text search capability. Ordering Literature from the Literature Distribution Center is available on line.

Other features of Motorola SPS's Internet server include the availability of a searchable press release database, technical training information with on–line registration capabilities, complete on–line access to the MFAX system for ordering faxes, an on–line technical support form to send technical questions and receive answers through email, information on product groups, full search capabilities of device models, a listing of the Domestic and International sales offices, and links directly to other Motorola world wide web servers.

After accessing the Internet, to locate the Motorola SPS server, use the following URL:

http://sps.motorola.com

For more information on Motorola SPS's Internet server you can request BR1307/D from MFAX.

6

Motorola Data and Application Literature

Complete technical data for the world's most comprehensive inventory of semiconductor components

To complement the industry's broadest line of semiconductor products, Motorola offers a complete library of Data books which detail the electrical characteristics of its products. These documents are supplemented by User's Manuals describing the capabilities of the products in circuit and system design.

Motorola attempts to fill the need for applications information concerning today's highly complex electronic components. Each year dozens of authors from colleges and universities, and from the industry, add their individual contributions to the collective literature. From these, Motorola has selected a number of texts which add substantially to the comprehension and applications of some of the more complex products. By buying these in large quantities and providing them to customers at lower than retail cost, Motorola hopes to foster a more comprehensive acquaintance with these products at greatly reduced prices.

Semiconductors in theory and practice

Application Notes, Engineering Bulletins and Article Reprints are part of a total information system to define the characteristics and applications of semiconductor devices. Motorola's library consists of such documents dealing with the applications of all types of semiconductors from discrete power transistors to the most complex microprocessors. All are described in an Application Note Catalog available from our Literature Distribution Center.

Individual application notes, application reports, engineering bulletins and article reprints can also be ordered from our Literature Distribution Center.

Contact the Literature Distribution Center for ordering information. In addition, there may be an alternative document available in some countries, contact your local Motorola Sales Office.

For complete summaries: order BR101/D from the Literature Distribution Center.

Data Books and Handbooks

BR1333/D, Timing Solutions
DL110/D, RF Device Data
DL156/D, Fast Static RAM – Component and Module Data
DL159/D, LonWorks Technology Device Data
DL160/D, Display Products Device Data
DL200/D, Pressure Sensor Device Data
HB215/D, RF Application Reports
HB218/D, Senseon: Pressure Sensor Distributor Handbook

6

Selector Guides & Application Literature

BR101/D, Technical and Applications Literature Catalog
BR729/D, Motorola 68K Source – Third Party Vendor Catalog
BR916/D, Packaging Manual for ASIC Arrays
BR1133/D, HIPPO: High–Performance Internal Product Portfolio Overview
BR1202/D, Motorola Quality System Review Guidelines
BR1305/D, Analog Integrated Circuits: New Product Calendar
CMRQS/D, CSIC Microcontrollers: Reliability and Quality Monitor Report
DSP56800WP1/D, Novel Digital Signal Processing Architecture with Microcontroller Features
EMDVPOC/D, Embedded Developer Pocket Guide
MRQSY96/D, Microcontroller Technologies Group: Reliability and Quality — 1996 Annual Report
PSTR3003/D, The Motorola Silicon Community
SG46/D, RF Products Selector Guide & Cross Reference
SG73/D, Master Product Selection Guide
SG162/D, Sensor Products Division
SG169/D, Mixed Signal Solutions from MOS Digital–Analog Integrated Circuits Division
SG171/D, Fast Static RAM Product Update Tools
SG175/D, RISC Microprocessor Division: The PowerPC Microprocessor Family
SG180/D, Microcontroller Technologies Group: Development Tools Selector Guide
SG183/D, 68HC705 MCU and Development Tools Selector Guide
SG373/D, Comm Plus & Mil/Aero Appl RF Prod Selector Guide
SG379/D, North America Sales and Distribution Price List
SG382/D, Motorola RF CATV Distribution Amplifiers
SG384/D, Motorola RF LDMOS Product Family
SG417/D, Semiconductor Products for Wireless Communications
SG419/D, EMU: European Microcontroller Update

Motorola Data and Application Literature: (continued)

Selector Guides & Application Literature (continued)

SG423/D, TIGER: The Integrated Guide to European RAMs

User's Manuals

ADCRM/AD, Analog–to–Digital Converter Reference Manual
C4PKGUSERGUIDE/D, C4PKG User's Guide
CPU08RM/AD, M68HC08 Central Processor Unit Reference Manual
CPU12RM/AD, 68HC12 CPU 12 Reference Manual
CPU16RM/AD, M68HC16 Family Reference Manual
CPU32RM/AD, CPU32 Central Processor Unit Reference Manual
CTMRM/D, Configurable Timer Module Reference Manual
DMA08RM/AD, DMA08 Direct Memory Access Reference Manual
DSP56KFAMUM/AD, DSP56000 Digital Signal Processor Family Manual
DSP56L811EMUM/AD, DSP56L811 Evaluation Module User's Manual
DSP56L811UM/AD, DSP56L811 User's Manual
DSP56LF812UM/AD, DSP 56LF812 User's Manual
DSP56002UM/AD, DSP56002 Digital Signal Processor User's Manual
DSP56004UM/AD, DSP56004 Digital Signal Processor User's Manual
DSP56007UM/AD, DSP56007 User's Manual
DSP56009UM/AD, DSP56009 User's Manual
DSP56011UM/AD, DSP56011 User's Manual
DSP56100FM/AD, DSP56100 Digital Signal Processor Family Manual
DSP56300FM/AD, DSP56300 24–Bit Digital Signal Processor Family Manual
DSP56301UM/AD, DSP56301 24–Bit Digital Signal Processor User's Manual
DSP56302EMUM/AD, DSP56302 Evaluation Module User's Manual
DSP56302UM/AD, DSP56302 User's Manual
DSP56303EMUM/AD, DSP56303 Evaluation Module User's Manual
DSP56303UM/AD, DSP56303 User's Manual
DSP56304UM/AD, DSP56304 User's Manual
DSP56307UM/D, DSP56307 User's Manual
DSP56309UM/D, DSP56309 User's Manual
DSP56362UM/D, DSP56362 User's Manual
DSP56600FM/AD, DSP56600 Family Manual
DSP56602UM/AD, DSP56602 User's Manual
DSP56603EMUM/AD, DSP56603 Evaluation Module User's Manual
DSP56603EVMP/D, Evaluation Module Product Brochure
DSP56603UM/AD, DSP56603 User's Manual
DSP56800FM/AD, DSP56800 Family Manual
DSP56824UM/AD, DSP56824 User's Manual
GPTRM/AD, Modular Microcontroller Family General Purpose Timer Reference Manual
H4CDM/D, H4C Series Design Reference Guide
H4CPDM/D, H4CPlus Series Design Reference Guide
HB219/D, Introduction to the Oncore ChipSet
HCA62A00DM/D, Macrocell Array Design Manual
HC05C0GRS/D, 68HC05C0 Specification (General Release)
HC05C12AGRS/D, MC68HC05C12A, MC68HCL05C12A, MC68HSC05C12A General Release Specification
HC05C4AGRS/D, MC68HC05C4A, MC68HCL05C4A, MC68HSC05C4A General Release Specification
HC05C8AGRS/D, MC68HC05C8A, MC68HCL05C8A, MC68HSC05C8A General Release Specification
HC05C9AGRS/D, MC68HC05C9A, MC68HCL05C9A, MC68HSC05C9A General Release Specification
HC05E5GRS/D, MC68HC05E5 General Release Specification
HC05RC18GRS/D, 68HC05RC9/68HC05RC18 General Release Specification
HC705MC4GRS/D, MC68HC705MC4 General Release Specification
HC705RC17GRS/D, 68HC705RC17 General Release Specification
HC708KL8GRS/D, 68HC708KL8 General Release Specification
HC708MP16GRS/D, MC68HC708MP 16 General Release Specification
HC908AT32GRS/D, MC68HC908AT32 General Release Specification
HDCDM/D, HDC Series Design Reference Guide
LONUG/AD, LonBuilder User's Guide
M5CDM/D, M5C Series Design Reference Guide
M68EM05C0UM/D, M68EM05C0 Emulation Module User's Module
M68EM05E5UM/D, Emulation Module–User's Manual
M68EM05JP7UM/D, M68EM05JP7 Emulation Module User's Manual
M68EM05P18UM/D, 68EM05P18 Emulation Module User's Manual

Motorola Data and Application Literature: (continued)

User's Manuals (continued)

M68EM05V12UM/D, M68EM05V12 Emulation Module User's Manual
M68EM05V8UM/D, Emulation Module User's Manual
M68EM08AX48UM/D, M68EM08AX48 Emulation Module User's Manual
M68EM08MP16UM/D, M68EM08MP16 Emulation Module User's Manual
M68EML05P6AUM/D, Emulation Module User's Manual
M68EML08LN56UM/D, M68EML08LN56 Emulation Module User's Manual
M68EML08XL36UM/D, M68EML08XL36 Emulation Module User's Manual
M68HC05AG/AD, M68HC05 Applications Guide
M68HC05EVM/AD4, M68HC05EVM Evaluation Module User's Manual
M68HC08RG/AD, HC08 Family Reference Guide
M68HC11RM/AD, M68HC11 Reference Manual
M68PRM/D, M6800 Programming Reference Manual
M6805UM/AD3, M6805 HMOS/M146805 CMOS Family User's Manual (1991)
M6809/AC3, MC6809/9E 8–Bit Microprocessor Reference Card
M6809PM/AD, MC6809–MC6809E Microprocessor Programming Manual (1981)
M68000PM/AD, M68000 Family Programmer's Reference Manual
M68000UM/AD, M68000 8–/16–/32–bit Microprocessors User's Manual, Ninth Edition
M68020UM/AD, MC68020/MC68EC020 Microprocessors User's Manual
M68040UM/AD, MC68040, MC68040V, MC68LC040, MC68EC040, MC68EC040V Microprocessors User's Manual
M68060UM/AD, MC68060, MC68LC060, MC68EC060 Microprocessors User's Manual
M68705EVM/AD5, Eval Mod User's Manual
MC141622EVK/D, ACF–II Evaluation Board Operating Manual
MC145220EVK/D, MC145220 Evaluation Board Manual
MC14LC5480EVK/D, PCM Codec Filter Evaluation Kit User's Manual
MC68EN302RM/AD, MC68EN302 Integrated Multiprotocol Processor with Ethernet Reference Manual (Supplement to MC68302UM/AD)
MC68F333UM/AD, MC68F333 User's Manual
MC68HC05CxRG/AD, MC68HC05Cx HCMOS Single–Chip Microcontrollers Programming Reference Guide
MC68HC11A8RG/AD, MC68HC11A8 Programming Reference Guide
MC68HC11C0RG/AD, MC68HC11C0 Programming Reference Guide
MC68HC11D3RG/AD, MC68HC11D3/MC68HC711D3 Programming Reference Guide
MC68HC11ED0RG/AD, HC11 MC68HC11ED0 Programming Reference Guide
MC68HC11ERG/AD, MC68HC11E Programming Reference Guide
MC68HC11F1RG/AD, MC68HC11F1 Programming Reference Guide
MC68HC11K4RG/AD, MC68HC11K4/MC68HC711K4 Programming Reference Guide
MC68HC11KA4RG/AD, MC68HC11KA4/MC68HC711KA4 Programming Reference Guide
MC68HC11L6RG/AD, MC68HCL6/MC68HC711L6 Programming Reference Guide
MC68HC11MRG/AD, M68HC11 M Series Programming Reference Guide
MC68HC11NRG/AD, MC68HC11N Series Programming Reference Guide
MC68HC16Y1UM/AD, MC68HC16Y1 User's Manual
MC68HC16ZUM/AD, M68HC16 Z Series User's Manual
MC68HC901UM/AD, MC68HC901 Multi–Function Peripheral User's Manual
MC68LC302RM/AD, MC68LC302 Low Power Integrated Multiprotocol Processor Reference Manual
MC68PM302RM/AD, Integrated Multiprotocol Processor with PCMCIA Interface Reference Manual
MC68PM302RMAD/AD, MC68PM302 Reference Manual Addendum
MC68SC302UM/AD, MC68SC302 Passive ISDN Protocol Engine User's Manual
MC68000/AC, MC68000 16/32 Microprocessor Prog Reference Manual
MC6801RM/AD2, MC6801 8–bit Single–Chip Microcomputer Reference
MC68030UM/AD, MC68030 Enhanced 32–bit MPU User's Manual, third edition
MC68302/D, Integrated Multiprotocol Processor MC68302

Motorola Data and Application Literature: (continued)

User's Manuals (continued)

MC68302UM/AD, MC68302 Integrated Multiprotocol Processor User's Manual
MC68306UM/AD, MC68306 Integrated EC000 Processor User's Manual
MC68322UM/AD, Bandit: MC68322 Integrated Printer Processor User's Manual
MC68328UM/AD, MC68328 (Dragonball) Integrated Processor User's Manual
MC68330UM/AD, MC68330 Integrated CPU32 Processor Users Manual
MC68331UM/AD, MC68331 User's Manual
MC68332UM/AD, MC68332 User's Manual
MC68336/376UM/AD, MC68300 Family User's Manual
MC68340UM/AD, MC68340 Integrated Processor User's Manual
MC68356UM/AD, MC68356 Signal Processing Communications Engine User's Manual
MC68360UM/AD, MC68360 Quad Integrated Communications Controller User's Manual
MC68605UM/AD, MC68605 X.25 Protocol Controller User's Manual
MC68824UM/AD, MC68824 Token Bus Products User's
Manual
MC68836UM/AD, MC68836 FDDI User's Manual
MC68837UM/AD, MC68837 FDDI User's Manual
MC68838UM/AD, MC68838 FDDI User's Manual
MC68839UM/AD, MC68839 FDDI System Interface User's Manual
MC68840UM/AD, MC68840 Integrated Fiber Distributed Data Interface User's Manual
MC68847UM/AD, MC68847 Quad ELM FDDI User's Manual
MC88200UM/AD, MC88200 Cache/Memory Management Unit User's Manual
MC88410UM/AD, MC88410 Secondary Cache Controller User's Manual
MC92500UM/D, MC92500 ATM Cell Processor Design Manual
MC92501UM/D, MC92501 ATM Cell Processor User's Manual
MCCIRM/AD, Multichannel Communication Interface Reference Manual
MCF5102UM/AD, MCF5102 ColdFire User's Manual
MCF5200PRM/AD, ColdFire Programmer's Reference Manual
MCF5202UM/AD, ColdFire MCF5202 User's Manual
MCF5204UM/AD, ColdFire MCF5204 User's Manual
MCF5206UM/AD, ColdFire User's Manual
MCF5307UM/AD, MCF5307 ColdFire User's Manual
MCORERM/AD, MCore Reference Manual
MCUDEVTLDIR/D, Motorola Microcontroller Development Tools Directory
MPCBUSIF/AD, PowerPC Microprocessor Family: the Bus Interface for 32–bit Microprocessors
MPCFPE32B/AD, MPCFPE32B/AD User's Manual 32–bit Pgm. Environment
MPCPRG/D, PowerPC Microprocessor Family: The Programmer's Reference Guide
MPCPRGREF/D, PowerPC Microprocessor Family: The Programmer's Pocket Reference Guide
MPC105UM/AD, PowerPC PCI Bridge/Memory Controller User's Manual
MPC106UM/AD, PCI/Bridge/Memory Controller User's Manual
MPC505UM/AD, MPC505 User's Manual
MPC509UM/AD, MPC509 User's Manual
MPC603eUM/AD, PowerPC 603e RISC Microprocessor User's Manual
MPC604eUM/AD, PowerPC 604e RISC Microprocessor User's Manual
MPC750UM/AD, MPC750 RISC Microprocessor User's Manual
MPC801UM/AD, MPC801 Integrated Microprocessor for Embedded Systems
MPC821UM/AD, MPC821 PowerPC Portable Systems Microprocessor User's Manual
MPC823RG/D, PowerPC MPC823 Pocket Guide
MPC823UM/D, PowerPC MPC823 User's Manual
MPC850UM/D, MPC850 Integrated Communications Microprocessor User's Manual
MPC860UM/AD, MPC860 PowerQUICC User's Manual
QADCRM/AD, Queued Analog–to–Digital Converter Reference Manual
QMCSUPPLEMENT/AD, QUICC Multichannel Controller User's Manual Supplement
QSMRM/AD, Queued Serial Module Reference Manual
RCPURM/AD, MPC500 Family: RCPU Reference Manual
SCIMRM/AD, Single–Chip Integration Module Reference Manual
SIMRM/AD, System Integration Module Reference Manual
SIURM/AD, MPC500 Family: System Integration Unit Reference Manual
TIM08RM/AD, TIM08 Timer Interface Module Reference Manual
TPURM/AD, M68300 Family Time Processor Unit Reference Manual

Technical Data Services

DK105/D, Scattering Parameter Library
DK106/D, Scattering Parameter Plotting Utility
DK107/D, Impedance Matching Program
DK306/D, PLL Lock–in Time Analysis
DK307/D, PLL Frequency Domain Analysis
SG73/D, Master Product Selection Guide

ON Semiconductor Literature

The following technical documentation is available from ON Semiconductor. Contact the ON Literature Distribution Center for ordering information at 1–800–344–3860 or 1–303–675–2175 or Email: ONlit@hibbertco.com.

BR1137/D, The Motorola Explorer's Guide to the World of Embedded Control Solutions
BR1306/D, CATS – Customer Analysis Tracking System
BR1339/D, LCX Data Low–Voltage CMOS Logic
BR1486/D, SCSI Terminators
BR1487/D, Thermal Modeling and Management of Discrete Surface Mount Packages
BR1491/D, TSOP–6
BR1492/D, LVX Data: Low–Voltage CMOS Logic
BR3021/D, "IMAGINE'' Magazine
BR518/D, Reliability & Quality Handbook
CR100/D, Communications, Power and Signal Technologies Group: Through–Hole to Surface Mount Cross Reference
CR105/D, High Performance SCR Cross Reference Data Sheet
CR107/D, Siemens to Motorola TO–92 Cross Reference Sheet
CR108/D, Low Voltage MOSFET Cross Reference
DL111/D, Bipolar Power Transistor Data
DL121/D, FAST and LS TTL Data
DL122/D, MECL Device Data
DL126/D, Small–Signal Transistors, FETs and Diodes Device Data
DL128/D, Analog/Interface ICs Device Data
DL129/D, High Speed CMOS Data
DL131/D, CMOS Logic Data
DL135/D, TMOS Power MOSFET Transistor Data
DL137/D, Thyristor Device Data
DL138/D, FACT Data
DL140/D, ECLinPS and ECLinPS Lite
DL150/D, TVS/Zener Device Data
DL151/D, Rectifier Device Data
DL202/D, Insulated Gate Bipolar Trans Device Data Book
DL203/D, Advanced High–Speed CMOS Data
H4EPDM/D, H4EPlus Series Design Reference Guide
HB205/D, MECL System Design Handbook
HB214/D, Rectifier Applications Handbook
MC145190EVKUM/D, MC145190–201 Evaluation Board Manual
SG96/D, Analog/Interface ICs Selector Guide & Cross Reference
SG134/D, VARO to Motorola Rectifier Cross Reference
SG370/D, Discrete Surface Mount Selector Guide
SG371/D, DPAK Surface Mount Selector Guide
SG378/D, Linear Voltage Regulators
SG425/D, Lamp Ballast Selector Guide

Motorola Technical Training Courses

About Motorola Customer Training

Motorola has been serving the training needs of its microprocessor, microcontroller and digital signal processor customers for more than 20 years. The Technical Training organization was formed in the mid–70s to provide quality training to customers who had purchased, who were evaluating, or who were implementing Motorola microprocessors and/or microcontrollers into their applications. Since its inception Motorola's Technical Training organization and its training partners have delivered technical training to thousands of customers each year for more than 2 decades.

In order to keep pace with global continued product training demands and an increased need for development of new training, Motorola has teamed with some quality external partners throughout the globe to extend the delivery of our training. Training partners in the Americas, Europe, and the Far East are available to provide training, using Motorola developed training materials, to help customers implement Motorola devices into their end products. This strategy has enabled internal Motorola resources to focus more completely on the development of courses for new products, and to develop new technologies for delivering these courses.

Motorola Technical Training carefully monitors the quality of training offered by both internal and external resources to assure the best training possible to its customer base. Motorola's training objective is to provide quality training to enable our customers to bring their product(s) to the market in the most efficient manner possible.

Please visit our web site at http://mot–sps.com/support/technical/training to see the global training being offered. The site contains a current list of scheduled courses, and offers training via open enrollment classes and "in plant" classes (classes at your facility).

6

Where to Buy

In Brief . . .

This section contains a current worldwide listing of all of Motorola's authorized distributors. Consult the following pages to find the Motorola distributor nearest to you.

7

7

United States – Authorized Distributors

Alabama

Huntsville

Allied Electronics, Inc. . . . . (256) 721–3500
Arrow Electronics . . . . . (256) 864–3300
FAI . . . . . (256) 837–9209
Future Electronic . . . . . (256) 971–2010
Hamilton/Hallmark . . . . . (256) 837–8700
Newark . . . . . (256) 837–9091
Wyle Electronics . . . . . (256) 830–1119

Mobile

Allied Electronics, Inc. . . . . (334) 476–1875

Arizona

Phoenix

Allied Electronics, Inc. . . . . (602) 831–2002
FAI . . . . . (602) 731–4661
Future Electronics . . . . . (602) 968–7140
Hamilton/Hallmark . . . . . (602) 736–7000
Wyle Electronics . . . . . (602) 804–7000

Tempe

Arrow Electronics . . . . . (602) 966–6600
Newark . . . . . (602) 966–6340
Penstock . . . . . (602) 967–1620

Arkansas

Little Rock

Newark . . . . . (501) 225–8130

California

Agoura Hills

Future Electronics . . . . . (818) 871–1740

Calabassas

Arrow Electronics . . . . . (818) 880–9686
Wyle Electronics . . . . . (818) 880–9000

Culver City

Hamilton/Hallmark . . . . . (310) 558–2000

Irvine

Arrow Electronics . . . . . (949) 587–0404
Arrow Zeus . . . . . (949) 581–4662
FAI . . . . . (949) 753–4778
Future Electronics . . . . . (949) 453–1515
Hamilton/Hallmark . . . . . (949) 789–4100
Wyle Electronics Corporate . . . . . (949) 753–9953
Wyle Electronics . . . . . (949) 789–9953

Los Angeles

FAI . . . . . (818) 879–1234
Wyle Electronics . . . . . (818) 880–9000

California (Con't.)

Manhattan Beach

Penstock . . . . . (310) 546–8953

Orange County

Allied Electronics, Inc. . . . . (949) 727–3010

Palo Alto

Newark . . . . . (650) 812–6300

Riverside

Allied Electronics, Inc. . . . . (909) 980–6522
Newark . . . . . (909) 980–2105

Rocklin

Hamilton/Hallmark . . . . . (916) 632–4500

Roseville

Wyle Electronics . . . . . (916) 783–9953

Sacramento

Allied Electronics, Inc. . . . . (916) 632–3104
FAI . . . . . (916) 782–7882
Newark . . . . . (916) 565–1760
Wyle Electronics . . . . . (916) 638–5282

San Diego

Allied Electronics, Inc. . . . . (619) 279–2550
Arrow Electronics . . . . . (619) 565–4800
Arrow Zeus . . . . . (619) 565–4800
FAI . . . . . (619) 623–2888
Future Electronics . . . . . (619) 625–2800
Hamilton/Hallmark . . . . . (619) 571–7540
Penstock . . . . . (619) 623–9100
Newark . . . . . (619) 453–8211
Wyle Electronics . . . . . (619) 558–6600

San Fernando Valley

Allied Electronics, Inc. . . . . (818) 598–0130

San Jose

Allied Electronics, Inc. . . . . (408) 383–0366
Arrow Electronics . . . . . (408) 441–9700
Arrow Zeus . . . . . (408) 629–4789
Arrow Electronics . . . . . (408) 428–6400
FAI . . . . . (408) 434–0369
Future Electronics . . . . . (408) 434–1122

Santa Clara

Wyle Electronics . . . . . (408) 727–2500

Santa Fe Springs

Newark . . . . . (650) 929–9722

Sierra Madre

Penstock . . . . . (818) 355–6775

Sunnyvale

Hamilton/Hallmark . . . . . (408) 435–3600
Penstock . . . . . (408) 730–0300

California (Con't.)

Thousand Oaks

Newark . . . . . (805) 449–1480

Woodland Hills

Hamilton/Hallmark . . . . . (818) 594–0404

Colorado

Lakewood

FAI . . . . . (303) 237–1400
Future Electronics . . . . . (303) 232–2008

Denver

Allied Electronics, Inc. . . . . (303) 790–1664
Newark . . . . . (303) 373–4540

Englewood

Arrow Electronics . . . . . (303) 799–0258
Hamilton/Hallmark . . . . . (303) 790–1662
Penstock . . . . . (303) 799–7845

Thornton

Wyle Electronics . . . . . (303) 457–9953

Connecticut

Bloomfield

Newark . . . . . (860) 243–1731

Cheshire

Allied Electronics, Inc. . . . . (203) 272–7730
FAI . . . . . (203) 250–1319
Future Electronics . . . . . (203) 250–0083
Hamilton/Hallmark . . . . . (203) 271–5700

Wallingford

Arrow Electronics . . . . . (203) 265–7741
Wyle Electronics . . . . . (203) 269–8077

Florida

Altamonte Springs

Future Electronics . . . . . (407) 865–7900

Clearwater

FAI . . . . . (813) 530–1665
Future Electronics . . . . . (813) 530–1222

Deerfield Beach

Arrow Electronics . . . . . (305) 429–8200
Wyle Electronics . . . . . (954) 420–0500

Ft. Lauderdale

FAI . . . . . (954) 428–9494
Future Electronics . . . . . (954) 426–4043
Hamilton/Hallmark . . . . . (954) 677–3500
Newark . . . . . (954) 486–1151

Florida (Con't.)

Jacksonville

Allied Electronics, Inc. . . . . (904) 739–5920
Newark . . . . . (904) 399–5041

Lake Mary

Arrow Electronics . . . . . (407) 333–9300
Arrow Zeus . . . . . (407) 333–3055

Largo/Tampa/St. Petersburg

Hamilton/Hallmark . . . . . (813) 507–5000
Newark . . . . . (813) 287–1578
Wyle Electronics . . . . . (813) 576–3004

Maitland

Wyle Electronics . . . . . (407) 740–7450

Miami

Allied Electronics, Inc. . . . . (305) 558–2511

Orlando

Allied Electronics, Inc. . . . . (407) 539–0055
FAI . . . . . (407) 865–9555
Newark . . . . . (407) 896–8350

Tallahassee

FAI . . . . . (904) 668–7772

Tampa

Allied Electronics, Inc. . . . . (813) 579–4660
Newark . . . . . (813) 287–1578
Penstock . . . . . (813) 247–7556

Plantation

Newark . . . . . (305) 424–4400

Winter Park

Hamilton/Hallmark . . . . . (407) 657–3300
Penstock . . . . . (407) 672–1114

Georgia

Atlanta

Allied Electronics, Inc. . . . . (770) 497–9544
FAI . . . . . (404) 447–4767

Duluth

Arrow Electronics . . . . . (404) 497–1300
Hamilton/Hallmark . . . . . (770) 623–4400

Norcross

Future Electronics . . . . . (404) 441–7676
Newark . . . . . (404) 448–1300
Wyle Electronics . . . . . (770) 441–9045
Penstock . . . . . (770) 734–9990

Idaho

Boise

Allied Electronics, Inc. . . . . (208) 331–1414
FAI . . . . . (208) 376–8080

Illinois

Addison

Wyle Electronics . . . . . (630) 620–0969

Arlington Heights

Hamilton/Hallmark . . . . . (847) 797–7300
Allied Electronics, Inc. (North) . . . . (847) 548–9330
Allied Electronics, Inc. (South) . . . . (708) 843–0034
FAI . . . . . (708) 843–0034
Newark Electronics Corp. . . . . (773) 784–5100

Hoffman Estates

Future Electronics . . . . . (708) 882–1255

Itasca

Arrow Electronics . . . . . (708) 250–0500
Arrow Zeus . . . . . (630) 595–9730

Lombard

Newark . . . . . (630) 317–1000

Palatine

Penstock . . . . . (708) 934–3700

Rockford

Allied Electronics, Inc. . . . . (815) 636–1010
Newark . . . . . (815) 229–0225

Springfield

Newark . . . . . (217) 787–9972

Wood Dale

Allied Electronics, Inc. . . . . (630) 860–0007

Indiana

Indianapolis

Allied Electronics, Inc. . . . . (317) 571–1880
Arrow Electronics . . . . . (317) 299–2071
FAI . . . . . (317) 469–0441
Future Electronics . . . . . (317) 469–0447
Hamilton/Hallmark . . . . . (317) 575–3500
Newark . . . . . (317) 844–0047
Wyle Electronics . . . . . (317) 581–6152

Ft. Wayne

Newark . . . . . (219) 484–0766
Penstock . . . . . (219) 432–1277

Iowa

Bettendorf

Newark . . . . . (319) 359–3711

Cedar Rapids

Allied Electronics, Inc. . . . . (319) 390–5730
Newark . . . . . (319) 393–3800

Kansas

Kansas City

Allied Electronics, Inc. . . . . (913) 541–9542
FAI . . . . . (913) 381–6800

Lenexa

Arrow Electronics . . . . . (913) 541–9542

Olathe

Penstock . . . . . (913) 829–9330

Overland Park

Future Electronics . . . . . (913) 649–1531
Hamilton/Hallmark . . . . . (913) 663–7900
Newark . . . . . (913) 677–0727

Kentucky

Louisville

Allied Electronics, Inc. . . . . (502) 452–2293
Newark . . . . . (502) 423–0280

Louisiana

New Orleans

Allied Electronics, Inc. . . . . (504) 466–7575
Newark . . . . . (504) 838–9771

Massachusetts

Bedford

Wyle Electronics . . . . . (781) 271–9953

Boston

Allied Electronics, Inc. . . . . (617) 255–0361
Arrow Electronics . . . . . (508) 658–0900
FAI . . . . . (508) 779–3111
Newark 1–800–4NEWARK

Bolton

Future Corporate . . . . . (978) 779–3000

Burlington

Penstock . . . . . (617) 229–9100

Lowell

Newark . . . . . (978) 551–4300

Peabody

Allied Electronics, Inc. . . . . (508) 538–2401
Hamilton/Hallmark . . . . . (508) 532–3701

Wilmington

Arrow Zeus . . . . . (978) 658–4776

Worchester

Newark . . . . . (508) 229–2200

Michigan

Detroit

Allied Electronics, Inc. . . . . (313) 416–9300
FAI . . . . . (313) 513–0015
Newark . . . . . (313) 967–0600

Grand Rapids

Future Electronics . . . . . (616) 698–6800
Newark . . . . . (616) 954–6700

Livonia

Arrow Electronics . . . . . (810) 455–0850
Future Electronics . . . . . (313) 261–5270
Hamilton/Hallmark . . . . . (313) 416–5800

Novi

Wyle Electronics . . . . . (248) 374–9953

Saginaw

Newark . . . . . (517) 799–0480

Troy

Newark . . . . . (248) 583–2899

Minnesota

Bloomington

Wyle Electronics . . . . . (612) 853–2280

Burnsville

Penstock . . . . . (612) 882–7630

Eden Prairie

Arrow Electronics . . . . . (612) 941–5280
FAI . . . . . (612) 947–0909
Future Electronics . . . . . (612) 944–2200
Hamilton/Hallmark . . . . . (612) 881–2600

Minneapolis

Allied Electronics, Inc. . . . . (612) 938–5633
Newark . . . . . (612) 331–6350
Hamilton/Hallmark . . . . . (314) 291–5350

Mississippi

Jackson

Newark . . . . . (601) 956–3834

Missouri

Earth City

Hamilton/Hallmark . . . . . (314) 770–6300

St. Louis

Allied Electronics, Inc. . . . . (314) 240–9405
Arrow Electronics . . . . . (314) 567–6888
FAI . . . . . (314) 542–9922
Future Electronics . . . . . (314) 469–6805
Newark . . . . . (314) 991–0400

Missouri (Con't.)

Novi

Wyle Electronics . . . . . (248) 374–9953

Nebraska

Omaha

Allied Electronics, Inc. . . . . (402) 697–0038
Newark . . . . . (402) 592–2423

Nevada

Las Vegas

Allied Electronics, Inc. . . . . (702) 258–1087
Wyle Electronics . . . . . (702) 765–7117

New Jersey

Bridgewater

Penstock . . . . . (908) 575–9490

East Brunswick

Allied Electronics, Inc. . . . . (908) 613–0828
Newark . . . . . (732) 937–6600

Fairfield

FAI . . . . . (201) 331–1133

Long Island

FAI . . . . . (516) 348–3700

Marlton

Arrow Electronics . . . . . (609) 596–8000
FAI . . . . . (609) 988–1500
Future Electronics . . . . . (609) 596–4080

Mt. Laurel

Hamilton/Hallmark . . . . . (609) 222–6400
Wyle Electronics . . . . . (609) 439–9020

Oradell

Wyle Electronics . . . . . (201) 261–3200

Parsippany

Future Electronics . . . . . (201) 299–0400
Hamilton/Hallmark . . . . . (201) 515–1641

Pinebrook

Wyle Electronics . . . . . (973) 882–8358

New Mexico

Albuquerque

Allied Electronics, Inc. . . . . (505) 872–2770
Hamilton/Hallmark . . . . . (505) 293–5119
Newark . . . . . (505) 828–1878

New York

Albany

Newark . . . . . (518) 489–1963

Buffalo

Newark . . . . . (716) 631–2311

New York (Con't.)

Great Neck

Allied Electronics, Inc. . . . . (516) 487–5211

Hauppauge

Allied Electronics, Inc. . . . . (516) 234–0485
Arrow Electronics . . . . . (516) 231–1000
FAI . . . . . (516) 348–3700
Future Electronics . . . . . (516) 234–4000
Hamilton/Hallmark . . . . . (516) 434–7400
Newark . . . . . (516) 567–4200
Penstock . . . . . (516) 724–9580
Wyle . . . . . (516) 231–7850

Henrietta

Wyle Electronics . . . . . (716) 334–5970

Konkoma

Hamilton/Hallmark . . . . . (516) 737–0600

Poughkeepsie

Allied Electronics, Inc. . . . . (914) 452–1470
Newark . . . . . (914) 298–2810

Purchase

Arrow Zeus . . . . . (914) 701–7400

Rochester

Allied Electronics, Inc. . . . . (716) 292–1670
Arrow Electronics . . . . . (716) 427–0300
FAI . . . . . (716) 387–9600
Future Electronics . . . . . (716) 387–9600
Hamilton/Hallmark . . . . . (716) 272–2740
Newark . . . . . (716) 381–4244

Syracuse

Allied Electronics, Inc. . . . . (315) 446–7411
FAI . . . . . (315) 451–4405
Future Electronics . . . . . (315) 451–2371
Newark . . . . . (315) 457–4873

North Carolina

Charlotte

Allied Electronics, Inc. . . . . (704) 525–0300
FAI . . . . . (704) 548–9503
Future Electronics . . . . . (704) 547–1107
Newark . . . . . (704) 535–5650

Greensboro

Newark . . . . . (910) 294–2142

Morrisville

Wyle Electronics . . . . . (919) 469–1502

Raleigh

Allied Electronics, Inc. . . . . (919) 876–5845
Arrow Electronics . . . . . (919) 876–3132
FAI . . . . . (919) 876–0088
Future Electronics . . . . . (919) 790–7111
Hamilton/Hallmark . . . . . (919) 872–0712

Ohio

Centerville

Arrow Electronics . . . . . (513) 435–5563

Cincinnati

Allied Electronics, Inc. . . . . (513) 771–6990
Newark . . . . . (513) 942–8700

Cleveland

Allied Electronics, Inc. . . . . (216) 831–4900
FAI . . . . . (216) 446–0061
Newark . . . . . (216) 391–9330

Columbus

Allied Electronics, Inc. . . . . (614) 785–1270
Newark . . . . . (614) 326–0352

Dayton

FAI . . . . . (513) 427–6090
Future Electronics . . . . . (513) 426–0090
Hamilton/Hallmark . . . . . (513) 439–6735
Newark . . . . . (937) 294–8980

Mayfield Heights

Future Electronics . . . . . (216) 449–6996

Miamisburg

Wyle Electronics . . . . . (937) 436–9953

Solon

Arrow Electronics . . . . . (216) 248–3990
Hamilton/Hallmark . . . . . (216) 498–1100
Wyle Electronics . . . . . (440) 248–9996

Toledo

Newark . . . . . (419) 866–0404

Worthington

Hamilton/Hallmark . . . . . (614) 888–3313

Oklahoma

Oklahoma City

Newark . . . . . (405) 943–3700

Tulsa

Allied Electronics, Inc. . . . . (918) 250–4505
FAI . . . . . (918) 492–1500
Hamilton/Hallmark . . . . . (918) 459–6000

Oregon

Beaverton

Arrow Electronics Corp. . . . . (503) 629–8090
Hamilton/Hallmark . . . . . (503) 526–6200
Wyle Electronics . . . . . (503) 598–9953

Portland

FAI . . . . . (503) 603–0866
Future Electronics . . . . . (503) 603–0956
Newark . . . . . (503) 297–1984
Penstock . . . . . (503) 646–1670

Pennsylvania

Allentown
Newark . . . . . (610) 434–7171

Chadds Ford
Allied Electronics, Inc. . . . . (610) 388–8455

Coatsville
Penstock . . . . . (610) 383–9536

Ft. Washington
Newark . . . . . (215) 654–1434

Harrisburg
Allied Electronics, Inc. . . . . (717) 540–7101

Philadelphia
Allied Electronics, Inc. . . . . (609) 234–7769

Pittsburgh
Allied Electronics, Inc. . . . . (412) 931–2774
Arrow Electronics . . . . . (412) 963–6807
Newark . . . . . (503) 297–1984

South Carolina

Greenville
Allied Electronics, Inc. . . . . (864) 288–8835
Allied Electronics, Inc. . . . . (864) 288–9610

Tennessee

Knoxville
Newark . . . . . (423) 588–6493

Memphis
Newark . . . . . (901) 396–7970

Texas

Austin
Allied Electronics, Inc. . . . . (512) 219–7171
Arrow Electronics . . . . . (512) 835–4180
FAI . . . . . (512) 346–6426
Future Electronics . . . . . (512) 502–0991
Hamilton/Hallmark . . . . . (512) 219–3700
Newark . . . . . (512) 338–0287
Penstock . . . . . (512) 346–9762
Wyle Electronics . . . . . (512) 833–9953

Benbrook
Penstock . . . . . (817) 249–0442

Brownsville
Allied Electronics, Inc. . . . . (210) 548–1129

Carrollton
Arrow Electronics . . . . . (972) 380–6464
Arrow Zeus . . . . . (972) 380–4330

Texas (Con't.)

Dallas
Allied Electronics, Inc. . . . . (214) 341–8444
FAI . . . . . (972) 231–7195
Future Electronics . . . . . (972) 437–2437
Hamilton/Hallmark . . . . . (214) 553–4300
Newark . . . . . (972) 458–2528

El Paso
Allied Electronics, Inc. . . . . (915) 779–6294
FAI . . . . . (915) 577–9531
Newark . . . . . (915) 772–6367

Ft. Worth
Allied Electronics, Inc. . . . . (817) 595–3500

Houston
Allied Electronics, Inc. . . . . (281) 446–8005
Arrow Electronics . . . . . (281) 647–6868
FAI . . . . . (713) 952–7088
Future Electronics . . . . . (713) 785–1155
Hamilton/Hallmark . . . . . (713) 781–6100
Newark . . . . . (281) 894–9334
Wyle Electronics . . . . . (713) 784–9953

Richardson
Penstock . . . . . (972) 479–9215
Wyle Electronics . . . . . (972) 235–9953

San Antonio
FAI . . . . . (210) 738–3330

Utah

Draper
Wyle Electronics . . . . . (801) 523–2335

Salt Lake City
Allied Electronics, Inc. . . . . (801) 261–5244
Arrow Electronics . . . . . (801) 973–6913
FAI . . . . . (801) 467–9696
Future Electronics . . . . . (801) 467–4448
Hamilton Halmark . . . . . (801) 266–2022
Newark . . . . . (801) 261–5660
Wyle Electronics . . . . . (801) 974–9953

West Valley City
Wyle Electronics . . . . . (801) 974–9953

Virginia

Herndon
Newark . . . . . (703) 707–9010

Richmond
Newark . . . . . (804) 282–5671

Springfield
Allied Electronics, Inc. . . . . (703) 644–9515

Virginia Beach
Allied Electronics, Inc. . . . . (757) 363–8662

Washington

Bellevue

Almac Electronics Group . . . . . (206) 643–9992
Penstock . . . . . (206) 454–2371

Bothell

Future Electronics . . . . . (206) 489–3400

Kirkland

Newark . . . . . (425) 814–6230

Redmond

Hamilton/Hallmark . . . . . (206) 882–7000
Wyle Electronics . . . . . (425) 881–1150

Seattle

Allied Electronics, Inc. . . . . (206) 251–0240
FAI . . . . . (206) 485–6616

Spokane

Newark . . . . . (509) 327–1935

Wisconsin

Brookfield

Arrow Electronics . . . . . (414) 792–0150
Future Electronics . . . . . (414) 879–0244
Wyle Electronics . . . . . (414) 879–0434

Madison

Newark . . . . . (608) 278–0177

Milwaukee

Allied Electronics, Inc. . . . . (414) 796–1280
FAI . . . . . (414) 792–9778

New Berlin

Hamilton/Hallmark . . . . . (414) 780–7200

Wauwatosa

Newark . . . . . (414) 453–9100

Canada – Autorized Distributors

Alberta

Future Active Calgary
(Bus. Accts.) 403–219–3443
Active Components Calgary
(Retail Sales) 403–291–5626
Future Active Edmonton
(Bus. Accts.) 780–438–5888
Active Components Edmonton
(Retail Sales) 780–438–0644
Avnet for Western Canada (OEM Contract,
Repair, Retail Sales) 1–800–332–8638
Avent for Western Canada
(Disty & Bus. Sales) 1–800–672–8638

British Columbia

Vancouver

Allied Electronics, Inc. . . . . (604) 420–9691
Arrow Electronics . . . . . (604) 421–2333
FAI . . . . . (604) 654–1050
Future Electronics . . . . . (604) 294–1166
Hamilton/Avnet Electronics . . . . . (604) 420–4101
Newark . . . . . (800) 463–9275

Manitoba

Winnipeg

FAI . . . . . (209) 786–3075
Future Electronics . . . . . (204) 944–1446
Hamilton/Hallmark . . . . . (800) 663–5500
Newark . . . . . (800) 463–9275

Ontario

Kanata

Penstock . . . . . (613) 592–6088

London

Newark . . . . . (519) 685–4280

Mississauga

Penstock . . . . . (905) 403–0724
Newark . . . . . (905) 670–2888

Ottawa

Allied Electronics, Inc. . . . . (613) 228–1964
Arrow Electronics . . . . . (613) 226–6903
FAI . . . . . (613) 820–8244
Future Electronics . . . . . (613) 727–1800
Hamilton/Hallmark . . . . . (613) 226–1700

Toronto

Arrow Electronics . . . . . (905) 670–7769
FAI . . . . . (905) 612–9888
Future Electronics . . . . . (905) 612–9200
Hamilton/Hallmark . . . . . (905) 564–6060
Newark . . . . . (905) 670–2888

Quebec

Montreal

Arrow Electronics . . . . . (514) 421–7411
FAI . . . . . (514) 694–8157
Future Electronics . . . . . (514) 694–7710
Hamilton/Hallmark . . . . . (514) 335–1000

Mt. Royal

Newark . . . . . (514)738–4488

Quebec City

Arrow Electronics . . . . . (418) 687–4231
FAI . . . . . (418) 877–1414
Future Electronics . . . . . (418) 877–6666

International – Authorized Distributors

Argentina

Electrocomponentes 54–11–4375–3366
Elko 54–11–4372–1101

Australia

Veltek Australia Pty. Ltd
9 Bastow Place
Mulgrave
VIC 3170
Australia
Tel ..... (61–3) 9574–9300
Fax ..... (61–3) 9574–9773
WWW ..... http://www.arrowveltek.com

Avnet Pacific Pty. Ltd
Unit C 6–8 Lyon Park Road
North Ryde NSW 2113
Australia
Tel ..... 132 732 (nationwide)
Fax ..... (61–2) 9878–1166
WWW ..... http://www.avnet.com

Future Electronics
1013 Whitehorse Road,
Box Hill,
3128,
VIC,
Australia
Tel ..... (61–3) 9899–7944
Fax ..... (61–3) 9899–3449
WWW ..... http://www.future.ca

Farnell ..... (61) 2 9644–7722

Austria

EBV Elektronik ..... (43)189152–0
Farnell ..... (49) 8961 393939
SEI/Elbatex GmbH ..... (43) 1 866420
Spoerle Electronic ..... (43) 1 360460

Belgium

EBV Elektronik ..... (32) 2 716 0010
Farnell ..... (31) 30 241 7333
Future Electronics ..... (32) 3 780 3001
SEI Belgium ..... (32) 2 460 0747
Spoerle Electronic ..... (32) 2 725 4660

Brazil

Avnet 55–11–5079–2150
Baron Electronics: 1–305–685–1400
Farnell 55–11–4066–9400
Future 55–19–235–1511
Intertek 55–11–266–2922
Karimex 55–11–5189–1900
Masktrade 55–11–3361–2766
Panamericana 55–11–3661–6133
Siletec 55–11–536–4401
Tec 55–11–5505–2046
Teleradio 55–11–574–0788

Bulgaria

Macro Group ..... (359) 2708140

Chile

Baron Electronics 1–305–685–1400

China

Nanco Electronics Supply Ltd
11/F. Kaiser Estate
51 Man Yue St.
Hunghom
Kowloon
Hong Kong
Tel ..... (852) 2333–5121
Fax ..... (852) 2764–3073
WWW ..... http://www.NANCO.com

Avnet WKK Components Ltd
10/F. WKK Building
418A Kwun Tong Road,
Kowloon
Hong Kong
Tel ..... (852) 2357–8888
Fax ..... (852) 2790–2182
WWW ..... http://www.avnet.com

China Electronic Appliance Corp.
Room 202, Heng Xin Business Building,
No. 61, Fu Xing Lu Avenue,
Bejing 100036,
P.R.C.
Tel ..... (86–10) 6823–9951
Fax ..... (86–10) 6817–4517

Qing Cheng Enterprises Ltd
Rm.1901 19/F. Nan Fung Centre
264–298 Castle Peak Rd.
Tsuen Wan
Hong Kong
Tel ..... (852) 2493–4202
Fax ..... (852) 2413–6307

China (Con't.)

Future Electronics
Shanghai Office
Room 122 Office Tower,
351 Wuyi Road,
Shanghai,
200050
Tel . . . . . (021) 6213–6801
Fax . . . . . (021) 6252–9356
WWW . . . . . http://www.future.ca

Future Electronics
Hong Kong Office
Unit 910, 9/F., Block B, Po Lung Centre
11 Wang Chiu Road, Kowloon Bay,
Hong Kong
Tel . . . . . (852) 2305–3633
Fax . . . . . (852) 2795–4877
WWW . . . . . http://www.future.ca

Arrow Electronics China Ltd
20/F, Tower Two, Ever Gain Plaza,
88 Container Port Road,
Kwai Chung,
Hong Kong
Tel . . . . . (852) 2484–2113
Fax . . . . . (852) 2484–2123
WWW . . . . . http://www.arrowasia.com

MARUBUN/ARROW (HK) Ltd.
10/Floor, No.1005,
Tower I, Silvercord Road,
30 Canton Road,
Kowloon,
Hong Kong.
Tel . . . . . (852) 2375–1126
Fax . . . . . (852) 2375–9858
WWW . . . . . http://www.marubunarrow.com

Colombia

Baron Electronics 1–305–685–1400

Costa Rica

Baron Electronics 1–305–685–1400

Czech Republic

EBV Elektronik . . . . . (420) 2 90022101
Spoerle Electronic . . . . . (420) 2 71737173
SEI/Elbatex . . . . . (420) 2 4763707
Macro Group . . . . . (420) 2 3412182

Denmark

Arrow Denmark A/S . . . . . (45) 44 508200
A/S Avnet EMG . . . . . (45) 44 880800
EBV Elektronik – Abyhoj . . . . . (45) 86250466
EBV Elektronik – Aabyhoej . . . . . (45) 86250660
Farnell . . . . . (45) 44 536644
Future Electronics . . . . . (45) 961 00 961

Estonia

Arrow Field Eesti . . . . . (372) 6503288
Avnet Baltronic . . . . . (372) 6397000
Farnell . . . . . (358) 9345 5400

Finland

Arrow Finland . . . . . (358) 9 476660
Avnet Nortek . . . . . (358) 9 613181
EBV Elektronik . . . . . (358) 9 27052790
Farnell . . . . . (358) 9345 5400
Future Electronics . . . . . (358) 9 3455400

France

Arrow Electronique . . . . . (33) 1 49 78 49 78
Avnet . . . . . (33) 1 49 65 27 00
EBV Elektronik . . . . . (33) 1 40963000
Farnell . . . . . (33) 474 659466
Future Electronics . . . . . (33) 1 69821111
Sonepar Electronique . . . . . (33) 1 69 19 89 00

Germany

Avnet EMG . . . . . (49) 89 4511001
EBV Elektronik GmbH . . . . . (49) 89 99114–0
Farnell . . . . . (49) 89 61 303103
Future Electronics GmbH . . . . . (49) 89–957 270
SEI/Jermyn GmbH . . . . . (49) 6431–5080
Spoerle Electronic . . . . . (49) 6103–304–0

Greece

EBV Elektronik . . . . . (30) 13414300

Hong Kong

Arrow Asia Pac Ltd
20/F., Tower Two, Ever Gain Plaza,
88 Container Port Road,,
Kwai Chung,
Hong Kong
Tel . . . . . (852) 2484–2484
Fax . . . . . (852) 2484–2468
WWW . . . . . http://www.arrowasia.com

Arrow/Components Agent Ltd
26/F, Metroplaza,
Tower II,
Hing Fong Road,
Kwai Chung,
Hong Kong
Tel . . . . . (852) 2484–2112
Fax . . . . . (852) 2484–2188
WWW . . . . . http://www.arrowasia.com

7

Hong Kong (Con't.)

EEC International (HK) Limited.
room 805, 8/F., Hung–Hom Commercial Centre
Tower B, 37–39, Ma Tau Wai Road,
Hung Hom,
Kowloon,
Hong Kong.
Tel . . . . . (852) 2365–7775 ext.512
Fax . . . . . (852) 2365–7767

MARUBUN/ARROW (HK) Ltd.
10/Floor, No.1005,
Tower I, Silvercord Road,
30 Canton Road,
Kowloon,
Hong Kong.
Tel . . . . . (852) 2375–1126
Fax . . . . . (852) 2375–9858
WWW . . . . . http://www.marubunarrow.com

Nanco Electronics Supply Ltd
11/F. Kaiser Estate
51 Man Yue St.
Hunghom
Kowloon
Hong Kong
Tel . . . . . (852) 2333–5121
Fax . . . . . (852) 2764–3073
WWW . . . . . http://www.NANCO.com

Avnet WKK Components Ltd
10/F. WKK Building
418A Kwun Tong Road,
Kowloon
Hong Kong
Tel . . . . . (852) 2357–8888
Fax . . . . . (852) 2790–2182
WWW . . . . . http://www.avnet.com

Future Electronics
Unit 4607–19,
Metro Plaza, Tower I
223 Hing Fong Road
Kwai Fong, Hong Kong.
Tel . . . . . (852) 2420–6238
Fax . . . . . (852) 2423–0767
WWW . . . . . http://www.future.ca

Arrow/Texny (HK) Ltd.
26/F, Metroplaza, Tower II,
Hing Fong Road,
Kwai Chung,
Hong Kong
Tel . . . . . (852) 2765–0118
Fax . . . . . (852) 2765–0557
WWW . . . . . http://www.arrowasia.com

Hong Kong (Con't.)

Qing Cheng Enterprises Ltd.
Rm. 1901, 19/F, Nan Fung Centre
264 – 298, Castle Peak Rd.
Tsuen Wan
Hong Kong
Tel . . . . . (852) 2493–4202
Fax . . . . . (852) 2413–6307

Hungary

Spoerle Electronic . . . . . (36) 11409194
(36) 11294202
Future Electronics . . . . . (36) 11409194
(36) 1 224 0510
Macro Group . . . . . (36) 11409194
(36) 12030277
SEI/Elbatex . . . . . (36) 11409194

India

Future Electronics
A–401, Mittal Towers,
M. G. Road,
Bangalore,
560 001
Tel . . . . . (91–80) 5593106
Fax . . . . . (91–80) 5592995
WWW . . . . . http://www.future.ca

Max India Ltd
1st Floor
No.5 Siri Fort Road
New Delhi –110 049
Tel . . . . . (91–11) 6250250
Fax . . . . . (91–11) 6449804

Arrow Electronics (India) Ltd.
34/4, Meanee Avenue Tank Road,
Bangalore –560 042,
India
Tel . . . . . (91) 80 5546125
Fax . . . . . (91) 80 5546319
WWW . . . . . http://www.arrowasia.com

Indonesia

PT. Ometraco
JL. Daan Mogot, Km. 12
No.9 Cengkareng
Jakarta 11730
Indonesia
Tel . . . . . (6221) 619–6166
Fax . . . . . (6221) 619–3447

Ireland

Arrow Electronics . . . . . (353) 14595540
EBV Elektronik . . . . . (353) 14564034
Farnell . . . . . (353) 18309277
Future Electronics . . . . . (353) 6541330
Macro Group . . . . . (353) 16766904

Italy

Avnet EMG ..... (39) 02 381901
EBV Elektronik Italy ..... (39) 02 66096290
Farnell ..... (44) 113 231 1311
Future Electronics ..... (39) 02 660941
Silverstar Ltd ..... (39) 02 66 12 51

Japan

AMSC Co., Ltd 81–422–54–6800
Fuji Electronics Co., Ltd 81–3–3814–1415
Marubun Corporation 81–3–3639–8951
Tokyo Electron Device Ltd. 81–45–474–7036

Korea

Arrow Electronics Korea Ltd.
7/F. CBS Building
917–01 Mok–Dong, Yangchon–Ku
Seoul Korea 135–090
Tel ..... (82–2) 650–6400
Fax ..... (82–2) 650–6464

Future Electronics
18F KyungAm Bldg, 15–27
Samsung–Dong, KangNam–Gu
Seoul Korea 135–090
Tel ..... (82–2) 555–6736
Fax ..... (82–2) 555–6420
WWW ..... http://www.future.ca

Segyung Electronics
Dansan–Segyung Bldg.,
270–45 Nonhyun–Dong,
Kangnam–Gu,
Seoul 135–010
Tel ..... (82–2) 514–5614
Fax ..... (82–2) 514–3323
WWW ..... http://www.segyung.com

Nasco Co. Ltd
NamSung Bldg, #345–30
Kasan–dong
KeumChun–Gu
Seoul
Korea 153–023
Tel ..... (82–2) 868–4988
Fax ..... (82–2) 868–2984

Liteon Korea Ltd
10/F. CBS Building
917–01 Mok–Dong,
Yangchon–Ku
Seoul
Korea
Tel ..... (82–2) 650–9700
Fax ..... (82–2) 653–2700

Korea (Con't.)

Jung Kwang Semiconductors Ltd
64 Jangsa–Dong
Chongro–Ku
Seoul
Korea
Tel ..... (82–2) 2278–5333
Fax ..... (82–2) 2267–8723

Latvia

Avnet Baltronic Ltd ..... (371) 8821118
Macro Group ..... (371) 7313195

Lithuania

Macro Group ..... (370) 7–764937

Malaysia

Ultro Technologies Pte. Ltd
47 Loyang Drive
Singapore 1750
Tel ..... (65) 545–7811 / 540–8328
Fax ..... (65) 545–6120 / 545–6108

Arrow Strong Electronics (M) Sdn Bhd
737–2–5, Jalan Sultan Azlan Shah,
11900 Penang
Malaysia
Tel ..... (604) 646–4768
Fax ..... (604) 646–4767
WWW ..... http://www.arrowasia.com

Arrow Components (M) Sdn Bhd
Suite 18.01,
Menara PSCI,
39 Jalan Sultan
Ahmad Shah,
10050 Penang
Malaysia
Tel ..... (604) 229–6613
Fax ..... (604) 229–6623
WWW ..... http://www.arrowasia.com

Future Electronics
51–19–F1 Menara BHL Bank,
51, Jalan Sultan Ahmad Shah,
Penang,
10050
Tel ..... (60–4) 2277213
Fax ..... (60–4) 2277263
WWW ..... http://www.future.ca

Mexico

Avnet ..... (3) 632–0182
Dicopel ..... (5) 705–7422
Future ..... (3) 122–0043
Semiconductores Professionales .... (5) 658–6011
Steren ..... (5) 325–0925

Netherlands

Holland

EBV Elektronik . . . . . (31) 3465 83010
Farnell . . . . . (31) 30 241 7333
Future Electronics . . . . . (31) 76 544 4888
SEI Benelux B.V. . . . . (31) 7657 22500
Spoerle Electronics Nieuwegen . . . (31) 306391234
Spoerle Electronics Veldhoven . . . (31) 402545430

New Zealand

Avnet Pacific Ltd
274 Church Street
Penrose
Private Bag 92821
Auckland
New Zealand
Tel . . . . . (64–9) 636–7801
Fax . . . . . (64–9) 636–7803 / (64–9) 634–4901
WWW . . . . . http://www.avnet.com

Arrow Components (NZ) Ltd
19 Pretoria Street
Lower Hutt.
Wellington, NZ
Tel . . . . . (64) 4570–2260
Fax . . . . . (64) 4566–2111
WWW . . . . . http://www.arrowasia.com

Future Electronics
c/o – Premier Freight,
20 Symes Road,
Sockburn,
Christchurch,
NZ
Tel . . . . . (64) 3348–0256
Fax . . . . . (64) 3343–5936
WWW . . . . . http://www.future.ca

Farnell . . . . . (612) 9 644–7722

Norway

Arrow Tahonic A/S . . . . . (47) 2237 8440
A/S Avnet EMG . . . . . (47) 6677 3600
EBV Elektronik . . . . . (47) 2267 1780
Future Electronics . . . . . (47) 2290 5800

Philippines

Ultro Technologies Pte. Ltd
47 Loyang Drive
Singapore 1750
Tel . . . . . (65) 545–7811 / 540–8328
Fax . . . . . (65) 545–6120 / 545–6108

Philippines (Con't.)

Future Electronics
Suite 203, Richville Corporate Center
1314 Commerce Avenue,
Madrigal Business Park,
Ayala Alabang, Muntinlupa City
Tel . . . . . (632–807) 5092 / 3512 / 3524
Fax (623–807) 5187
WWW . . . . . http://www.future.ca

Poland

EBV Elektronik . . . . . (48) 713422944
Future Electronics . . . . . (48) 22 61 89202
Macro Group . . . . . (48) 22 224337
SEI/Elbatex . . . . . (48) 22 6217122
Spoerle Electronic . . . . . (48) 22 6465227

Portugal

Amitron Arrow . . . . . (35) 114714182
Farnell . . . . . (34) 90120 2080
SEI–Selco . . . . . (351) 2–973–82–03

Romania

Macro Group . . . . . (401) 6343129

Russia

St. Petersburg

Macro Group . . . . . (781) 25311476

Moscow

Macro Group – Moscow . . . . . (7) 095 30600266
EBV Elektronik . . . . . (7) 095 976 11 76

Scotland

EBV Elektronik . . . . . (44) 1414202070
Future . . . . . (44) 1 419413999

Singapore

Avnet Cinergi Pte Ltd.
Block 5012,
Ang Mo Kio Avenue 5
#04–02/04
Singapore 569876
Tel . . . . . (65) 481–6776
Fax . . . . . (65) 482–6776 / 483–6776
WWW . . . . . http://www.avnet.com

MARUBUN/ARROW Electronics (S) Pte. Ltd.
77 Robinson Road
#21–02 Sia Building
Singapore 068896
Tel . . . . . (65) 536–0050
Fax . . . . . (65) 536–2400
WWW . . . . . http://www.marubunarrow.com

Singapore (Con't.)

Future Electronics Ltd
396 Alexandra Road
#15–02 BP Tower
Singapore 119954
Tel . . . . . (65) 479–1300
Fax . . . . . (65) 479–3151
WWW . . . . . http://www.future.ca

Ultro Technologies Pte. Ltd
47 Loyang Drive
Singapore 1750
Tel . . . . . (65) 545–7811 / 540–8328
Fax . . . . . (65) 545–6120 / 545–6108

Arrow Strong Electronics (S) Pte. Ltd
Blk. 203, Wing B
#07–07 Henderson Road
Henderson Industrial Park
Singapore 159548
Tel . . . . . (65) 276–3996
Fax . . . . . (65) 276–5765
WWW . . . . . http://www.arrowasia.com

Arrow Electronics (S) Pte Ltd.
31 Kaki Bukit Rd 3,
#04–08/09 Tech Link,
Singapore 417818
Tel . . . . . (65) 8458388
Fax . . . . . (65) 8458288
WWW . . . . . http://www.arrowasia.com

Farnell . . . . . (66) 788–3922

Slovakia

Macro Group . . . . . (42) 89634181
SEI/Elbatex . . . . . (42) 17295007

Slovenia

EBV Elektronik . . . . . (386) 611 330216
SEI/Elbatex . . . . . (386) 611 597198

South Africa

Avnet–ASD . . . . . (27) 11 4442333
Reutech Components . . . . . (27) 11 3972992

Spain

Amitron Arrow . . . . . (34) 91 3043040
EBV Elektronik . . . . . (34) 91 8043256
Farnell . . . . . (44) 113 231 0447
SEI/Selco S.A. . . . . (34) 91 637 10 11

Sweden

Arrow–TH:s AB . . . . . (46) 8 56265500
Avnet EMG AB . . . . . (46) 8 629 14 00
EBV Elektronik . . . . . (46) 405 92100
Farnell . . . . . (46) 8 730–5000
Future Electronics . . . . . (46) 8 441 5470

Switzerland

EBV Elektronik . . . . . (41) 1 7456161
Farnell . . . . . (41) 1204 6464
SEI/Elbatex AG . . . . . (41) 56 4375111
Spoerle Electronic . . . . . (41) 1 8746262

Taiwan

Elitetron Electronic Co. Ltd
11 F–3, No. 160. Sec 6,
Min Chuan E.Road,
Taipei
Taiwan, R.O.C.
Tel . . . . . (886–2) 2796–2400
Fax . . . . . (886–2) 2792–4901
WWW . . . . . http://www.eeco.com.tw

Avnet Mercuries Co. Ltd
6/F. No.145
Sec 2, Chien Kuo N. Road
Taipei
Taiwan, R.O.C.
Tel . . . . . (886–2) 2516–7303
Fax . . . . . (886–2) 2505–7391
WWW . . . . . http://www.avnet.com

Solomon Technology Corp.
7/F. No. 2. Lane 47, Section 3
Namkang Road
Taipei
Taiwan
Tel . . . . . (886–2) 2788–8989
Fax . . . . . (886–2) 2788–8284
WWW . . . . . http://www.solomon.com.tw

Arrow/Ally Inc.
16F, No 100, Sec 1,
Hsin Tai Wu Road,
Hsi Chih, Taipei
Taiwan, R.O.C.
Tel . . . . . (886–2) 2696–7388
Fax . . . . . (886–2) 2696–7399

Strong Electronics Co. Ltd
3/F., No. 4, Lane 235,
Pad Chaio Road
Hsintien City
Taipei
Taiwan
Tel . . . . . (886–2) 2917–9917
Fax . . . . . (886–2) 2917–8439
WWW . . . . . http://www.strong.com.tw

Future Electronics
Taipei,
12–1, F, No 67 Sung Chian Road
Taipei,
Taiwan.
Tel . . . . . (886–2) 2517–0900
Fax . . . . . (886–2) 2507–4100
WWW . . . . . http://www.future.ca

Thailand

Ultro Technologies Pte. Ltd
47 Loyang Drive
Singapore 1750
Tel . . . . . (65) 545–7811 / 540–8328
Fax . . . . . (65) 545–6120 / 545–6108

Sahapiphat Ltd
70 Pan Rd.
Sataporn Building Room No. 203
Silom Bangruk
Bangkok 10500
Thailand
Tel . . . . . (662) 237–9474 / 5 / 6 / 7
Fax . . . . . (662) 237–9473
WWW . . . . . http://www.sahapiphat.th.com

Future Electronics (Thailand) Ltd.
Thosapol Land 3 Building,
Fl 21, Room #C2,
947 M.12 Bangna–trad Rd K.M.3,
Bangna Prakanong,
Bangkok 10260
Tel . . . . . (662) 361–8400–2
Fax . . . . . (662) 361–8433
WWW . . . . . http://www.future.ca

Thailand (Con't.)

3Arrow Strong Electronics (S) Pte Ltd.
Room 301, Rangsit Building,
315/118 Rangsit–Pathumthani Road,
Prachathipat, Thanyaburi,
Pathnumthani 12130, Thailand
Te . . . . . (662) 567 5025–6
Fa . . . . . (662) 567 5027
WWW . . . . . http://www.arrowasia.com

Turkey

EBV Elektronik . . . . . (90) 216 4631352
Motorola Representative . . . . . (90) 212 274 66 48

United Kingdom

Arrow Electronics (UK) Ltd . . . . . (44) 1 234 270027
Avnet EMG 44 . . . . . (1) 438788300
EBV Elektronik . . . . . (44) 1 628 783688
Farnell . . . . . (44) 1 132 636311
Future Electronics Ltd. . . . . (44) 1 753 763000
Macro Group . . . . . (44) 1 628 606000
Newark . . . . . (44) 1 420 543333

Venezuela

Baron Electronics 1–305–685–140

Device Index and Subject Index

In Brief . . .

Device Index

The following index lists the device numbers of the products contained in this selector guide and references the page number where each device is described in greater detail.(1) The listing is in a numeric sequence organized in a "computer sort." This means that all the devices listed herein follow a 39 character alphabet. This "new" alphabet starts with a Period, a Dash and a Slash (. – /), followed by the 26 letter alphabet (A thru Z), which is then followed by 10 numbers (0 thru 9).

The ranking or hierarchy of this 39 character alphabet is as follows:

. – / A B C D E F G H I J K L M N O P Q R S T U V W X Y Z 0 1 2 3 4 5 6 7 8 9

Therefore, if you are looking for a device starting with a letter of the alphabet like an MC3419, it would appear before a device starting with a number, such as 68HC12.

To find a device in this index, start with the first character of the device and find that section of the index; next move to the second character in the device number, and move to that character within the same portion of the listing; and so on until the device number is found. In other words, it is used just like a dictionary, character by character.

For example, to find the MC3419, go to that section of the listing that begins with the letter "M". Next, find that portion of the listing that begins with "MC" (Notice it follows those devices that begin with "MB"). Next, find that portion of the listing that begins with "MC3" (Notice it follows those devices that begin with "MC2"). Continue looking for those portions that begin with the next consecutive character until you have found the entire number.

Because of the way "Computer Sort" works it is not necessary to be concerned with the absolute value or number of characters in a part number, just move across the device part number, left to right, one character at a time until you find the number.

Subject Index

This listing is intended to simplify the identification of products where specific device numbers are not known.

(1) The device numbers contained in this index are for reference only and do not necessarily represent the complete device number necessary to order the device. Contact your local Sales Office or Authorized Distributor for complete ordering information.

8

8

Device Index

Device Index

Device Index

Device Index

Device Index

8

General Index

8

General Index

General Index

R (continued)

S

T

T (continued)

U

V

W

Z

Subject Index

8

Subject Index

M

M (continued)

P

R

S

Subject Index

S (continued)

T

8

MOTOROLA AUTHORIZED DISTRIBUTOR & WORLDWIDE SALES OFFICES

NORTH AMERICAN DISTRIBUTORS

UNITED STATES

ALABAMA

Huntsville
- Allied Electronics, Inc. ..... (256) 721–3500
- Arrow Electronics ..... (256) 864–3300
- FAI ..... (256) 837–9209
- Future Electronic ..... (256) 971–2010
- Hamilton/Hallmark ..... (256) 837–8700
- Newark ..... (256) 837–9091
- Wyle Electronics ..... (256) 830–1119

Mobile
- Allied Electronics, Inc. ..... (334) 476–1875

ARIZONA

Phoenix
- Allied Electronics, Inc. ..... (602) 831–2002
- FAI ..... (602) 731–4661
- Future Electronics ..... (602) 968–7140
- Hamilton/Hallmark ..... (602) 736–7000
- Wyle Electronics ..... (602) 804–7000

Tempe
- Arrow Electronics ..... (602) 966–6600
- Newark ..... (602) 966–6340
- Penstock ..... (602) 967–1620

ARKANSAS

Little Rock
- Newark ..... (501) 225–8130

CALIFORNIA

Agoura Hills
- Future Electronics ..... (818) 871–1740

Calabassas
- Arrow Electronics ..... (818) 880–9686
- Wyle Electronics ..... (818) 880–9000

Culver City
- Hamilton/Hallmark ..... (310) 558–2000

Irvine
- Arrow Electronics ..... (949) 587–0404
- Arrow Zeus ..... (949) 581–4622
- FAI ..... (949) 753–4778
- Future Electronics ..... (949) 453–1515
- Hamilton/Hallmark ..... (949) 789–4100
- Wyle Electronics Corporate ..... (949) 753–9953
- Wyle Electronics ..... (949) 789–9953

Los Angeles
- FAI ..... (818) 879–1234
- Wyle Electronics ..... (818) 880–9000

Manhattan Beach
- Penstock ..... (310) 546–8953

Orange County
- Allied Electronics, Inc. ..... (949) 727–3010

Palo Alto
- Newark ..... (650) 812–6300

Riverside
- Allied Electronics, Inc. ..... (909) 980–6522
- Newark ..... (909) 980–2105

Rocklin
- Hamilton/Hallmark ..... (916) 632–4500

Roseville
- Wyle Electronics ..... (916) 783–9953

Sacramento
- Allied Electronics, Inc. ..... (916) 632–3104
- FAI ..... (916) 782–7882
- Newark ..... (916) 565–1760
- Wyle Electronics ..... (916) 638–5282

San Diego
- Allied Electronics, Inc. ..... (619) 279–2550
- Arrow Electronics ..... (619) 565–4800
- Arrow Zeus ..... (619) 565–4800
- FAI ..... (619) 623–2888
- Future Electronics ..... (619) 625–2800

San Diego– Continued
- Hamilton/Hallmark ..... (619) 571–7540
- Penstock ..... (619) 623–9100
- Newark ..... (619) 453–8211
- Wyle Electronics ..... (619) 558–6600

San Fernando Valley
- Allied Electronics, Inc. ..... (818) 598–0130

San Jose
- Allied Electronics, Inc. ..... (408) 383–0366
- Arrow Electronics ..... (408) 441–9700
- Arrow Zeus ..... (408) 629–4789
- Arrow Electronics ..... (408) 428–6400
- FAI ..... (408) 434–0369
- Future Electronics ..... (408) 434–1122

Santa Clara
- Wyle Electronics ..... (408) 727–2500

Santa Fe Springs
- Newark ..... (650) 929–9722

Sierra Madre
- Penstock ..... (818) 355–6775

Sunnyvale
- Hamilton/Hallmark ..... (408) 435–3600
- Penstock ..... (408) 730–0300

Thousand Oaks
- Newark ..... (805) 449–1480

Woodland Hills
- Hamilton/Hallmark ..... (818) 594–0404

COLORADO

Lakewood
- FAI ..... (303) 237–1400
- Future Electronics ..... (303) 232–2008

Denver
- Allied Electronics, Inc. ..... (303) 790–1664
- Newark ..... (303) 373–4540

Englewood
- Arrow Electronics ..... (303) 799–0258
- Hamilton/Hallmark ..... (303) 790–1662
- Penstock ..... (303) 799–7845

Thornton
- Wyle Electronics ..... (303) 457–9953

CONNECTICUT

Bloomfield
- Newark ..... (860) 243–1731

Cheshire
- Allied Electronics, Inc. ..... (203) 272–7730
- FAI ..... (203) 250–1319
- Future Electronics ..... (203) 250–0083
- Hamilton/Hallmark ..... (203) 271–5700

Wallingford
- Arrow Electronics ..... (203) 265–7741
- Wyle Electronics ..... (203) 269–8077

FLORIDA

Altamonte Springs
- Future Electronics ..... (407) 865–7900

Clearwater
- FAI ..... (813) 530–1665
- Future Electronics ..... (813) 530–1222

Deerfield Beach
- Arrow Electronics ..... (305) 429–8200
- Wyle Electronics ..... (954) 420–0500

Ft. Lauderdale
- FAI ..... (954) 428–9494
- Future Electronics ..... (954) 426–4043
- Hamilton/Hallmark ..... (954) 677–3500
- Newark ..... (954) 486–1151

Jacksonville
- Allied Electronics, Inc. ..... (904) 739–5920
- Newark ..... (904) 399–5041

FLORIDA – continued

Lake Mary
- Arrow Electronics ..... (407) 333–9300
- Arrow Zeus ..... (407) 333–3055

Largo/Tampa/St. Petersburg
- Hamilton/Hallmark ..... (813) 507–5000
- Newark ..... (813) 287–1578
- Wyle Electronics ..... (813) 576–3004

Maitland
- Wyle Electronics ..... (407) 740–7450

Miami
- Allied Electronics, Inc. ..... (305) 558–2511

Orlando
- Allied Electronics, Inc. ..... (407) 539–0055
- FAI ..... (407) 865–9555
- Newark ..... (407) 896–8350

Tallahassee
- FAI ..... (904) 668–7772

Tampa
- Allied Electronics, Inc. ..... (813) 579–4660
- Newark ..... (813) 287–1578
- Penstock ..... (813) 247–7556

Plantation
- Newark ..... (305) 424–4400

Winter Park
- Hamilton/Hallmark ..... (407) 657–3300
- Penstock ..... (407) 672–1114

GEORGIA

Atlanta
- Allied Electronics, Inc. ..... (770) 497–9544
- FAI ..... (404) 447–4767

Duluth
- Arrow Electronics ..... (404) 497–1300
- Hamilton/Hallmark ..... (770) 623–4400

Norcross
- Future Electronics ..... (404) 441–7676
- Newark ..... (404) 448–1300
- Wyle Electronics ..... (770) 441–9045
- Penstock ..... (770) 734–9990

IDAHO

Boise
- Allied Electronics, Inc. ..... (208) 331–1414
- FAI ..... (208) 376–8080

ILLINOIS

Addison
- Wyle Electronics ..... (630) 620–0969

Arlington Heights
- Hamilton/Hallmark ..... (847) 797–7300
- Allied Electronics, Inc. (North) ... (847) 548–9330
- Allied Electronics, Inc. (South) ... (708) 843–0034
- FAI ..... (708) 843–0034
- Newark Electronics Corp. .. (773) 784–5100

Hoffman Estates
- Future Electronics ..... (708) 882–1255

Itasca
- Arrow Electronics ..... (708) 250–0500
- Arrow Zeus ..... (630) 595–9730

Lombard
- Newark ..... (630) 317–1000

Palatine
- Penstock ..... (708) 934–3700

Rockford
- Allied Electronics, Inc. ..... (815) 636–1010
- Newark ..... (815) 229–0225

Springfield
- Newark ..... (217) 787–9972

Wood Dale
- Allied Electronics, Inc. ..... (630) 860–0007

AUTHORIZED DISTRIBUTORS – continued

UNITED STATES – continued

INDIANA
Indianapolis
- Allied Electronics, Inc. ..... (317) 571–1880
- Arrow Electronics ..... (317) 299–2071
- FAI ..... (317) 469–0441
- Future Electronics ..... (317) 469–0447
- Hamilton/Hallmark ..... (317) 575–3500
- Newark ..... (317) 844–0047
- Wyle Electronics ..... (317) 581–6152

Ft. Wayne
- Newark ..... (219) 484–0766
- Penstock ..... (219) 432–1277

IOWA
Bettendorf
- Newark ..... (319) 359–3711

Cedar Rapids
- Allied Electronics, Inc. ..... (319) 390–5730
- Newark ..... (319) 393–3800

KANSAS
Kansas City
- Allied Electronics, Inc. ..... (913) 541–9542
- FAI ..... (913) 381–6800

Lenexa
- Arrow Electronics ..... (913) 541–9542

Olathe
- Penstock ..... (913) 829–9330

Overland Park
- Future Electronics ..... (913) 649–1531
- Hamilton/Hallmark ..... (913) 663–7900
- Newark ..... (913) 677–0727

KENTUCKY
Louisville
- Allied Electronics, Inc. ..... (502) 452–2293
- Newark ..... (502) 423–0280

LOUISIANA
New Orleans
- Allied Electronics, Inc. ..... (504) 466–7575
- Newark ..... (504) 838–9771

MASSACHUSETTS
Bedford
- Wyle Electronics ..... (781) 271–9953

Boston
- Allied Electronics, Inc. ..... (617) 255–0361
- Arrow Electronics ..... (508) 658–0900
- FAI ..... (508) 779–3111
- Newark 1–800–4NEWARK

Bolton
- Future Corporate ..... (978) 779–3000

Burlington
- Penstock ..... (617) 229–9100

Lowell
- Newark ..... (978) 551–4300

Peabody
- Allied Electronics, Inc. ..... (508) 538–2401
- Hamilton/Hallmark ..... (508) 532–3701

Wilmington
- Arrow Zeus ..... (978) 658–4776

Worchester
- Newark ..... (508) 229–2200

MICHIGAN
Detroit
- Allied Electronics, Inc. ..... (313) 416–9300
- FAI ..... (313) 513–0015
- Newark ..... (313) 967–0600

Grand Rapids
- Future Electronics ..... (616) 698–6800
- Newark ..... (616) 954–6700

Livonia
- Arrow Electronics ..... (810) 455–0850
- Future Electronics ..... (313) 261–5270
- Hamilton/Hallmark ..... (313) 416–5800

MICHIGAN – continued
Novi
- Wyle Electronics ..... (248) 374–9953

Saginaw
- Newark ..... (517) 799–0480

Troy
- Newark ..... (248) 583–2899

MINNESOTA
Bloomington
- Wyle Electronics ..... (612) 853–2280

Burnsville
- Penstock ..... (612) 882–7630

Eden Prairie
- Arrow Electronics ..... (612) 941–5280
- FAI ..... (612) 947–0909
- Future Electronics ..... (612) 944–2200
- Hamilton/Hallmark ..... (612) 881–2600

Minneapolis
- Allied Electronics, Inc. ..... (612) 938–5633
- Newark ..... (612) 331–6350
- Hamilton/Hallmark ..... (314) 291–5350

MISSISSIPPI
Jackson
- Newark ..... (601) 956–3834

MISSOURI
Earth City
- Hamilton/Hallmark ..... (314) 770–6300

St. Louis
- Allied Electronics, Inc. ..... (314) 240–9405
- Arrow Electronics ..... (314) 567–6888
- FAI ..... (314) 542–9922
- Future Electronics ..... (314) 469–6805
- Newark ..... (314) 991–0400

Novi
- Wyle Electronics ..... (248) 374–9953

NEBRASKA
Omaha
- Allied Electronics, Inc. ..... (402) 697–0038
- Newark ..... (402) 592–2423

NEVADA
Las Vegas
- Allied Electronics, Inc. ..... (702) 258–1087
- Wyle Electronics ..... (702) 765–7117

NEW JERSEY
Bridgewater
- Penstock ..... (908) 575–9490

East Brunswick
- Allied Electronics, Inc. ..... (908) 613–0828
- Newark ..... (732) 937–6600

Fairfield
- FAI ..... (201) 331–1133

Long Island
- FAI ..... (516) 348–3700

Marlton
- Arrow Electronics ..... (609) 596–8000
- FAI ..... (609) 988–1500
- Future Electronics ..... (609) 596–4080

Mt. Laurel
- Hamilton/Hallmark ..... (609) 222–6400
- Wyle Electronics ..... (609) 439–9020

Oradell
- Wyle Electronics ..... (201) 261–3200

Parsippany
- Future Electronics ..... (201) 299–0400
- Hamilton/Hallmark ..... (201) 515–1641

Pinebrook
- Wyle Electronics ..... (973) 882–8358

NEW MEXICO
Albuquerque
- Allied Electronics, Inc. ..... (505) 872–2770
- Hamilton/Hallmark ..... (505) 293–5119
- Newark ..... (505) 828–1878

NEW YORK
Albany
- Newark ..... (518) 489–1963

Buffalo
- Newark ..... (716) 631–2311

Great Neck
- Allied Electronics, Inc. ..... (516) 487–5211

Hauppauge
- Allied Electronics, Inc. ..... (516) 234–0485
- Arrow Electronics ..... (516) 231–1000
- FAI ..... (516) 348–3700
- Future Electronics ..... (516) 234–4000
- Hamilton/Hallmark ..... (516) 434–7400
- Newark ..... (516) 567–4200
- Penstock ..... (516) 724–9580
- Wyle ..... (516) 231–7850

Henrietta
- Wyle Electronics ..... (716) 334–5970

Konkoma
- Hamilton/Hallmark ..... (516) 737–0600

Poughkeepsie
- Allied Electronics, Inc. ..... (914) 452–1470
- Newark ..... (914) 298–2810

Purchase
- Arrow Zeus ..... (914) 701–7400

Rochester
- Allied Electronics, Inc. ..... (716) 292–1670
- Arrow Electronics ..... (716) 427–0300
- FAI ..... (716) 387–9600
- Future Electronics ..... (716) 387–9600
- Hamilton/Hallmark ..... (716) 272–2740
- Newark ..... (716) 381–4244

Syracuse
- Allied Electronics, Inc. ..... (315) 446–7411
- FAI ..... (315) 451–4405
- Future Electronics ..... (315) 451–2371
- Newark ..... (315) 457–4873

NORTH CAROLINA
Charlotte
- Allied Electronics, Inc. ..... (704) 525–0300
- FAI ..... (704) 548–9503
- Future Electronics ..... (704) 547–1107
- Newark ..... (704) 535–5650

Greensboro
- Newark ..... (910) 294–2142

Morrisville
- Wyle Electronics ..... (919) 469–1502

Raleigh
- Allied Electronics, Inc. ..... (919) 876–5845
- Arrow Electronics ..... (919) 876–3132
- FAI ..... (919) 876–0088
- Future Electronics ..... (919) 790–7111
- Hamilton/Hallmark ..... (919) 872–0712

OHIO
Centerville
- Arrow Electronics ..... (513) 435–5563

Cincinnati
- Allied Electronics, Inc. ..... (513) 771–6990
- Newark ..... (513) 942–8700

Cleveland
- Allied Electronics, Inc. ..... (216) 831–4900
- FAI ..... (216) 446–0061
- Newark ..... (216) 391–9330

Columbus
- Allied Electronics, Inc. ..... (614) 785–1270
- Newark ..... (614) 326–0352

Dayton
- FAI ..... (513) 427–6090
- Future Electronics ..... (513) 426–0090
- Hamilton/Hallmark ..... (513) 439–6735
- Newark ..... (937) 294–8980

Mayfield Heights
- Future Electronics ..... (216) 449–6996

AUTHORIZED DISTRIBUTORS – continued

UNITED STATES – continued

OHIO – continued

Miamisburg
Wyle Electronics ..... (937) 436–9953

Solon
Arrow Electronics ..... (216) 248–3990
Hamilton/Hallmark ..... (216) 498–1100
Wyle Electronics ..... (440) 248–9996

Toledo
Newark ..... (419) 866–0404

Worthington
Hamilton/Hallmark ..... (614) 888–3313

OKLAHOMA

Oklahoma City
Newark ..... (405) 943–3700

Tulsa
Allied Electronics, Inc. ..... (918) 250–4505
FAI ..... (918) 492–1500
Hamilton/Hallmark ..... (918) 459–6000

OREGON

Beaverton
Arrow Electronics Corp. .... (503) 629–8090
Hamilton/Hallmark ..... (503) 526–6200
Wyle Electronics ..... (503) 598–9953

Portland
FAI ..... (503) 603–0866
Future Electronics ..... (503) 603–0956
Newark ..... (503) 297–1984
Penstock ..... (503) 646–1670

PENNSYLVANIA

Allentown
Newark ..... (610) 434–7171

Chadds Ford
Allied Electronics, Inc. ..... (610) 388–8455

Coatesville
Penstock ..... (610) 383–9536

Ft. Washington
Newark ..... (215) 654–1434

Harrisburg
Allied Electronics, Inc. ..... (717) 540–7101

Philadelphia
Allied Electronics, Inc. ..... (609) 234–7769

Pittsburgh
Allied Electronics, Inc. ..... (412) 931–2774
Arrow Electronics ..... (412) 963–6807
Newark ..... (503) 297–1984

SOUTH CAROLINA

Greenville
Allied Electronics, Inc. ..... (864) 288–8835
Allied Electronics, Inc. ..... (864) 288–9610

TENNESSEE

Knoxville
Newark ..... (423) 588–6493

Memphis
Newark ..... (901) 396–7970

TEXAS

Austin
Allied Electronics, Inc. ..... (512) 219–7171
Arrow Electronics ..... (512) 835–4180
FAI ..... (512) 346–6426
Future Electronics ..... (512) 502–0991
Hamilton/Hallmark ..... (512) 219–3700
Newark ..... (512) 338–0287
Penstock ..... (512) 346–9762
Wyle Electronics ..... (512) 833–9953

Benbrook
Penstock ..... (817) 249–0442

Brownsville
Allied Electronics, Inc. ..... (210) 548–1129

Carrollton
Arrow Electronics ..... (972) 380–6464
Arrow Zeus ..... (972) 380–4330

TEXAS – continued

Dallas
Allied Electronics, Inc. ..... (214) 341–8444
FAI ..... (972) 231–7195
Future Electronics ..... (972) 437–2437
Hamilton/Hallmark ..... (214) 553–4300
Newark ..... (972) 458–2528

El Paso
Allied Electronics, Inc. ..... (915) 779–6294
FAI ..... (915) 577–9531
Newark ..... (915) 772–6367

Ft. Worth
Allied Electronics, Inc. ..... (817) 595–3500

Houston
Allied Electronics, Inc. ..... (281) 446–8005
Arrow Electronics ..... (281) 647–6868
FAI ..... (713) 952–7088
Future Electronics ..... (713) 785–1155
Hamilton/Hallmark ..... (713) 781–6100
Newark ..... (281) 894–9334
Wyle Electronics ..... (713) 784–9953

Richardson
Penstock ..... (972) 479–9215
Wyle Electronics ..... (972) 235–9953

San Antonio
FAI ..... (210) 738–3330

UTAH

Draper
Wyle Electronics ..... (801) 523–2335

Salt Lake City
Allied Electronics, Inc. ..... (801) 261–5244
Arrow Electronics ..... (801) 973–6913
FAI ..... (801) 467–9696
Future Electronics ..... (801) 467–4448
Hamilton/Hallmark ..... (801) 266–2022
Newark ..... (801) 261–5660
Wyle Electronics ..... (801) 974–9953

West Valley City
Wyle Electronics ..... (801) 974–9953

VIRGINIA

Herndon
Newark ..... (703) 707–9010

Richmond
Newark ..... (804) 282–5671

Springfield
Allied Electronics, Inc. ..... (703) 644–9515

Virginia Beach
Allied Electronics, Inc. ..... (757) 363–8662

WASHINGTON

Bellevue
Almac Electronics Group ... (206) 643–9992
Penstock ..... (206) 454–2371

Bothell
Future Electronics ..... (206) 489–3400

Kirkland
Newark ..... (425) 814–6230

Redmond
Hamilton/Hallmark ..... (206) 882–7000
Wyle Electronics ..... (425) 881–1150

Seattle
Allied Electronics, Inc. ..... (206) 251–0240
FAI ..... (206) 485–6616

Spokane
Newark ..... (509) 327–1935

WISCONSIN

Brookfield
Arrow Electronics ..... (414) 792–0150
Future Electronics ..... (414) 879–0244
Wyle Electronics ..... (414) 879–0434

Madison
Newark ..... (608) 278–0177

WISCONSIN – continued

Milwaukee
Allied Electronics, Inc. ..... (414) 796–1280
FAI ..... (414) 792–9778

New Berlin
Hamilton/Hallmark ..... (414) 780–7200

Wauwatosa
Newark ..... (414) 453–9100

CANADA

ALBERTA

Future Active Calgary
(Bus. Accts.) 403–219–3443
Active Components Calgary
(Retail Sales) 403–291–5626
Future Active Edmonton
(Bus. Accts.) 780–438–5888
Active Components Edmonton
(Retail Sales) 780–438–0644
Avnet for Western Canada
(OEM Contract, Repair,
Retail Sales) 1–800–332–8638
Avnet for Western Canada
(Disty & Bus. Sales) 1–800–672–8638

BRITISH COLUMBIA

Vancouver
Allied Electronics, Inc. ..... (604) 420–9691
Arrow Electronics ..... (604) 421–2333
FAI ..... (604) 654–1050
Future Electronics ..... (604) 294–1166
Hamilton/Avnet Electronics ..... (604) 420–4101
Newark ..... (800) 463–9275

MANITOBA

Winnipeg
FAI ..... (209) 786–3075
Future Electronics ..... (204) 944–1446
Hamilton/Hallmark ..... (800) 663–5500
Newark ..... (800) 463–9275

ONTARIO

Kanata
Penstock ..... (613) 592–6088

London
Newark ..... (519) 685–4280

Mississauga
Penstock ..... (905) 403–0724
Newark ..... (905) 670–2888

Ottawa
Allied Electronics, Inc. ..... (613) 228–1964
Arrow Electronics ..... (613) 226–6903
FAI ..... (613) 820–8244
Future Electronics ..... (613) 727–1800
Hamilton/Hallmark ..... (613) 226–1700

Toronto
Arrow Electronics ..... (905) 670–7769
FAI ..... (905) 612–9888
Future Electronics ..... (905) 612–9200
Hamilton/Hallmark ..... (905) 564–6060
Newark ..... (905) 670–2888

QUEBEC

Montreal
Arrow Electronics ..... (514) 421–7411
FAI ..... (514) 694–8157
Future Electronics ..... (514) 694–7710
Hamilton/Hallmark ..... (514) 335–1000

Mt. Royal
Newark ..... (514) 738–4488

Quebec City
Arrow Electronics ..... (418) 687–4231
FAI ..... (418) 877–1414
Future Electronics ..... (418) 877–6666

INTERNATIONAL DISTRIBUTORS

ARGENTINA
Electrocomponentes 54–11–4375–3366
Elko 54–11–4372–1101

AUSTRALIA
Valtek Australia Pty. Ltd ..... (61–3) 9574–9300
Avnet Pacific Pty. Ltd .... 132 732 (nationwide)
Future Electronics ..... (61–3) 9899–7944
Farnell ..... (61) 2 9644–7722

AUSTRIA
EBV Elektronik ..... (43) 189152–0
Farnell ..... (49) 8961 393939
SEI/Elbatex GmbH ..... (43) 1 866420
Spoerle Electronic ..... (43) 1 360460

BELGIUM
EBV Elektronik ..... (32) 2 716 0010
Farnell ..... (31) 30 241 7333
Future Electronics ..... (32) 3 780 3001
SEI Belgium ..... (32) 2 460 0747
Spoerle Electronic ..... (32) 2 725 4660

BRAZIL
Avnet 55–11–5079–2150
Baron Electronics: 1–305–685–1400
Farnell 55–11–4066–9400
Future 55–19–235–1511
Intertek 55–11–266–2922
Karimex 55–11–5189–1900
Masktrade 55–11–3361–2766
Panamericana 55–11–3661–6133
Siletec 55–11–536–4401
Tec 55–11–5505–2046
Teleradio 55–11–574–0788

BULGARIA
Macro Group ..... (359) 2708140

CHILE
Baron Electronics 1–305–685–1400

CHINA
Nanco Electronics Supply Ltd .. (852) 2333–5121
Avnet WKK Components Ltd. .... (852) 2357–8888
China Eltronic Appliance Corp.
..... (86–10) 6823–9951
Qing Cheng Enterprises Ltd .... (852) 2493–4202
Future Electronics ..... (021) 6213–6801
Future Electronics ..... (852) 2305–3633
Arrow Electronics China Ltd .... (852) 2484–2113
MARUBUN/ARROW (HK) Ltd. ... (852) 2375–1126

COLUMBIA
Baron Electronics 1–305–685–1400

COSTA RICA
Baron Electronics 1–305–685–1400

CZECH REPUBLIC
EBV Elektronik ..... (420) 2 90022101
Spoerle Electronic ..... (420) 2 71737173
SEI/Elbatex ..... (420) 2 4763707
Macro Group ..... (420) 2 3412182

DENMARK
Arrow Denmark A/S ..... (45) 44 508200
A/S Avnet EMG ..... (45) 44 880800
EBV Elektronik – Abyhoj .... (45) 86250466
EBV Elektronik – Aabyhoej .. (45) 86250660
Farnell ..... (45) 44 536644
Future Electronics ..... (45) 961 00 961

ESTONIA
Arrow Field Eesti ..... (372) 6503288
Avnet Baltronic ..... (372) 6397000
Farnell ..... (358) 9345 5400

FINLAND
Arrow Finland ..... (358) 9 476660
Avnet Nortek ..... (358) 9 613181
EBV Elektronik ..... (358) 9 27052790
Farnell ..... (358) 9345 5400
Future Electronics ..... (358) 9 3455400

FRANCE
Arrow Electronique ..... (33) 1 49 78 49 78
Avnet ..... (33) 1 49 65 27 00
EBV Elektronik ..... (33) 1 40963000
Farnell ..... (33) 474 659466
Future Electronics ..... (33) 1 69821111
Sonepar Electronique .... (33) 1 69 19 89 00

GERMANY
Avnet EMG ..... (49) 89 4511001
EBV Elektronik GmbH .... (49) 89 99114–0
Farnell ..... (49) 89 61 303103
Future Electronics GmbH ..... (49) 89–957 270
SEI/Jermyn GmbH ..... (49) 6431–5080
Spoerle Electronic ..... (49) 6103–304–0

GREECE
EBV Elektronik ..... (30) 13414300

HONG KONG
Arrow Asia Pac Ltd ..... (852) 2484–2484
Arrow/Components Agent Ltd .. (852) 2484–2112
EEC International (HK) Limited.
..... (852) 2365–7775 ext. 512
MARUBUN/ARROW (HK) Ltd. .. (852) 2375–1126
Nanco Electronics Supply Ltd
..... (852) 2333–5121
Avnet WKK Components Ltd. .... (852) 2357–8888
Future Electronics ..... (852) 2420–6238
Arrow/Texny (HK) Ltd. .... (852) 2765–0118
Qing Cheng Enterprises Ltd. ... (852) 2493–4202

HUNGARY
Spoerle Electronics ..... (36) 11409194
..... (36) 11294202
Future Electronics ..... (36) 11409194
..... (36) 1 224 0510
Macro Group ..... (36) 11409194
..... (36) 12030277
SEI/Elbatex ..... (36) 11409194

INDIA
Future Electronics ..... (91–80) 5593106
Max India Ltd ..... (91–11) 6250250
Arrow Electronics (India) Ltd. ... (91) 80 5546125

INDONESIA
PT. Ometraco ..... (6221) 619–6166

IRELAND
Arrow Electronics ..... (353) 14595540
EBV Elektronik ..... (353) 14564034
Farnell ..... (353) 18309277
Future Electronics ..... (353) 6541330
Macro Group ..... (353) 16766904

ITALY
Avnet EMG ..... (39) 02 381901
EBV Elektronik Italy ..... (39) 02 66096290
Farnell ..... (44) 113 231 1311
Future Electronics ..... (39) 02 660941
Silverstar Ltd ..... (39) 02 66 12 51

JAPAN
AMSC Co., Ltd 81–422–54–6800
Fuji Electronics Co., Ltd 81–3–3814–1415
Marubun Corporation 81–3–3639–8951
Tokyo Electron Device Ltd. ... 81–45–474–7036

KOREA
Arrow Electronics Korea Ltd. ... (82–2) 650–6400
Future Electronics ..... (82–2) 555–6736
Segyung Electronics ..... (82–2) 514–5614
Nasco Co. Ltd ..... (82–2) 868–4988
Liteon Korea Ltd ..... (82–2) 650–9700
Jung Kwang Semiconductors Ltd
..... (82–2) 2278–5333

LATVIA
Avnet Baltronic Ltd ..... (371) 8821118
Macro Group ..... (371) 7313195

LITHUANIA
Macro Group ..... (370) 7–764937

MALAYSIA
Ultro Technologies Pte. Ltd
..... (65) 545–7811 / 540–8328
Arrow Strong Electronics (M) Sdn Bhd
..... (604) 646–4768
Arrow Components (M) Sdn Bhd
..... (604) 229–6613
Future Electronics ..... (60–4) 2277213

MEXICO
Avnet ..... (3) 632–0182
Dicopel ..... (5) 705–7422
Future ..... (3) 122–0043
Semiconductores Profesionales .... (5) 658–6011
Steren ..... (5) 325–0925

NETHERLANDS
Holland
EBV Elektronik ..... (31) 3465 83010
Farnell ..... (31) 30 241 7333
Future Electronics ..... (31) 76 544 4888
SEI/Benelux B.V. ..... (31) 7657 22500
Spoerle Electronics – Nieuwegen
..... (31) 306391234
Spoerle Electronics – Veldhoven
..... (31) 402545430

NEW ZEALAND
Avnet Pacific Ltd ..... (64–9) 636–7801
Arrow Components (NZ) Ltd .... (64) 4570–2260
Future Electronics ..... (64) 3348–0256
Farnell ..... (612) 9 644–7722

NORWAY
Arrow Tahonic A/S ..... (47) 2237 8440
A/S Avnet EMG ..... (47) 6677 3600
EBV Elektronik ..... (47) 2267 1780
Future Electronics ..... (47) 2290 5800

PHILIPPINES
Ultro Technologies Pte. Ltd
..... (65) 545–7811 / 540–8328
Future Electronics
..... (632–807) 5092 / 3512 / 3524

POLAND
EBV Elektronik ..... (48) 713422944
Future Electronics ..... (48) 22 61 89202
Macro Group ..... (48) 22 224337
SEI/Elbatex ..... (48) 22 6217122
Spoerle Electronic ..... (48) 22 6465227

PORTUGAL
Amitron Arrow ..... (35) 114714182
Farnell ..... (34) 90120 2080
SEI–Selco ..... (351) 2–973–82–03

ROMANIA
Macro Group ..... (401) 6343129

RUSSIA
St. Petersburg
Macro Group ..... (781) 25311476

Moscow
Macro Group – Moscow ..... (7) 095 30600266
EBV Elektronik ..... (7) 095 976 11 76

SCOTLAND
EBV Elektronik ..... (44) 1414202070
Future ..... (44) 1 419413999

SINGAPORE
Avnet Cinergi Pte Ltd. ..... (65) 481–6776
MARUBUN/ARROW Electronics (S) Pte. Ltd.
..... (65) 536–0050
Future Electronics Ltd ..... (65) 479–1300
Ultro Technologies Pte. Ltd
..... (65) 545–7811 / 540–8328
Arrow Strong Electronics (S) Pte. Ltd
..... (65) 276–3996
Arrow Electronics (S) Pte Ltd. ..... (65) 8458388
Farnell ..... (66) 788–3922

For changes to this information contact Technical Publications at FAX (602) 244-6560

INTERNATIONAL DISTRIBUTORS – continued

SLOVAKIA
Macro Group . . . . . (42) 89634181
SEI/Elbatex . . . . . (42) 17295007

SLOVENIA
EBV Elektronik . . . . . (386) 611 330216
SEI/Elbatex . . . . . (386) 611 597198

SOUTH AFRICA
Avnet–ASD . . . . . (27) 11 4442333
Reutech Components . . . . (27) 11 3972992

SPAIN
Amitron Arrow . . . . . (34) 91 3043040
EBV Elektronik . . . . . (34) 91 8043256
Farnell . . . . . (44) 113 231 0447
SEI/Selco S.A. . . . . (34) 91 637 10 11

SWEDEN
Arrow–Th:s AB . . . . . (46) 8 56265500
Avnet EMG AB . . . . . (46) 8 629 14 00
EBV Elektronik . . . . . (46) 405 92100
Farnell . . . . . (46) 8 730–5000
Future Electronics . . . . . (46) 8 441 5470

SWITZERLAND
EBV Elektronik . . . . . (41) 1 7456161
Farnell . . . . . (41) 1204 6464
SEI/Elbatex AG . . . . . (41) 56 4375111
Spoerle Electronic . . . . . (41) 1 8746262

TAIWAN
Elitetron Electronic Co. Ltd . . (886–2) 2796–2400
Avnet–Mercuries Co. Ltd . . . . (886–2) 2516–7303
Solomon Technology Corp. . . (886–2) 2788–8989
Arrow/Ally Inc. . . . . (886–2) 2696–7388
Strong Electronics Co. Ltd . . . (886–2) 2917–9917
Future Electronics . . . . . (886–2) 2517–0900

THAILAND
Ultro Technologies Pte. Ltd
. . . . . (65) 545–7811 / 540–8328
Sahapiphat Ltd . . . (662) 237–9474 / 5 / 6 / 7
Future Electronics (Thailand) Ltd.
. . . . . (662) 361–8400–2
3Arrow Strong Electronics (S) Pte Ltd.
. . . . . (662) 567–5025–6

TURKEY
EBV Elektronik . . . . . (90) 216 4631352
Motorola Representative . . . . (90) 212 274 66 48

UNITED KINGDOM
Arrow Electronics (UK) Ltd . . . . (44) 1 234 270027
Avnet EMG 44 . . . . . (1) 438788300
EBV Elektronik . . . . . (44) 1 628 783688
Farnell . . . . . (44) 1 132 636311
Future Electronics Ltd. . . . (44) 1 753 763000
Macro Group . . . . . (44) 1 628 606000
Newark . . . . . (44) 1 420 543333

VENEZUELA
Baron Electronics 1–305–685–1400

MOTOROLA WORLDWIDE SALES OFFICES

UNITED STATES

ALABAMA
Huntsville . . . . . (256) 464–6800
ALASKA . . . . . (800) 635–8291
CALIFORNIA
Calabasas . . . . . (818) 878–6800
Irvine . . . . . (949) 753–7360
Los Angeles/El Segundo . . . (818) 878–6800
San Diego . . . . . (619) 541–2163
Sunnyvale . . . . . (408) 749–0510
COLORADO
Denver . . . . . (303) 337–3434
CONNECTICUT
Wallingford . . . . . (203) 949–4100
FLORIDA
Clearwater . . . . . (813) 524–4177
Maitland . . . . . (407) 628–2636
GEORGIA
Lawrenceville . . . . . (770) 338–3810
IDAHO
Boise . . . . . (208) 323–9413
ILLINOIS
Chicago/Schaumburg . . . . . (847) 413–2500
INDIANA
Indianapolis . . . . . (317) 571–0400
Kokomo . . . . . (765) 455–5100
MARYLAND
Columbia . . . . . (410) 381–1570
MASSACHUSETTS
Marlborough . . . . . (508) 357–8207
Woburn . . . . . (781) 932–9700
MICHIGAN
Detroit/Northville . . . . . (248) 347–6800
MINNESOTA
Minnetonka . . . . . (612) 932–1500
MISSOURI
St. Louis/Chesterfield . . . . . (314) 275–7380
NEW JERSEY
Fairfield . . . . . (973) 808–2400
NEW YORK
Fairport . . . . . (716) 425–4000
Fishkill . . . . . (914) 896–0511
Hauppauge . . . . . (516) 361–7000
NORTH CAROLINA
Raleigh . . . . . (919) 870–4355
OHIO
Cleveland/Solon . . . . . (440) 349–3100
Dayton/Miamisburg . . . . . (937) 438–6800
OREGON
Portland . . . . . (503) 641–3681
PENNSYLVANIA
Colmar . . . . . (215) 997–1020
Philadelphia/Horsham . . . . . (215) 957–4100
TENNESSEE
Knoxville . . . . . (423) 584–4841
TEXAS
Austin . . . . . (512) 502–2100
Houston . . . . . (281) 251–0006
Dallas/Plano . . . . . (972) 516–5100
WASHINGTON
Bellevue . . . . . (425) 454–4160
Seattle (toll free) . . . . . (206) 622–9960
WISCONSIN
Milwaukee/Brookfield . . . . . (414) 792–0122

Field Applications Engineering Available
Through All Sales Offices

CANADA

ALBERTA
Calgary . . . . . (403) 216–2190
BRITISH COLUMBIA
Vancouver . . . . . (604) 606–8502
ONTARIO
Ottawa . . . . . (613) 226–3491
Mississauga . . . . . (905) 501–3500
QUEBEC
Montreal . . . . . (514) 333–3300

INTERNATIONAL

AUSTRALIA
Melbourne . . . . . (61–3) 9765 2333
Sydney . . . . . (61–2) 9437 8944
BRAZIL
Sao Paulo . . . . . 55(011) 3030–5244
CHINA
Beijing 86–10–65642288
Guangzhou 86–20–87537888
Shanghai 86–21–63747668
Tianjin 86–22–25325050
CZECH REPUBLIC
. . . . . (420) 2 21852222
FINLAND
Helsinki . . . . . (358) 9 6866 880
Direct Sales Lines . . . . . (358) 9 6866 8844
. . . . . (358) 9 6866 8845
FRANCE
Paris 33134 635900
GERMANY
Langenhagen/Hanover . . . . 49(511) 786880
Munich 49 89 92103–0
Nuremberg 49 911 96–3190
Sindelfingen 49 7031 79 710
Wiesbaden 49 611 973050
HONG KONG
Kwai Fong 852–2–610–6888
Tai Po 852–2–666–8333
HUNGARY
. . . . . (36) 1 250 83 29
INDIA
Bangalore 91–80–5598615
ISRAEL
Herzlia 972–9–9522333
ITALY
Milan . . . . . 39(2) 82201
JAPAN
Kyushu 81–92–725–7583
Nagoya 81–52–232–3500
Osaka 81–6–305–1801
KOREA
Pusan . . . . . 82(51) 442–3964
Seoul 82–2–3440–7200
MALAYSIA
Penang . . . . . 60(4) 228–2514
MEXICO
Chihuahua . . . . . 52(14) 39–3120
Mexico City . . . . . 52(5) 282–0230
Guadalajara . . . . . 52(36) 78–0750
Zapopan Jalisco . . . . . 52(36) 78–0750
Marketing . . . . . 52(36) 21–2023
Customer Service . . . . . 52(36) 669–9160
NETHERLANDS
Best . . . . . (31) 4993 612 11
PHILIPPINES
Manila . . . . . (63) 2 807–8455
Paranaque . . . . . (63) 2 824–4551
Salcedo Village . . . . . (63) 2 810–0762
POLAND
. . . . . (48) 34 27 55 75
PUERTO RICO
Hato Rey . . . . . (787) 641–4100
RUSSIA
. . . . . (7) 095 929 90 25
SCOTLAND
East Kilbride 01355–355000
SINGAPORE . . . . . (65) 4818188
SPAIN
Madrid . . . . . 34(1) 457–8204
or . . . . . 34(1) 457–8254
SWEDEN
Solna . . . . . 46(8) 734–8800
SWITZERLAND
Geneva . . . . . 41(22) 799 11 11
Zurich . . . . . 41(1) 730–4074
TAIWAN
Taipei . . . . . 886(2) 27058000
THAILAND
Bangkok . . . . . 66(2) 254–4910
TURKEY
. . . . . (90) 212 274 66 48
UNITED KINGDOM
Aylesbury 44 1 (296) 395252

NORTH AMERICA

FULL LINE REPRESENTATIVES

ARIZONA, Tempe
S&S Technologies, Inc. . . . . (602) 414–1100
CALIFORNIA, Loomis
Galena Technology Group . . (916) 652–0268
INDIANA, Indianapolis
Bailey's Electronics . . . . . (317) 848–9958
NEVADA, Clark County
S&S Technologies, Inc. . . . . (602) 414–1100
NEVADA, Reno
Galena Tech. Group . . . . . (702) 746–0642
NEW MEXICO, Albuquerque
S&S Technologies, Inc. . . . . (602) 414–1100
TEXAS, El Paso
S&S Technologies, Inc. . . . . (915) 833–5461
UTAH, Salt Lake City
Utah Comp. Sales, Inc. . . . . (801) 572–4010
WASHINGTON, Spokane
Doug Kenley . . . . . (509) 924–2322

NORTH AMERICA

HYBRID/MCM COMPONENT SUPPLIERS

Chip Supply . . . . . (407) 298–7100
Elmo Semiconductor . . . . . (818) 768–7400
Minco Technology Labs Inc. . . . . (512) 834–2022
Semi Dice Inc. . . . . (310) 594–4631

NOTES

NOTES

Mfax is a trademark of Motorola, Inc.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3–20–1, Minami–Azabu. Minato–ku, Tokyo 106–8573 Japan. 81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Customer Focus Center: 1–800–521–6274
Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

HOME PAGE: http://motorola.com/sps/