

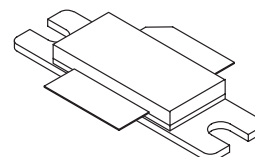
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications from frequencies up to 1.9 to 2.0 GHz. Suitable for CDMA, TDMA, GSM and multicarrier amplifier applications.

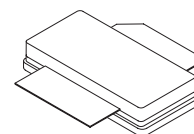
- Typical CDMA Performance: 1960 MHz, 26 Volts
IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
Output Power — 7.5 Watts
Power Gain — 12.5 dB
Adjacent Channel Power —
885 kHz: -47 dBc @ 30 kHz BW
1.25 MHz: -55 dBc @ 12.5 kHz BW
2.25 MHz: -55 dBc @ 1 MHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3 Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 60 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

MRF19060
MRF19060S

60 W, 1990 MHz, 26 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 465-04, STYLE 1
(MRF19060)



CASE 465A-04, STYLE 1
(MRF19060S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C \geq 25^\circ\text{C}$ Derate above 25°C	P_D	180 1.03	Watts W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

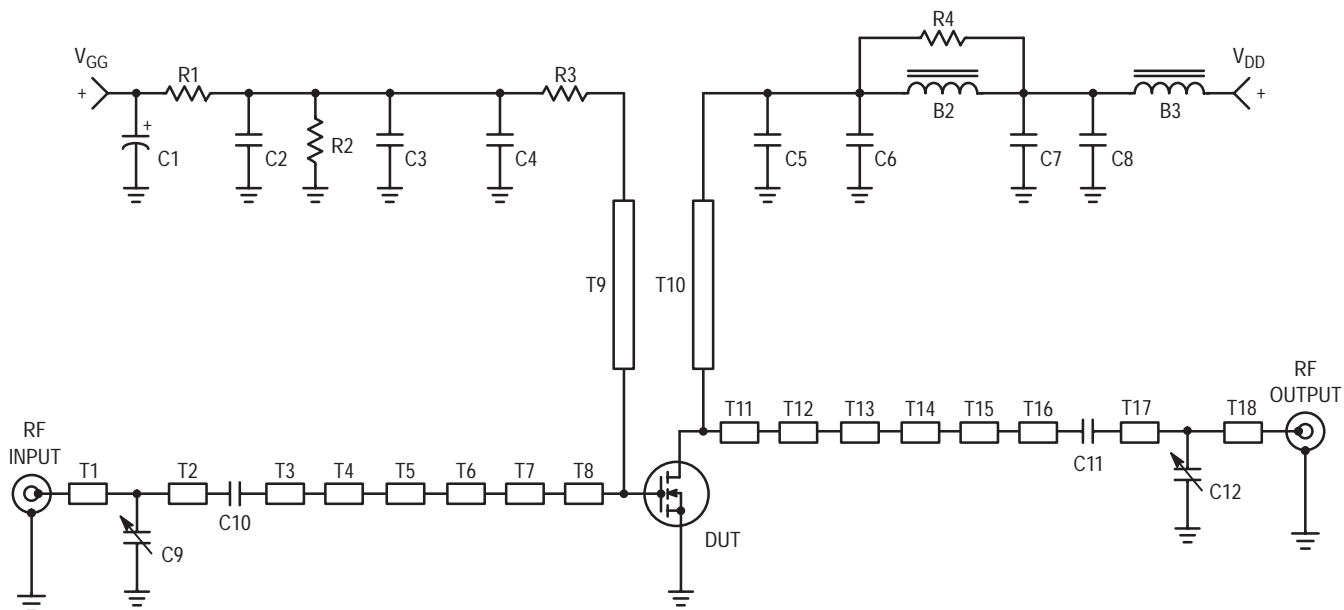
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.97	°C/W

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\ \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$)	I_{DSS}	—	—	6	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	g_{fs}	—	4.7	—	S
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$)	$V_{GS(th)}$	2	—	4	V
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 500\text{ mAdc}$)	$V_{GS(Q)}$	2.5	3.9	4.5	V
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2\text{ Adc}$)	$V_{DS(on)}$	—	0.27	—	V
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	2.7	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	G_{ps}	11	12.5	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	η	33	36	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IMD	—	–31	–28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W PEP}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$ and 1990 MHz , Tone Spacing = 100 kHz)	IRL	—	–12	—	dB
P_{out} , 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W CW}$, $f = 1990\text{ MHz}$)	P1dB	—	60	—	W
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 60\text{ W CW}$, $I_{DQ} = 500\text{ mA}$, $f = 1930\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B2 – B3	Ferrite Bead, Fair Rite, 2743019447	T4	0.152" x 0.140" Microstrip
C1	10 μ F, 50 V Electrolytic, ECEV1HV100R Panasonic	T5	0.090" x 0.102" Microstrip
C2, C7	1000 pF, B Case Chip Capacitor, 100B102JCA500X, ATC	T6	0.245" x 0.217" Microstrip
C3, C8	0.10 μ F, B Case Chip Capacitor, CDR33BX104AKWS, Kemet	T7	0.090" x 0.737" Microstrip
C4	5.1 pF, B Case Chip Capacitor, 100B5R1JCA500X, ATC	T8	0.530" x 0.941" Microstrip
C5	6.2 pF, B Case Chip Capacitor, 100B6R2JCA500X, ATC	T9	1.010" x 0.050" Microstrip
C6	22 μ F, 35 V Tantalum, SMT, Sprague	T10	1.060" x 0.050" Microstrip
C9	0.8 pF – 8.0 pF, Variable Capacitor, Johanson Gigatrim	T11	0.446" x 1.137" Microstrip
C10, C11	10 pF, B Case Chip Capacitor, 100B100JCA500X, ATC	T12	0.152" x 0.567" Microstrip
C12	0.4 pF – 2.5 pF, Variable Capacitor, Johanson Gigatrim	T13	0.183" x 0.220" Microstrip
R1	1 k Ω , 1/4 W, Fixed Film Chip Resistor, 0.08" x 0.13"	T14	0.100" x 0.338" Microstrip
R2	560 k Ω , 1/4 W, Fixed Film Chip Resistor, 0.08" x 0.13"	T15	0.480" x 0.142" Microstrip
R3	15 Ω , 1/4 W, Fixed Film Chip Resistor, 0.08" x 0.13"	T16	0.140" x 0.080" Microstrip
R4	10 Ω , 1/4 W, Fixed Film Chip Resistor, 0.08" x 0.13"	T17	0.173" x 0.080" Microstrip
T1	0.580" x 0.074" Microstrip	T18	0.420" x 0.080" Microstrip
T2	0.100" x 0.074" Microstrip	Board	0.030" Glass Teflon [®] Arlon
T3	0.384" x 0.074" Microstrip		GX-0300-55-22, 2 oz Cu

Figure 1. MRF19060 Schematic

TYPICAL CHARACTERISTICS

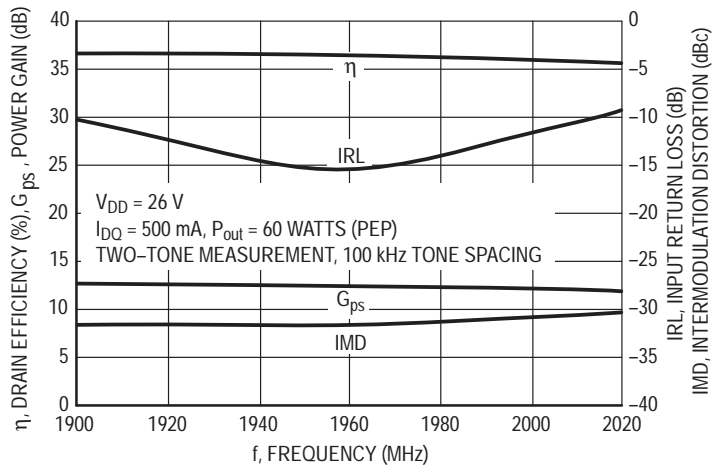


Figure 2. Class AB Broadband Circuit Performance

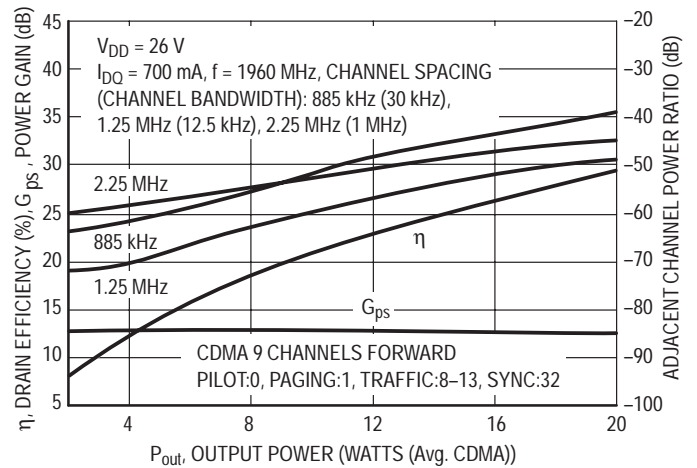


Figure 3. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

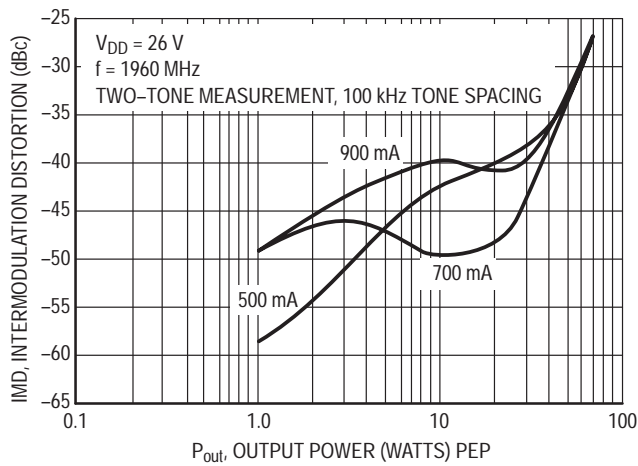


Figure 4. Intermodulation Distortion versus Output Power

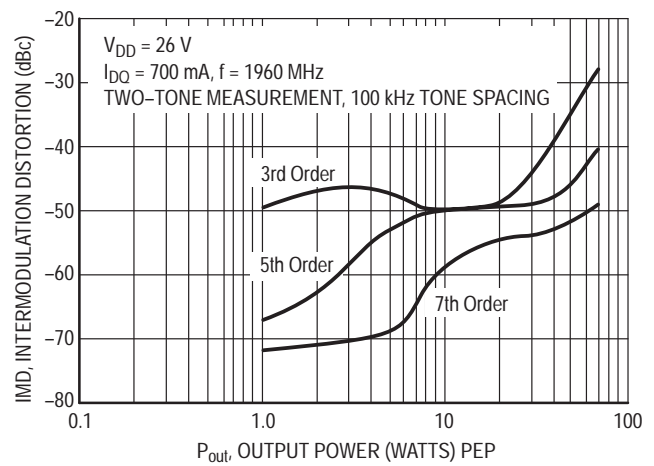


Figure 5. Intermodulation Products versus Output Power

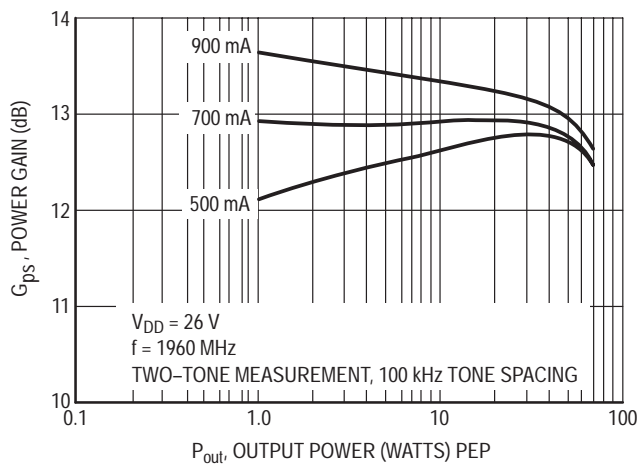


Figure 6. Power Gain versus Output Power

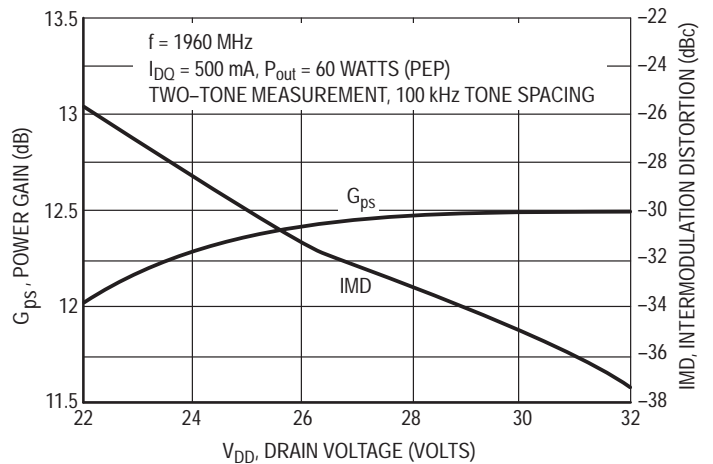
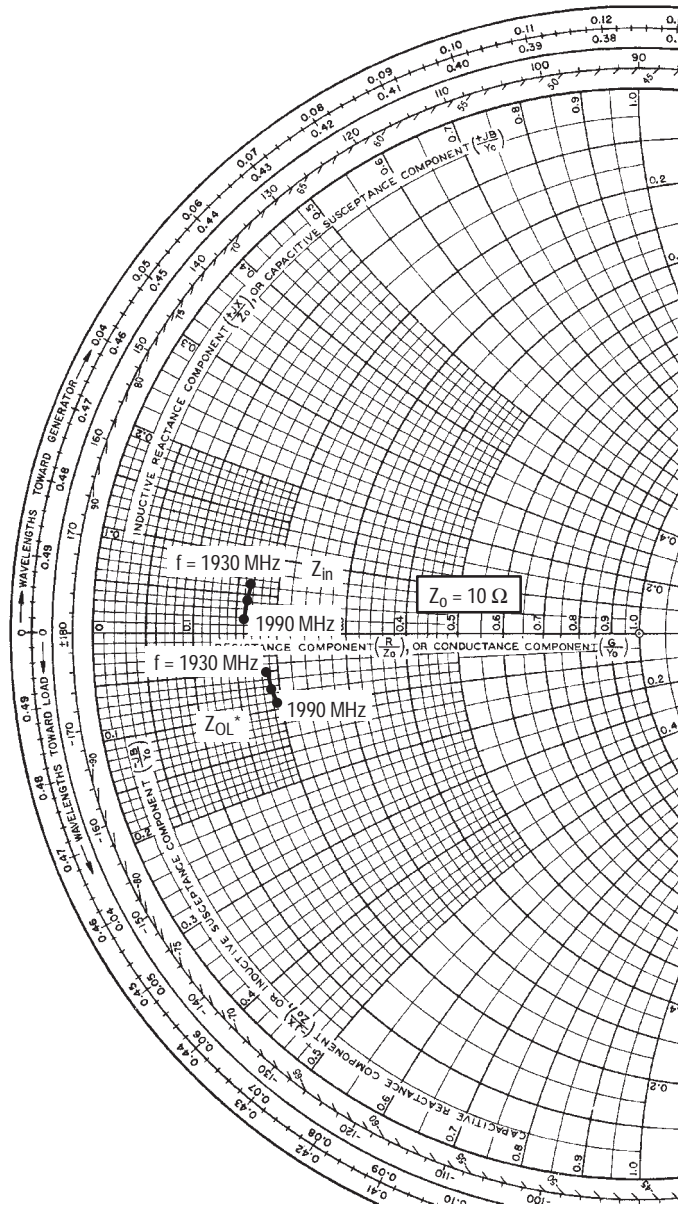


Figure 7. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 26\text{ V}$, $I_{DQ} = 500\text{ mA}$, $P_{out} = 60\text{ Watts (PEP)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1930	$1.65 + j0.67$	$1.85 - j0.50$
1960	$1.64 + j0.45$	$1.89 - j0.74$
1990	$1.60 + j0.20$	$1.96 - j0.94$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

Figure 8. Series Equivalent Input and Output Impedance

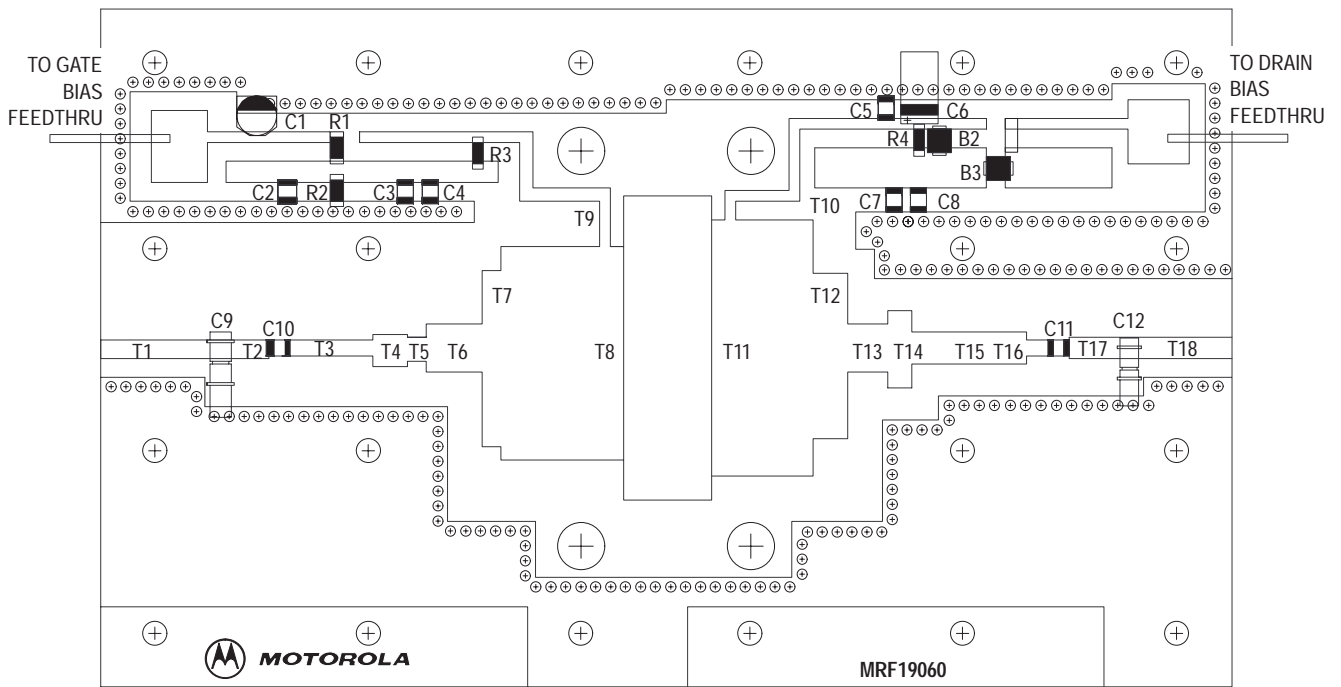
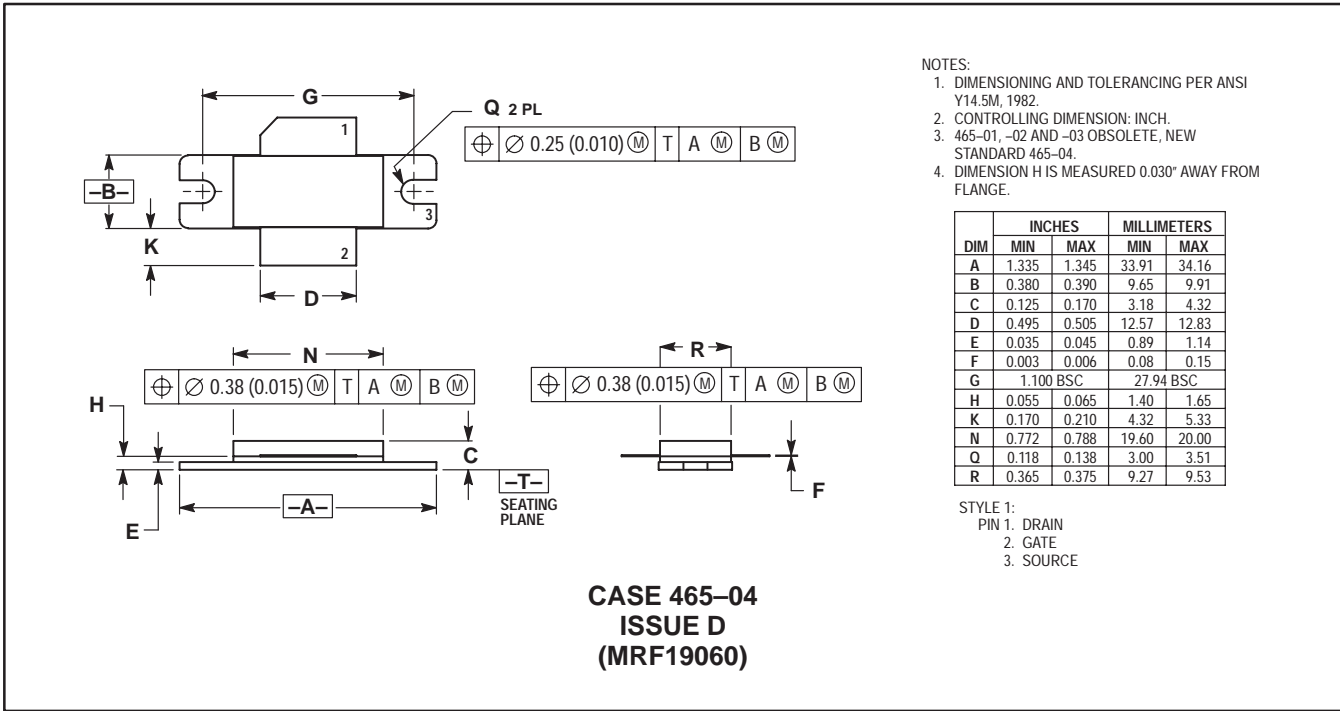


Figure 9. MRF19060 Populated PC Board Layout Diagram

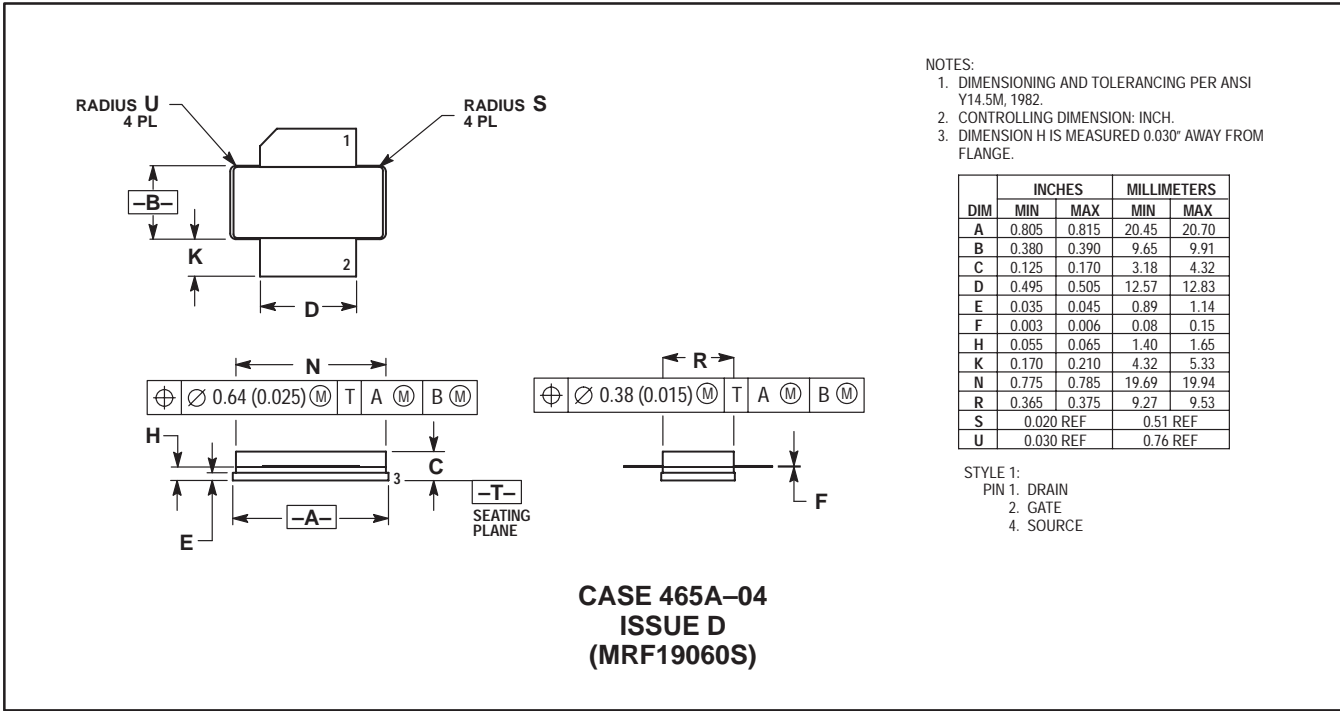
PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 465-01, -02 AND -03 OBSOLETE, NEW STANDARD 465-04.
 4. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.772	0.788	19.60	20.00
Q	0.118	0.138	3.00	3.51
R	0.365	0.375	9.27	9.53


- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.055	0.065	1.40	1.65
K	0.170	0.210	4.32	5.33
N	0.775	0.785	19.69	19.94
R	0.365	0.375	9.27	9.53
S	0.020 REF		0.51 REF	
U	0.030 REF		0.76 REF	

- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 4. SOURCE

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