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SEMICONDUCTOR TECHNICAL DATA

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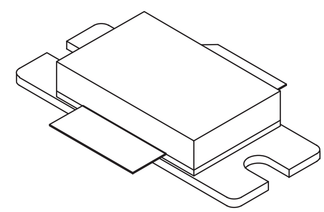
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18090B
MRF18090BS

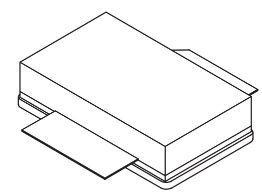
Designed for GSM and EDGE base station applications from frequencies up to 1.9 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
  Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
  Efficiency — 45% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection: Class 2 Human Body Model, Class M3 Machine Model
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters

90 W, 1.90 – 1.99 GHz, 26 V
LATERAL N–CHANNEL
BROADBAND
RF POWER MOSFETS



CASE 465B–02, STYLE 1



CASE 465C–01, STYLE 1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 1.43	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

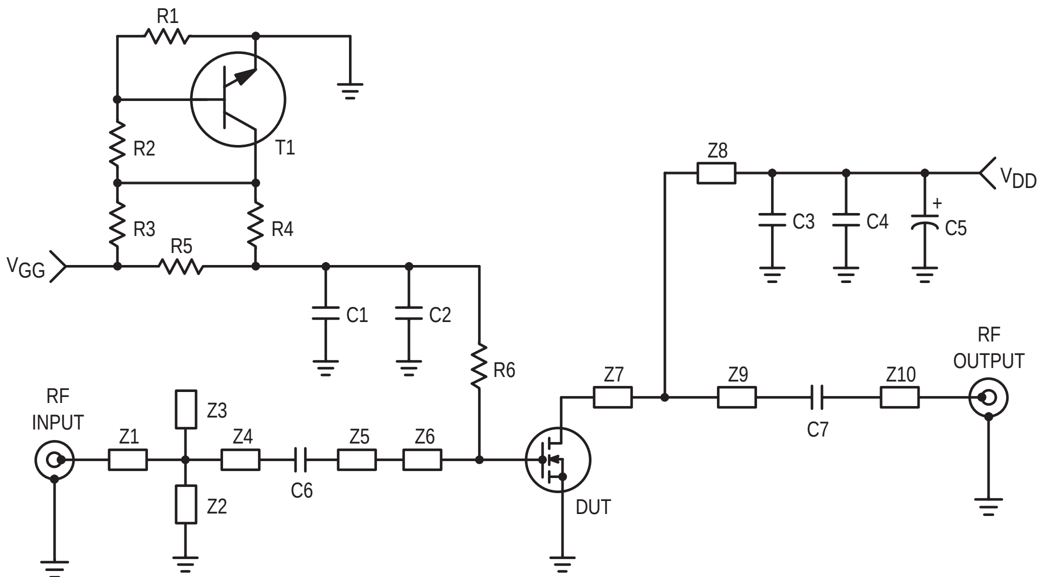
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3 Adc)	g_{fs}	—	7.2	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	4.2	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Common–Source Amplifier Power Gain @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	G_{ps}	12	13.5	—	dB
Drain Efficiency @ 90 W (1) (V_{DD} = 26 Vdc, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	η	40	45	—	%
Input Return Loss (1) (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA, f = 1930 – 1990 MHz)	IRL	10	—	—	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 90 W CW, I_{DQ} = 750 mA VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1900 band, ensuring batch–to–batch consistency.



C1	1.0 μF, Chip Capacitor 0805	R2, R3, R6	1.0 kΩ, Chip Resistor 0805
C2	1.0 nF, Chip Resistor 0805	R4	10 kΩ, Chip Resistor 0805
C3, C4	6.8 pF, 100B Chip Capacitor	R5	6.8 kΩ, Chip Resistor 0805
C5	220 μF, 50 V Electrolytic Capacitor	T1	BC847 SOT–23
C6, C7	12 pF, 100B Chip Capacitor	Z1 – Z10	Printed Microstrip Line
R1	2.2 kΩ, Chip Resistor 0805	PCB	Teflon® Glass

Figure 1. 1.93 – 1.99 MHz Test Fixture Schematic

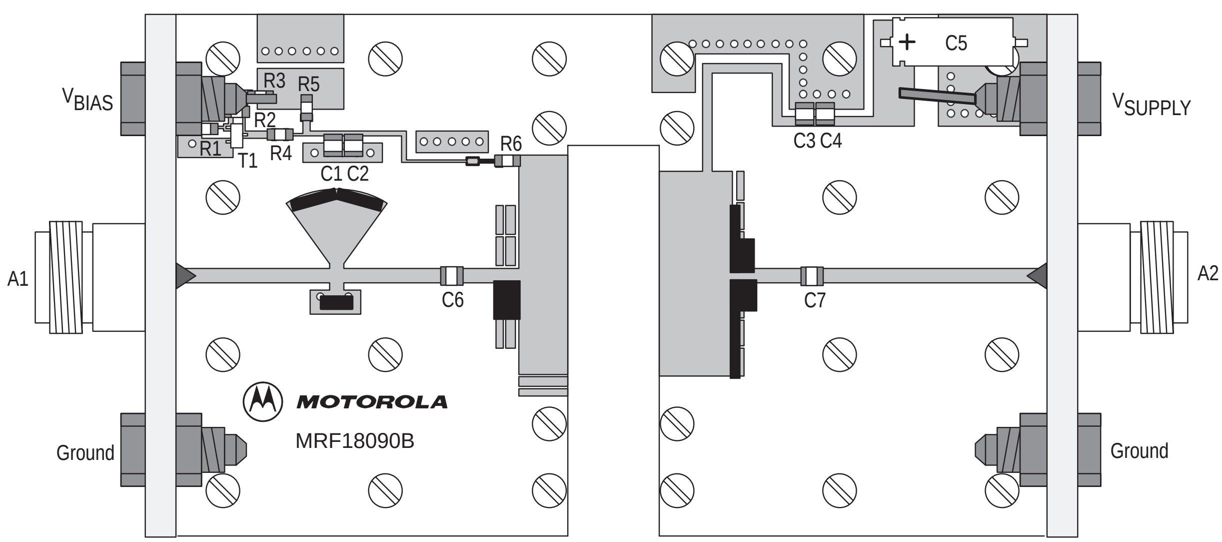
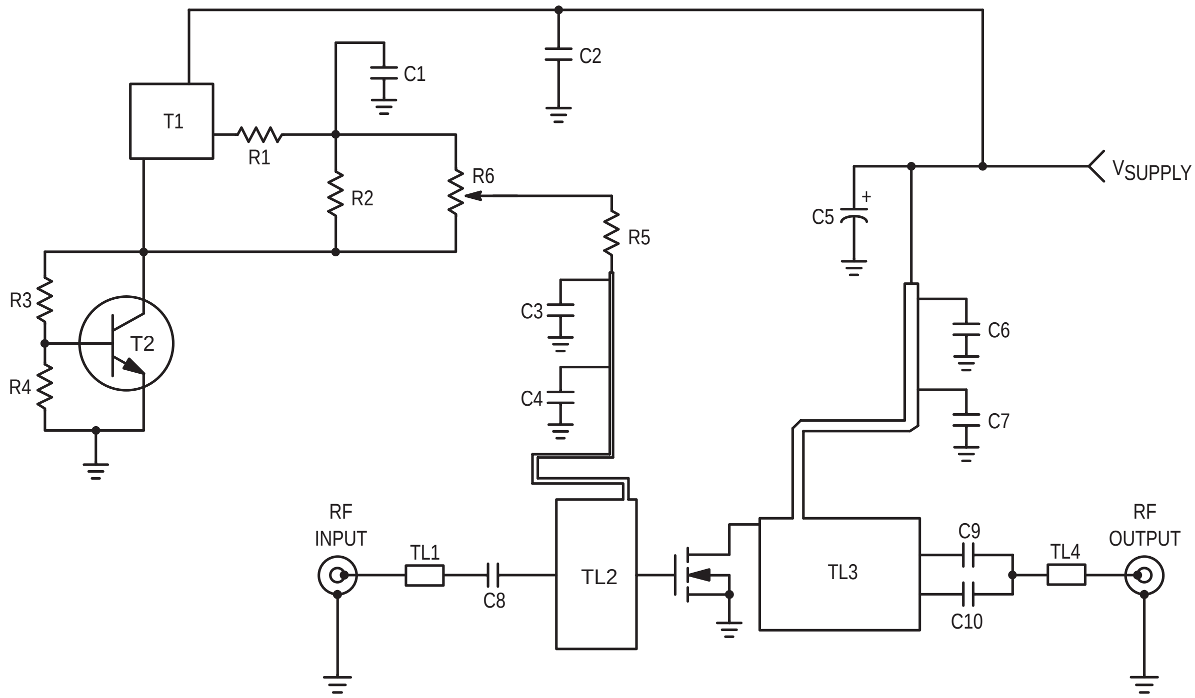


Figure 2. 1.93 – 1.99 GHz Test Fixture Component Layout



C1, C3	1 μF, Chip Capacitor 0805
C2	0.1 μF, Chip Capacitor 0805
C4	1 nF, Chip Capacitor 0805
C5	220 μF, 50 V Electrolytic Capacitor
C6, C7	8.2 pF, 100A Chip Capacitor
C8, C9, C10	22 pF, 100A Chip Capacitor
R1	10 Ω, Chip Resistor 0805
R2, R3	1 kΩ, Chip Resistor 0805
R4	2.2 kΩ, Chip Resistor 0805
R5	10 kΩ, Chip Resistor 0603
R6	5 kΩ, SMD Potentiometer
T1	LP2951 Micro–8 Voltage Regulator
T2	BC847 SOT–23 NPN Transistor
TL1 – TL4	Printed Transmission Lines

Substrate = 0.5 mm Teflon® Glass

Figure 3. 1.93 – 1.99 GHz Demo Board Schematic

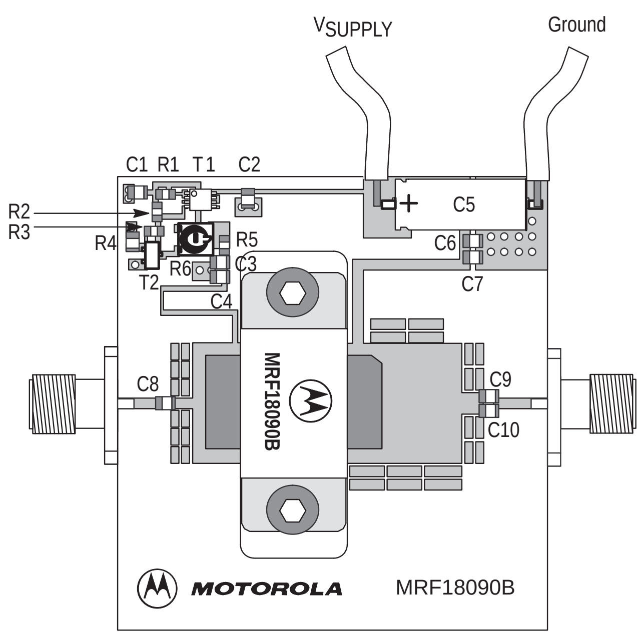


Figure 4. 1.93 – 1.99 GHz Demo Board Component Layout

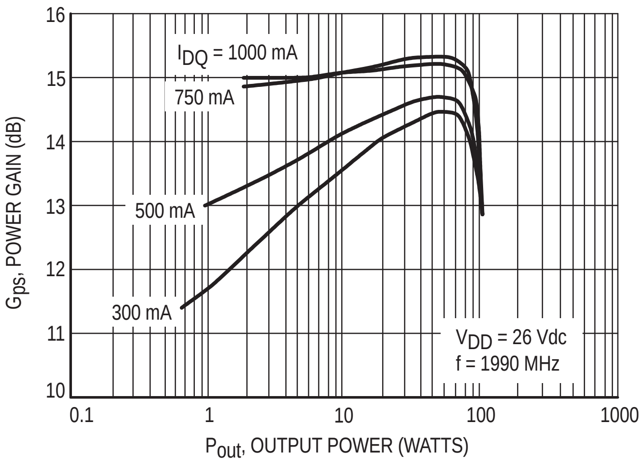


Figure 5. Power Gain versus Output Power

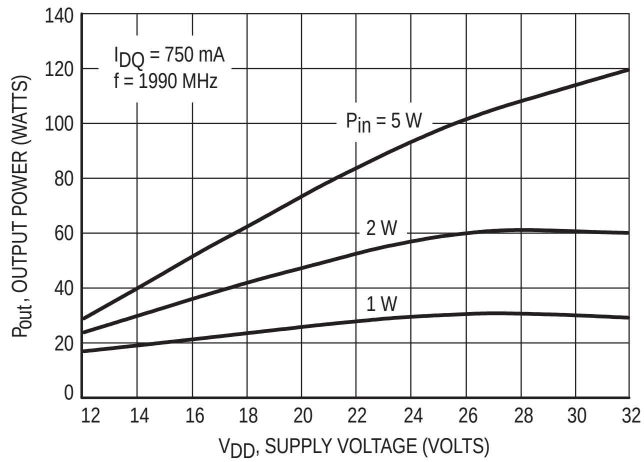


Figure 6. Output Power versus Supply Voltage

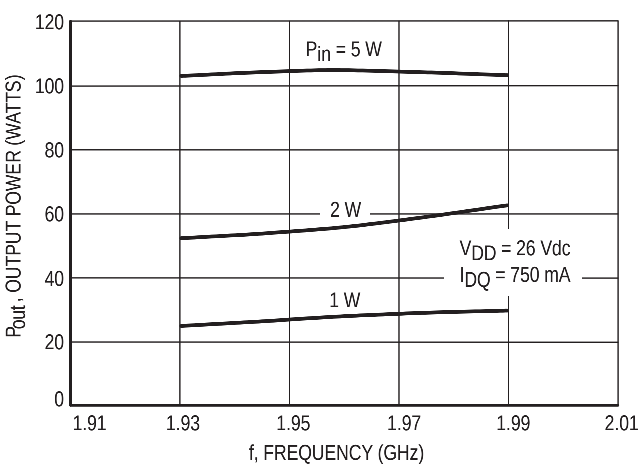


Figure 7. Output Power versus Frequency

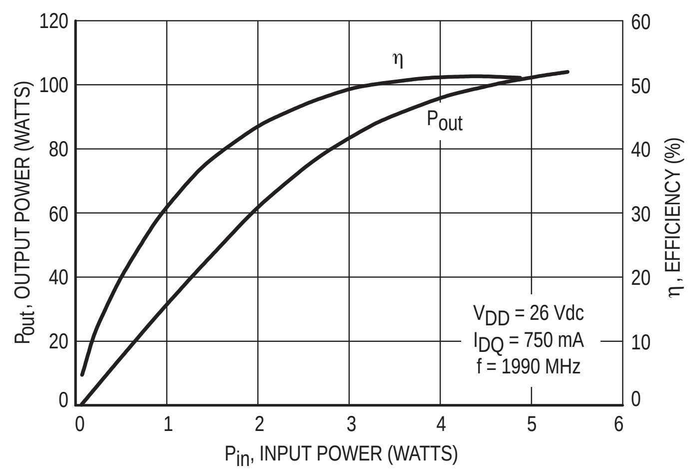


Figure 8. Output Power and Efficiency versus Input Power

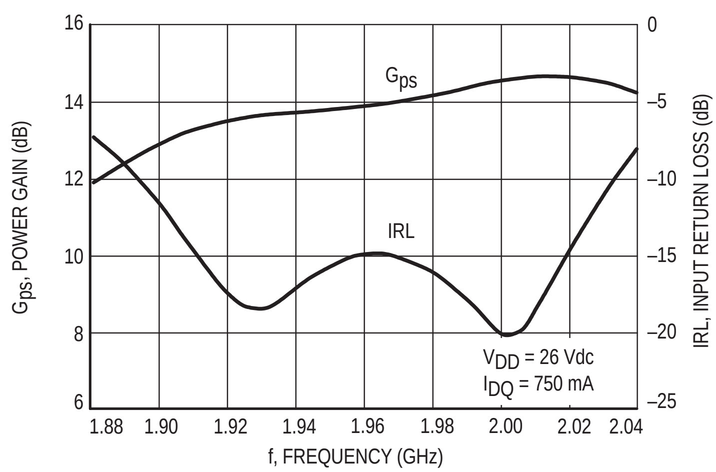


Figure 9. Wideband Gain and IRL (at Small Signal)

V_{DD} = 26 V, I_{DQ} = 750 mA, P_{out} = 90 Watts (CW)

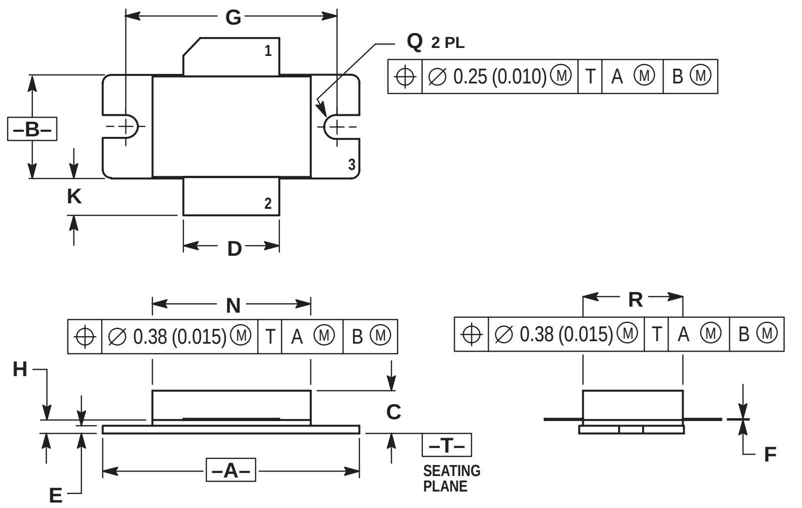
f MHz	Z_{in} Ω	Z_{OL}* Ω
1805	1.1 + j5.85	1.15 + j2.16
1880	1.56 + j6.75	1.13 + j2.6
1930	2.05 + j8.0	1.30 + j2.23
1990	2.3 + j7.3	0.82 + j2.90

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Table 1. Large Signal Input and Output Impedance

PACKAGE DIMENSIONS

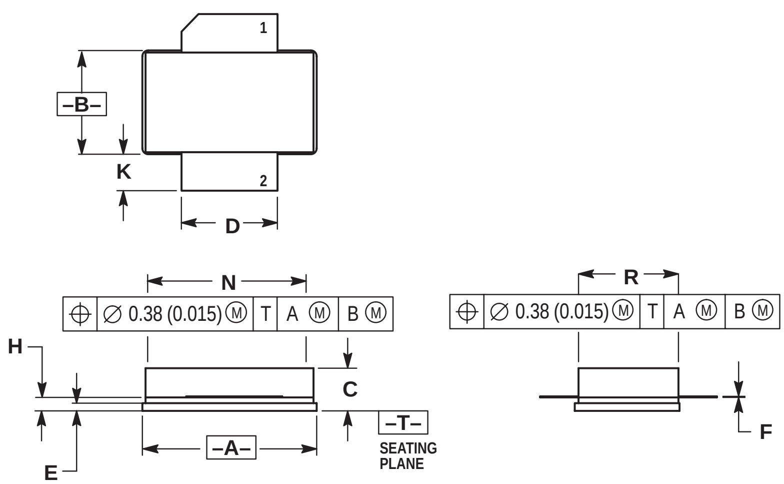


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.535	0.545	13.6	13.8
C	0.155	0.200	3.94	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
N	0.871	0.889	19.30	22.60
Q	0.118	0.138	3.00	3.51
R	0.515	0.525	13.10	13.30

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465B–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030" AWAY FROM FLANGE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.905	0.915	22.99	23.24
B	0.535	0.545	13.6	13.8
C	0.155	0.200	3.94	5.08
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
N	0.871	0.889	19.30	22.60
R	0.515	0.525	13.10	13.30

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465C–01
ISSUE O

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