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MOTOROLA

MC2800

Advance Information

FSK FM IF Receiver BiCMOS

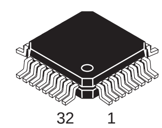
MC2800 is a high performance M–ary FSK FM IF Receiver for FLEX™ pagers. The circuit includes oscillator, mixer, IF amplifier, limiting IF circuitry, RSSI, quadrature discriminator, switchable bitrate filter, peak detector and A/D converter.

- 2/4 Level FSK Comparator and A/D Converter
- Fully Adaptive Data Slicer
- Coilless and Resonatorless Demodulator
- Current Consumption: 1.5 mA Typical
- Operating Voltage: V_{CC} = 1.1 to 3.0 V, V_{DD} = 1.1 to 3.0 V
- Input Bandwidth: 75 MHz
- Excellent Sensitivity: –110 dBm
- Switchable Bitrate Filter up to 6400 b/s Data Rate
- Start–up Time: 5.0 ms
- 1.0 V Regulator with Source Capability of 5.0 mA Typical
- RSSI Function
- Low Battery Detector
- Small Package 5 x 5 32–Pin LQFP

FLEX is a trademark of Motorola, Inc.

FSK FM IF RECEIVER BiCMOS INTEGRATED CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

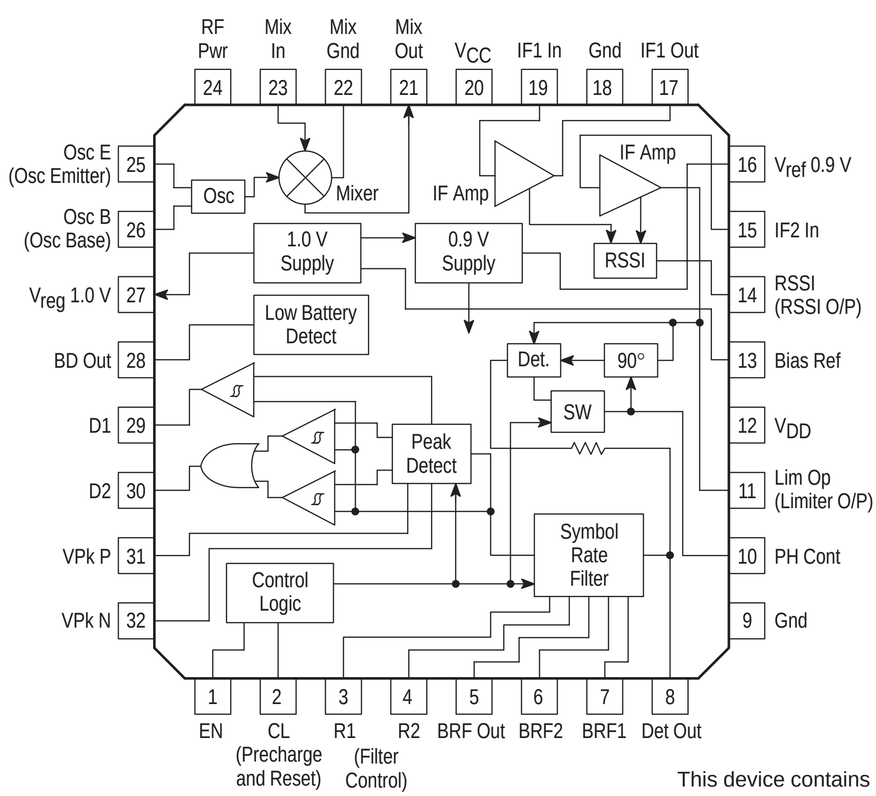


FTA SUFFIX
PLASTIC PACKAGE
CASE 873C
(LQFP–32)

ORDERING INFORMATION

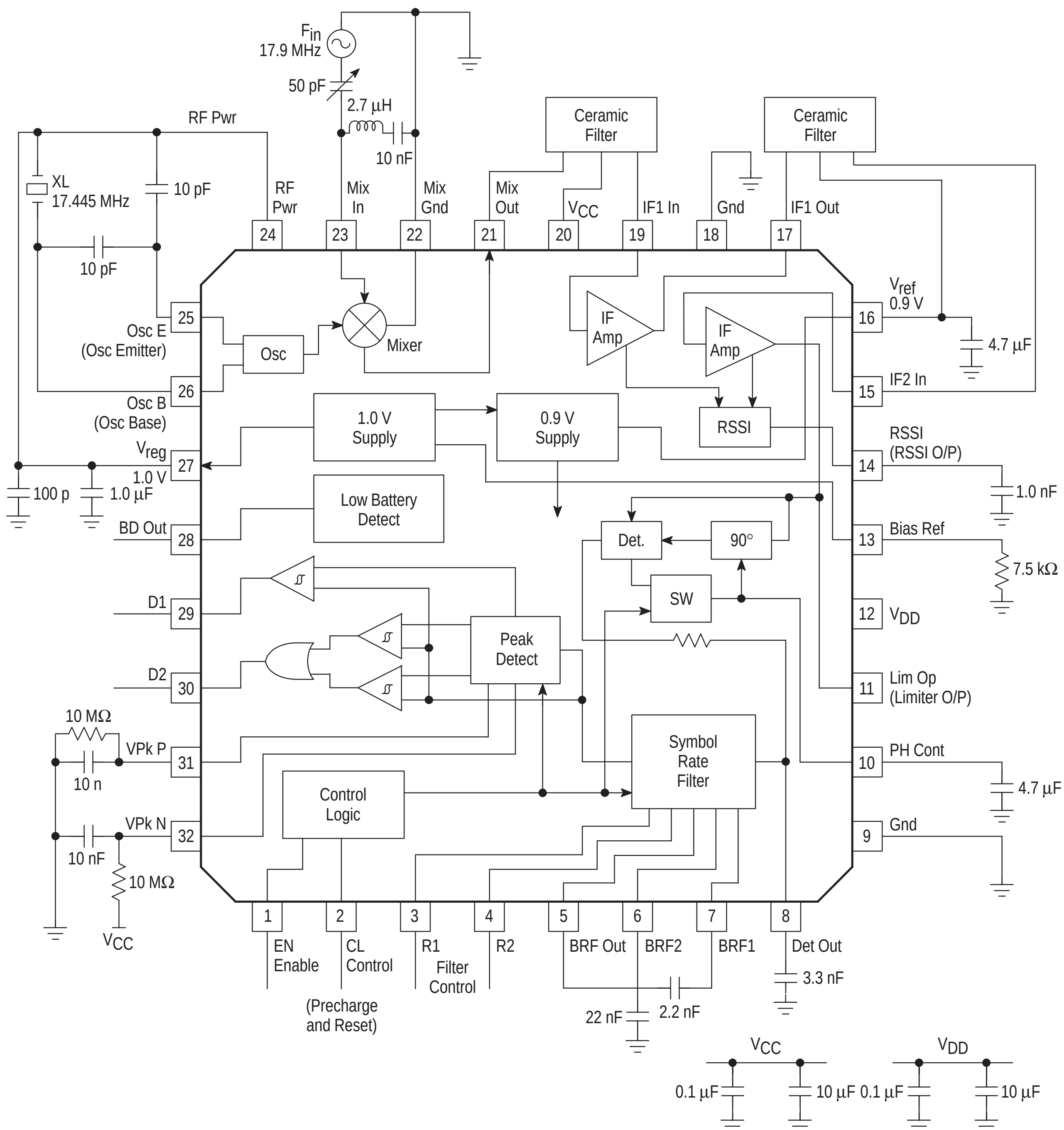
Device	Operating Temperature Range	Package
MC2800FTA	T_A = –10 to 75°C	LQFP–32

Representative Block Diagram



This device contains 1241 active transistors.

Figure 1. Typical Application Circuit for F_{in} = 17.9 MHz



MAXIMUM RATINGS

Rating	Condition	Symbol	Value	Unit
Power Supply Voltage	–	$V_{CC(max)}$ $V_{DD(max)}$	5.0 5.0	V
Junction Temperature	–	T_{JMAX}	150	°C
Storage Temperature	–	T_{stg}	–65 to 150	°C

NOTES: 1. Meets Human Body Model (HBM) ≤2000 V and Machine Model (MM) ≤200 V.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Condition	Symbol	Value	Unit
Power Supply Voltage 1	–	V_{CC}	1.1 to 3.0	V
Power Supply Voltage 2	[Note]	V_{DD}	1.1 to 3.0	V
Input Frequency at Mix In	–	f_{in}	10 to 75	MHz
Ambient Temperature Range	–	T_A	–10 to 75	°C

NOTE: V_{DD} is equal or greater than V_{CC}.

SYSTEM PERFORMANCE CHARACTERISTICS

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
Supply Voltage 1 [Note]	–	V_{CC}	1.1	1.4	3.0	V
Supply Voltage 2 [Note]	–	V_{DD}	1.1	1.8	3.0	V
Current 1	V_{CC} = 1.1 V	I_{CC}	–	1.5	1.7	mA
Current 2	V_{DD} = 1.8 V	I_{DD}	5.0	20	50	µA
Stand–By Current (“off”)	Disable (EN = “L”)	$I_{CC} + I_{DD}$	–	0	2.0	µA
Mixer Input Sensitivity	BER ≤ 1/100; f_{RF} = 17.9 MHz; Data Rate 6400 Bits/s; T_A = 25°C	Sens	–	–	–110	dBm
Detection Threshold for Battery “Low” Indicator	–	V_{th}	–	1.1	1.15	V
Ambient Temperature	–	T_A	–10	–	75	°C

NOTE: V_{DD} is equal or greater than V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.1 V, V_{DD} = 1.8 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
Total Current 1	Active (EN = “H”)	I_{CC}	–	1.5	1.7	mA
Total Current 2	Active (EN = “H”)	I_{DD}	5.0	20	50	µA
Total Current 3	Disable (EN = “L”)	$I_{CC} + I_{DD}$	–	–	2.0	µA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
MIXER (RF Pwr @ 1.0 V)						
Mixer Conversion Gain	Without Load With 1.5 kΩ Load (Ceramic Filter)	G_{max} G_{max}	– –	12 6.0	– –	dB
Maximum Input Level at Mix In	–	V_{im}	–	–15	–	dBm
Third Order Intercept Point	@ Mix In	IIP_3	–	–25	–	dBm
1.0 dB Gain Compression Level	@ Mix In	P_{1dB}	–	–35	–	dBm
Input Impedance	–	R_p	–	2.0	–	kΩ
Maximum Input Frequency	@ Mix In	f_{max}	75	–	–	MHz
Noise Figure @ Mix Out	Frequency = 17.9 MHz	NF1	–	12	–	dB

AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
OSCILLATOR (RF Pwr @ 1.0 V)						
Input Impedance (DC)	@ Osc B	R_{in}	–	15	–	kΩ
Signal Level at Osc B	–	$V_{Osc\ B}$	–	300	–	mVpp
IF AMP (First IF Amplifier)						
Gain	V_{CC} = 1.1 V; 455 kHz; AC Coupling	G_{IF1}	–	45	–	dB
Bandwidth		BW	–	25	–	kHz
Noise Figure		NF	–	18	–	dB
I/P Impedance		–	–	1.5	–	kΩ
O/P Impedance		–	–	1.5	–	kΩ
1.0 dB Compression		–	–	–70	–	dBm
IF AMP (Second IF Amplifier)						
Gain	V_{CC} = 1.1 V; 455 kHz; AC Coupling	G_{IF2}	–	69	–	dB
I/P Impedance		–	–	1.5	–	kΩ
Output Level		Lim Op	–	5.0	10	mVpp
RSSI						
Dynamic Range	–	–	40	–	–	dB
Output Impedance	@ RSSI	R_{rs}	–	50	–	kΩ
RSSI Output Voltage	–	V_{rs}	0	–	V_{CC}	V
RSSI Output Slope	@ RF_{in} = –80 dBm	V_{rs}	–	18	–	mV/dB
OVERALL WITH DETECTOR (@ BRF Out)						
12 dB Sensitivity (SINAD)	–	SINAD	–	–112	–	dBm
Recovered Audio	–	V_{au}	–	300	–	mVpp
Noise Output Level	Input Carrier Only	V_{no}	–	10	–	mVrms
CHARGE TIME						
Charge Time (See Figure 4)	CL = “L” to “H” EN = “H”	t_{ch}	–	5.0	6.0	ms
DATA COMPARATORS (D1, D2)						
Rise and Fall Time	f_{in} = 600 Hz	t_r, t_f	–	5.0	10	µs
Duty Cycle	D1, D2	–	–	50	–	%
Output High Voltage	R_L = 100 kΩ	V_{oh1}	V_{DD} – 0.3	–	–	V
Output Low Voltage	R_L = 100 kΩ	V_{ol1}	–	–	0.2	V
BIT RATE LOW PASS FILTER CUT–OFF FREQUENCY						
Cut–Off Frequency 1 (512 bps) [Note]	(R1, R2) = (0, 0)	f_{cl1}	350	410	480	Hz
Cut–Off Frequency 2 (1200 bps) [Note]	(R1, R2) = (1, 0)	f_{cl2}	820	960	1100	Hz
Cut–Off Frequency 3 (1600 bps) [Note]	(R1, R2) = (1, 1)	f_{cl3}	1100	1280	1480	Hz
Cut–Off Frequency 4 (3200 bps) [Note]	(R1, R2) = (0, 1)	f_{cl4}	2180	2560	2950	Hz

NOTE: Cut–off frequency is depending on the two external capacitors connected between BRF1, BRF Out, BRF2 and ground. The respective values are 2.2 nF ±1% and 22 nF ±1%.

AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.1 V, V_{DD} = 1.1 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
AUDIO OUTPUT (@ Det Out)						
Output Level 1	f_{dev} = ±4.5 kHz, f_{mod} = 600 Hz	V_{au1}	–	100	–	mVpp
Output Level 2	f_{dev} = ±4.8 kHz, f_{mod} = 800 Hz	V_{au2}	–	120	–	mVpp
Output Level 3	f_{dev} = ±4.8 kHz, f_{mod} = 1.6 kHz	V_{au3}	–	120	–	mVpp
BATTERY DETECT (Active Low)						
Threshold Voltage	–	V_{th}	–	1.1	1.15	V
Output High Voltage	R_L = 100 kΩ	V_{oh2}	V_{DD} – 0.3	–	–	V
Output Low Voltage	R_L = 100 kΩ	V_{ol2}	–	–	0.3	V
1.0 V VOLTAGE REGULATOR						
Output Voltage	No Load	V_{reg}	0.95	1.0	1.05	V
External Source Capability	V_{reg} = 0.95 V	I_{Smax}	–	5.0	–	mA
0.9 V VOLTAGE REGULATOR						
Output Voltage	No Load	V_{ref}	0.85	0.9	0.95	V
External Source Capability	V_{ref} = 0.9 V	I_{Smax}	–20	100	300	µA
INPUT PIN DC CHARACTERISTICS						
Input Voltage Low	R1, R2	V_{il1}	–	–	0.3	V
Input Voltage High	R1, R2	V_{ih1}	V_{DD} – 0.3	–	–	V
Input Voltage Low	CL	V_{il2}	–	–	0.3	V
Input Voltage High	CL	V_{ih2}	V_{DD} – 0.3	–	–	V
Input Voltage Low	EN	V_{il3}	–	–	0.3	V
Input Voltage High	EN	V_{ih3}	V_{DD} – 0.3	–	–	V

SYMBOL/BAUD RATE FILTER SELECTION

R1	R2	
L	L	512 POCSAG (Baud Per Second), 2 Levels
H	L	1200 POCSAG (Baud Per Second), 2 Levels
H	H	1600 FLEX (Symbol Per Second), 2/4 Levels
L	H	3200 FLEX (Symbol Per Second), 2/4 Levels

ENABLE (BATTERY SAVE FUNCTION)

Enable	
H	Active
L	Disable (Battery Saving)

CONTROL (CIRCUIT MODE FUNCTION)

Control	
H	Reset Mode
L	Normal Operation Mode

BD Out WITH 100 kΩ (LOW BATTERY DETECTOR)

BD Out	
H	Low Battery
L	–

D1 WITH 100 kΩ (D1)

D1	
H	Dev –4.8 kHz or Dev –1.6 kHz
L	Dev 1.6 kHz or Dev 4.8 kHz

D2 WITH 100 kΩ (D2)

D2	
H	Dev ±1.6 kHz
L	Dev ±4.8 kHz

FUNCTIONAL DESCRIPTION

The complete circuit consists of the following functional blocks as shown in the Block Diagram on page 1.

Oscillator

The oscillator is based on a transistor in common collector configuration. It requires two external capacitors and a crystal to form the tank circuit. External capacitors between base and emitter and from emitter to RF Pwr make the oscillator transistor to have a negative resistance for small signals which is the start–up condition for oscillation.

Mixer

The mixer consists of input v–to–i stage and upper switching stage driven from the oscillator. The LO drive is fed from the built–in oscillator. The mixer output is obtained at Mix Out.

IF Amplifier and Limiter

The first ceramic filter is to obtain the 455 kHz IF and to remove all other harmonics from the mixing process. The mixer output signal is then amplified in the first IF Amplifier. The signal is then fed into the second IF Amplifier through the second ceramic filter. The final IF signal can be monitored at the limiter output pin Lim Op.

RSSI function

The RSSI function is an indication of the strength of the incoming signal.

Demodulator

The limiter output @ 455 kHz is fed into the gyrator for carrier recovery and 90° phase shift. This LO signal is then mixed with the FSK signal fed by the IF Amp for demodulation. The demodulator output can be obtained at Det Out.

Bit–Rate Filter

The cut–off frequencies of the filter can be determined by the 2.2 nF external capacitor between Pins BRF Out and BRF1, and the 22 nF external capacitor at Pin BRF2. The filter bandwidth can be switched by Pins R1 and R2 for both POCSAG and FLEX requirements.

A/D Convertor

The A/D converter features a fully adaptive data slicer. The input to the converter at Pin BRF Out is initially peak–detected. Its peak and valley voltages are obtained at Pins VPk P and VPk N. Three threshold voltages at 1/6, 1/2 and 5/6 of the input signal level are determined dynamically regardless the actual peak–to–peak value. The final digital data are obtained at Pins D1 and D2 depending upon the 2 or 4 levels FSK signal.

Low Battery Detector

The battery low indicator senses the supply voltage and sets its output High when the voltage at input V_{CC} is less than V_{th} (typically 1.1 V).

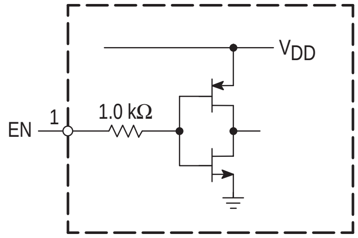
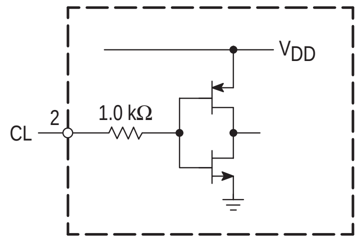
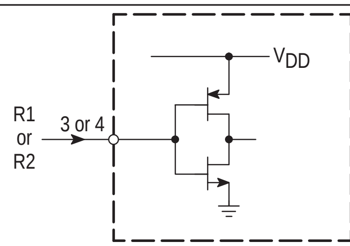
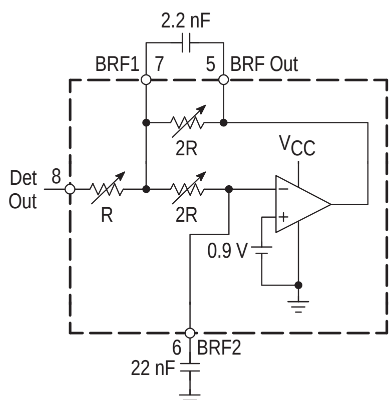
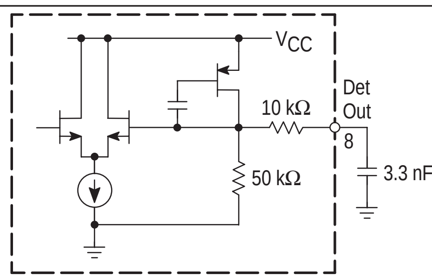
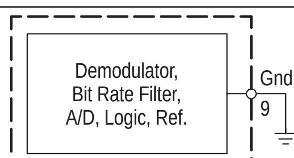
Band Gap Reference

The whole chip can be powered–up and powered–down by enabling and disabling the band gap reference via the Pin EN (Enable).

1.0 V Regulator

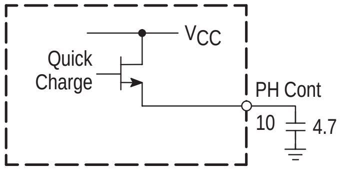
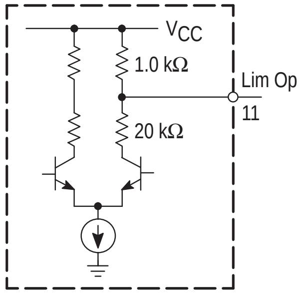
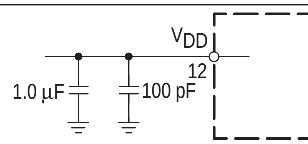
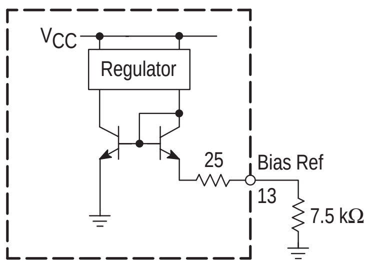
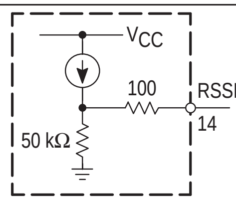
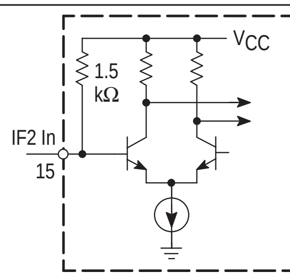
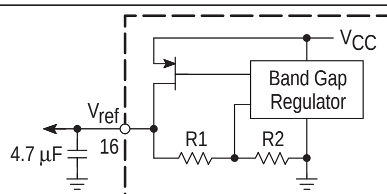
The 1.0 V voltage at Pin V_{reg} is used to supply the regulated voltage for the oscillator and the mixer. It can also be used to supply other external circuits.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Schematic (Excluding ESD)	Description
1	EN		Enables the circuit.
2	CL (Precharge and Reset)		This pin is used to precharge the circuit to accelerate the initial start–up process (particularly the 4.7 µF capacitor at Pin 10).
3 4	R1 R2		These pins are set to “high” or “low”. They are used for the selection of the filter’s symbol rate.
5	BRF Out		Symbol Rate Filter Output for connection of feedback capacitor. This is also the audio output before A/D.
6	BRF2		Symbol Rate Filter Input for connection of filter capacitor.
7	BRF1		Symbol Rate Filter Input.
8	Det Out		Audio output from FSK FM detector. This pin is also audio input for testing purposes (signal of 100 mVpp with DC offset of 0.9 V).
9	Gnd		Ground pin for IC covering Pins 1 through 13 and 27 through 32.

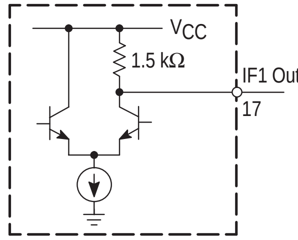
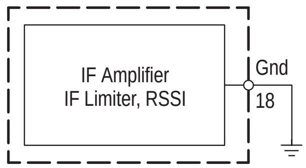
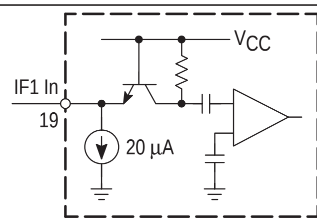
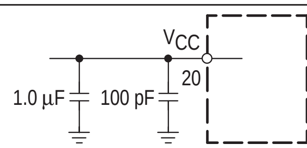
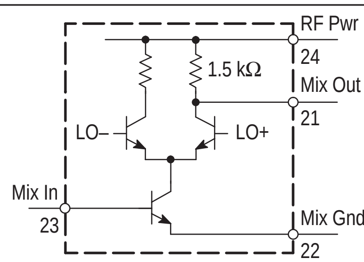
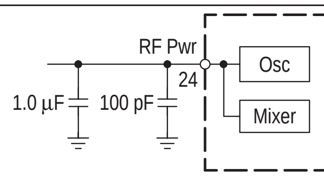
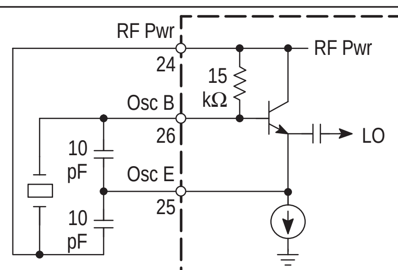
NOTE: Care in PCB layout should be taken to avoid compromising of sensitivity performance.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Schematic (Excluding ESD)	Description
10	PH Cont		This Phase Detector Control pin is connected to a 4.7 µF capacitor. It is precharged to 0.9 V during initial start–up (when the CTL signal is high).
11	Lim Op		IF Amp/Limiter Output (small signal 5.0 mVpp typical). (For test purpose only.)
12	V_{DD}		Digital Power Supply. V_{DD} can be greater or equal to V_{CC}.
13	Bias Ref		A 7.5 k resistor is connected to this pin for bias the reference of the gyrator filter included in the demodulator block.
14	RSSI		Receive Signal Strength Indicator. It should be decoupled with a small capacitor.
15	IF2 In		Signal input for second IF Amplifier/Limiter.
16	V_{ref} 0.9 V		0.9 V reference for internal use only. Minimum 4.7 µF capacitor required for decoupling. Not recommended for external use. (Do not draw current from it.)

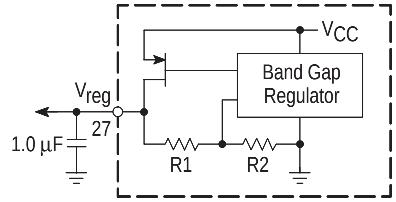
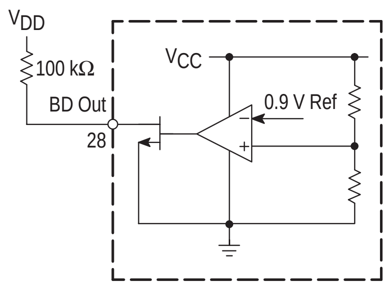
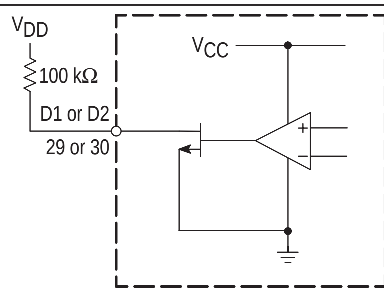
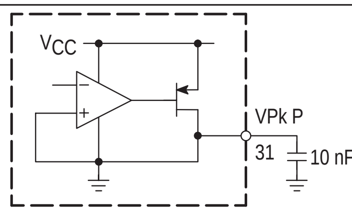
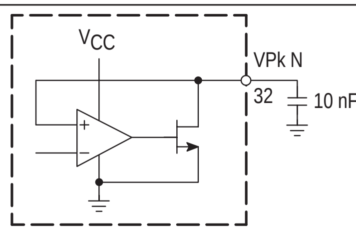
NOTE: Care in PCB layout should be taken to avoid compromising of sensitivity performance.

PIN FUNCTION DESCRIPTION (continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Schematic (Excluding ESD)</th><th>Description</th></tr>
<tr><td>17</td><td>IF1 Out</td><td>
</td><td>First IF Amplifier output.</td></tr>
<tr><td>18</td><td>Gnd</td><td>
</td><td>Ground pin for IC covering Pins 14 through 20.</td></tr>
<tr><td>19</td><td>IF1 In</td><td>
</td><td>First IF Amplifier input.</td></tr>
<tr><td>20</td><td>V_{CC}</td><td>
</td><td>Main Analog Power Supply for the circuit.</td></tr>
<tr><td>21</td><td>Mix Out</td><td rowspan="3">
</td><td>Mixer Output.</td></tr>
<tr><td>22</td><td>Mix Gnd</td><td>Ground pin for the RF Part.</td></tr>
<tr><td>23</td><td>Mix In</td><td>Mixer input relative to Pin 22.</td></tr>
<tr><td>24</td><td>RF Pwr</td><td>
</td><td>Power Supply for the RF part. It is not internally connected to the other Power Supply. It must be connected externally to V_{reg} 1.0 V, with the appropriate decoupling.</td></tr>
<tr><td>25
26</td><td>Osc E
Osc B</td><td>
</td><td>These pins form the reference oscillator when connected to an external parallel–resonant crystal (17.445 MHz typical).</td></tr>
</table>

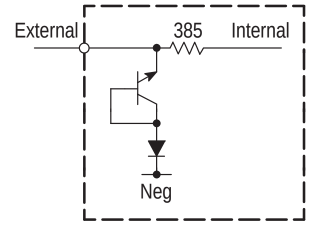
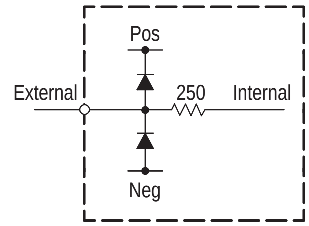
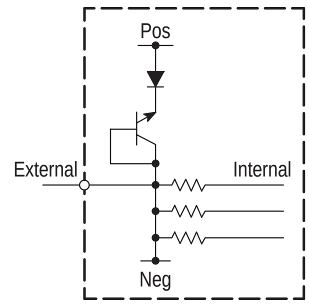
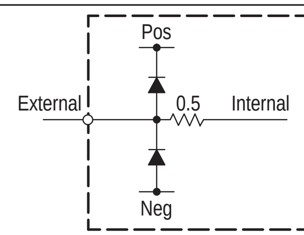
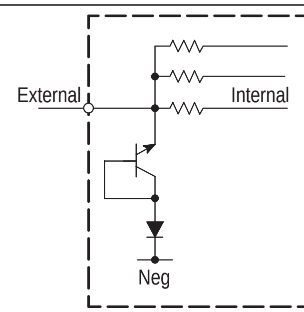
NOTE: Care in PCB layout should be taken to avoid compromising of sensitivity performance.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Schematic (Excluding ESD)	Description
27	V_{reg} 1.0 V		1.0 V regulator output. Minimum 1.0 µF capacitor required for decoupling. It can supply up to 3.0 mA for external use.
28	BD Out		Low Battery Detector Output (open collector requires external pull–up resistor typically at 100 kΩ.). It toggles with V_{CC} at 1.1 V typical.
29 30	D1 D2		Digital output of data slicers D1 and D2 (A/D converter). It is an open collector and requires an external pull–up resistor typically at 100 kΩ.
31	VPk P		Peak Detector Output voltage of peak. It can be monitored with a high impedance (FET) probe.
32	VPk N		Peak Detector Output voltage of valley. It can be monitored with a high impedance (FET) probe.

NOTE: Care in PCB layout should be taken to avoid compromising of sensitivity performance.

ESD PROTECTION SCHEMATIC

Pin	Symbol	Type	Schematic
1	EN	Digital Input (385 Ω)	
2	CL		
3	R1		
4	R2		
5	BRF Out	Analog Input/Output (250 Ω)	
6	BRF2		
7	BRF1		
8	Det Out		
9	Gnd	Gnd (0 Ω)	
10	PH Cont	Analog Output (0 Ω)	
11	Lim Op	Analog (250 Ω)	Same as Pin 5
12	V_{DD}	Power Input (High Voltage) (0 Ω)	
13	Bias Ref	Analog (250 Ω)	Same as Pin 5
14	RSSI	Analog (250 Ω)	Same as Pin 5
15	IF2 In	Analog (250 Ω)	Same as Pin 5
16	V_{ref} 0.9 V	Power (0 Ω)	Same as Pin 12
17	IF1 Out	Analog (250 Ω)	Same as Pin 5
18	Gnd	Gnd (0 Ω)	Same as Pin 9
19	IF1 In	Analog (250 Ω)	Same as Pin 5

ESD PROTECTION SCHEMATIC (continued)

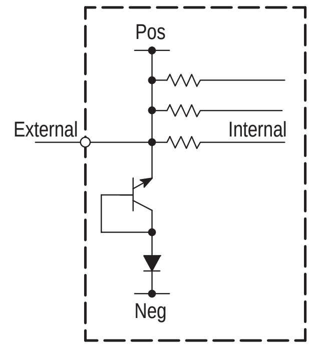
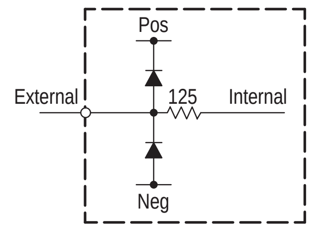
Pin	Symbol	Type	Schematic
20	V_{CC}	Supply Input (0 Ω)	
21	Mix Out	Analog (250 Ω)	Same as Pin 5
22	Mix Gnd	Gnd (0 Ω)	Same as Pin 9
23	Mix In	RF Input (125 Ω)	
24	RF Pwr	Supply (0 Ω)	Same as Pin 20
25	Osc E	Analog (250 Ω)	Same as Pin 5
26	Osc B	Analog (250 Ω)	Same as Pin 5
27	V_{reg} 1.0 V	Power (0 Ω)	Same as Pin 12
28	BD Out	Power (0 Ω)	Same as Pin 12
29	D1	Power (0 Ω)	Same as Pin 12
30	D2	Power (0 Ω)	Same as Pin 12
31	VPk P	Analog (250 Ω)	Same as Pin 5
32	VPk N	Analog (250 Ω)	Same as Pin 5

Figure 2. Data Slicer Operation

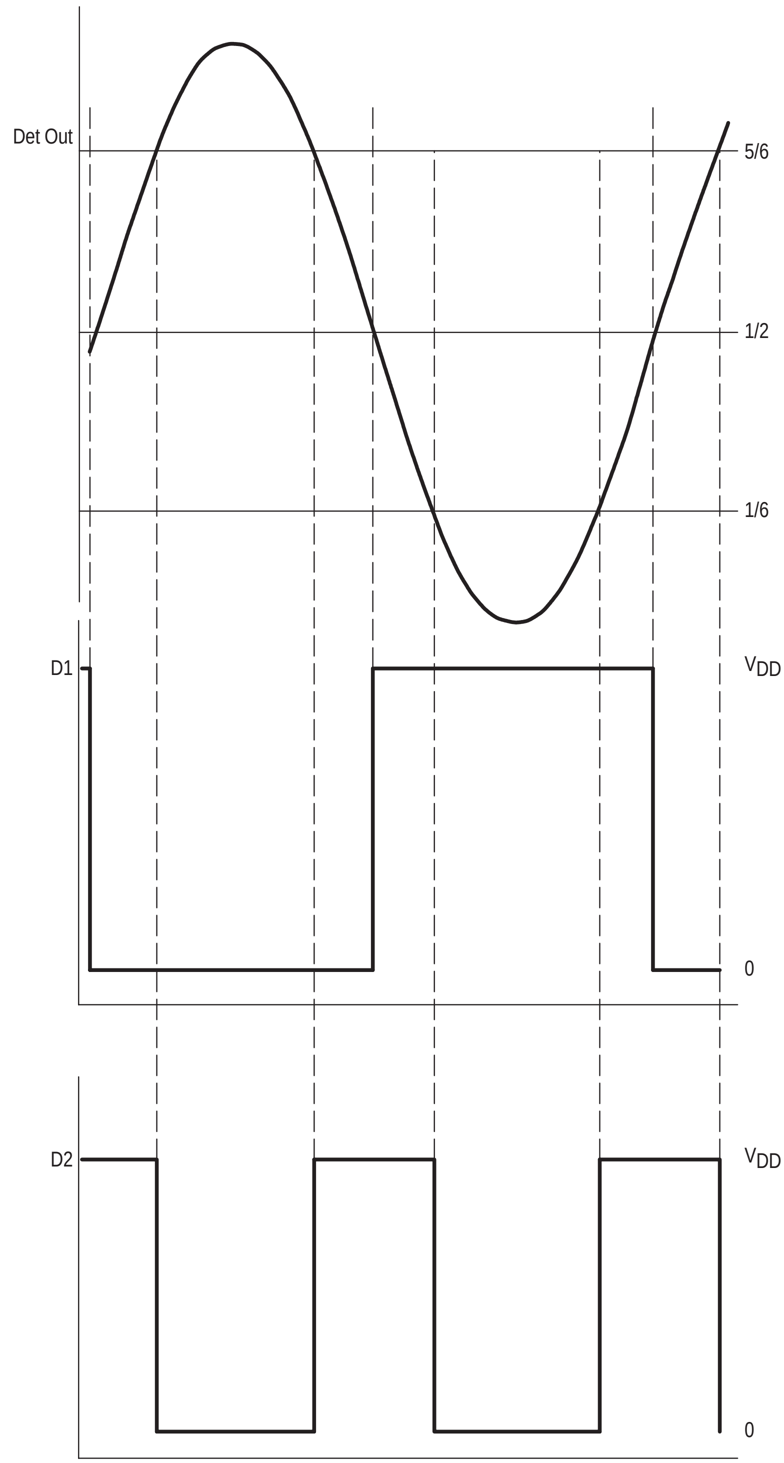


Figure 3. Typical BRF Response

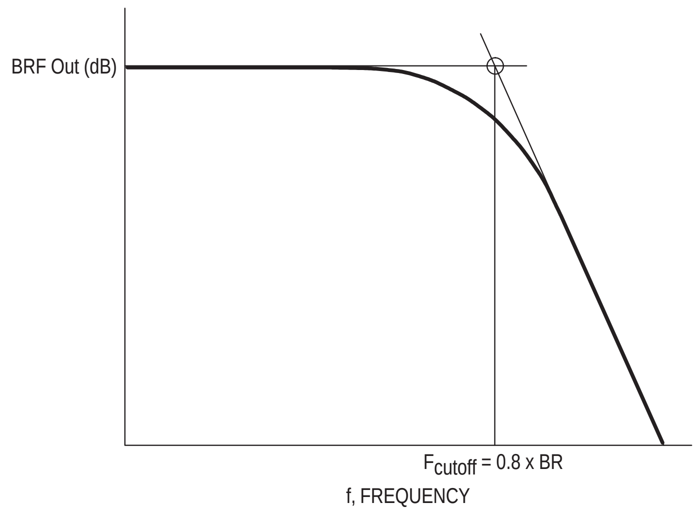


Figure 4. Start–Up Operation

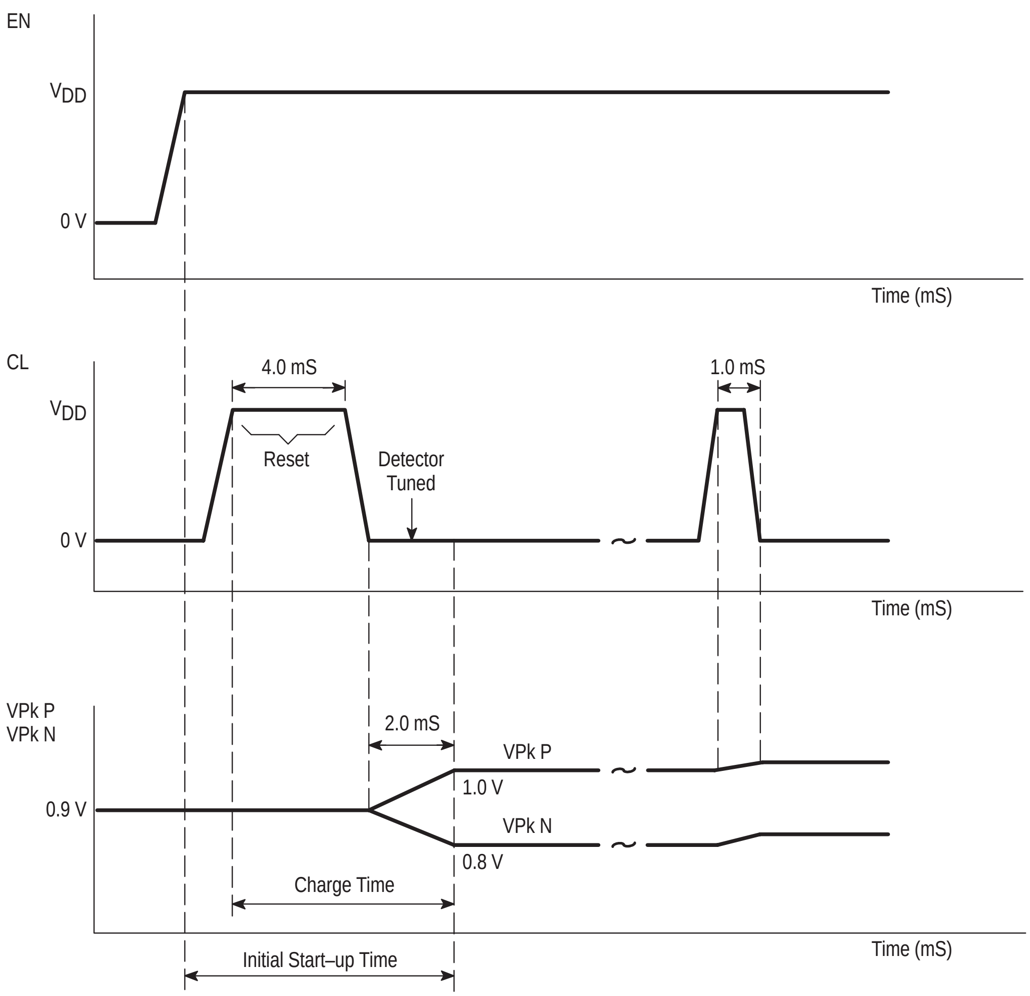
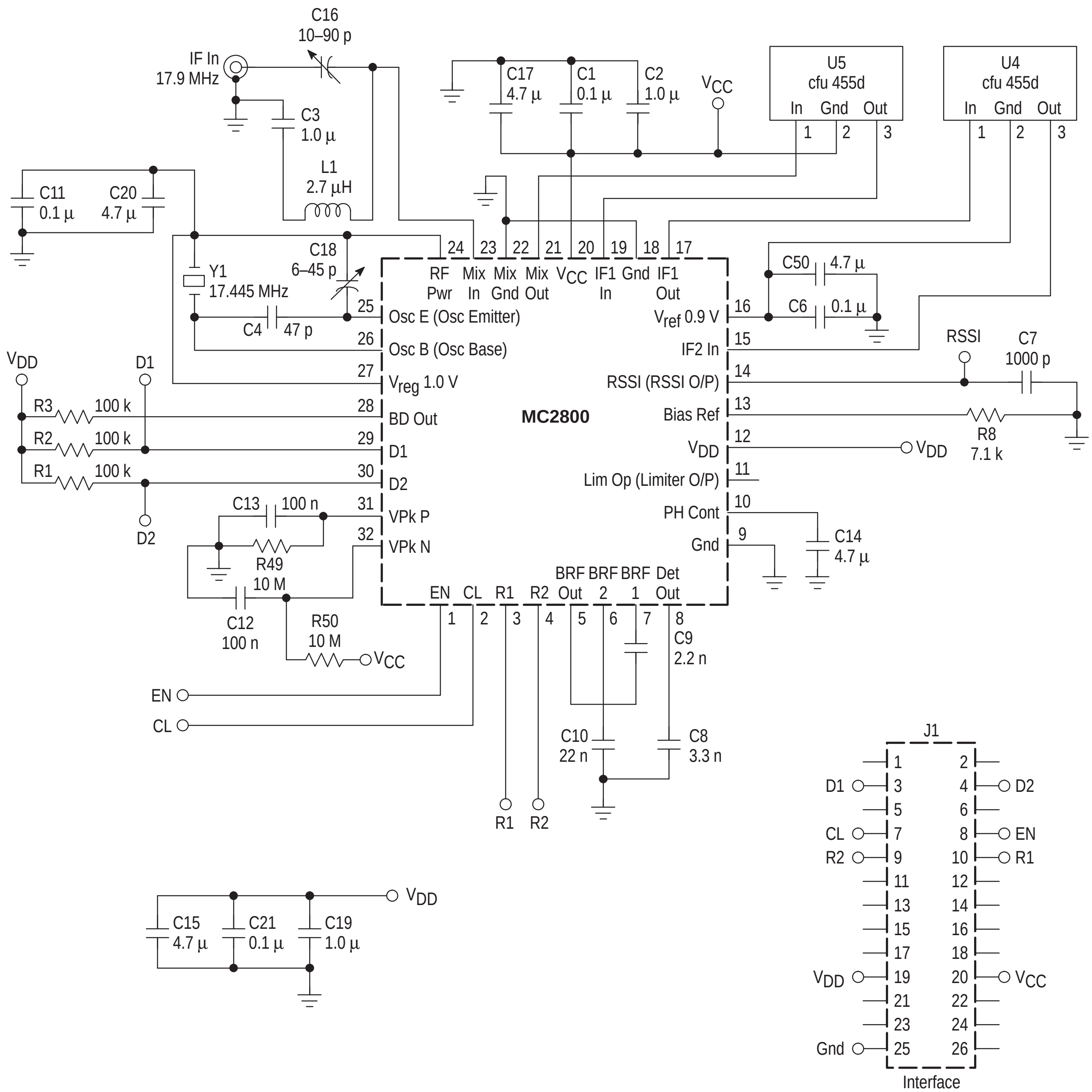


Figure 5. Schematics of MC2800 Demo Board (Two 455 kHz Ceramic Filters)



Capacitors	
C1,C6,C11,C12,C13,C21	0.1 µF
C2,C3,C19	1.0 µF
C4	47 pF
C7	1.0 nF
C8	3.3 nF
C9	2.2 nF
C10	22 nF
C14,C15,C17,C20,C50	4.7 µF
Variable capacitors	
C16	10 to 90 pF
C18	6.0 to 45 pF

Inductor	
L1	2.7 µH
Resistors	
R1,R2,R3	100 kΩ
R8	7.1 kΩ
R49,R50	10 MΩ
Ceramic filters (455 kHz)	
U4,U5	CFU455D
Crystal (17.445 MHz)	
Y1	1U0174450B2035BOX

MC2800 Application Board

The typical application circuit of MC2800 is shown in Figure 5. The performance of the system kit consisting of the MC2800, MC68175 and MC68HC705L32 is measured. The system has a typical sensitivity of –115 dBm @ Phase A. Table 1 shows the sensitivity measurements of the system at different symbol rates along with the Symbol Rate Filter (SRF) filter selections. The test input to the MC2800 is a single message of 12 characters. The first two columns of Table 1 show the SRF's R1 and R2 conditions during synchronization. The third and fourth columns show the R1 and R2 conditions during data sampling. In operation, the original digital baseband data is encoded by the Encoder Software in the computer before this encoded message is sent out via the Data Acquisition card (DAQ) to the signal generator HP8657B. The MC2800 receives the modulated signal from the HP8657B and then converts it into baseband data D1 and D2. When retrieving data from Pins D1 and D2, it is essential to observe the timing requirements for the EN and CL signals. This is illustrated in EN and CL Timing Requirements. The computer at the other end then retrieves the D1 and D2 data through the L32EVS board and displays it in the HC05 Pager Development Board. The test setup of this system measurement is shown in Figure 6.

With the input frequency at 17.9 MHz the input impedance of the mixer is measured to be 2.1k–j2.67 kΩ. The input impedance does not vary significantly with the supply voltage and frequency of interest. Figure 7 shows the input impedance of the mixer over a range of frequencies in the Smith Chart. From the Smith Chart, the matching network connecting between the 50 Ω signal generator and the MC2800 mixer is worked out to be consisting of a shunt inductor of 3.8 µH and a series capacitor of 19 pF. A varicap of 10 to 90 pF is selected for the series capacitor as this will make the fine tuning of the input stage easier. The other input to the mixer is internally connected to a Local Oscillator (LO). The LO has a Colpitts amplifier which amplifies the external crystal frequency of 17.445 MHz. The natural oscillation frequency of the crystal is not exactly 17.445 MHz, therefore the capacitor C4 is set to 47 pF and the varicap C18 is selected to have a range of 6.0 to 45 pF for making sure that the LO can oscillate at 17.445 MHz. The conversion voltage gain of the mixer is about 20 dB @ –110 dBm. Table 2 shows the mixer gain with different input signal levels. After the input signal is amplified and down converted to 455 kHz, it is then filtered before entering the amplifier 1st IF Amp. The voltage gain of this amplifier is measured to be 40 dB. This is shown in Figure 8. From the first stage of amplification the input signal strength is also detected and it can be monitored at the RSSI Pin. The relationship between the input signal strength and the RSSI output is shown in Figure 9. In applications where component cost is critical, the second 455 kHz ceramic filter may be replaced by an LC π network. This is shown in Figure 10. The 1.0 µF capacitors are used for blocking dc voltages. The network consisting of 560 pF capacitors and the 470 µH inductor acts as both a low pass filter centered at 455 kHz and a matching between the first amplifier output and the second amplifier input. The output resistance of the first amplifier is 1.1 kΩ and the input resistance of the second amplifier is 1.5 kΩ. Based on the setup as shown previously in Figure 6, the system performance of the MC2800 (one 455 kHz ceramic filter plus one LC network combination) together with the MC68175 and the MC68HC705L32 is measured and the test result is tabulated in Table 3.

Coming back to the device MC2800, the demodulator is coilless and it does not need any resonator. The external resistor connected to the pin Bias Ref is used to give the reference bias loop current for the demodulator. The frequency response of the demodulator is measured and it is shown in Figure 11. At the Demodulator Output (Det Out Pin) a capacitor is used to decouple the high frequency noise. Figure 12 shows the differences of the signal measured at this pin with different values of capacitors used. This highlights the importance in the selection of this capacitor value. If this value is too small then the SINAD will be very poor and hence the sensitivity will be very bad. If it is too big then the high frequency contents in the step input signal will be decoupled and this will make the decoding very difficult after analog to digital conversion. The SRF filter is a two pole active filter. The filter characteristics are plotted in Figure 14 and Figure 15 for which the selections of R1 = 0 and R2 = 1 are used during measurements. R1 and R2 are used to select the amount of resistors in the filter. The four level Data Slicer converts the analog signal into D1 and D2 digital outputs. This A–D conversion is best illustrated by the plots in Figures 16 and 17. A brief outline of the A–D conversion can be found in Data Slicer A/D Conversion. Figure 22 shows how the MC2800 is connected to the decoding device (MC68175) which is used after analog to digital conversion. The interface between the two devices is tabulated in Table 6. The operating procedure is also outlined.

Table 1. Test Result of the Typical MC2800 Demo Board with Different Symbol Rates (bps Means Bits Per Second and sps Means Symbols Per Second)

					6400 bps or 3200 sps	6400 bps or 3200 sps	3200 bps or 1600 sps	3200 bps or 1600 sps
					4 level	4 level	4 level	4 level
SRF Filter Control					Sensitivity (dBm)			
1600 sps R1	1600 sps R2	3200 sps R1	3200 sps R2		Phase A	Phase B	Phase A	Phase C
1	1	0	1		–112	–109	–112	–109

Figure 6. Test Equipment Setup

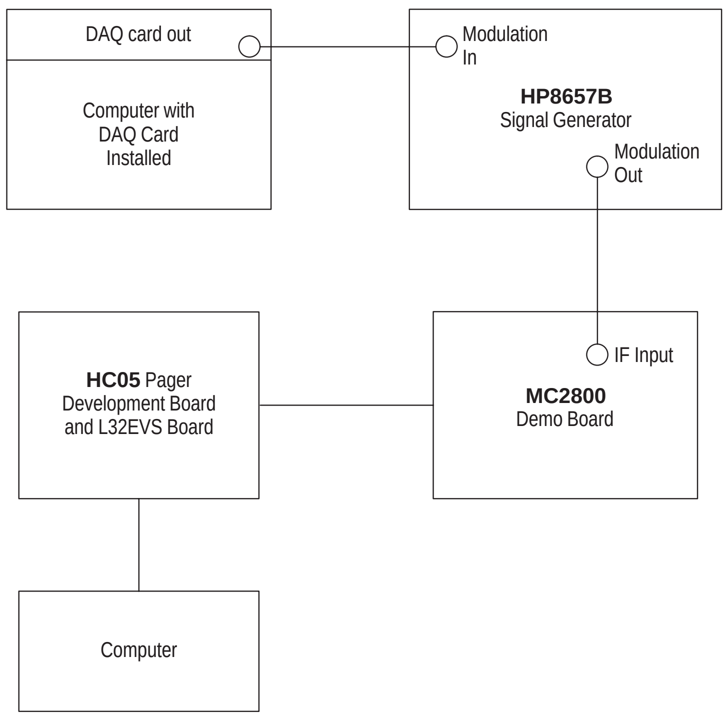


Figure 7. Input Impedence of MC2800 Mixer with Frequency Range 15 to 30 MHz

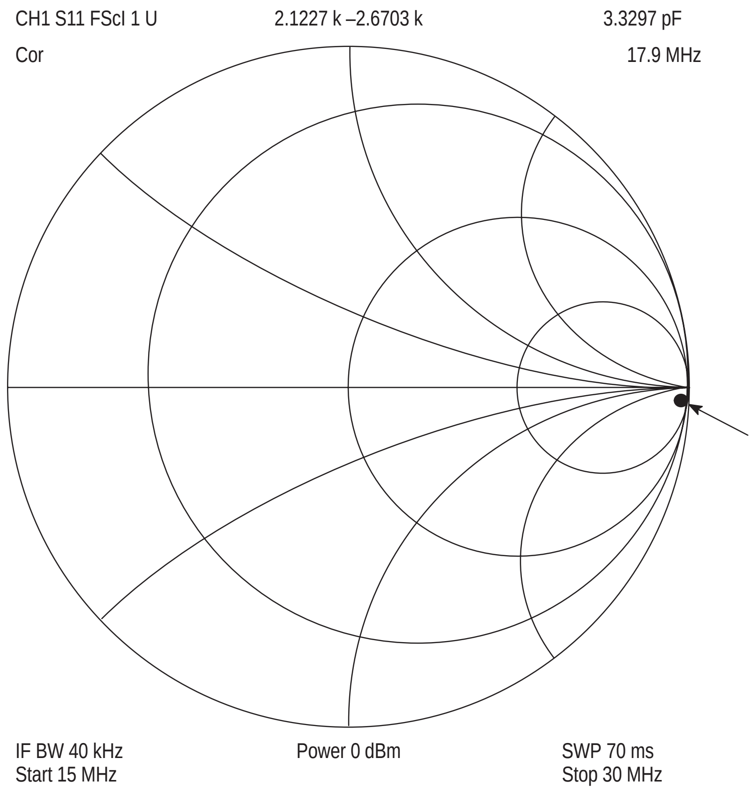


Table 2. Mixer Gain (with Matching Circuit)

Mixer Input (dBm)	–120	–110	–100	–90	–80	–70	–60	–50	–40	–30	–20	–10
Mixer Voltage Gain (dBm)	21.5	19.6	18.6	18	17.8	17.6	17.7	17.8	17.6	17.4	12.6	3.0
Mixer Power Gain (dBm)	6.7	4.75	3.83	3.21	3.0	2.79	2.9	2.99	2.87	2.64	–2.16	–11.7

Figure 8. 1st IF Amplifier Voltage Gain

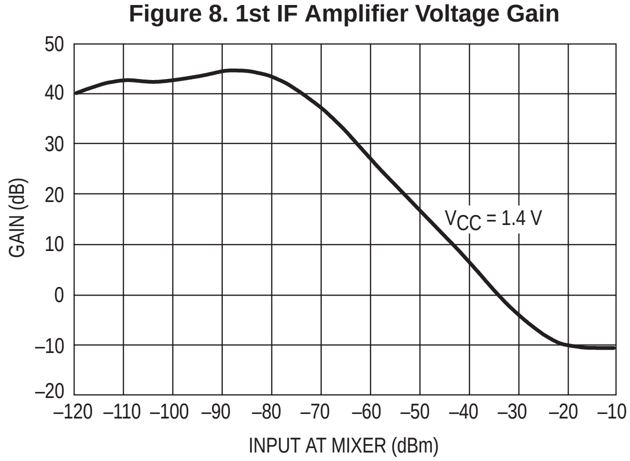


Figure 9. RSSI Output versus Mix In

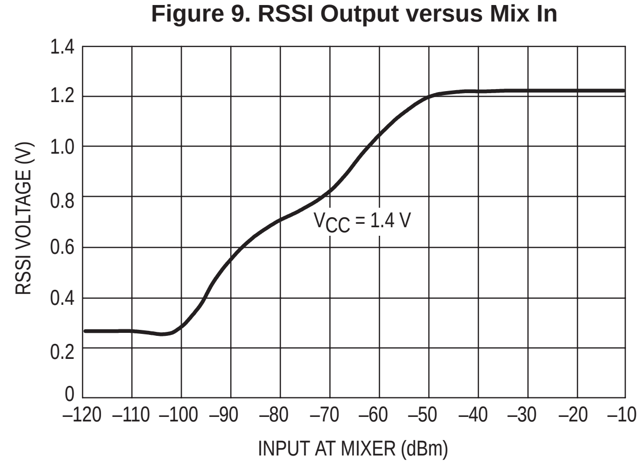
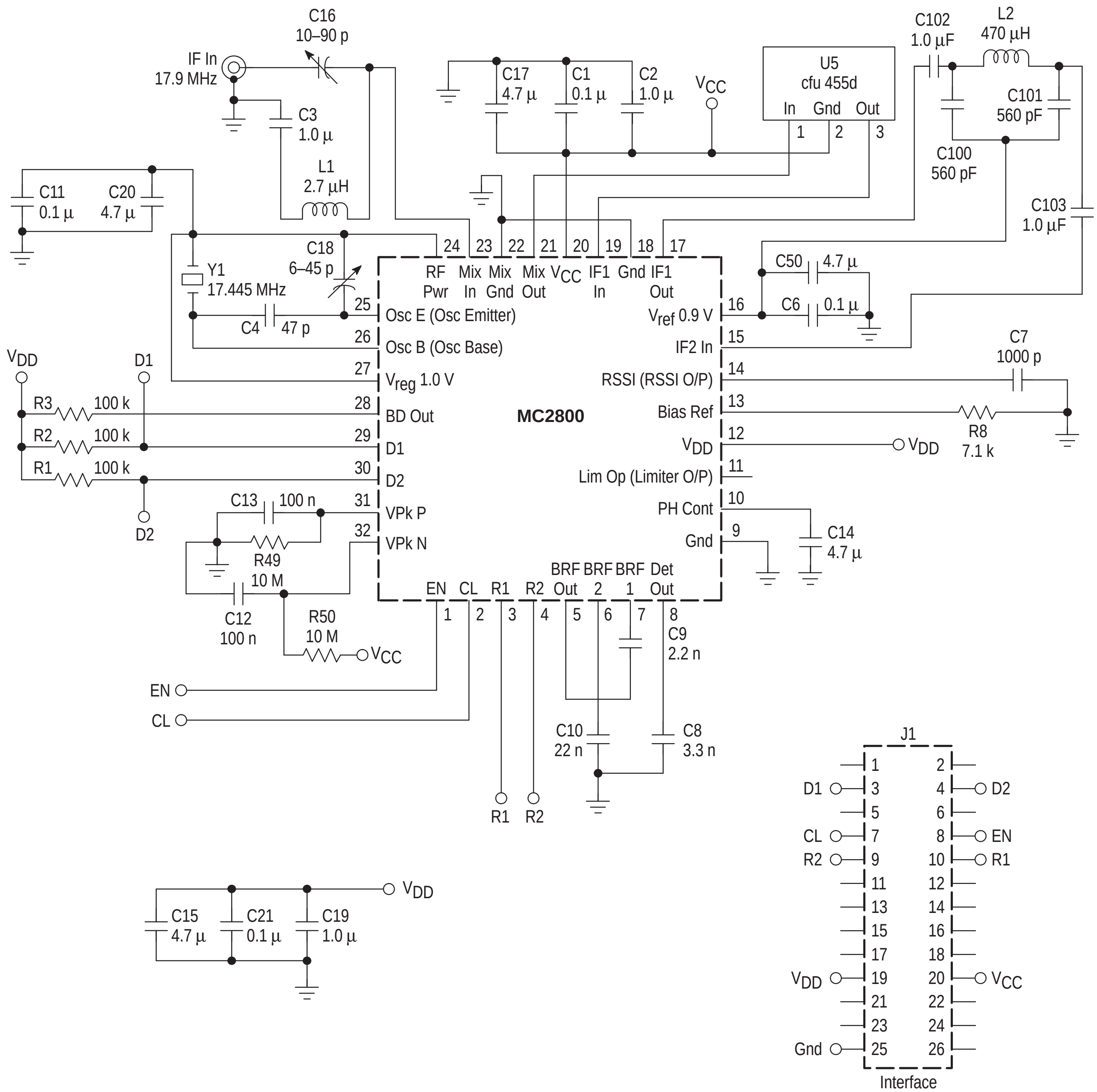


Figure 10. Schematics of MC2800 Demo Board (One 455 kHz Ceramic Filter)



Capacitors

C1,C6,C11,C12,C13,C21	0.1 µF
C2,C3,C19,C102,C103	1.0 µF
C4	47 pF
C7	1.0 nF
C8	3.3 nF
C9	2.2 nF
C10	22 nF
C14,C15,C17,C20,C50	4.7 µF

Variable capacitors

C16	10 to 90 pF
C18	6.0 to 45 pF

Capacitors

C100,C101	560 pF

Inductors

L1	2.7 µH
L2	470 µH

Resistors

R1,R2,R3	100 kΩ
R8	7.1 kΩ
R49,R50	10 MΩ

Ceramic filter (455 kHz)

U5	CFWC455D–TC

Crystal (17.445 MHz)

Y1	1U0174450B2035BOX

Table 3. Test Result of the One 455 kHz Ceramic Demo Board

					6400 bps or 3200 sps	6400 bps or 3200 sps	3200 bps or 1600 sps	3200 bps or 1600 sps
					4 level	4 level	4 level	4 level
SRF Filter Control					Sensitivity (dBm)			
1600 sps R1	1600 sps R2	3200 sps R1	3200 sps R2		Phase A	Phase B	Phase A	Phase C
1	1	1	0		–108	–105	–108	–105

Figure 11. Demodulator Response at Det Out with Reference to Mixer Input

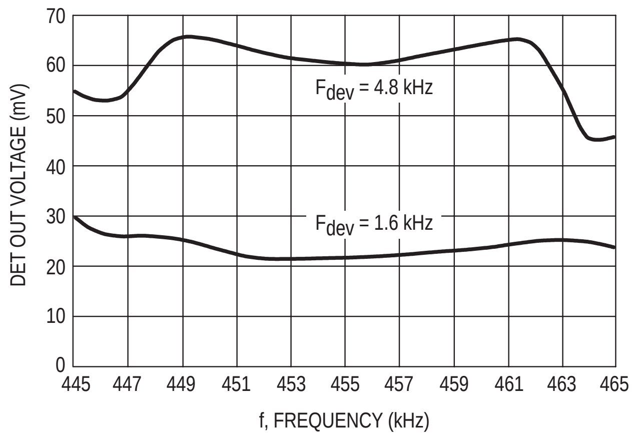


Figure 12. Det Out Characteristics with Different Capacitors (C = 20 nF)

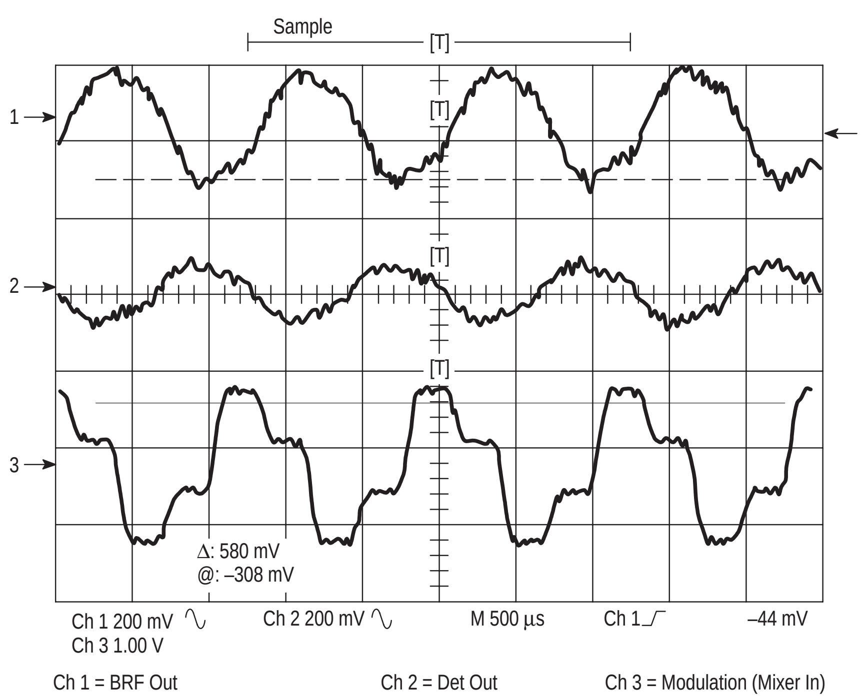


Figure 13. Det Out Characteristics with Different Capacitors (C = 3.3 nF)

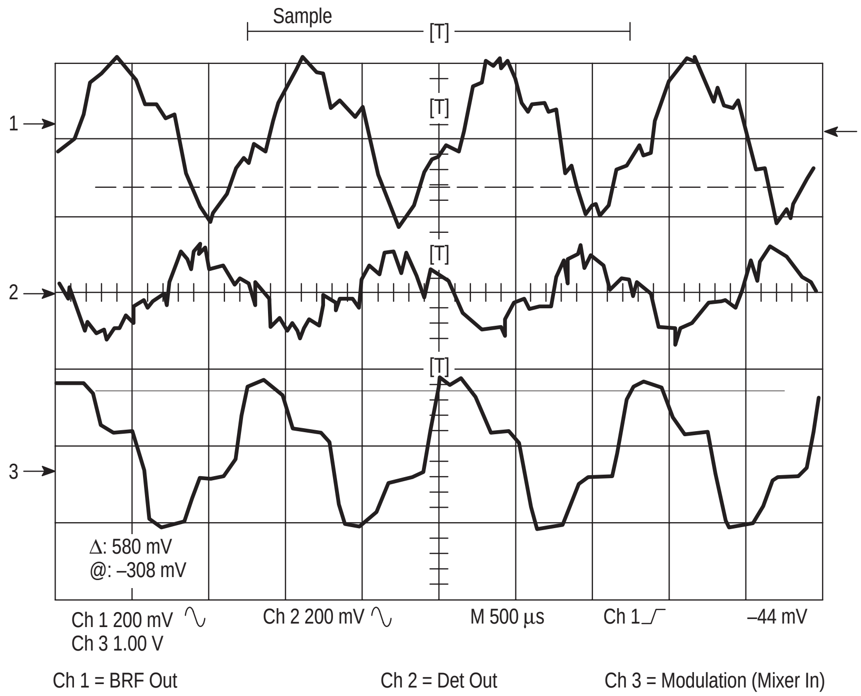


Figure 14. Symbol Rate Filter – Phase Response (R1 = 0, R2 = 1)

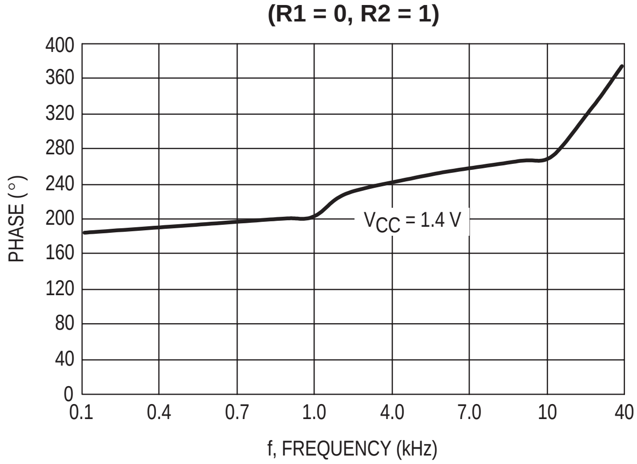


Figure 15. Symbol Rate Filter – Gain Response (R1 = 0, R2 = 1)

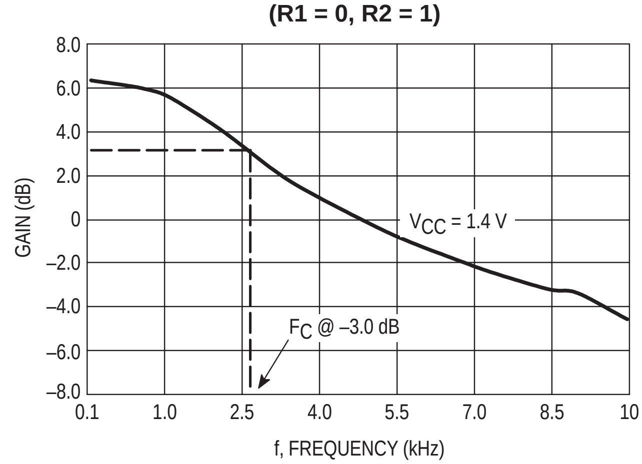


Figure 16. Modulation and Signal at BRF Out Pin

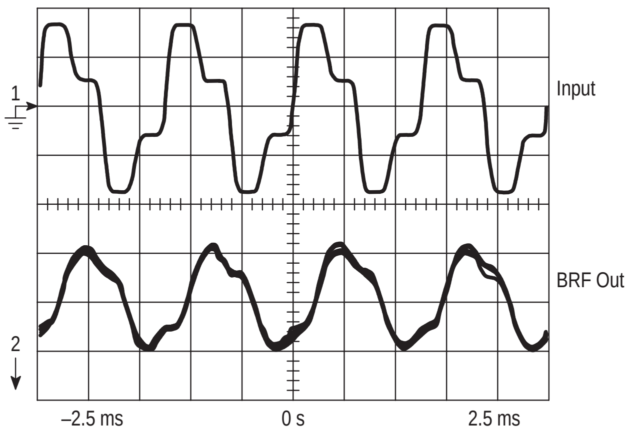
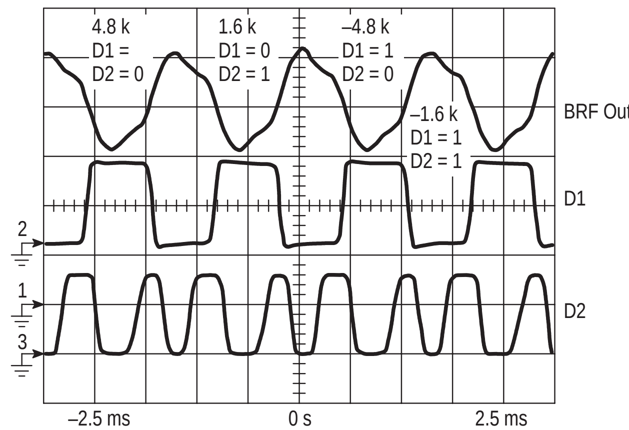


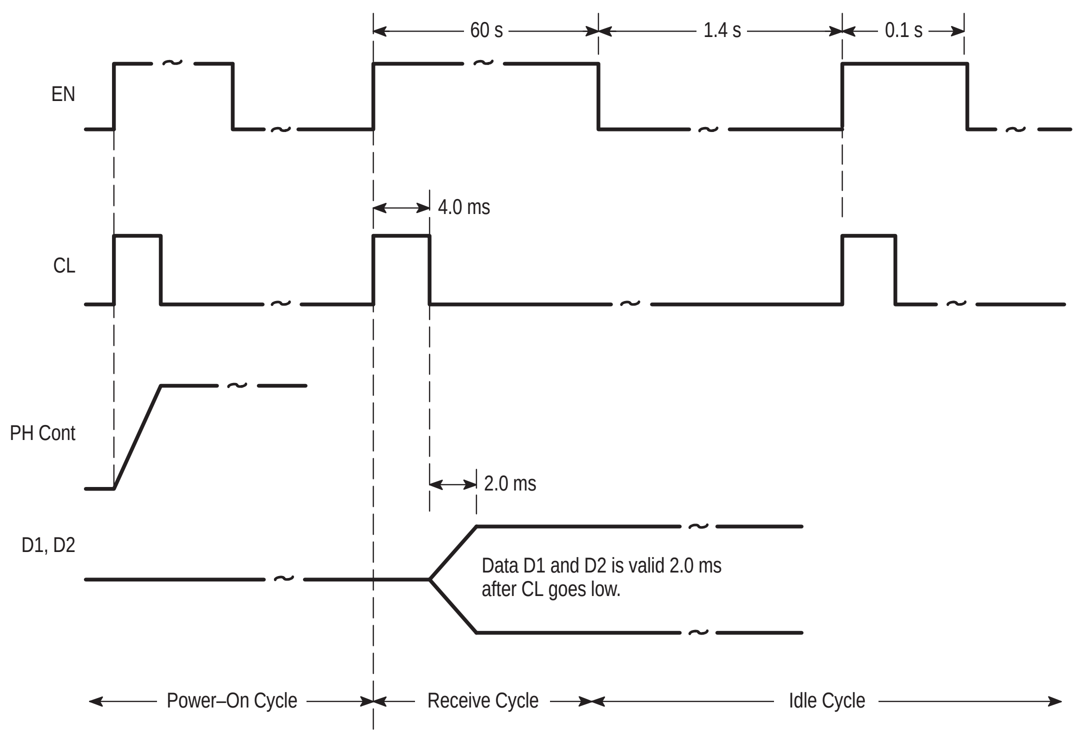
Figure 17. Digital D1 and D2 Outputs



EN and CL Timing Requirements

When power is first applied to the MC2800 the capacitor connecting to the Pin PH Cont is pre–charged to 0.9 V. The voltages at Pins EN and CL must be set to high during this Power On cycle of time. In the typical system application as shown in Figure 6 the voltage at Pin EN is pulled to high for a duration of 60 seconds at first. During this period the device MC2800 is enabled and data at Pins D1 and D2 is valid 6.0 ms after EN is high. When EN goes high, CL can also go high at the same instance without any delay. The purpose of pulling CL to high is to set up the voltages at Pins 31 and 32. It has been tried that 4.0 ms is adequate to get these pins to the correct voltages. However some delay must be allowed for the transient to die down after CL goes low. In application, it is observed that the data D1 and D2 will be valid 2.0 ms after CL goes low in this receive cycle. When there is no incoming message to receive, it is best to disable the MC2800 to save power. In this idle cycle, the MC2800 is disabled most of the time and it is enabled once every 1.5 s (or in some cases 1.875 s) to open the channel for the MCU to detect if there is any message coming in or not. These typical conditions are all illustrated in Figure 18.

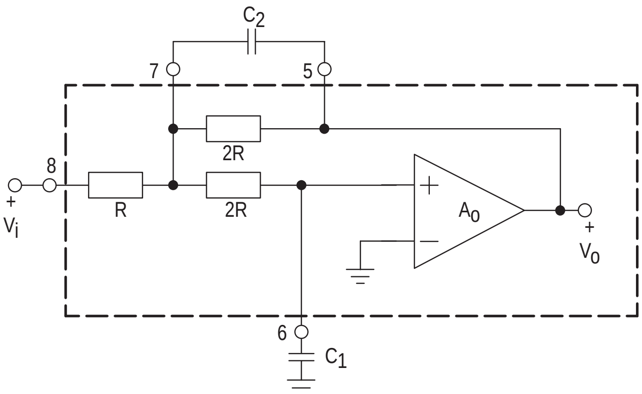
Figure 18. Timing of EN and CL



Low Pass Bit–Rate Filter

This section is a short description of the Architecture of the Bit–Rate Filter used in the MC2800.

Figure 19.



Based on the schematics described above, the equation of this filter is:

$$\frac{v_o}{v_i}(S) = \frac{-\frac{2A_o}{1+A_o}}{1 + s2RC_2 + \frac{2}{1+A_o}\left(1 + s4RC_1 + s^2 2R^2 C_1 C_2\right)}$$

$$= -\frac{\frac{2A_o}{3+A_0}}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

Assume A_o = 200, and $C_1 = 10C_2$, this equation can be simplified as:

$$p_1 = -\frac{0.44}{RC_2} \quad \text{and} \quad p_2 = -\frac{11.56}{RC_2}$$

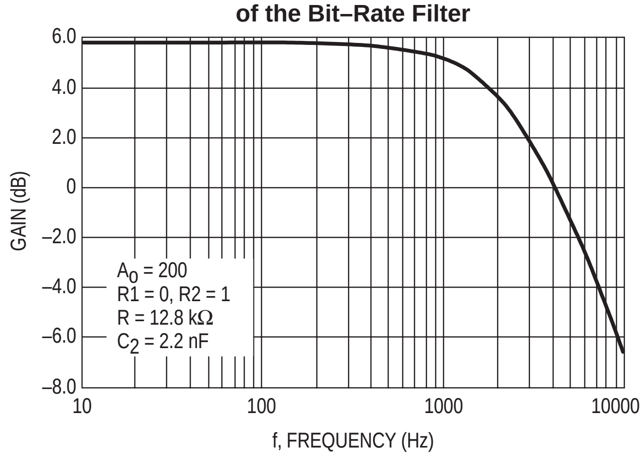
With the different combinations of R1, R2 to setup the Bit–Rate Filter, the cut–off frequencies has been defined according to the table below:

Table 4. Bit–Rate Filter Frequency Responses
(assume $C_1 = 10C_2$ = 22 nF)

R1	R2	R/kΩ	f_{p1}/Hz	f_{p2}/Hz
0	0	84.0	379	9.96 k
1	0	35.6	894	23.5 k
1	1	26.5	1.20 k	31.6 k
0	1	12.8	2.49 k	65.3 k

A typical frequency response of the bit–rate filter is shown in Figure 20.

Figure 20. Gain Response of the Bit–Rate Filter



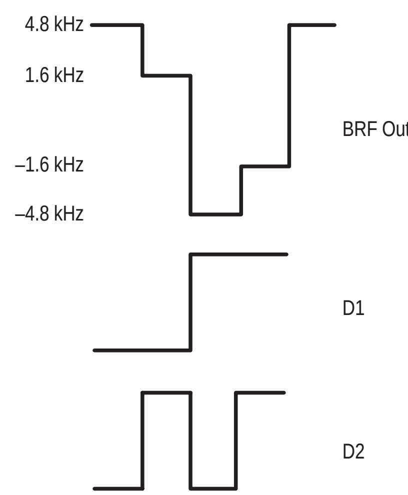
Data Slicer A/D Conversion

In the data slicer of the MC2800 there is a block of comparators which can compare four different kinds of input voltage levels. This “4 level” comparator compares the incoming signal (BRF Out) and then turns it into digital D1 and D2 outputs. This is shown graphically in Figure 21. The state table of D1 and D2 is shown in Table 5.

Table 5. State Table of D1 and D2

Frequency Deviation	D1	D2
4.8 kHz	0	0
1.6 kHz	0	1
–1.6 kHz	1	1
–4.8 kHz	1	0

Figure 21. D1 and D2 Outputs



MC2800 with HP8648

Figure 22. MC2800 Demo Board Test Circuit (See Figures 5 and 10 for component list)

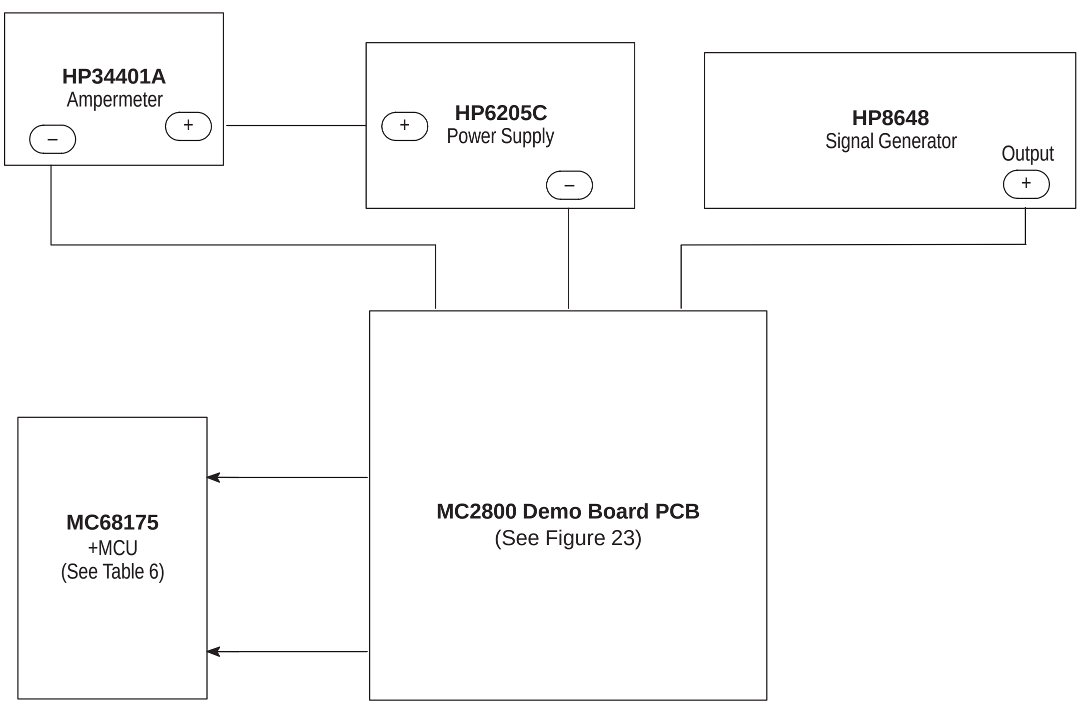
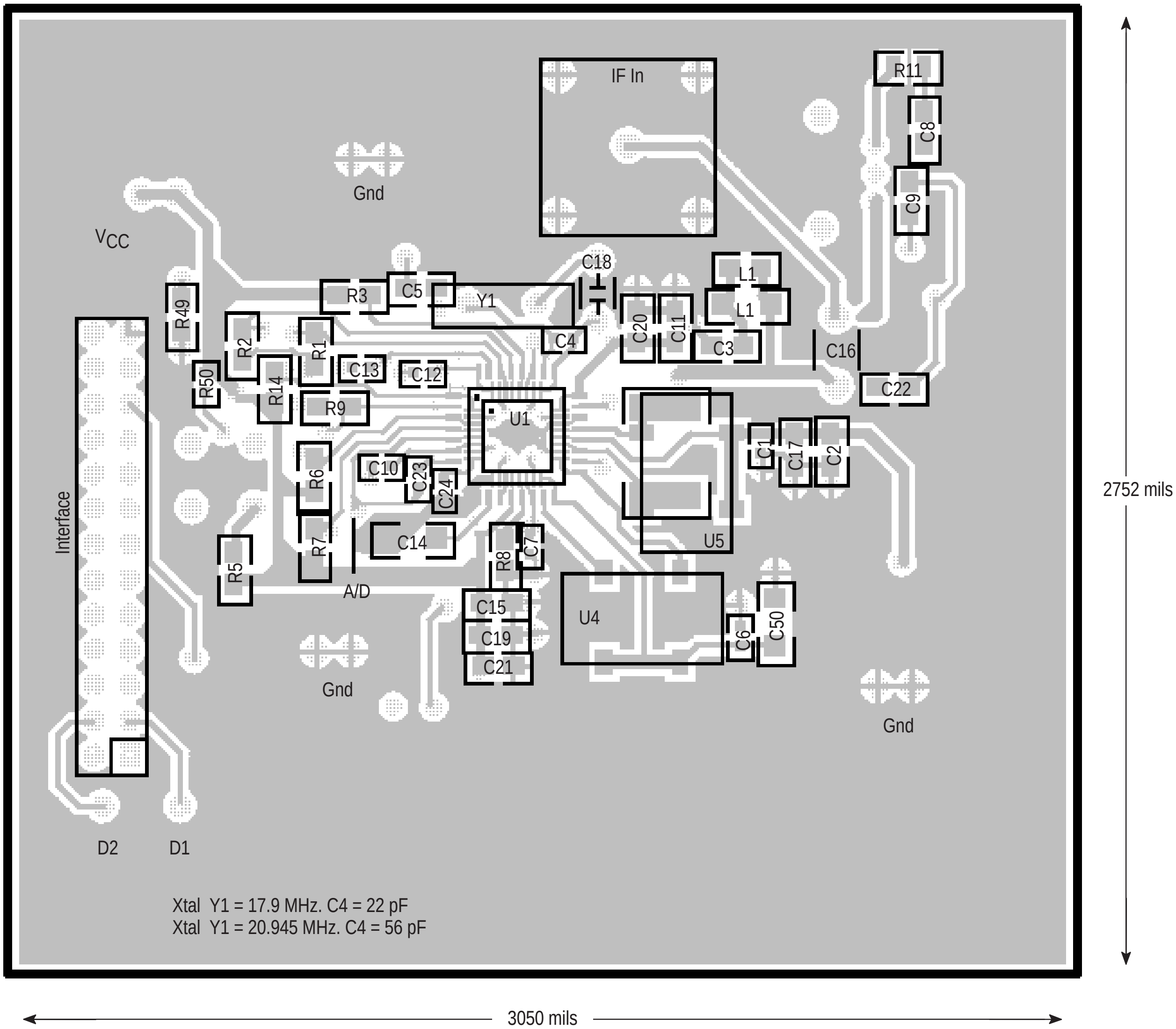


Figure 23. MC2800 Demo Board PCB (Top Layer)



C1,C6,C11,C21	0.1 µF
C2,C3,C5,C8, C9,C19,C22	1.0 µF
C4	22 pF
C7	1000 pF
C10	22 nF
C12,C13	100 nF
C14	22 µF
C15,C17,C20, C50	4.7 µF
C16	10 to 90 pF
C18	4 to 25 pF
C23	2.2 nF
C24	3.3 nF

L1	2.7 µH
R1, R2, R3, R6, R7, R14	100 k
R5, R11	2.0 k
R8	7.5 k
R9	10 k
R49	10 M
R50	910 k
U1	MC2800
U4,U5	CFWC455D–TC
Y1	17.445 MHz

Table 6. Interface Between the MC2800 and the MC68175

MC2800 Pin No.	MC2800 Pin Description	Interface Connector Pin No.	MC68175 Pin No.	MC68175 Pin Description
30	D2	3	12	EXTS0
29	D1	4	11	EXTS1
2	CL	7	23	S0
1	EN	8	22	S1
4	R2	9	21	S2
3	R1	10	20	S3
12	V_{DD}	19	–	–
20	V_{CC}	20	–	–
14	RSSI	21	–	–
9, 18	Gnd	25	–	–

Operating Procedures

1. Connect up the circuit as shown in Figure 22.
2. Set the power supply to 1.4 V (typical value of an AA battery).
3. Set the HP8648A signal generator to the following:

FORMAT FLEX
POLARITY NORMAL FILTER ON

ROAMING MODE NONE

CYCLE 00 FRAME 000 PHASE A
COLLAPSE CYCLE 0

ADDRESS TYPE SHORT
ADDRESS1 2031715

PAGER CODE A0000001
DUMMY CALL OFF

IMMEDIATE STOP OFF
HEADER ON TERMINATOR ON

MODE SINGLE AMPLITUDE –110 dBm

MESSAGE NO.6 MESSAGE LENGTH 10
1234567890

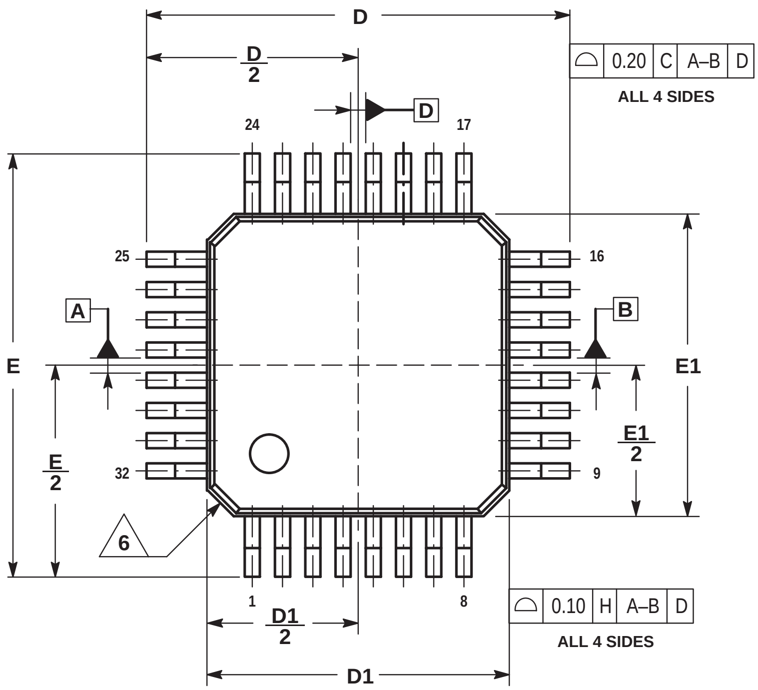
VECTOR TYPE STANDARD

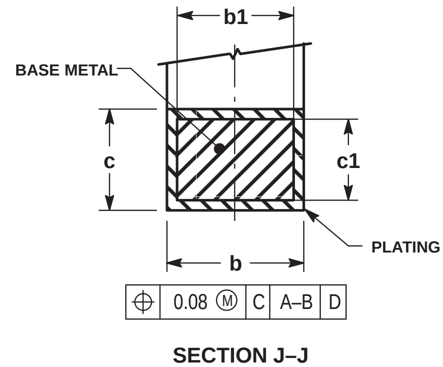
DATA RATE 6400/4
PAGER TYPE NUMERIC

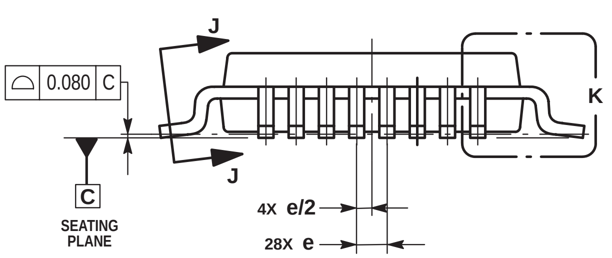
4. Connect V_{DD} (Pin 19 of Interface Connector) to the digital voltage supply (usually 3.0 V).
5. Connect the MC2800 to the Flex decoder MC68175 as shown in Table 6. For example, Pin 1 of MC2800 is connected to Pin 22 of MC68175 via the Interface Connector Pin 8.
6. Program the MCU such that it can generate the timing for the EN and CL Pins as shown in Figure 18.

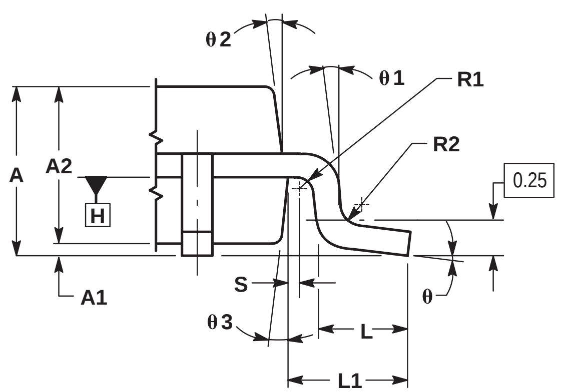
OUTLINE DIMENSIONS

FTA SUFFIX
PLASTIC PACKAGE
CASE 873C–01
(LQFP–32)
ISSUE A









NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	—–	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.18	0.27
b1	0.17	0.23
c	0.10	0.20
c1	0.09	0.16
D	7.00 BSC	
D1	5.00 BSC	
E	7.00 BSC	
E1	5.00 BSC	
e	0.50 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	—–
R2	0.08	0.20
S	0.20	—–
θ	0°	7°
θ1	0°	—–
θ2	11°	13°
θ3	11°	13°

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