AN1639

Phase Noise Measurement Using the Phase Lock Technique

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INTRODUCTION

This application note explains the phase locked loop (PLL) method of phase noise measurement. The PLL method shown in Figure 1 uses a diode ring mixer, OP–AMP based amplifiers, and a integrator to phase lock two signal sources. In the open loop state, there is a frequency difference between the sources which produces a beat at the mixer IF port. This is the reference level for the measurement. At phase lock, the beat disappears and 0 VDC is present at the IF port, along with all the phase noise of both sources. All test systems that measure low level phase noise use the PLL technique. Data presented in this application note was measured on a prototype phase noise measurement system. Additional information is listed in **References** at the end of this document.

Phase noise is the noise skirts that surround the carrier of any signal source. It may be caused by amplitude modulation (AM) or frequency modulation (FM). Due to amplitude limiting in oscillators, FM is the dominant cause of phase noise. Phase noise is measured in dBc/Hz (dB's relative to carrier in a 1 Hz noise bandwidth). When measured using the PLL technique, it is the level difference with corrections between the unlocked beat note power of two signal sources and the phase noise power density when phase locked. One of the sources must be voltage tunable. Since only the sum total of the noise can be viewed, it is assumed that either both sources have the same phase noise, or one has 10 dB or better phase noise than the other.

Figure 1 shows the block diagram of the system. A 1 MHz low pass filter removes the mixer sum product. The signal then passes to a dc coupled amplifier. Loop bandwidth is directly proportionate to gain in the dc coupled amplifier. Following the amplifier is an integrator. The integrator reset switch when momentarily closed sets the integrator output voltage to the same level as the positive input. This starts phase lock acquisition. When opened, the integrator output will slew to a voltage which forces its positive input to 0 V. An adder combines the integrator output (fine tune voltage), coarse tune voltage, and a noise test input. Usually coarse tune voltage is 0 – 10 V and fine tune voltage varies ±1 V. Noise input to the adder allows the loop bandwidth to be viewed at the loop bandwidth output. Adder output can tune any signal source that is voltage tunable.

Figure 2 shows the mixer LO to RF phase difference versus output voltage. At phase lock, mixer output is 0 V with an input phase difference of ±90°. This allows the mixer to operate at maximum sensitivity. The mixer IF port is fed to a Low Noise Amplifier (LNA), which at phase lock has no beat signals present. After a gain stage, the phase noise is viewed on a spectrum analyzer as shown in Figure 12. Phase lock at 90° or –90° depends on the tuning sense of the loop.

Motorola's newer PLL products (MC145xxx PLLs) are at or below the phase noise floor of many spectrum analyzers. Building a phase noise system provided portability, ease of use, and a cost reduction of an order of magnitude relative to commercially available units.

The system measures phase noise between offsets of 10 Hz and 1 MHz on signals between 10 MHz and 2 GHz. Design objectives are ±2.0 dB accuracy and a noise floor of –150 dBc/Hz at 10 Hz and –174 dBc/Hz at 10 kHz.

CORRECTION FACTORS

The reference beat note is measured with the LNA bypassed, to avoid overload. Therefore, LNA gain is subtracted from the noise level measured with it in circuit. Mixing signals down to dc, folds one sideband's noise into the other. Sideband noise is in phase, resulting in voltage addition. To account for folding, 6 dB is subtracted from the measured noise. If two equal phase noise sources are used, 3 dB is subtracted from the noise measured. This accounts for power addition. If one source is much lower than the other, no correction is made.

Analog spectrum analyzers without noise markers need correction for the effective noise bandwidth of their resolution bandwidth filters, noise response of peak detectors, and log amplifiers. These should be in the manual. Being able to manually add in the correction factors makes many old spectrum analyzers suitable. They need to tune the range of offset frequencies of interest and have a resolution bandwidth 10% to 20% of the lowest noise offset. Used HP141Ts have been seen selling for less than $1000.

If both sources are of equal phase noise and noise markers are used, then:

$$P_{SSB} = P_N - P_B - G_{LNA} - 9\ dB \qquad \textbf{(1)}$$

P_{SSB} is single sideband phase noise relative to carrier (dBc/Hz), P_N is the noise level measured (dBm/Hz), P_B is the power level of the beat (dBm), and G_{LNA} is the LNA gain (dB).

If the reference source has 10 dB lower noise than the VCO under test, then:

$$P_{SSB} = P_N - P_B - G_{LNA} - 6\ dB \qquad \textbf{(2)}$$

A low noise reference source is a convenience, to avoid simultaneous optimization of two VCOs or PLLs.

BEAT MEASUREMENT

Accurate noise measurement by comparison to a beat power level depends on the mixer beat's zero crossing slope (K_p) in Volts/Radian (V/rad) being equal to its peak voltage in volts. This is a reasonable assumption, if the second and third order beat harmonics are kept below –30 dB. Zero crossing slope is the conversion factor between radians of phase jitter and volts of noise output.

Figure 1. Phase Detector Noise Measurement

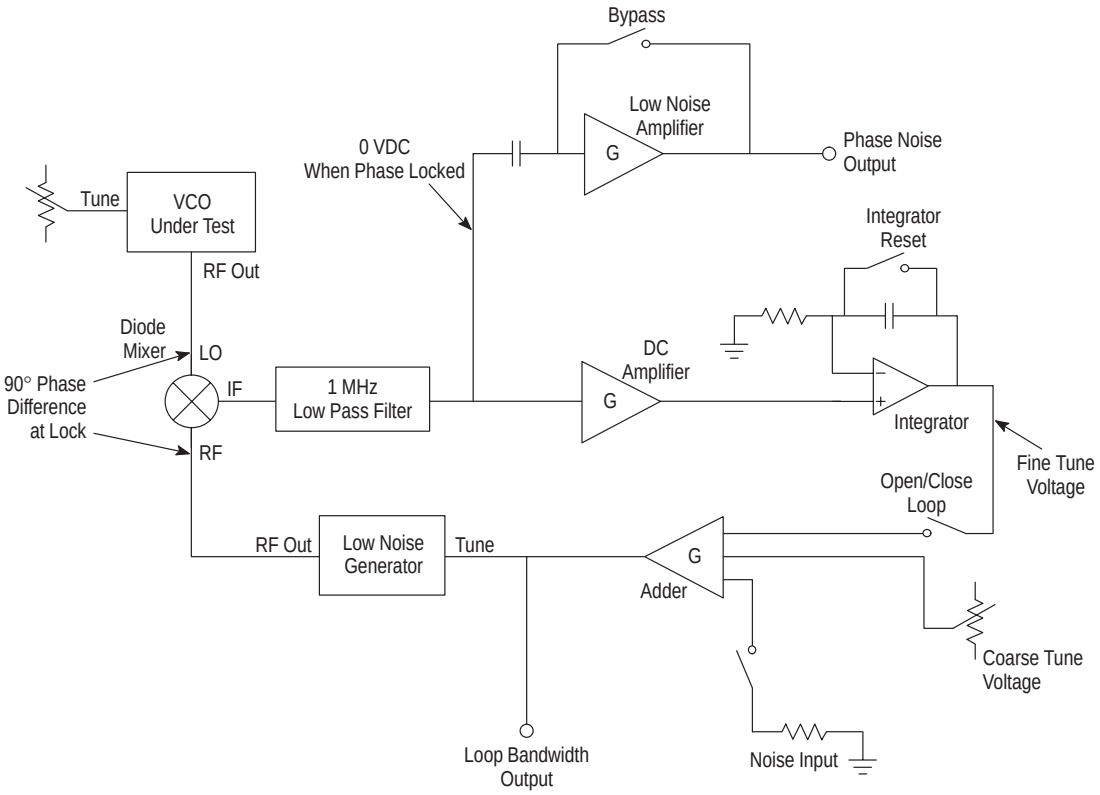
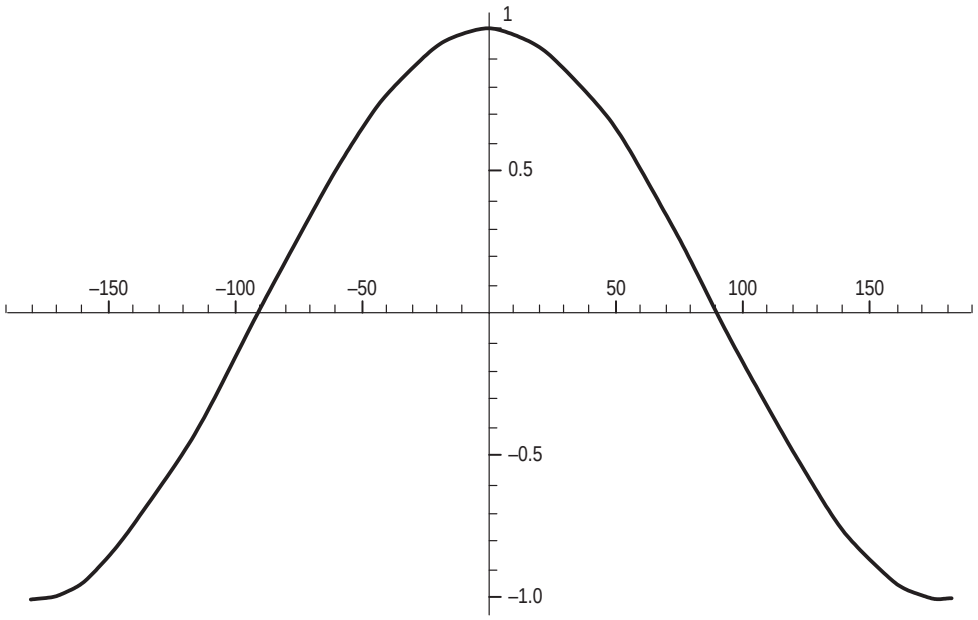


Figure 2. Mixer Output Voltage versus Phase Difference of Inputs



To use the phase noise formulas that assume sine wave beats with distorted beats, an equivalent sine wave power in dBm is computed from either the positive or negative zero crossing slope. Depending on polarity of tuning voltages and mixer phase, the loop will settle on either one. The beat slope in V/rad is:

$$K_p = \frac{T}{2\pi}\left(\frac{\Delta v}{\Delta t}\right) \quad \textbf{(3)}$$

T is the beat period, Δv is the voltage change, and Δt is the time change in a small region at the zero crossing. The equivalent beat power (dBm) is:

$$P_B = 10 + 20\,\mathrm{Log}\left|K_p\right| \quad \textbf{(4)}$$

$\left|K_p\right|$ is the absolute value of the zero crossing slope.

Zero crossing slope calibration allows higher mixer levels to be used to increase dynamic range. The mixer may be saturated without reducing measurement accuracy.

QUADRATURE VOLTAGE WINDOW

The straight line approximation of K_p relies on the identity $\sin\theta \cong \theta$ valid for small angles. Operating within ±10° of the zero crossing will keep the phase noise level error below 0.13 dB (1.5%), which is not significant. K_p is computed from an oscilloscope trace. The corresponding voltage window is:

$$\pm V_{max} = \pm 0.1745\left|K_p\right| \quad \textbf{(5)}$$

The radian equivalent of 10° is 0.1745. Two 13 dBm inputs to a mixer can produce 0.4 V/rad slope. The window would be ±70 mV at the mixer IF port.

LOOP BANDWIDTH AND DAMPING

Noise is suppressed within the loop bandwidth as shown in Figure 3. Without showing the intermediate steps and choosing the integrator time constant RC = 0.1, the loop bandwidth is:

$$LB = K_p G_L K_V \quad \textbf{(6)}$$

LB is in Hz, G_L is the loop gain in volts/volt, and K_V is VCO sensitivity in Hz/V. It is valid within 4.9% for loop bandwidths ≥7 Hz and 9.2% for bandwidths ≥5 Hz. By using a single mixer input level, K_pG_L can be combined into a Loop Bandwidth Factor (LF) which is multiplied by VCO gain to give the loop bandwidth. Typically, loop gain or LF is stepped in decade or half–decade steps to achieve the required loop bandwidths.

Again with RC = 0.1, the damping is:

$$\zeta = 0.396\sqrt{LB} \quad \textbf{(7)}$$

Damping is one or more at loop bandwidths of greater than or equal to 6.37 Hz ($\zeta \propto \sqrt{LB}$). Loop bandwidth or noise suppression can be quickly viewed by injecting thermal noise at the adder as shown in Figure 1.

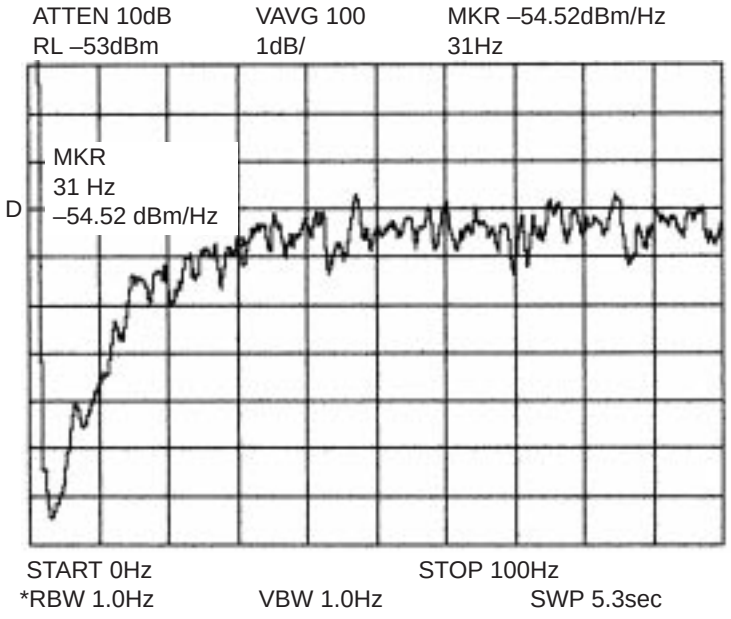
Suitable noise levels range from about 30 dB above the measurement noise floor up to the level at which the peak voltage is equal to the peak of the beat at the mixer IF. PLLs can only correct for noise voltages at the mixer output that are within the peak to peak voltage range of the beat. If it is exceeded, the PLL doesn't track and viewed noise is spectrally flat. VCOs can appear phase locked when overdriven with noise, since they track the time averaged voltage.

DYNAMIC RANGE

System dynamic range is the level difference between the beat and mixer, LNA noise floor with corrections. A 13 dBm LO and 13 dBm RF results in about 2 dBm at the IF beat. With thermal noise at –174 dBm/Hz and a perfect LNA, the noise floor could be –185 dBc/Hz. Low noise op amps currently available would limit that to –173 dBc/Hz at 10 Hz and –176 dBc/Hz at 1.0 kHz.

Phase noise can be amplified sufficiently to overcome the internal noise of any spectrum analyzer. LNA compression level on the board was set at 20 dBm. Spectrum analyzers are typically protected up to 1 W.

Figure 3. Check of PLL Phase Noise Suppression (Two Saber TCXOs) Within the Loop Bandwidth (0.5 dB corner is at 31 Hz)



Line related sidebands (60 Hz) are present in any signal source. The spectrum analyzer used (HP8563) requires suppression by greater than the LNA gain added, plus 6 dB or 9 dB. It has a 0 to –100 dBm/Hz level range with 10 dB of input attenuation for 10 to 600 Hz offsets. To see the ultimate system noise floor at 10 Hz, 60 Hz sidebands must be <–90 dB.

THERMAL NOISE PERFORMANCE CHECK

Control line voltage for the free running oscillator can be provided by a voltage divider. A known amount of thermal noise voltage (flat spectral density) is produced from the parallel equivalent of the two resistors. The RMS noise voltage is:

$$V_n = \sqrt{4KTR} \quad \textbf{(8)}$$

V_n is measured in V/$\sqrt{Hz}$, K is Boltzmans constant (1.38 x 10^{-23} Joules/°K), T is temperature in degrees Kelvin (25°C = 298°K), and R is resistance in Ω. Resistor dividers tied to the supply voltage pick up 60 Hz along with other spurs. An amplified noise diode avoids this problem.

Noise generator power P_n (W/Hz) is converted to V_n. R below is the spectrum analyzer load (R = 50 Ω):

$$V_n = \sqrt{P_n R} \quad \textbf{(9)}$$

Most current spectrum analyzers can measure directly in V/$\sqrt{Hz}$, however for those that can't (assuming a 50 Ω load):

$$V_n = 0.2236\left(10^{PdBm/20}\right) \quad \textbf{(10)}$$

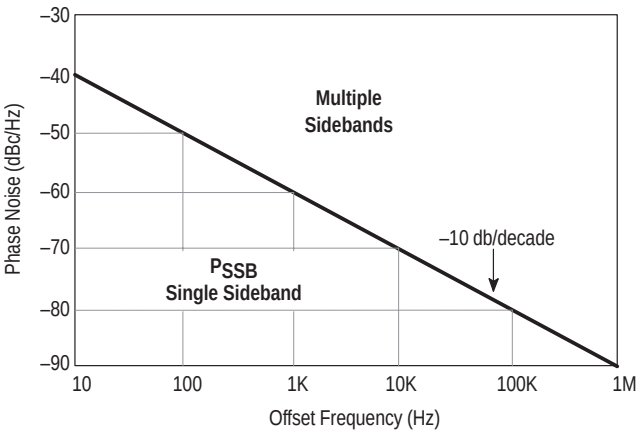
PdBm is the noise power in dBm/Hz. A typical noise source with an op–amp output has very low output impedance. V_n is the same with or without a 50 Ω load. The phase noise level (dBc/Hz) for a given thermal noise voltage is:

$$P_{SSB} = 20\,Log\left(K_V V_n\right) - 3.01 - 20\,Log\,(f) \quad \textbf{(11)}$$

This assumes narrowband FM modulation where only the first sideband pair is significant. f is offset frequency in Hz and K_V is VCO gain in Hz/V. Refer to Figure 4 when checking for single sideband modulation.

A 50 Ω resistor has noise of 0.9 nV/$\sqrt{Hz}$. If it modulates a 3 MHz/V VCO, the phase noise will be –74 dBc/Hz at 10 Hz and –134 dBc/Hz at 10 kHz. Small amounts of noise have a big effect on a VCO.

Figure 4. Single Sideband Modulation



By using metal film resistors to avoid introducing other types of noise and looking at offsets below the modulation bandwidth of the VCO, an accurate performance check can be made. All sources have low pass filtering on the tune line that rolls off the noise at higher offsets.

PERFORMANCE BENCHMARK

The design goal was to be able to measure the best 10 MHz oven oscillator that could be found. Noise performance of a unit available from Wenzel Associates was quoted as:

Offset	Phase Noise (dBc/Hz)
10 Hz	–144
100 Hz	–164
1000 Hz	–168
10 kHz	–168

System noise floor measured at 1.0 GHz with 13 dBm levels was:

Offset	Phase Noise (dBc/Hz)
10 Hz	–143
100 Hz	–153
1 kHz	–163
10 kHz	–170
100 kHz	–174
1 MHz	–170

Modifications are being made to reduce the noise floor.

SOURCE MODULATION BANDWIDTH

Filtering on the tune line of a controlled source, adds a pole to the PLL. As loop bandwidth is increased this pole will become visible as peaking at the corner frequency of the PLL response to injected noise. Normally it is an overdamped response. If visible, restrict the PLL to more narrow bandwidths. To see close in phase noise usually the lowest loop bandwidth that maintains phase lock is used even without this limitation.

HIGH SOURCE PHASE NOISE

Peaking in the loop response to injected noise can be caused by high phase noise on the input signals. This will occur at the corner frequency. If noise peaking becomes visible as loop bandwidth is decreased, source noise is too high.

Use only loop bandwidths that are high enough to remove the peaking. Noise injected for loop bandwidth measurement has a flat spectral density. As loop bandwidth decreases the increasing phase noise at lower offset frequencies becomes visible.

INJECTION LOCKING

Injection locking occurs when small amounts of power coupled from one oscillator to the other causes phase lock between them. If the PLL is open loop and the sources are tuned towards each other, injection locking bandwidth is the frequency of the beatnote just before it disappears. Adding amplifiers and step attenuators to the signal paths greatly

reduces the problem. Also it helps to use high Q sources. The mixer alone has a minimum 25 dB, typical 40 dB of isolation.

Use a minimum loop bandwidth of twice the injection locking bandwidth to maintain phase lock. For best accuracy a loop bandwidth of four times the injection locking bandwidth may be needed.

SECOND ORDER LOOP CAPTURE AND TRACKING

To phase lock a source, a switch across the integrator capacitor in Figure 1 is closed and opened. This resets the Integrator output to zero. Without shorting the integrator it's output would be at one of the supply rails from integrating internal offsets. The capture and tracking range (Peak Tuning Range or PTR) of the voltage controlled source (second order loop) is:

$$PTR = \left[\frac{V_{max} - V_{min}}{2}\right] K_V \qquad \textbf{(12)}$$

V_{min} to V_{max} is the PLL voltage tuning range. If the VCO is tuned well beyond its PTR, the PLL will always shift it in the direction to minimize the beat frequency. Loop bandwidth (loop gain) does not affect the capture range, but it does determine the speed of lock acquisition. It is best to acquire the lock at a wide loop bandwidth and step down the loop bandwidth as needed. For stability, the loop bandwidth must be kept well below the tuned source modulation bandwidth.

Phase lock will always occur if the tuned source can be shifted by the beat frequency with a 1 V change in tuning voltage. This applies to beats up to 1 MHz (mixer filter bandwidth) and assumes a ±1 V fine tune voltage range. If there is not enough source tune range, the PLL will minimize the beat frequency within its ±1 V fine tune range. There is also a 0 V to 10 V coarse tune voltage which is summed with the fine tune voltage to control the VCO. Looking at a beat, the PLL is open loop so only the coarse tune voltage is present.

FIRST ORDER LOOP CAPTURE AND TRACKING

Shorting the integrator capacitor makes the PLL first order. PTR can be found using the second order formula with V_{min}, V_{max} being redefined as the peak voltages of the beat at the VCO tune port. The peak voltage depends on loop gain. PTR is the capture range, tracking range and is equal to the loop bandwidth.

Phase noise measurement at low offset frequencies requires stable sources. VCOs are best measured after they have been phase locked to a voltage tunable crystal reference.

SINGLE SOURCE METHOD

There are systems that use the single source delay line discriminator method. The single source RF output is split with part going to the mixer through a phase shifter and the rest to the other port through a delay line. Adjusting the phase shifter on one input establishes quadrature.

The fixed delay time of the delay line converts frequency fluctuations at its input to phase fluctuations at its output. A mixer converts the phase fluctuations to voltage fluctuations. Voltage fluctuations are phase noise and are measured. In practice the systems provide poor phase noise dynamic range. The longest delay line offers the best sensitivity close to carrier. However, at offsets further out, there are nulls which move closer to the carrier as the line is lengthened.

Single source systems promote their speed and simplicity. However, phase noise specs should be guaranteed by design.

HIGH FREQUENCY LNA FLATNESS

In any phase noise measurement there is an offset where the source phase noise goes below its thermal noise floor. Above this point the noise output of the LNA should be perfectly flat. When viewed, its non–flatness shows the system response to noise at high offsets.

This test is best with source phase noise that drops off fast but has thermal noise well above the system noise floor.

NOISE FLOOR TEST

Noise floor is measured as shown in Figure 5 by driving both mixer inputs from one source with a splitter. One leg goes directly to the mixer while the other passes through a delay line. Delay line length is adjusted for quadrature at the mixer output. Source phase noise will be correlated and will not appear at the LNA output. Measured noise will be the system noise floor.

Calibration is performed by substituting a signal of equal level and slight frequency offset on one side of the mixer as in Figure 6. This produces a beat note. The equations used when measuring signal sources are also used here.

Figure 5. System Noise Floor or Signal Processing Component Measurement

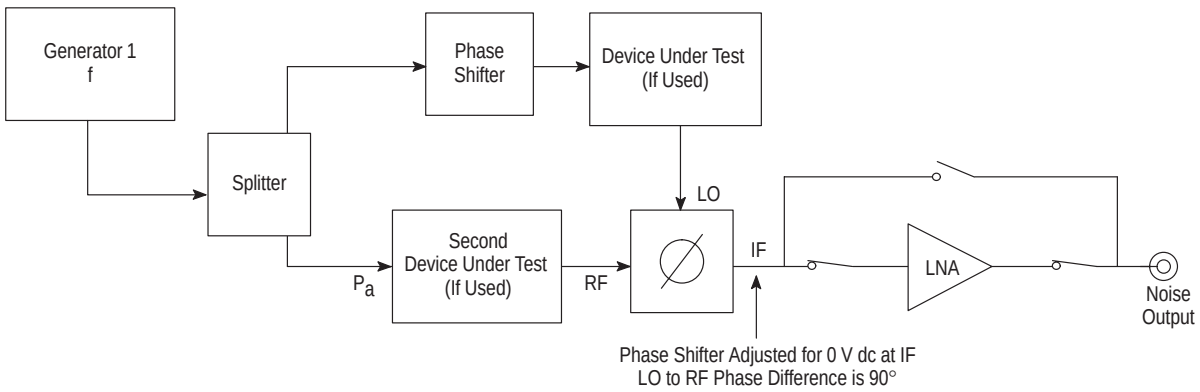
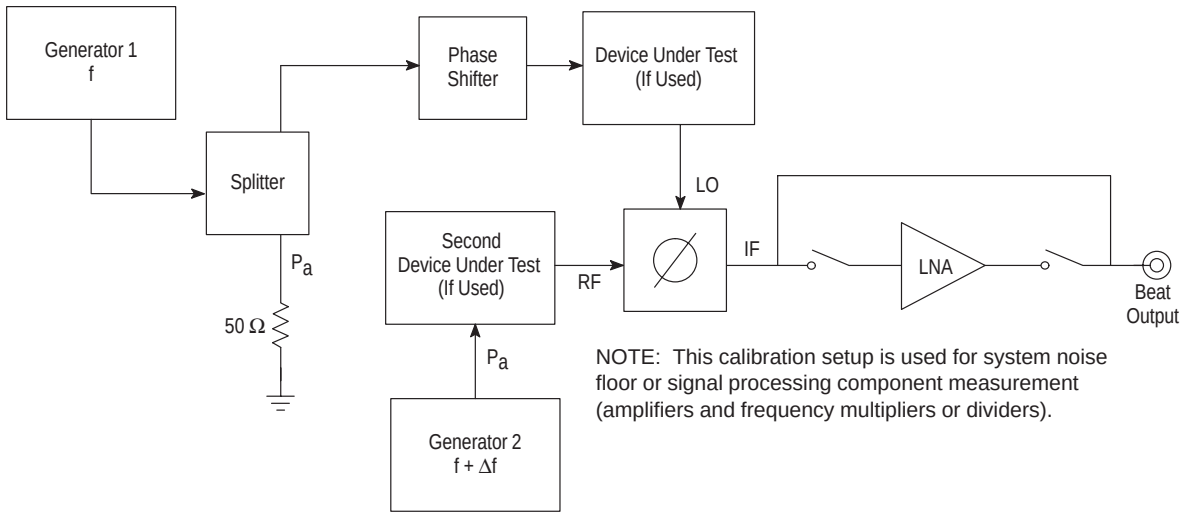


Figure 6. Phase Noise Calibration



NOTE: This calibration setup is used for system noise floor or signal processing component measurement (amplifiers and frequency multipliers or dividers).

TUNE PORT NOISE

Noise due to the system tuning circuits, limits the measurement floor when tuning VCOs. As shown in Figure 7, the thermal noise of a 50 Ω resistor modulating a 5 MHz/V VCO results in –70 dBc/Hz at 10 Hz declining by 20 dB/decade. With a limit of –130 dBc/Hz at 10 kHz offset, any low noise VCO will have to be locked to a low tune sensitivity source.

Tune circuit noise is measured at the PLL's tune port with no signals at the mixer RF and LO inputs and the integrator shorted (to avoid integration of offsets). The same noise levels are present when the PLL is phase locked without shorting the integrator. Typically, tune noise is spectrally flat with some increase at high loop gain. To achieve narrow loop bandwidths, attenuation rather than gain is used for almost all measurements. On the prototype, –140 dBm/Hz has been achieved. Converting to RMS noise voltage the phase noise floor is computed. Phase locking to a 5 Hz/V TCXO instead of a 5 MHz/V VCO improves the tune noise floor by 120 dB.

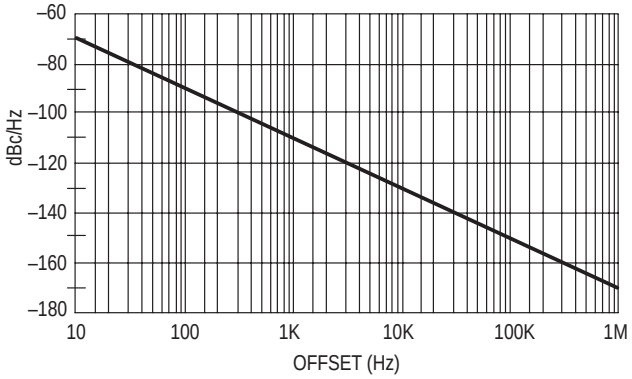
Power supply noise frequency modulates a VCO in the same manner as noise on the tune line. In this case, the VCO gain (K_V) is the pushing factor or change in frequency for a small change in supply voltage ($\Delta f/\Delta V$). All regulator data sheets that the author is aware of quote total noise summed over a given bandwidth rather than noise density. Until this changes, the level needs to be measured. Popular devices such as the LM317 regulator can have noise levels of 280 nV/$\sqrt{Hz}$, not including their 1/f characteristic. They may be used to build noise generators (this has not been tried).

SIGNAL PROCESSING COMPONENTS

Amplifiers, frequency multipliers and dividers or any other signal processing component can be measured by calibrating to a substitute signal of equal level and slight frequency offset. Devices which do not frequency translate can be tested singly or in pairs. Frequency translation devices must be tested in pairs.

A single device under test (DUT) has the same 6 dB correction factor as the phase locked technique with one source of much better noise than the other. A pair of DUTs has the 9 dB correction factor of two equal noise phase locked sources.

Figure 7. Phase Noise of a 5 MHz/V VCO Modulated by 50 Ω (0.9 nV/$\sqrt{Hz}$)



SINGLE SIDEBAND PHASE NOISE

Phase noise is the product of either a single noise sideband or multiple sidebands. This is similar to wideband or narrowband FM.

If the total peak phase deviations are much less than 1 radian, phase noise will be composed of one significant sideband. Figure 4 shows the noise levels representing 0.2 radians of peak phase deviation integrated over any one decade of offset frequency.

Below the line phase noise is single sideband while above increasingly it becomes multi sideband. High levels of phase noise can be above the carrier power, typically at low offsets.

TYPICAL SYSTEM FEATURES

- GaAs amplifiers and step attenuators to set proper levels.
- A noise generator for loop suppression and noise modulated performance checks.
- A low dc drift tuning loop capable of capturing signals separated by 1 MHz and driving generators such as the HP8662. Tuning voltage of 0 V to 10 V with ±1 V phase lock range.
- Low noise floor and 2 dB accuracy.

- Two TCXOs and two high frequency VCOs to check system function.
- 10 MHz –2 GHz frequency range.

A prototype's LNA noise floor is shown in Figure 8, noise source output is shown in Figure 9, and system noise floor is shown in Figure 10. The prototype was built on a single board about 10 inches x 10 inches.

EQUIPMENT NEEDED

- An oscilloscope to monitor phase lock and possibly zero crossing beat slope.
- A spectrum analyzer with a low enough frequency limit and appropriate resolution bandwidth. An HP8563 was used for the sample plots.
- 15 V and –15 V, 1 amp power supply.

SAMPLE MEASUREMENT

A Motorola Saber TCXO was measured:

Offset Frequency	Phase Noise (dBc/Hz)
50 Hz	–108.9
100 Hz	–116.4
1 kHz	–137.5
10 kHz	–148.1

Beat and spurious product levels are shown in Figure 11. Since the worst case spurious beat product was suppressed better than 30 dB, noise levels were measured with delta markers relative to the beat. The 0.5 dB corner frequency of loop bandwidth is 31 Hz, as shown in Figure 3. Figure 12 shows the 50 Hz phase noise.

SIGNAL GENERATORS

A signal generator while convenient has disadvantages. If tuned it needs dc FM achieved by analog means. All three such generators (with low close in noise) that the author is aware of, guarantee their phase noise specifications only if the 10 MHz reference is tuned. Tune range is only a few Hz.

It is better to use the generator as the free running source. The concern then is whether the device under test has more noise, less noise, or similar noise relative to the specifications of the generator.

It is easier to phase lock two of the sources under test and assume they are the same. Generally, this is true and two can be optimized at the same time. To measure the exact noise of each, use three sources and make three measurements (all three combinations). Three equations are solved for the three unknowns.

The MC145230EVK (a Motorola PLL evaluation kit) has been designed for two source phase locking. Each kit has a dual PLL with a dc tune input for the crystal reference. The control software can program four boards simultaneously through one PC printer port. To measure phase noise, one crystal reference is phase locked to the other. Due to high resonator Q and low tuning sensitivity, system generated tune line noise and injection locking can be ignored.

MEASUREMENT BLOCK DIAGRAM

Figure 13 is a block diagram of all the steps to make a valid measurement. Often many steps can be dropped. Phase locking two crystal stabilized sources greatly reduces tune port noise and injection locking bandwidth. The unlocked beat will not drift. Noise injection to measure the resulting phase noise and comparison with the computed value is to build confidence in the system accuracy.

REFERENCES

1. Product Note 11729B–1, *Phase Noise Characterization of Microwave Oscillators–Phase Detector Method,* Hewlett Packard, March 1984.
2. Jeff Hinderer, Crystal oscillator noise measurement notes, Wenzel Associates, 1992.
3. Harold T. McAleer, *A New Look at the Phased Locked Oscillator,* IRE Proceedings, June 1959.
4. Application Note 93–0002, *PN–9000 Automated Phase Noise Measurement System,* Comstron 1993.

Figure 8. LNA Noise Floor When Using 60 dB of Gain
(–163.9 dBm/Hz at 10 Hz)

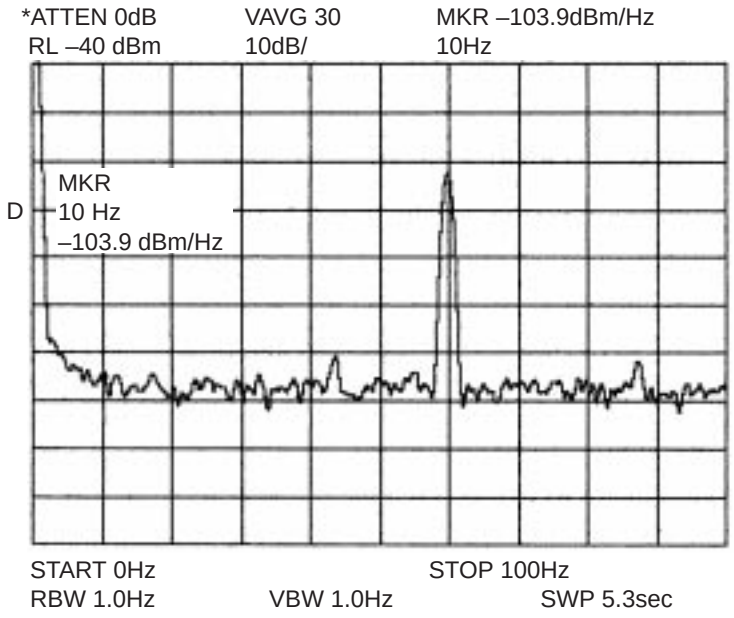


Figure 9. Noise Source Output Used to Measure Loop Suppression Bandwidth

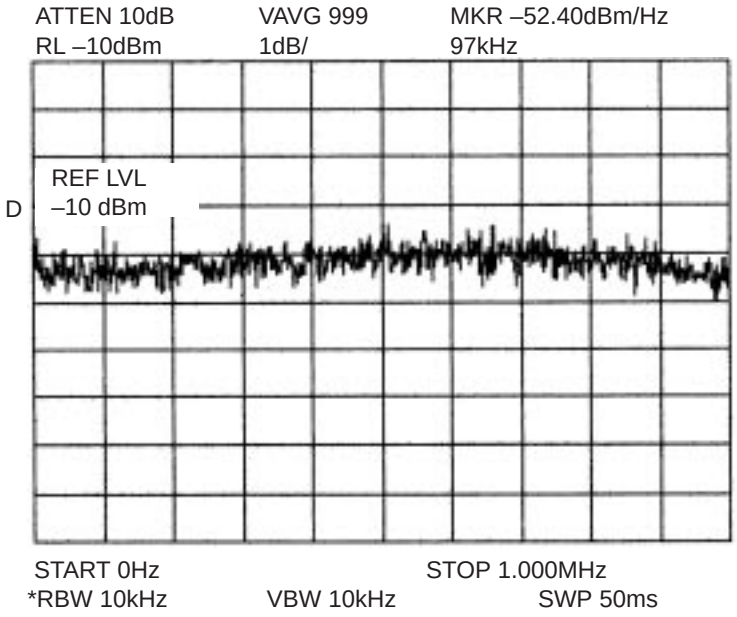


Figure 10. System Noise Floor
Phase noise is –142.9 dBc/Hz at 10 Hz offset with
13 dBm input levels at 1 GHz. LNA gain is 60 dB.

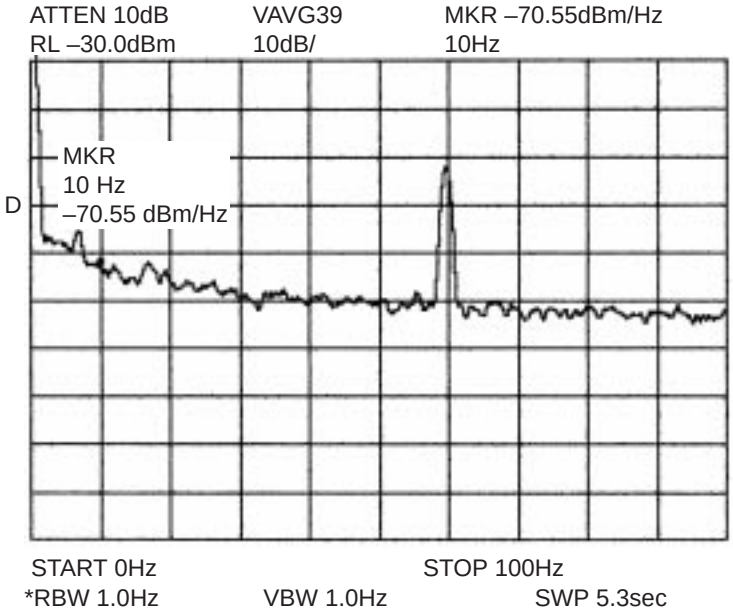


Figure 11. Beat Analysis for Saber TCXO Measurement
The highest level harmonic is the third at –38 db. Therefore,
spectrum analyzer delta markers can be used for calibration.

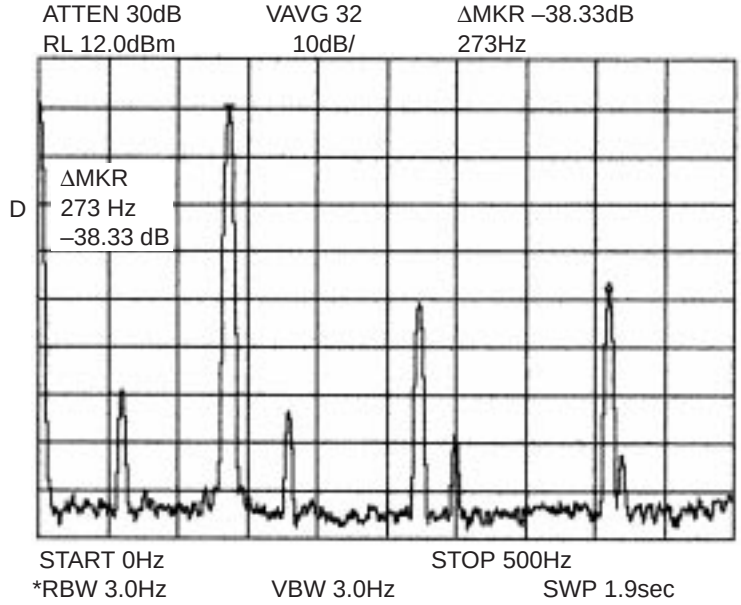


Figure 12. Phase Noise at 50 Hz Offset of Two Saber TCXOs
Loop bandwidth is 31 Hz and 40 dB LNA gain is used. Phase noise (–108.9 dBc/Hz) was measured with a delta marker to the beat.

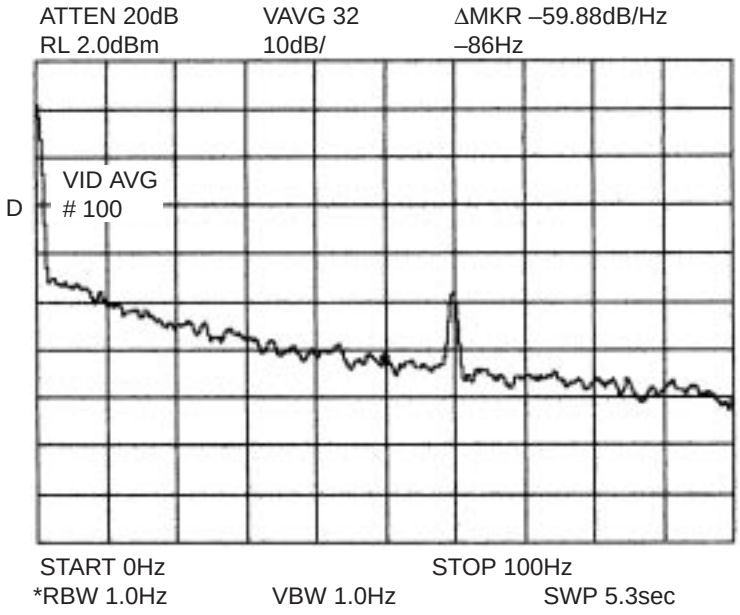
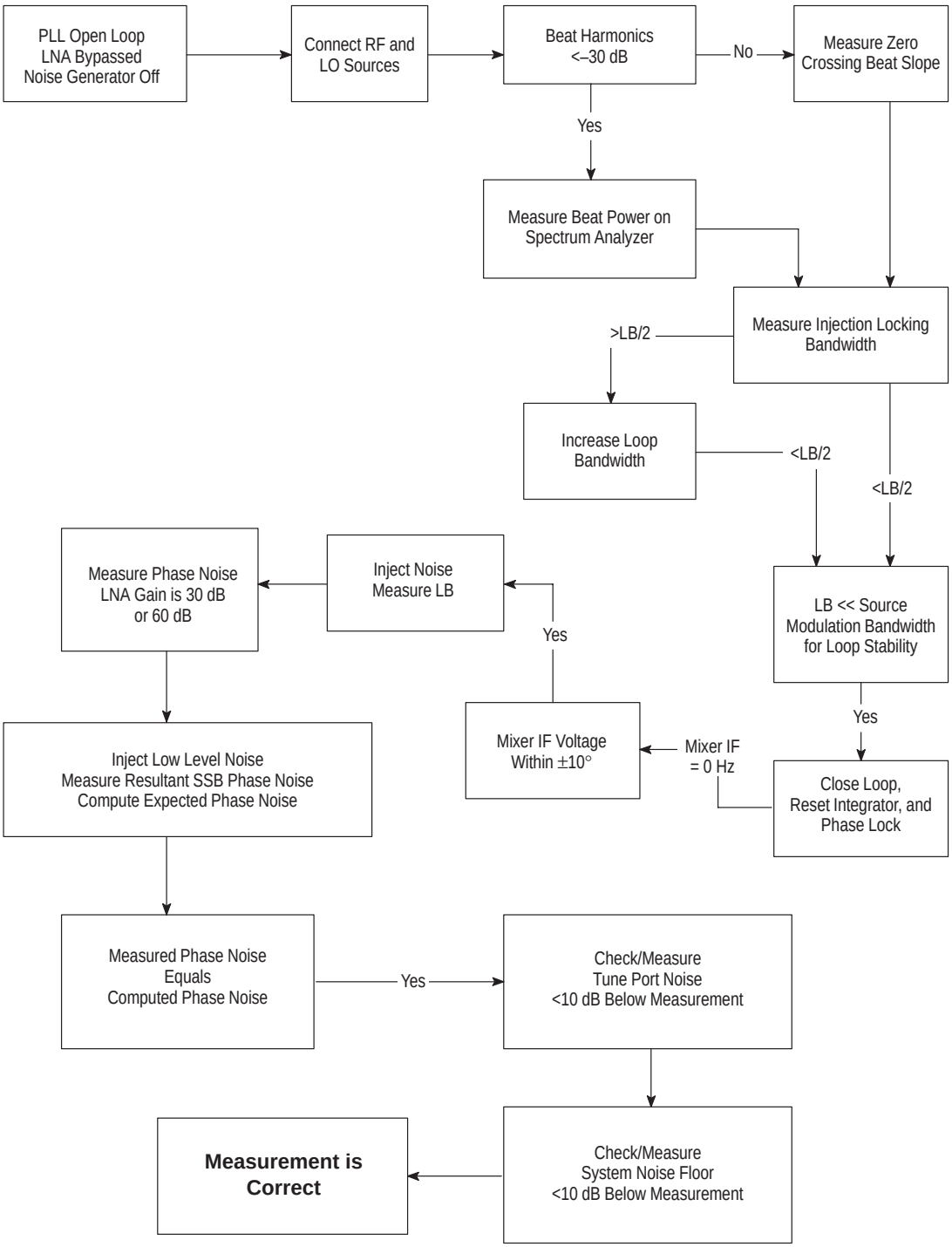


Figure 13. Measurement Steps to Ensure Valid Measurements



NOTE: LB is the desired loop bandwidth in Hz.

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