

Intel® Embedded Development Board Mini-ITX Carrier

Carrier Board Schematics supporting Intel® Embedded
Development Board Compute Modules

January 2011

Revision 001



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Revision History

Document Number	Revision Number	Description	Revision Date
324768	001	Initial release.	January 2011

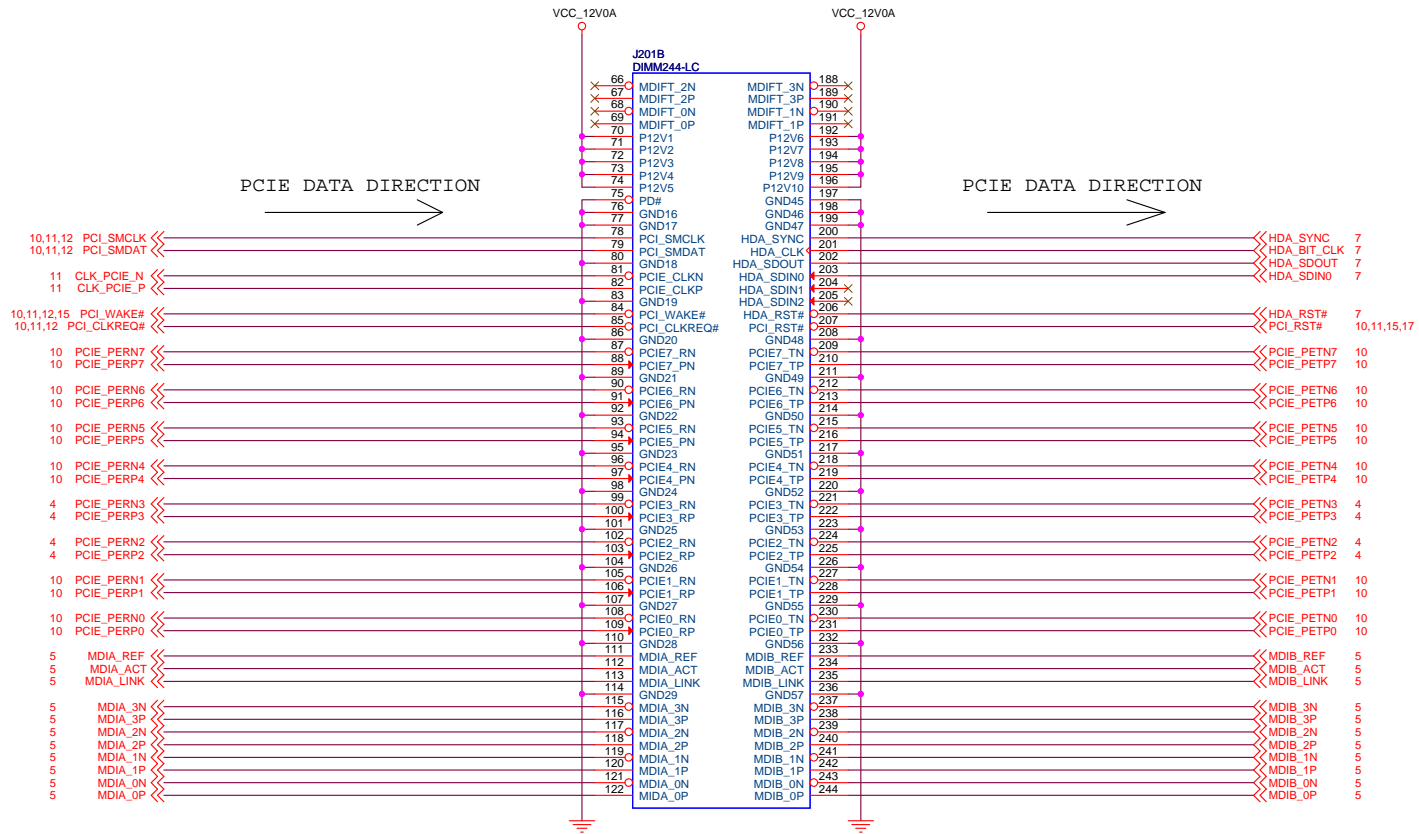
INTEL CORPORATION

Embedded & Communications Group

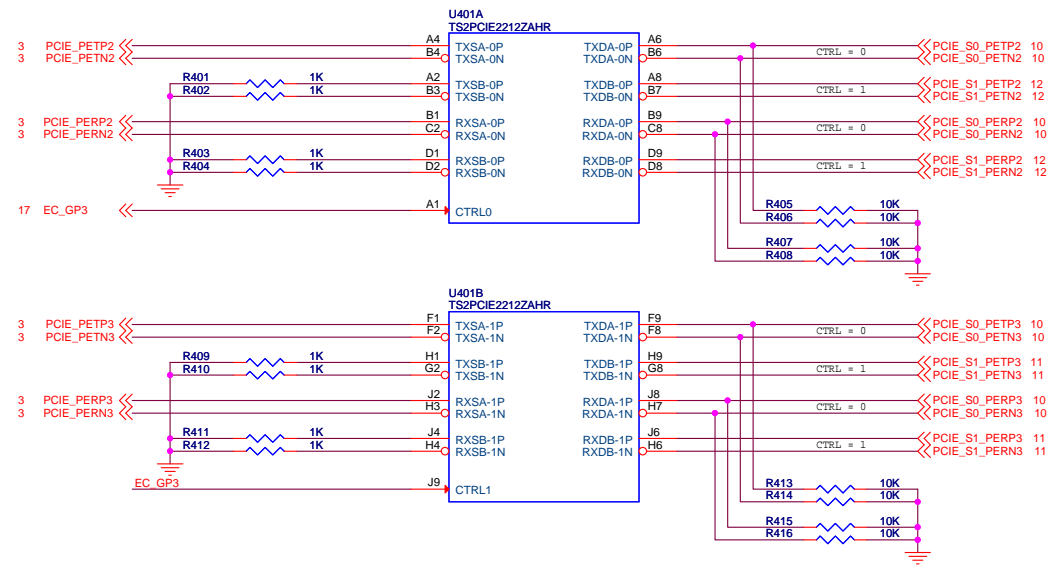
Intel® Embedded Development Board -Mini-ITX Carrier Schematics - Revision: B

Note: Development Boards will be marked with Viking Modular Solutions*

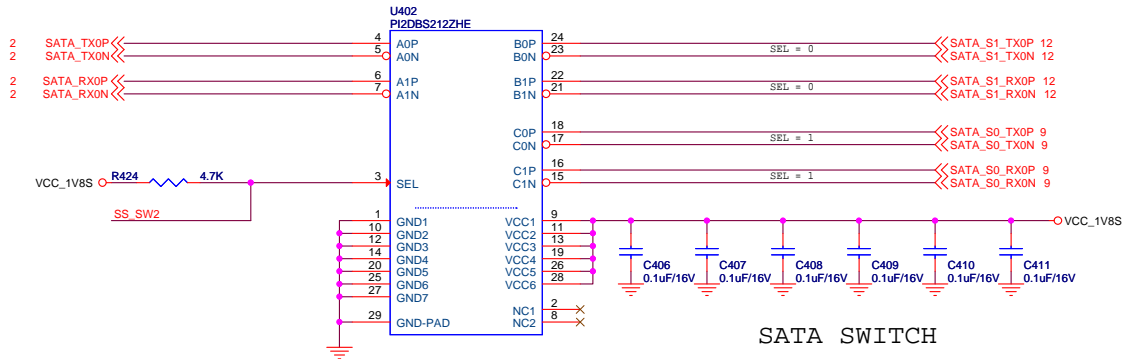
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Title ITX Carrier Schematics		
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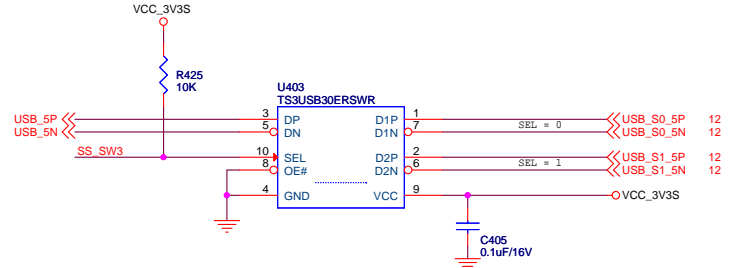
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Title: MiniDIMM 2 of 2		
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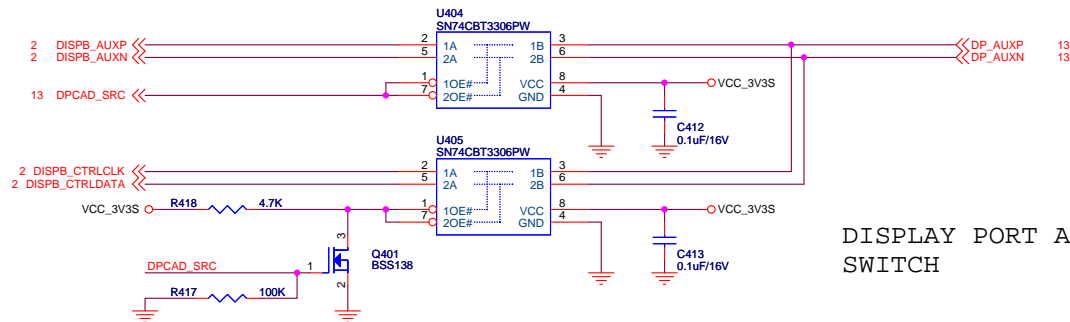
PCI EXPRESS SWITCH



SATA SWITCH

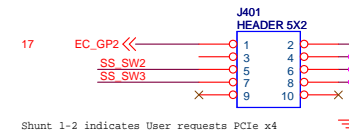


USB SWITCH



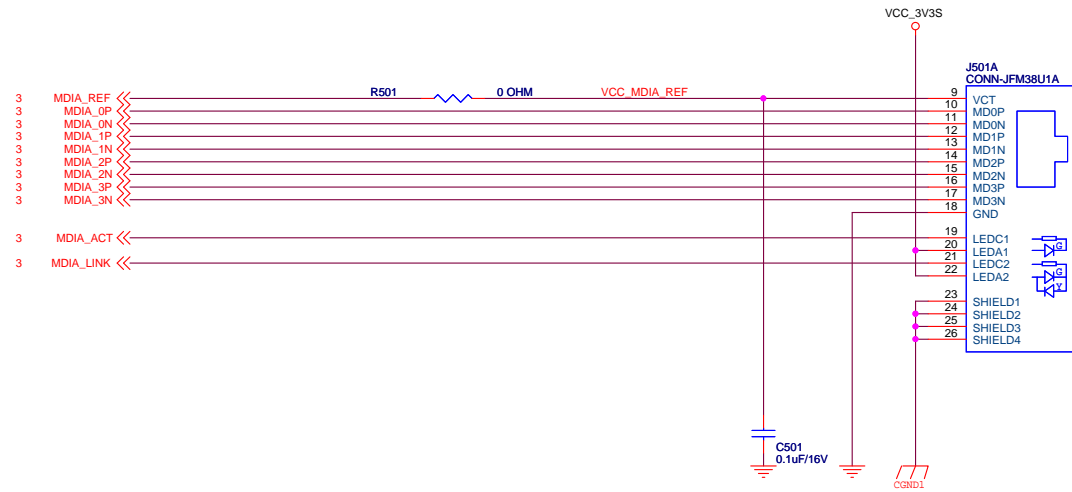
DISPLAY PORT AUX SWITCH

SWITCH SELECT JUMPER

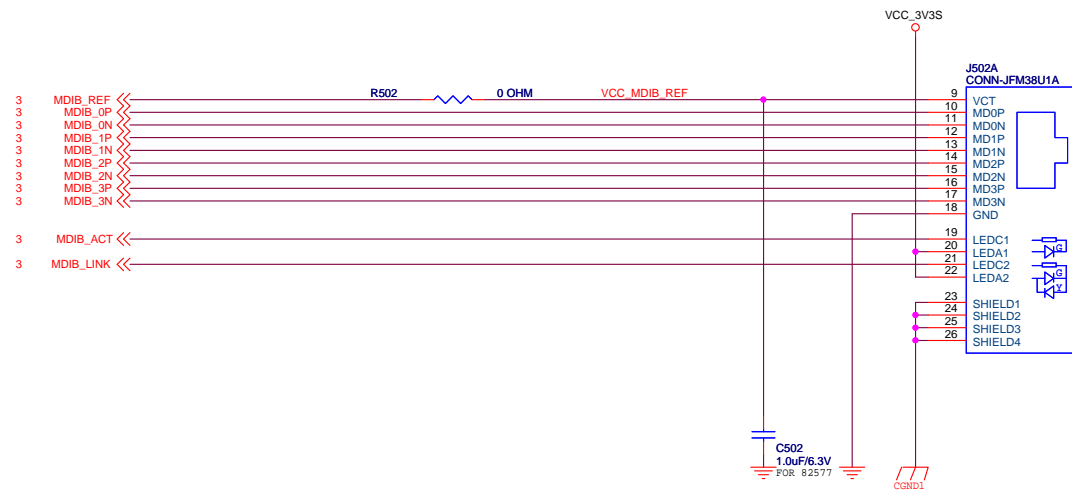


Shunt 1-2 indicates User requests PCIe x4
 No shunt (default) indicates mPCIe may be used
 (See user guide Doc#324421 for detailed description of jumper settings and system configurations)

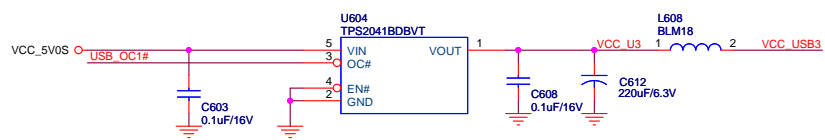
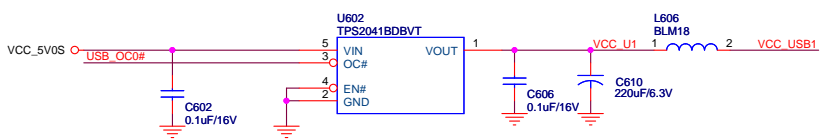
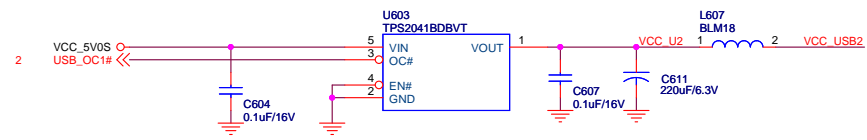
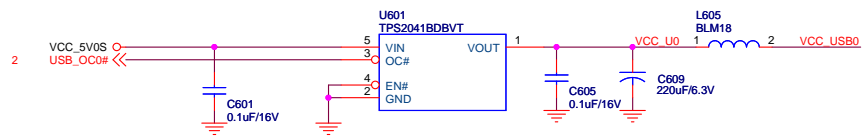
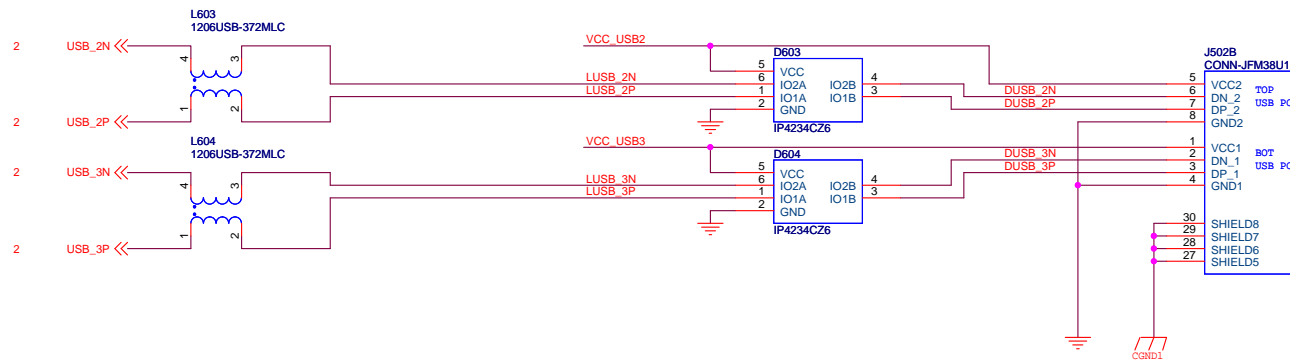
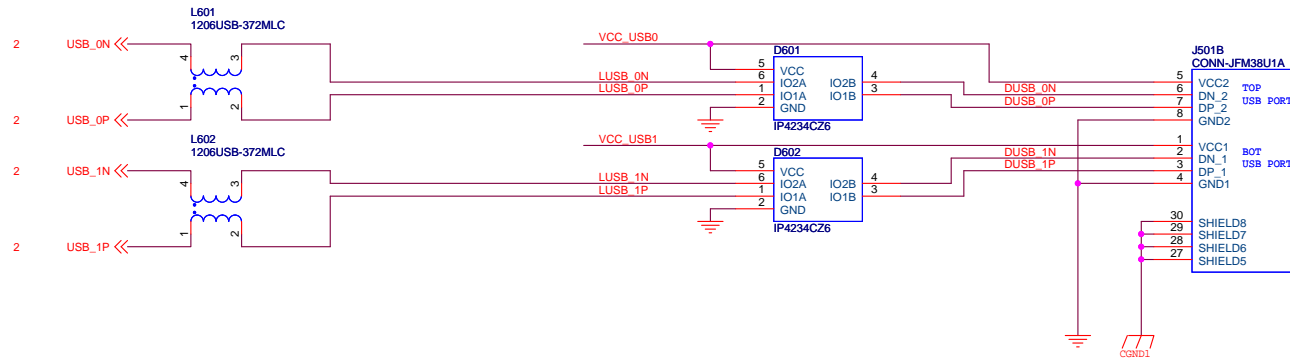
EMP-CAI-CAP-IAQ-Intel		
Title: Switches		
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Reference Design Note:
 Selected RJ-45 jacks include integrated Magnetics
 and must be supported by the MAC/Phy on the
 compute module per supplier design guidelines.

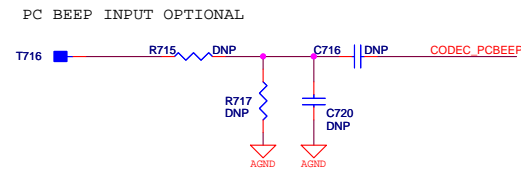
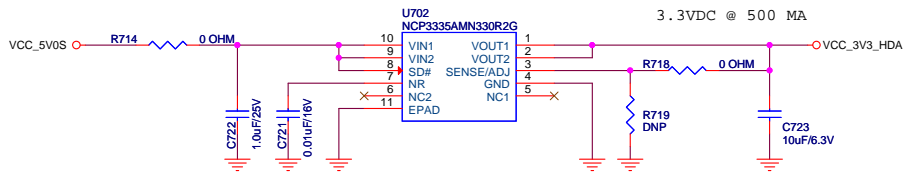
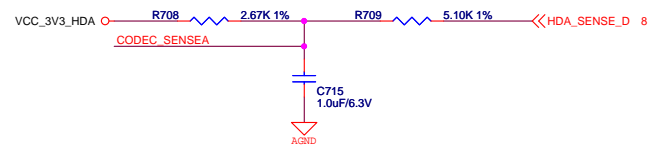
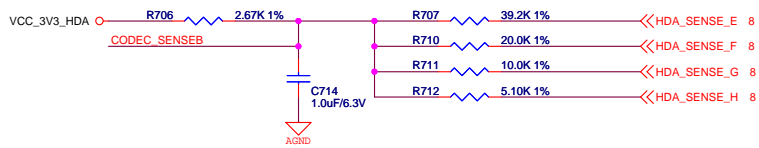
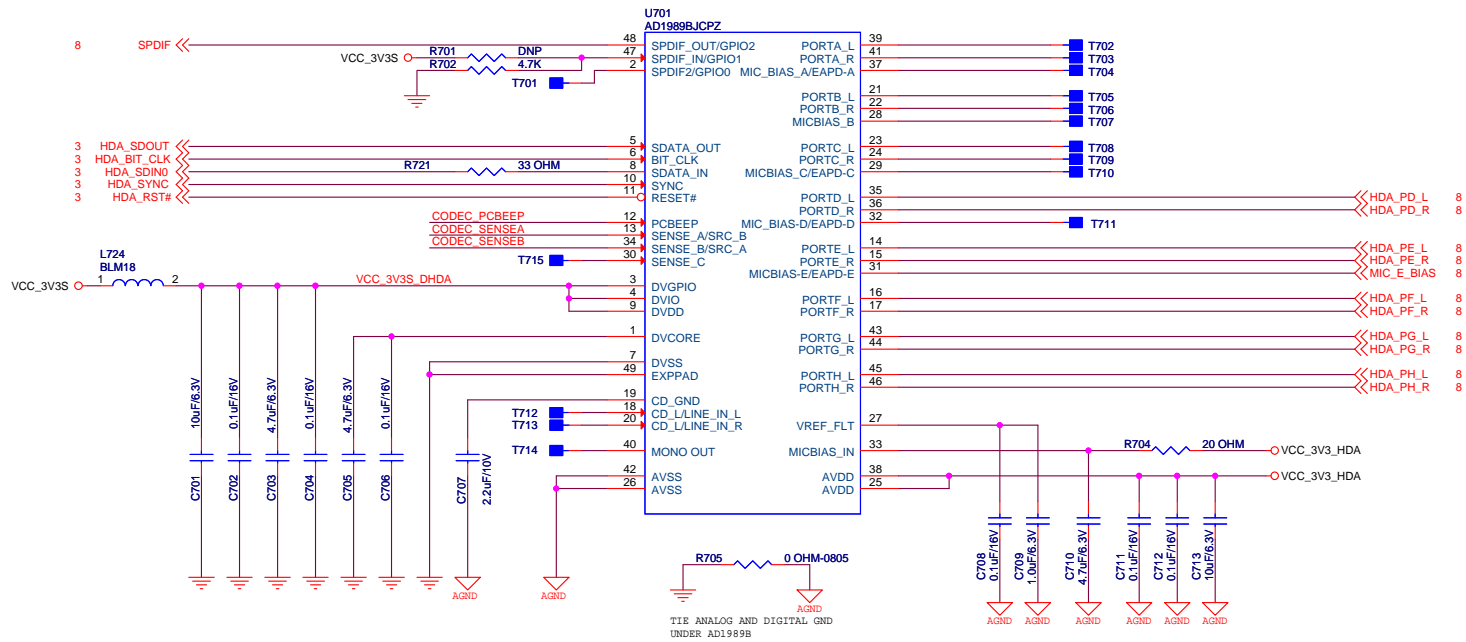


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Title RJ-45		
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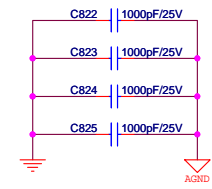
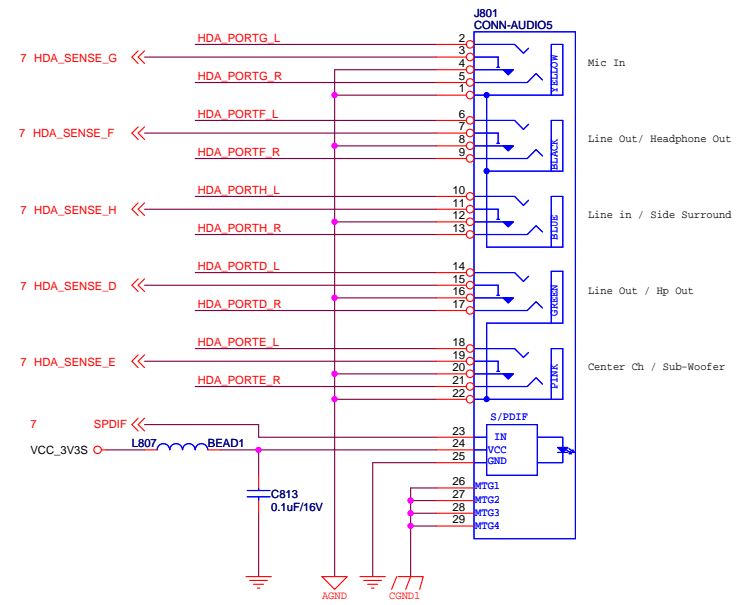
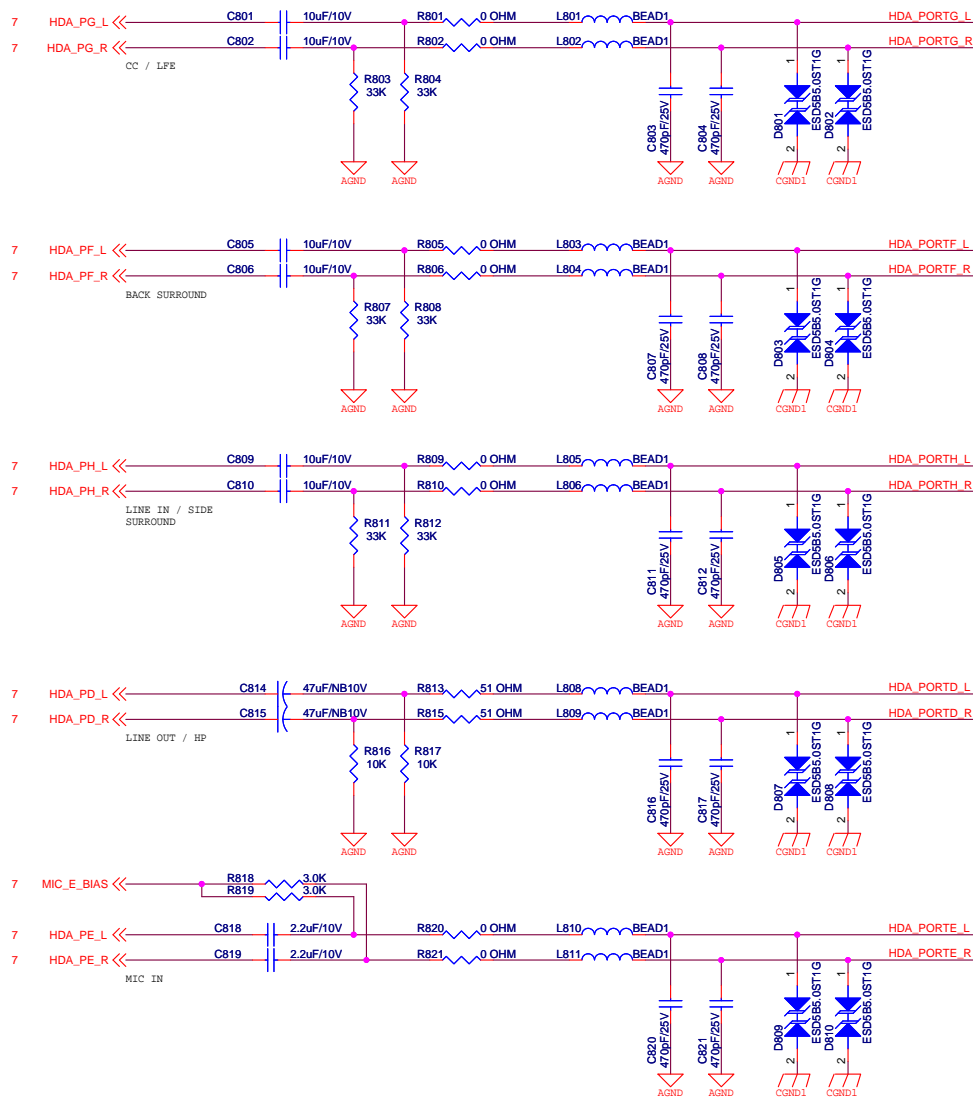
7.1 SURROUND HIGH DEFINITION AUDIO CODEC



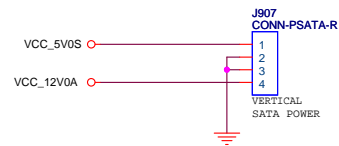
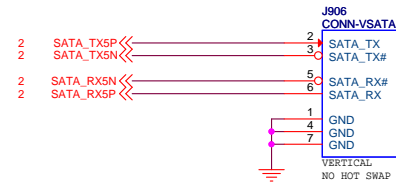
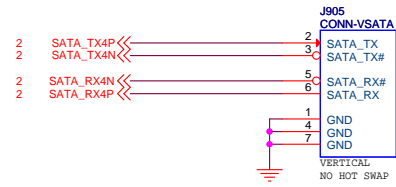
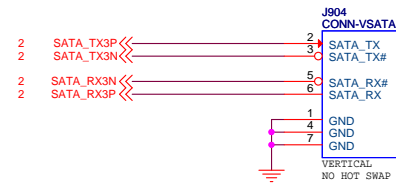
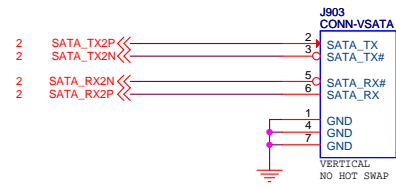
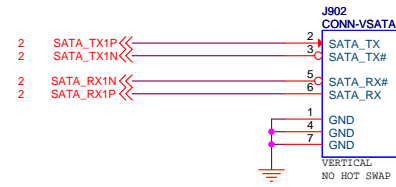
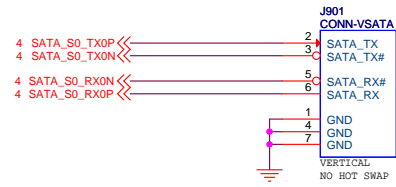
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Title: HD Audio Codec		
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HD AUDIO CONNECTORS

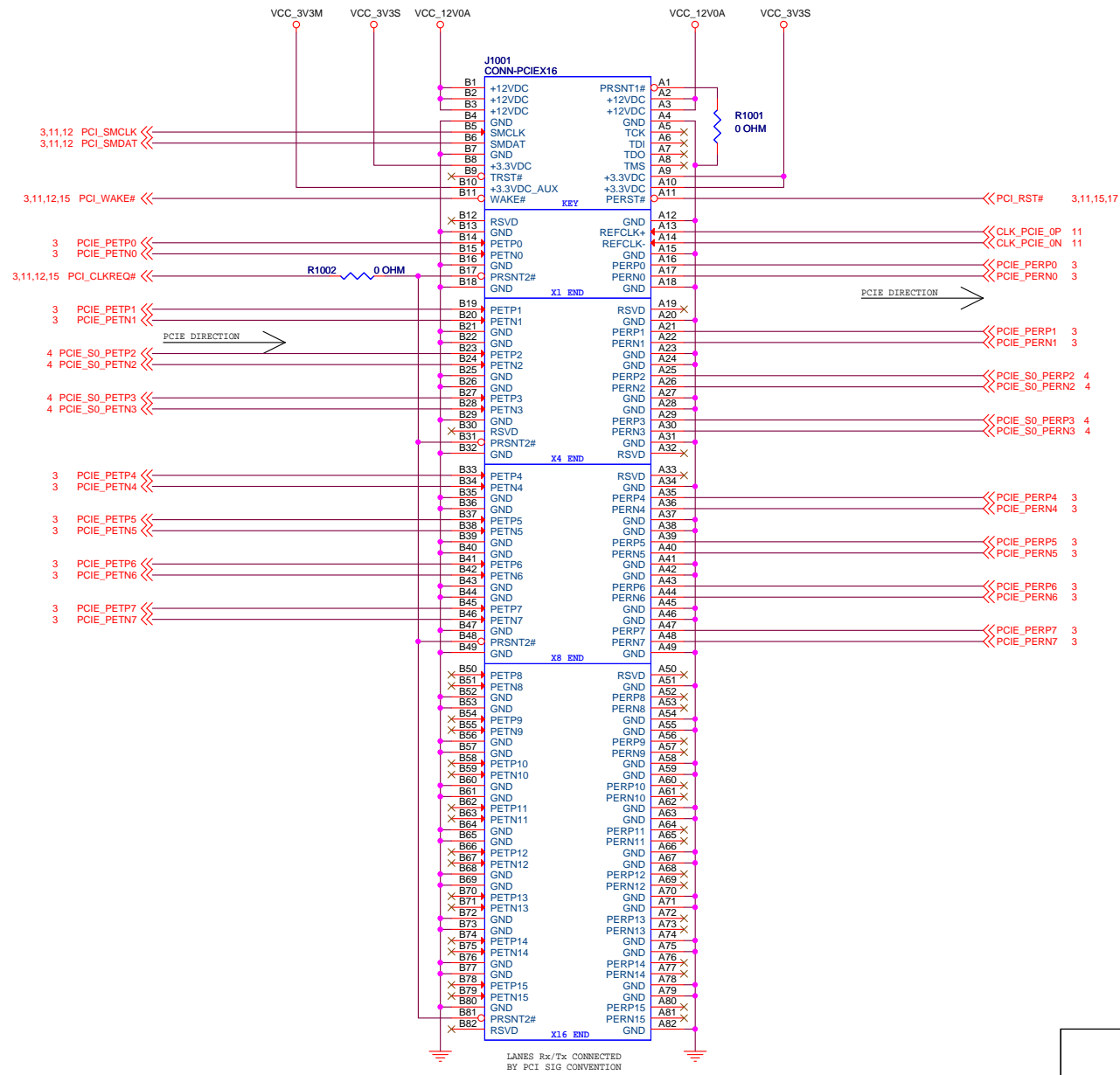
Note: Mapping of HD Audio Function to Colors does not follow typical PC mapping - See color notes below



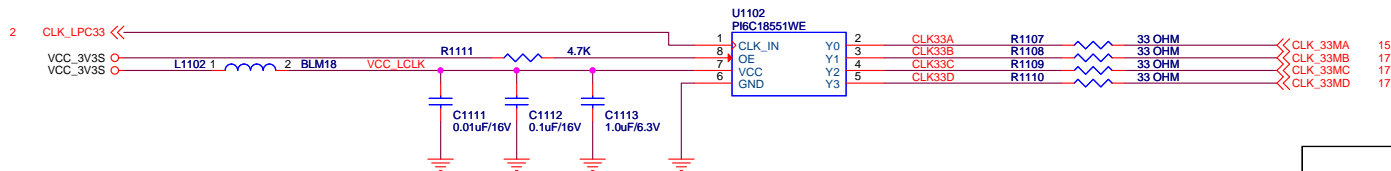
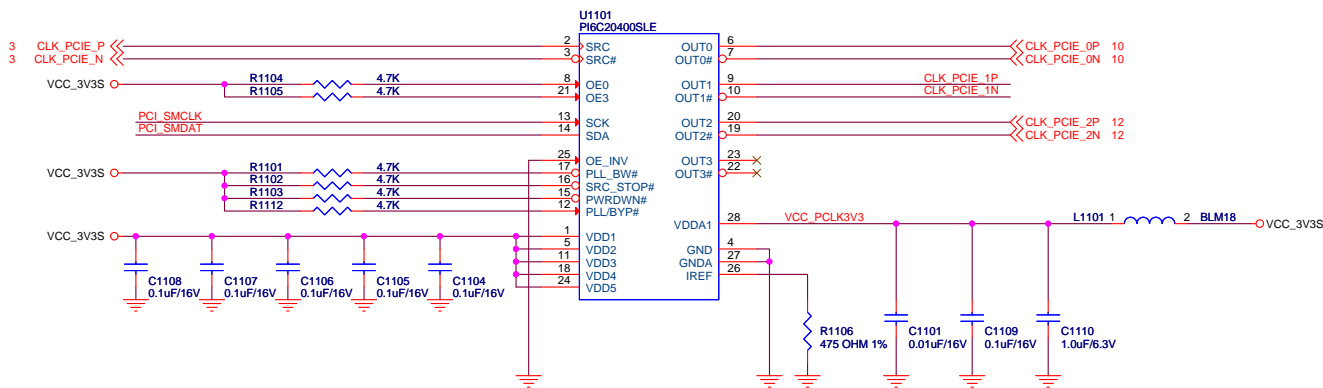
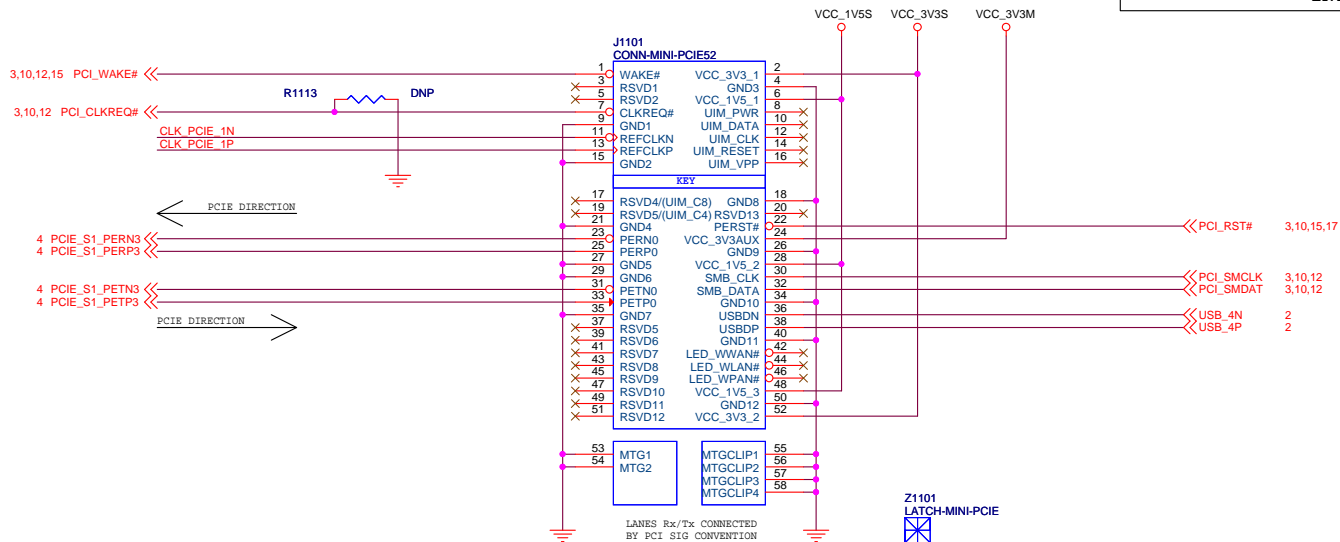
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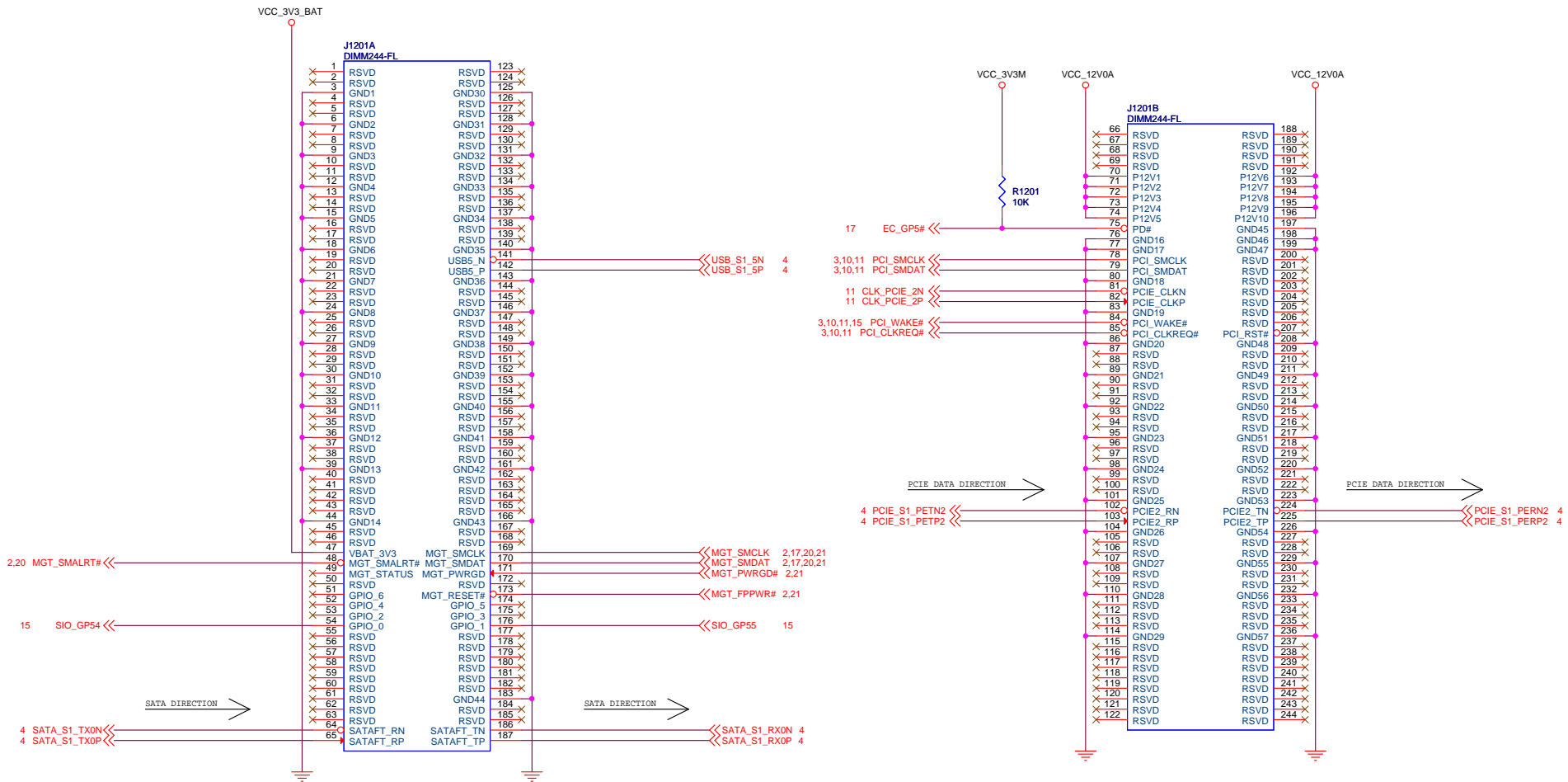
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SATA		
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Title		PCIe
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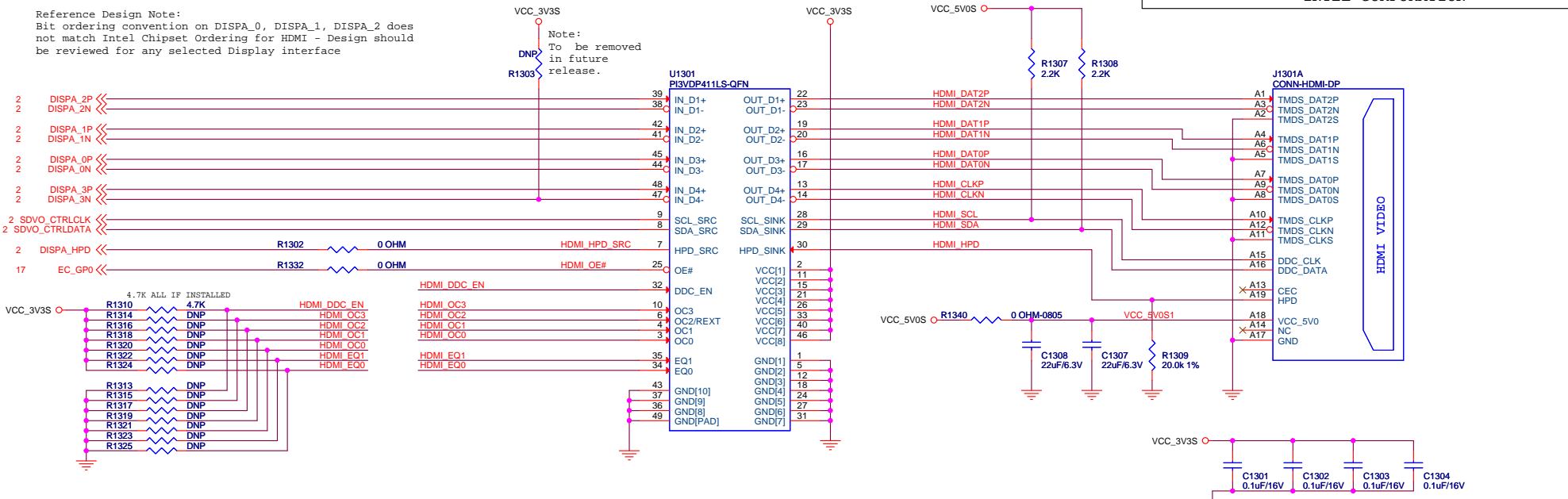
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Title Mini PCIe, CLK		
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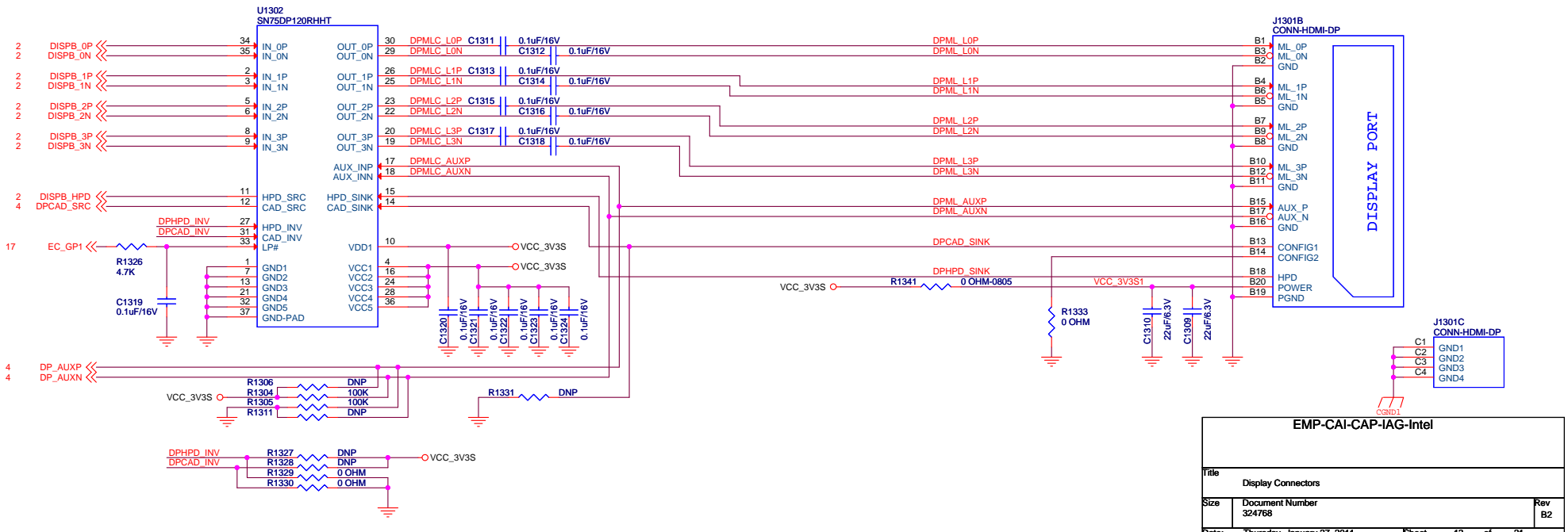
EMP-CAI-CAP-IAG-Intel		
Title Flash DIMM		
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Reference Design Note:
 Bit ordering convention on DISPA_0, DISPA_1, DISPA_2 does not match Intel Chipset Ordering for HDMI - Design should be reviewed for any selected Display interface

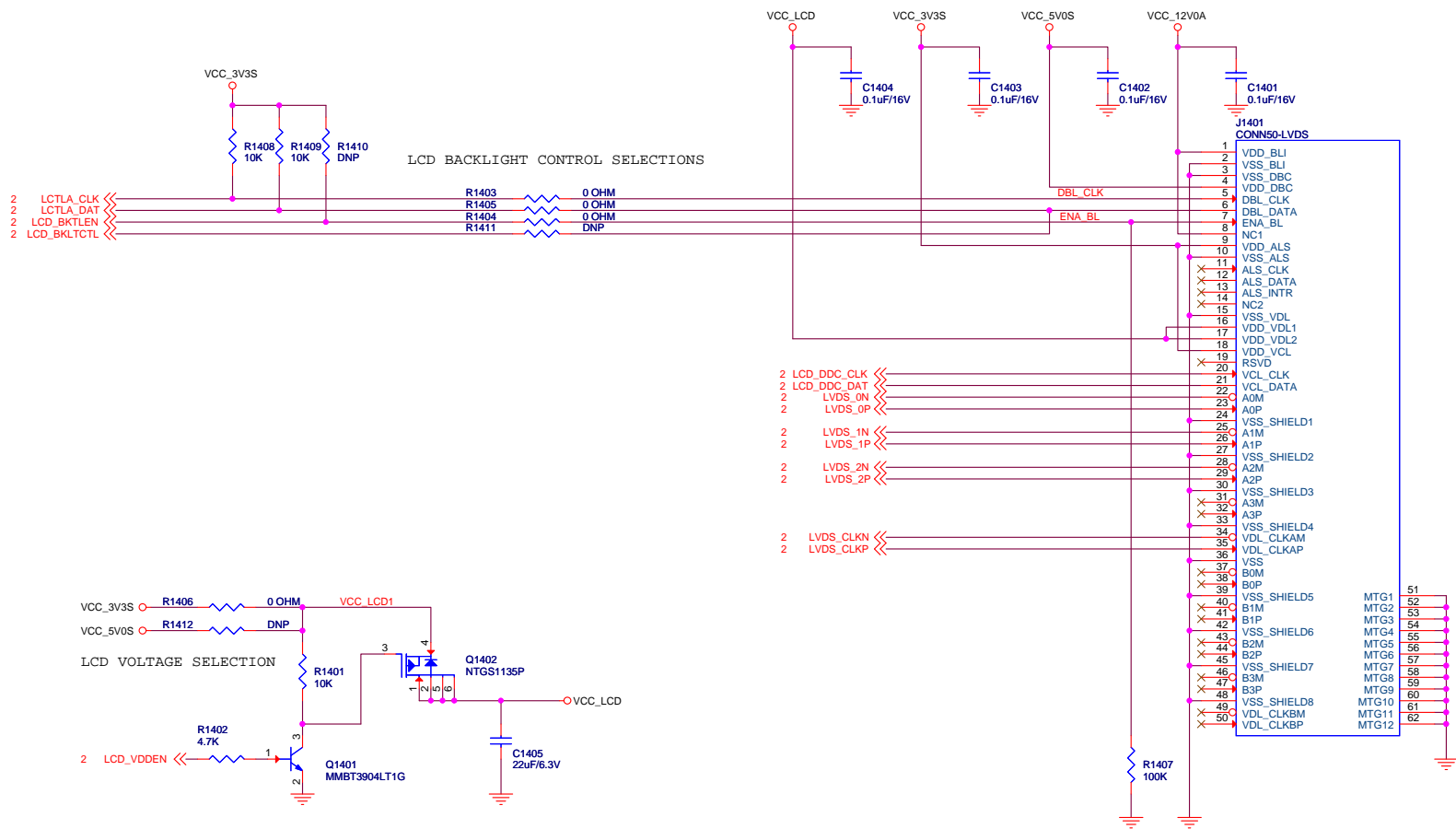
Note:
 To be removed in future release.



Reference Design Note:
 Pericom Design Guidelines call for signals "SCL_SRC" and "SDA_SRC" to be pulled up to 3.3V - Any reuse of this circuit should be validated against supplier design guidelines.



EMP-CAI-CAP-IAG-Intel		
Title		
Display Connectors		
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Note: No standard configuration has been defined for LVDS Panel Interfaces. Care should be taken to validate correct signal compatibility with any LVDS cable and panel before connection to this platform.

LVDS DISPLAY

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Title: LVDS		
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U1501
W83627UHG

5	CTSF#/DRVDEN0	4	RIE#/GP50
6	GP6#/INDEX#	3	DCDE#/GP51
7	DSRF#/MOA#	2	SOUTE/GP52
8	RTSF#/DSA#	1	SINE/GP53
9	DTRF#/DIR#	128	DTR#/#GP54
10	SINF#/STEP#	127	RTSE#/GP55
11	SOUTF#/WD#	126	DSRE#/GP56
13	DCDF#/WE#	125	CTSE#/GP57
14	GP63/TRAKO#		
15	GP62/WP#		
16	GP61/RDATA#		
17	RIF#HEAD#		
18	GP60/DSKCHG#		
21	PCICLK		
29	LFRAME#		
24	LAD3		
25	LAD2		
26	LAD1		
27	LAD0		
30	LRESET#		
23	SERIRQ		
22	LDRO#		
21	PD7		
35	PD6		
36	PD5		
37	PD4		
38	PD3		
39	PD2		
40	PD1		
41	PD0		
42	SLIN#		
43	SLIN#		
44	INIT#		
45	ERR#		
46	AFD#		
47	STB#		
48	FE		
32	SLCT		
33	BUSY		
34	ACK#		
49	CTSA#		
50	DSRA#		
51	VTT		
52	RTSA#(HEFRAS)		
53	DTRA#(PFDCUART)		
54	SINA		
55	SOUTA(PENKBC)		
56	DCDA#		
57	RIA#		
59	KBRST		
60	GP27		
62	KCLK		
63	KDAT		
65	MCLK		
66	MDAT		
19	CLKIN		
58	GA20M		
64	SUSLED		
77	WDT0#		
12	VCC_5V0		
48	VCC_5V0		
28	VCC_3V3		
61	VSB_5V0		
74	VBAT		
20	GND1		
55	GND2		

11	CLK_33MA
2,17	LPC_LFRAME#
2,17	LPC_LAD3
2,17	LPC_LAD2
2,17	LPC_LAD1
2,17	LPC_LAD0
3,10,11,17	PCI_RST#
2,17	SERIRQ
17	SIO_LDRO#

16	SIO_PD7[7:0]
35	RSIO PD7
36	RSIO PD6
37	RSIO PD5
38	RSIO PD4
39	RSIO PD3
40	RSIO PD2
41	RSIO PD1
42	RSIO PD0
43	RSIO SLIN#
44	RSIO INT#
45	RSIO APD#
47	RSIO STB#

16	SIO_LPT_SLIN#
16	SIO_LPT_INTR#
16	SIO_LPT_ERR#
16	SIO_LPT_AFD#
16	SIO_LPT_STB#
16	SIO_LPT_SLCT
16	SIO_LPT_PE
16	SIO_LPT_BUSY
16	SIO_LPT_ACK#

16	SIO_CTS#
16	SIO_DSR#
16	SIO_RTS#
16	SIO_DTR#
16	SIO_SINA
16	SIO_SOUTA
16	SIO_DCD#
16	SIO_RIA#

18	SIO_KBCLK
18	SIO_KBDAT
18	SIO_MCLK
18	SIO_MDAT

UART E	RIE#/GP50	4	X
	DCDE#/GP51	3	X
	SOUTE/GP52	2	X
	SINE/GP53	1	X
	DTR#/#GP54	128	X
	RTSE#/GP55	127	X
	DSRE#/GP56	126	X
	CTSE#/GP57	125	X

UART D	RID#/GP40	124	X
	DCDD#/GP41	123	X
	RTSD#(GP1_MUL)/SOUTD/GP42	122	X
	SIND/GP43	121	X
	DTRD#/GP44	120	X
	(FANSET)/RTSD#(GP45)	119	X
	DSRD#(GP46)	118	X
	CTSD#(GP47)	117	X

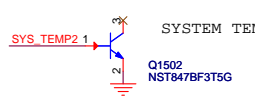
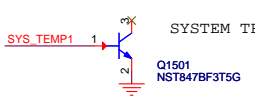
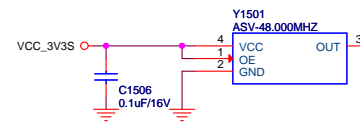
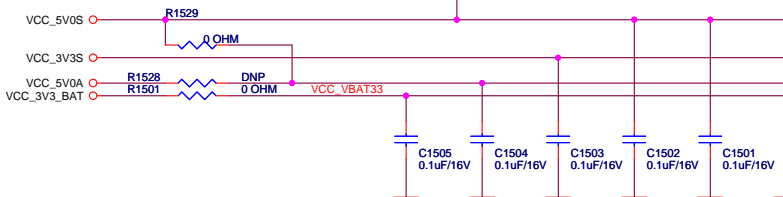
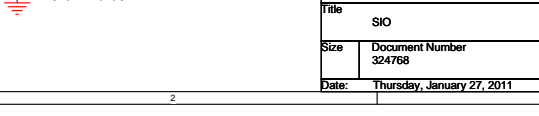
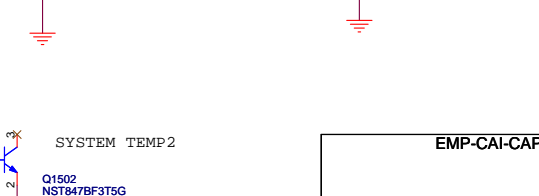
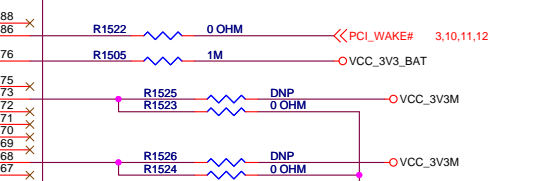
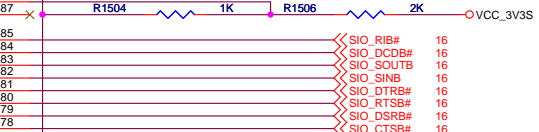
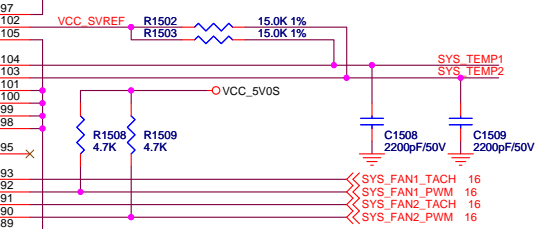
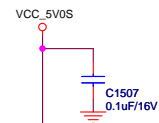
UART C	RIC#/GP30	116	X
	DCDC#/GP31	115	X
	SOUTC/GP32	114	X
	SINCC/GP33	113	X
	DTRC#/GP34	112	X
	RTSC#/GP35	111	X
	DSRC#/GP36	110	X
	CTSC#/GP37	109	X

ANALOG I/O	VCCA	97	X
	VREF	102	X
	AGND	105	X
	SYSTEM	104	X
	CPUTIN	103	X
	CPUVCORE	101	X
	VIN0	100	X
	VIN1	99	X
	VIN2	98	X
	OVT#/SMI#	95	X
	SYSFANIN	93	X
	SYSFANOUT	92	X
	CPUFANIN	91	X
	CPUFANOUT	90	X
	SST	89	X

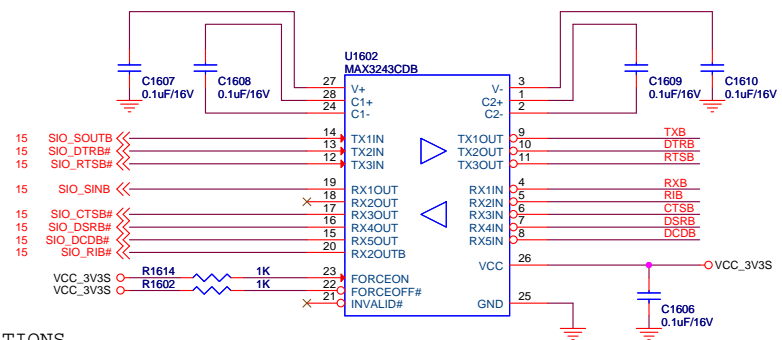
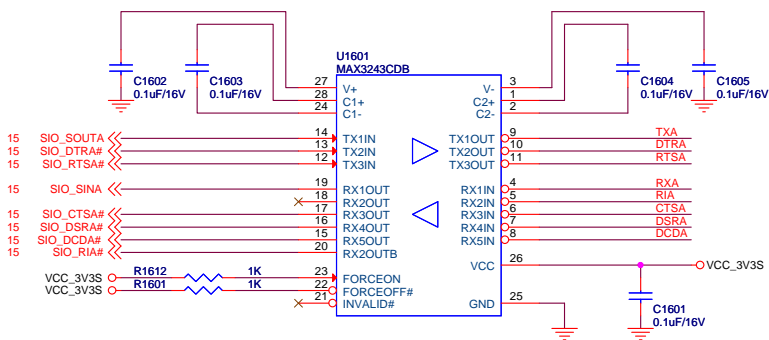
UART B	GP10/RI#	85	X
	GP11/DCD#	84	X
	GP12/SOUTB/IRTX	83	X
	GP13/SINB/IRRX	82	X
	GP14/DTRB#	81	X
	GP15/RTSB#	80	X
	GP16/DSRB#	79	X
	GP17/CTSB#	78	X

GPIO	GP24	94	X
	GP23	96	X
	GP22	106	X
	GP21/BEEP	107	X
	GP20/PLED	108	X

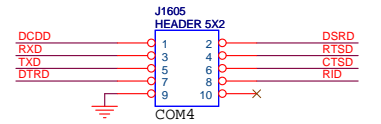
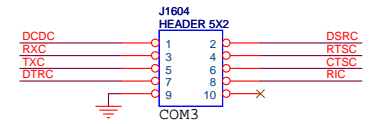
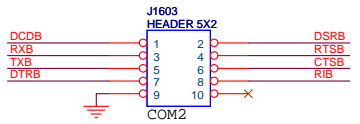
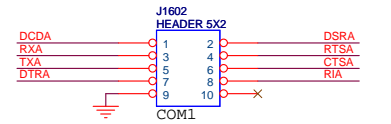
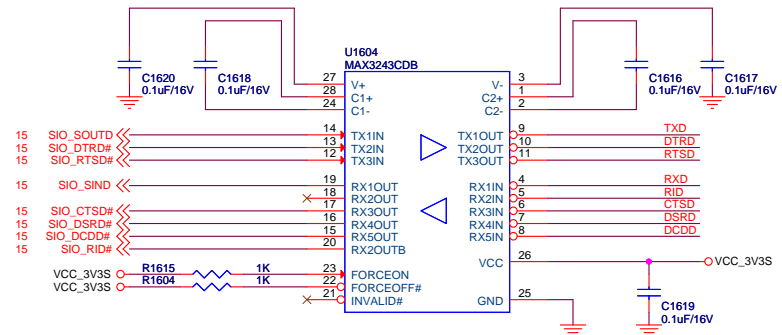
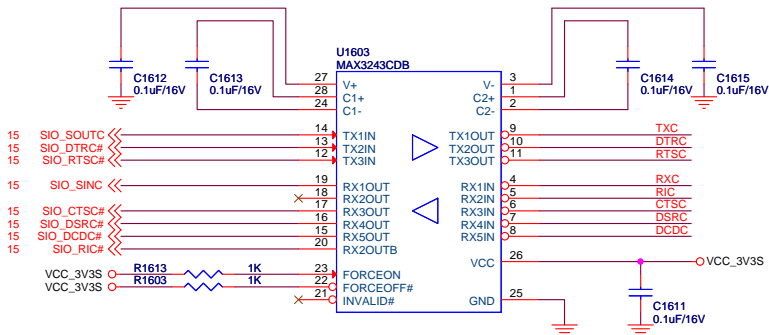
HARDWARE INTERFACE	PECI	88	X
	PME#	86	X
	CASEOPEN#	76	X
	RSMRST#	75	X
	SUS#	73	X
	PSON#	72	X
	PWROK	71	X
	GP25/SCL	70	X
	GP26/SDA	69	X
	PSIN#	68	X
	PSOUT#	67	X



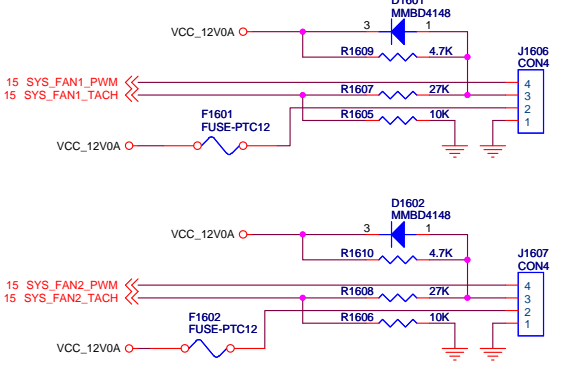
EMP-CAI-CAP-IAG-Intel		
Title	SIO	
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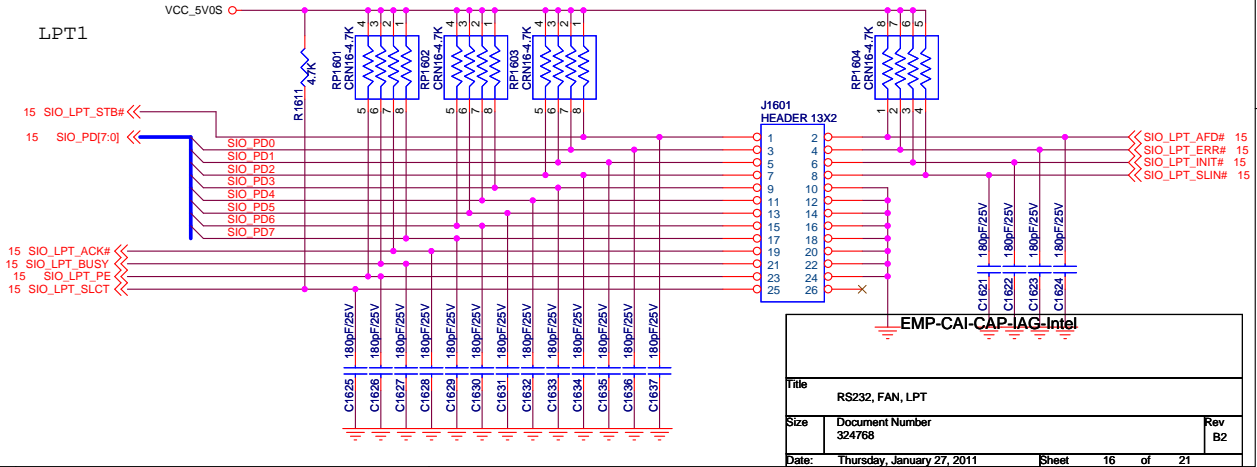
RS232 COMMUNICATIONS



FAN CONNECTORS

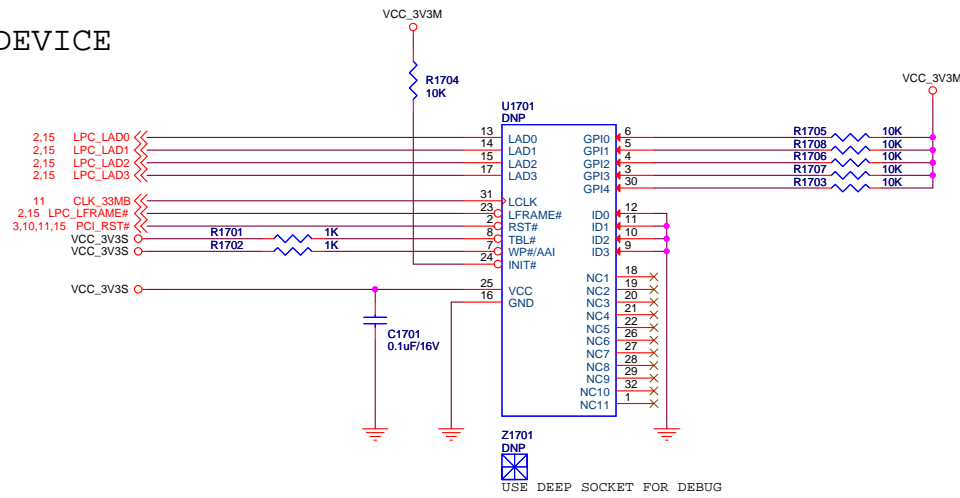


LPT1

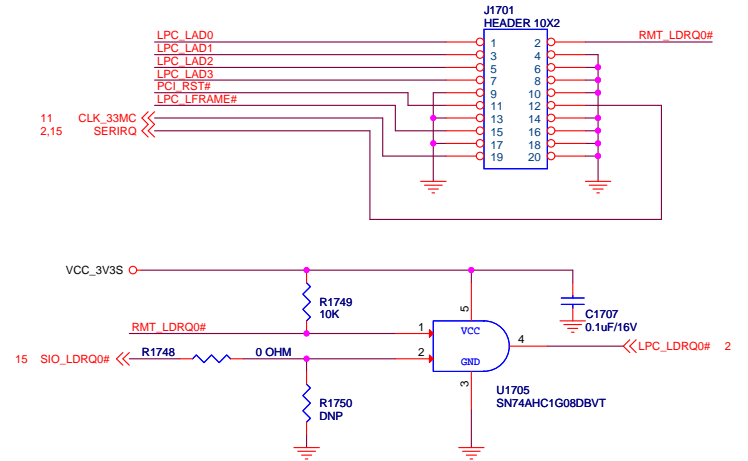


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Title	RS232, FAN, LPT	
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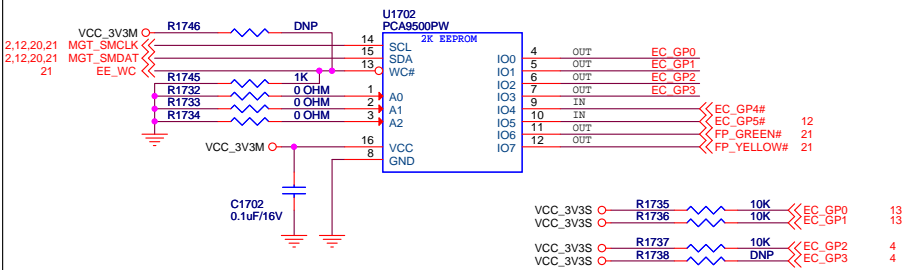
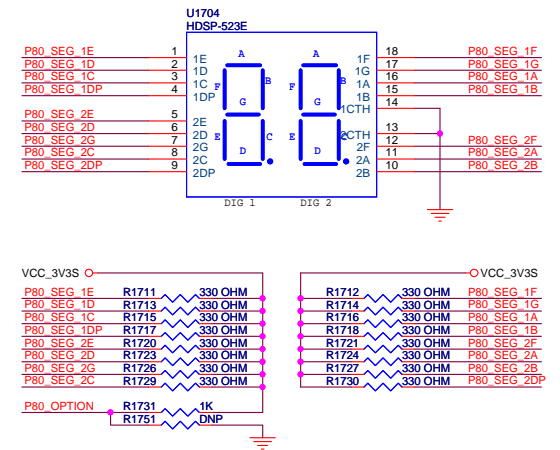
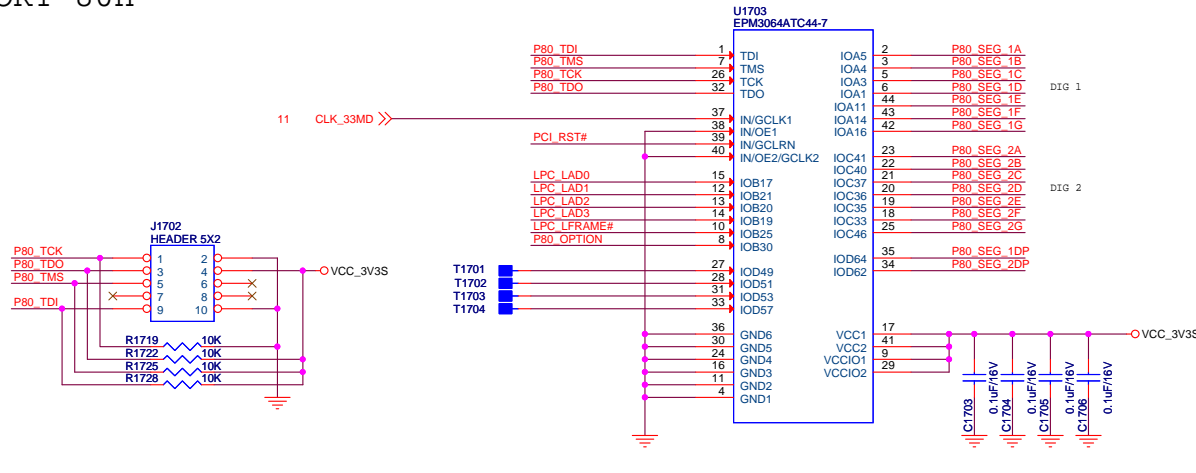
LPC FWH DEVICE



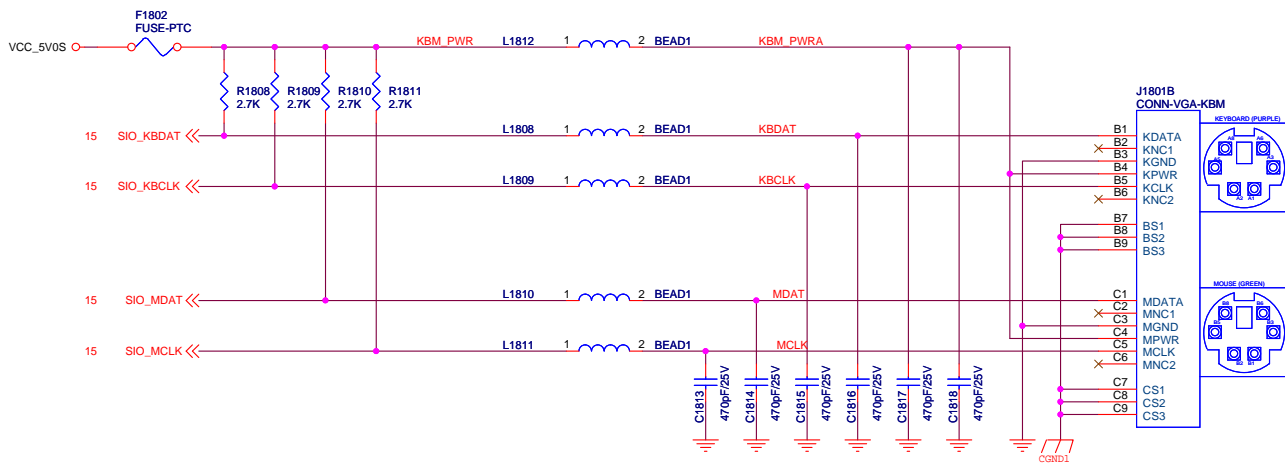
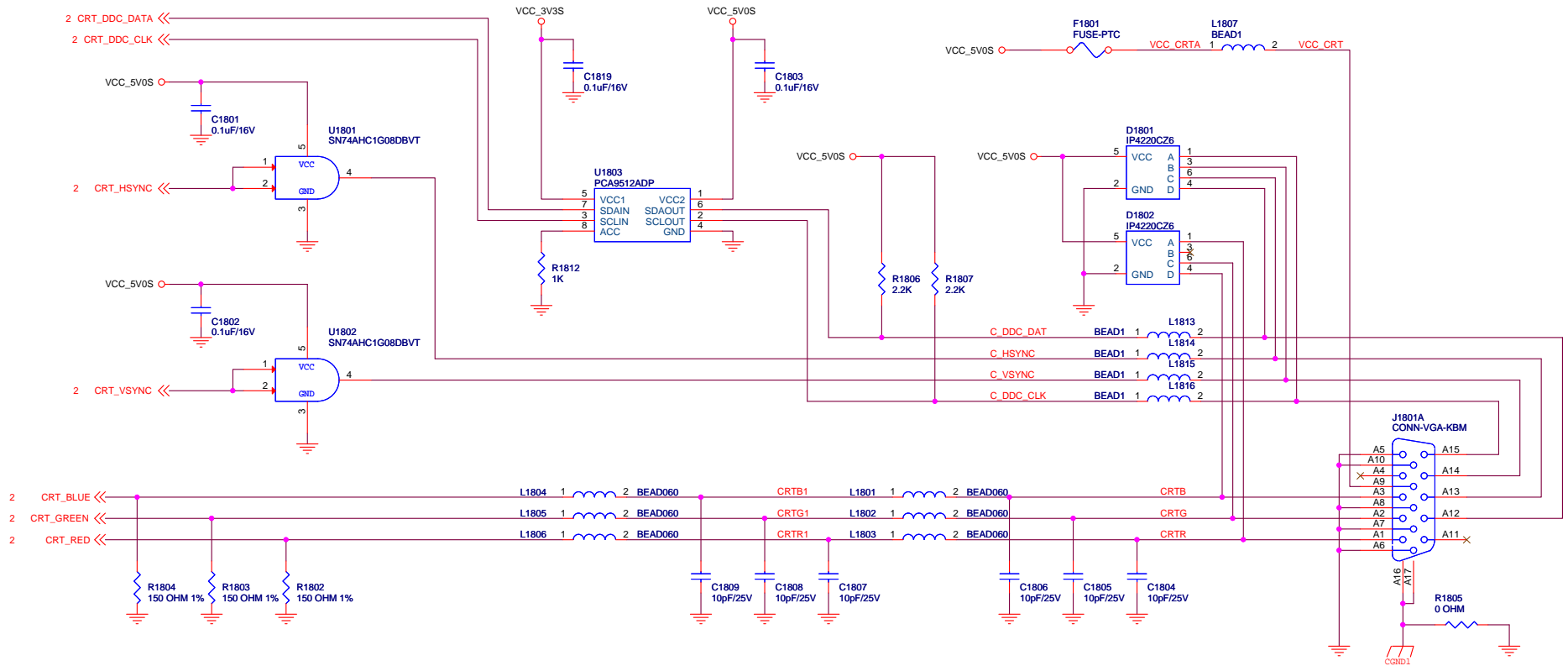
LPC CONNECTOR



PORT 80H



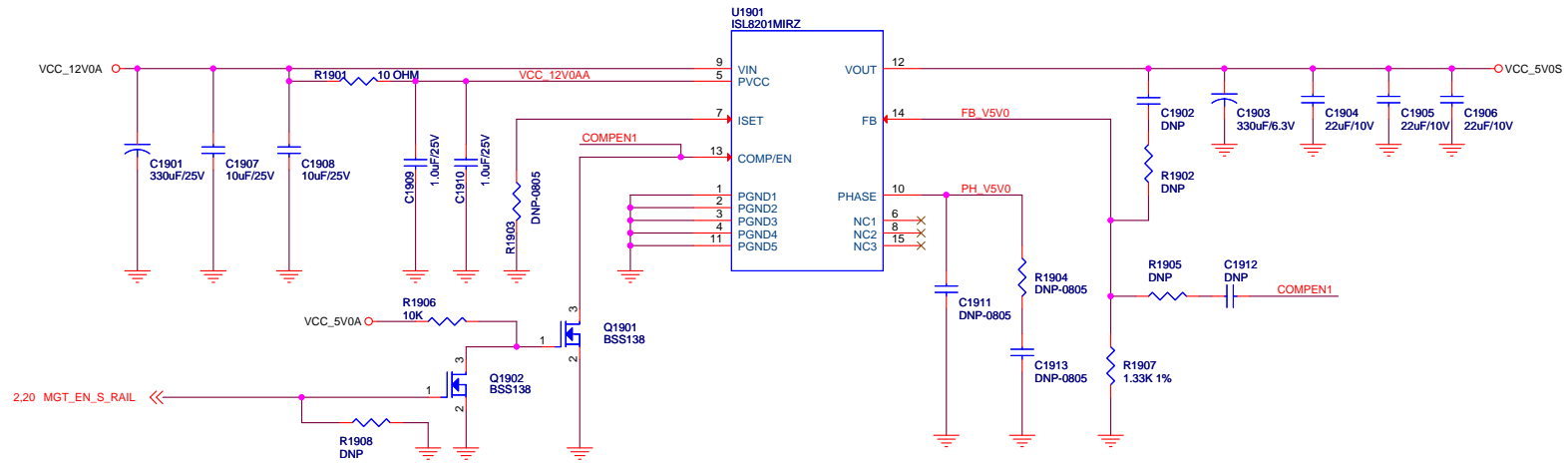
EMP-CAI-CAP-IAG-Intel		
Title LPC, Port 80, EC		
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EMP-CAI-CAP-IAG-Intel		
Title CRT, PS2		
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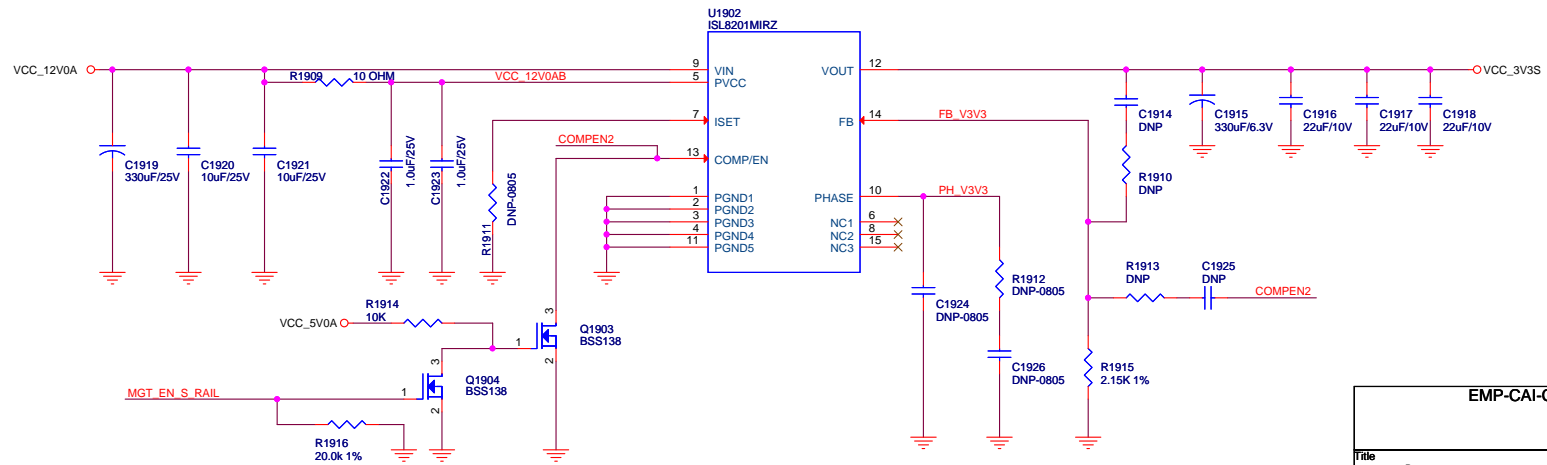
VCC 5.0 VDC 10 AMPS

MASTER



VCC 3.3 VDC 10 AMPS

MASTER

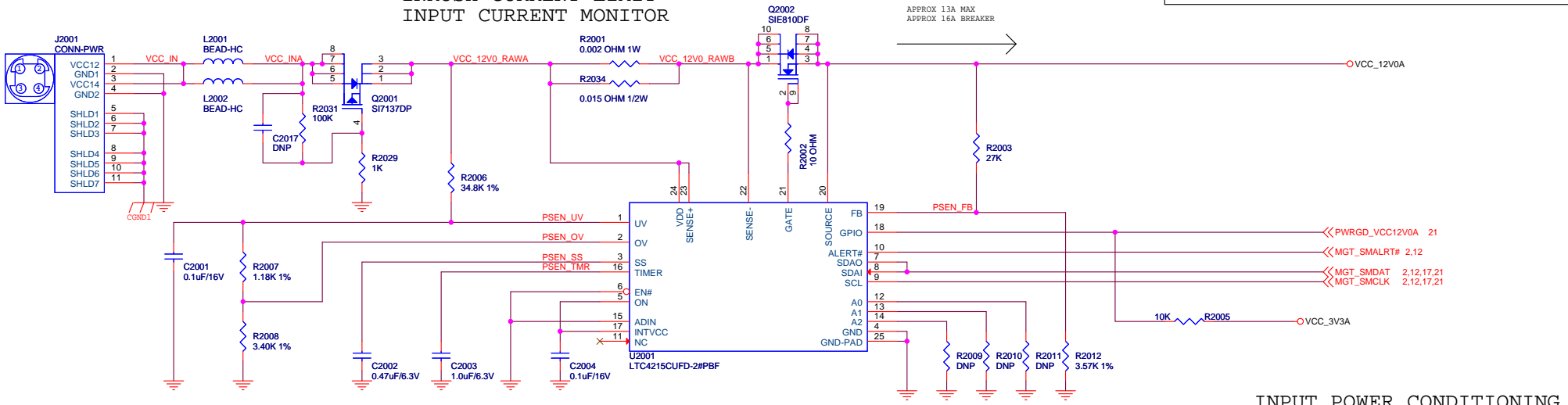


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INRUSH CURRENT LIMIT INPUT CURRENT MONITOR

INTEL CORPORATION



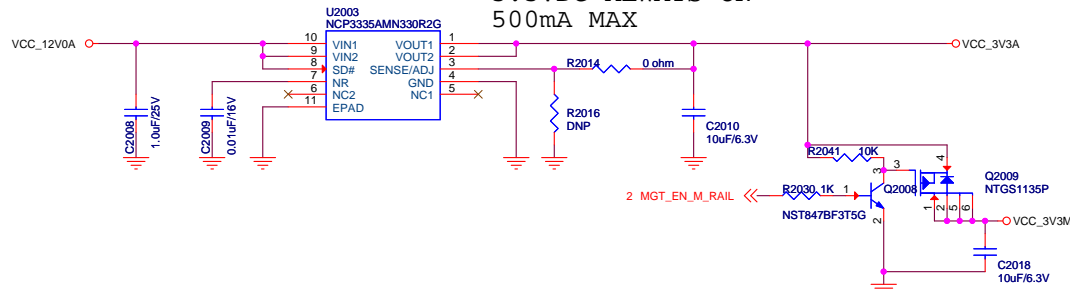
APPROX 13A MAX
APPROX 16A BREAKER

INPUT POWER CONDITIONING

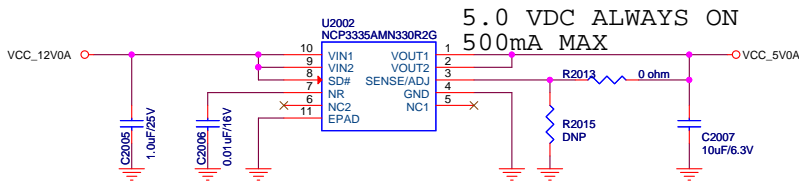
NOTE!!!
"VCC_5V0A" has been implemented using a 3.3 Volt Regulator due to component availability issues. This is functionally correct for this platform, but U2002 should be populated with the pin-compatible 5.0 Volt regulator for subsequent revisions. See Changes needed below.

- CHANGES:**
- R1529: Change to DNP
 - R1528: Change to 0 OHM
 - R1916: Change to DNP
 - U2002: Change to NCP3335AMADJR2G
 - R2015: Change to 9.09K, 1%
 - R2013: Change to 27.4K, 1%

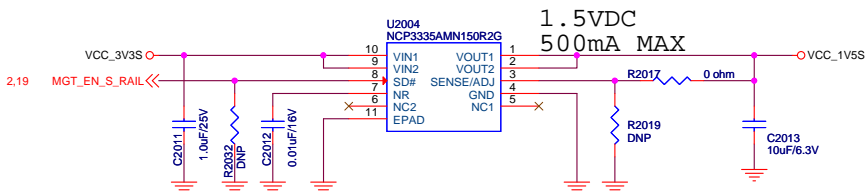
3.3VDC ALWAYS ON 500mA MAX



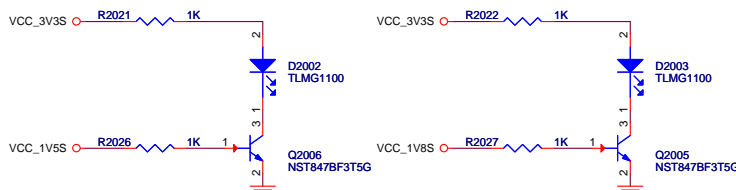
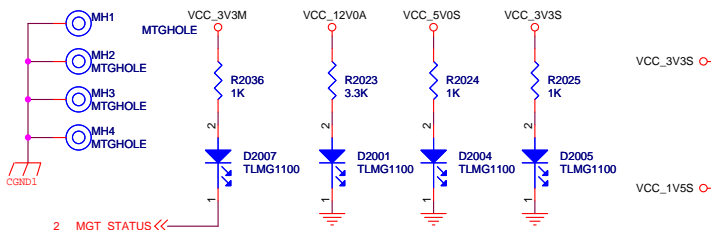
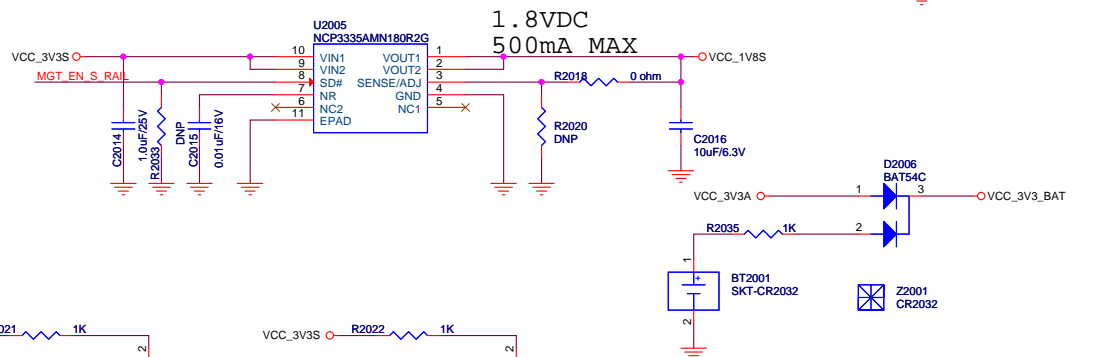
5.0 VDC ALWAYS ON 500mA MAX



1.5VDC 500mA MAX

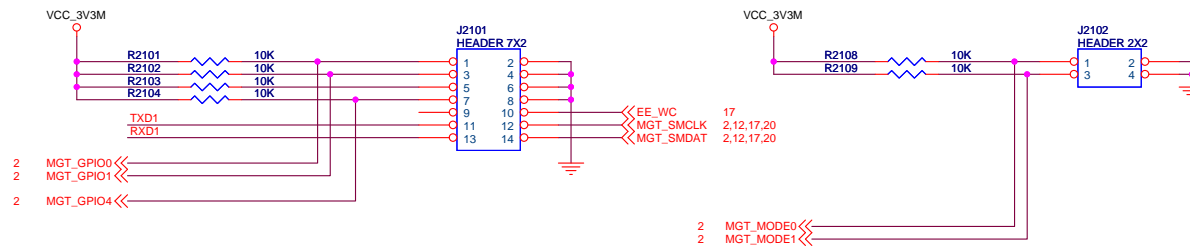


1.8VDC 500mA MAX

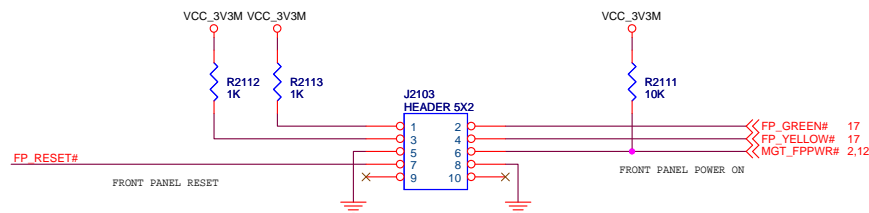


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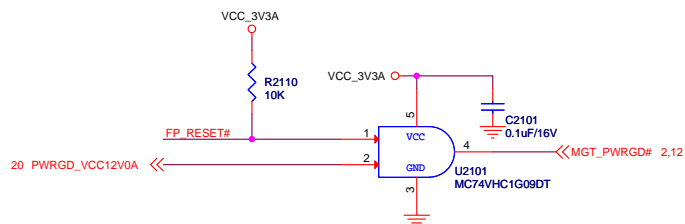
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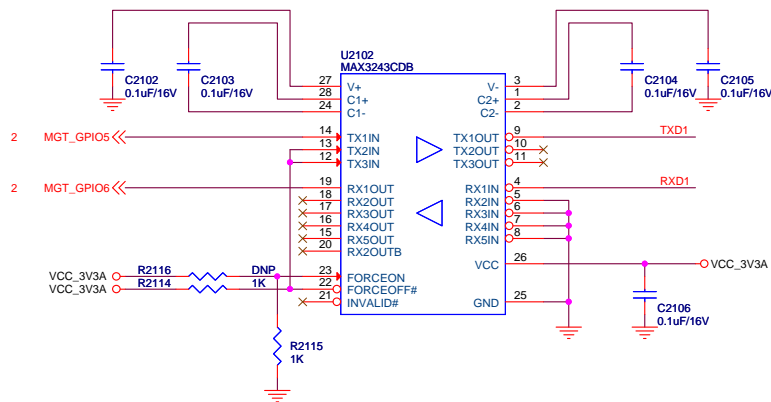
MODE SETUPS



FRONT PANEL SW



MANAGEMENT CONTROLLER SERIAL PORT



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