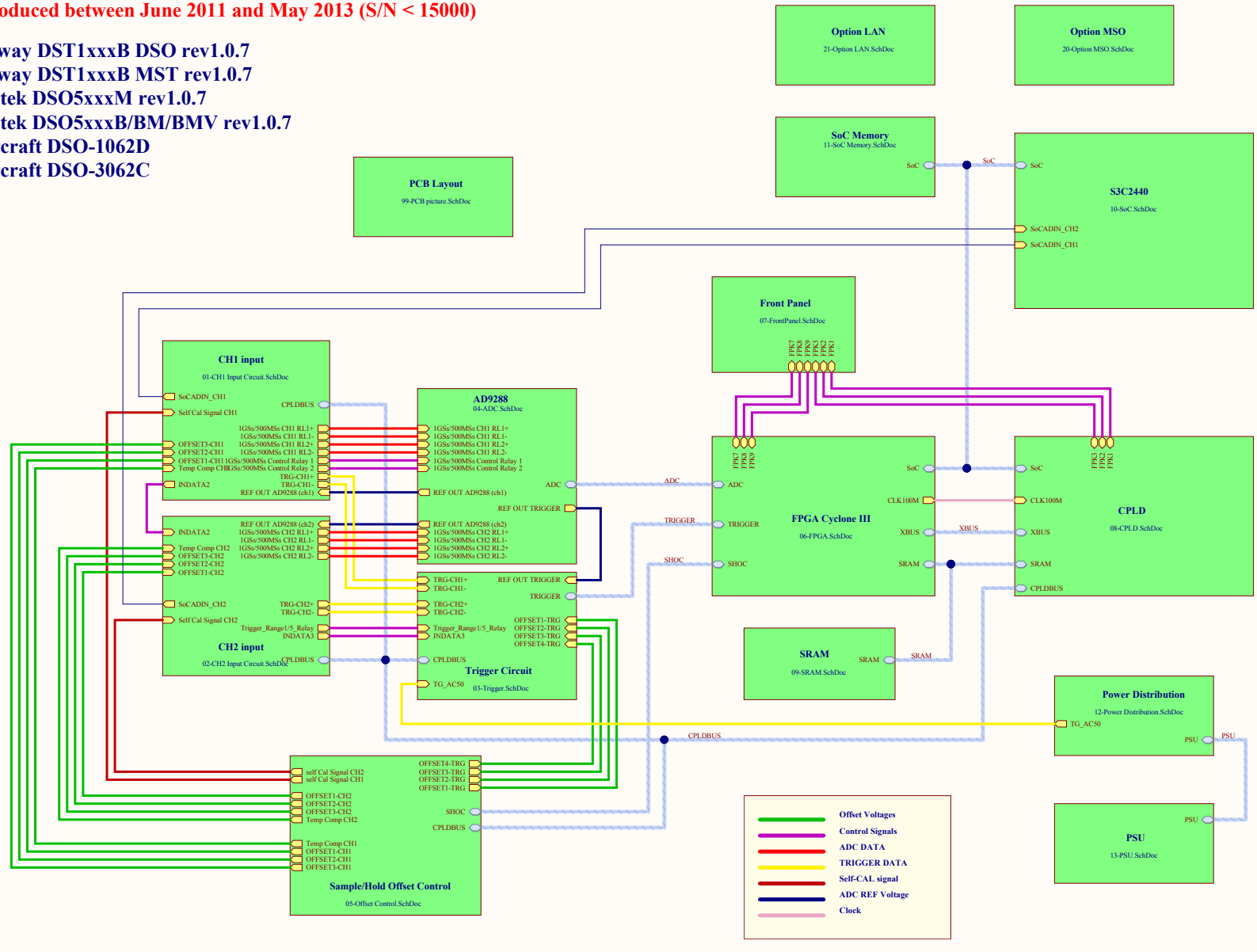
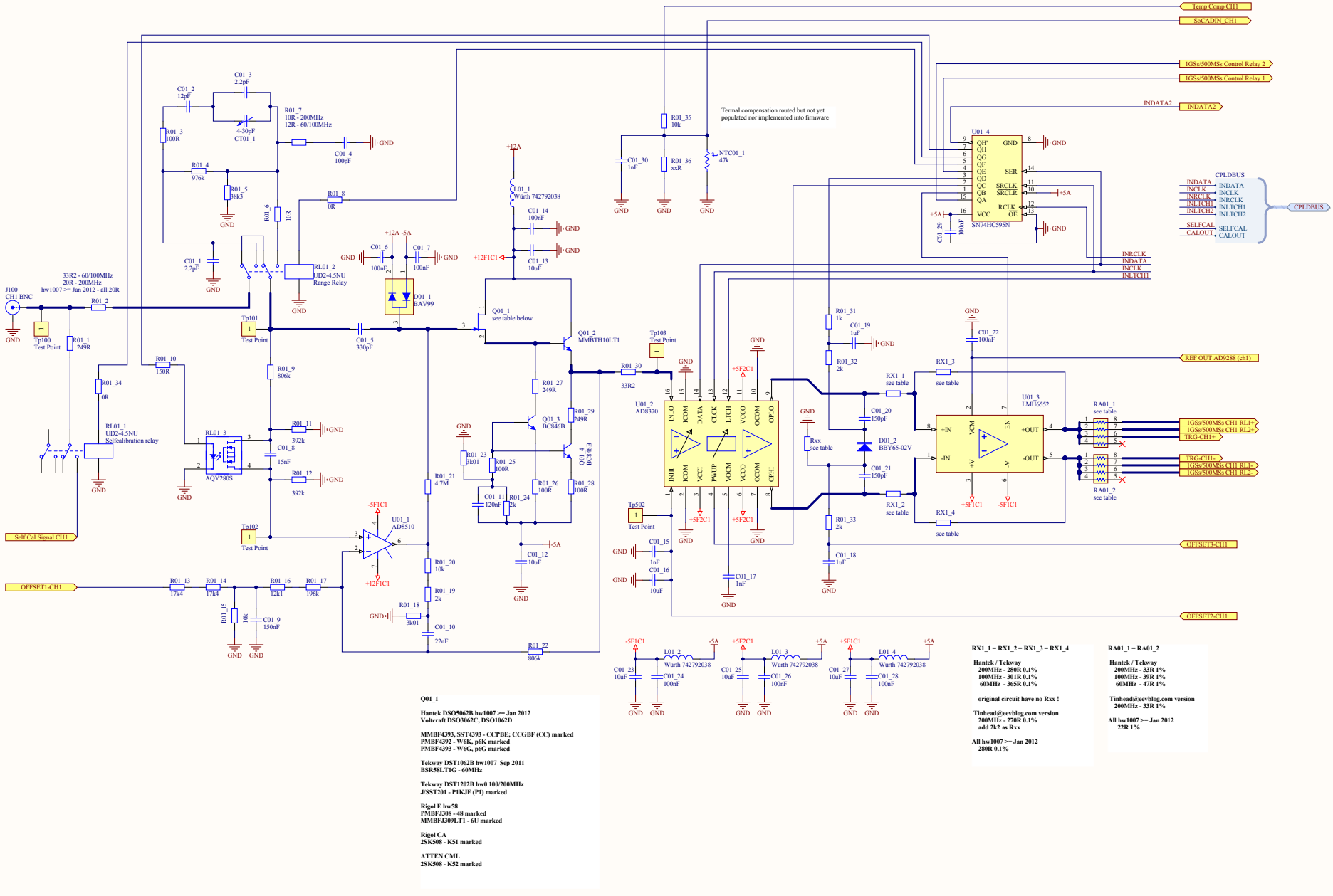
DSOs produced between June 2011 and May 2013 (S/N < 15000)

Tekway DST1xxxB DSO rev1.0.7
Tekway DST1xxxB MST rev1.0.7
Hantek DSO5xxxM rev1.0.7
Hantek DSO5xxxB/BM/BMV rev1.0.7
Voltcraft DSO-1062D
Voltcraft DSO-3062C



CH1 Input Circuit



Q01_1

Hantek DSO5062B hw1007 >= Jan 2012
Voltcraft DSO3062C, DSO1062D

MMBF4393, SST4393 - CCPBE; CCGBF (CC) marked
PMBF4392 - W6K, p6K marked
PMBF4393 - W6G, p6G marked

Tekway DST1062B hw1007 Sep 2011
BSR58LT1G - 60MHz

Tekway DST1202B hw0 100/200MHz
J/SST201 - P1KJF (P1) marked

Rigol E hw58
PMBFJ308 - 48 marked
MMBFJ309LT1 - 6U marked

Rigol CA
2SK508 - K51 marked

ATTEN CML
2SK508 - K52 marked

RX1_1 ~ RX1_2 ~ RX1_3 ~ RX1_4

Hantek / Tekway
200MHz - 280R 0.1%
100MHz - 301R 0.1%
60MHz - 365R 0.1%

original circuit have no Rxx !

Tinhead@eevblog.com version
200MHz - 270R 0.1%
add 2k2 as Rxx

All hw1007 >= Jan 2012
280R 0.1%

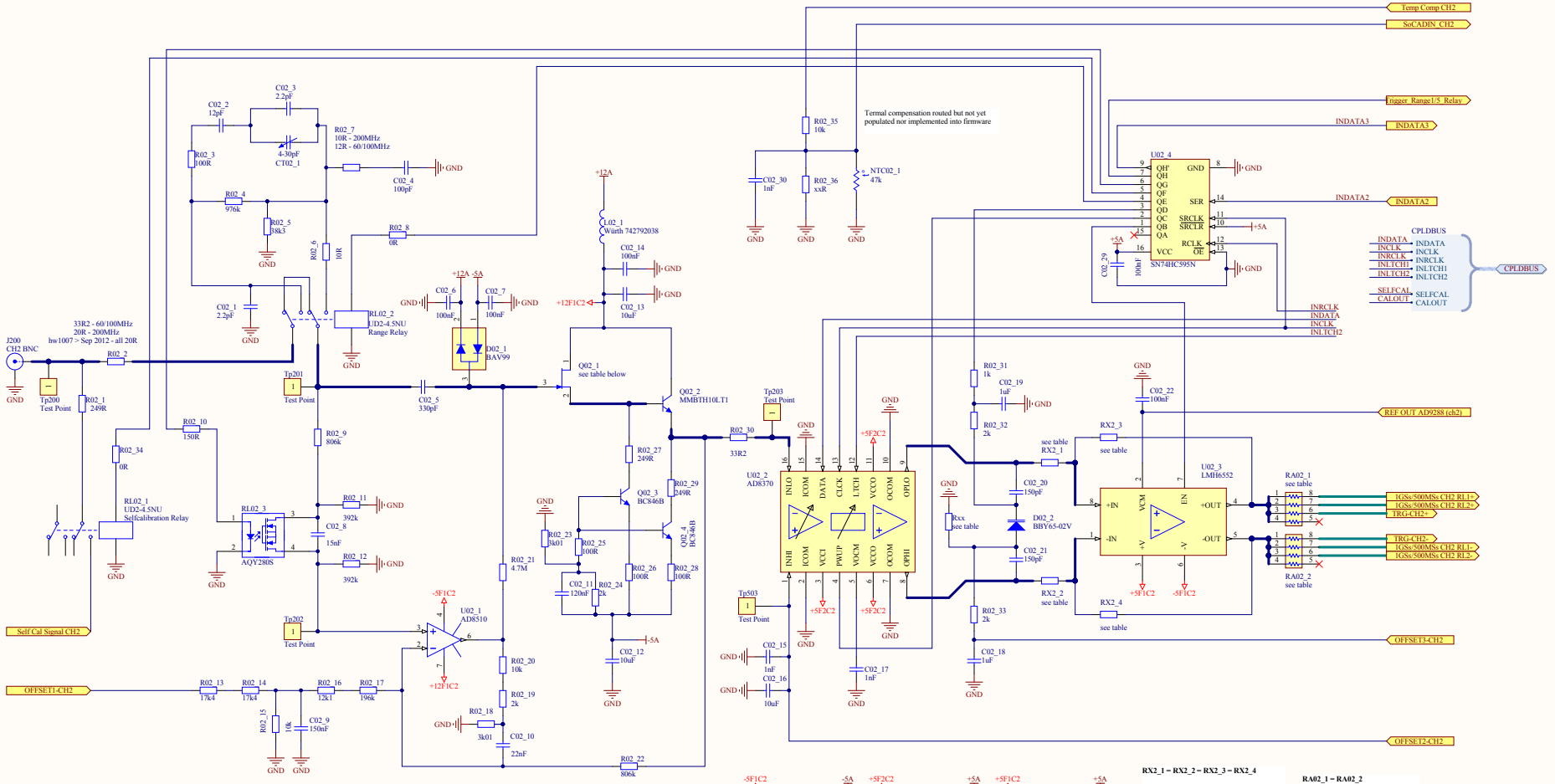
RA01_1 ~ RA01_2

Hantek / Tekway
200MHz - 33R 1%
100MHz - 39R 1%
60MHz - 47R 1%

Tinhead@eevblog.com version
200MHz - 33R 1%

All hw1007 >= Jan 2012
22R 1%

CH2 Input Circuit



Q02_1

Hantek DSO5062B hw1007 >= Jun 2012
Voltcraft DSO3062C, DSO1062D

MMBF4393, SST4393 - CCPBE; CCGBF (CC) marked
PMBF4392 - W6K, p6K marked
PMBF4393 - W6G, p6G marked

Tekway DST1062B hw1007 Sep 2011
BSR58LT1G - 60MHz

Tekway DST1202B hw0 100/200MHz
J/SST201 - P1KJF (P1) marked

Rigol E hw58
PMBFJ308 - 48 marked
MMBFJ309LT1 - 6U marked

Rigol CA
2SK508 - K51 marked

ATTEN CML
2SK508 - K52 marked

RX2_1 = RX2_2 = RX2_3 = RX2_4

Hantek / Tekway
200MHz - 280R 0.1%
100MHz - 301R 0.1%
60MHz - 365R 0.1%

original circuit have no Rxx !

Tinhead@eevblog.com version
200MHz - 270R 0.1%
add 2k2 as Rxx

All hw1007 >= Jun 2012
280R 0.1%

RA02_1 = RA02_2

Hantek / Tekway
200MHz - 33R 1%
100MHz - 39R 1%
60MHz - 47R 1%

Tinhead@eevblog.com version
200MHz - 33R 1%

All hw1007 >= Jun 2012
22R 1%

Trigger Circuit

Q03_1

Hantek DSO5062B hw1007 >= Jun 2012
Voltcraft DSO3062C, DSO1062D

MMBF4393, SST4393 - CCPBE; CCGBF (CC) marked

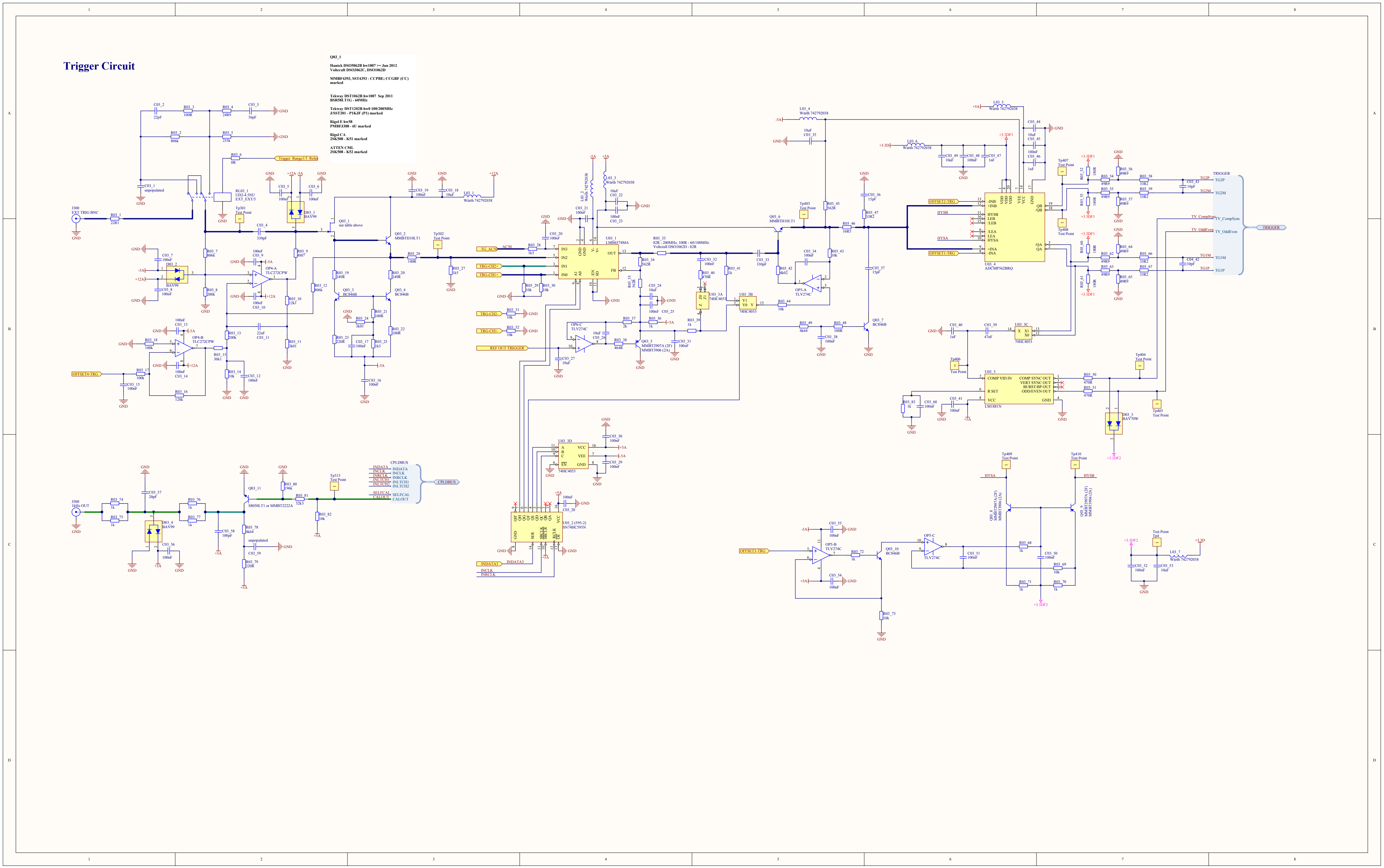
Tekway DST1062B hw1007 Sep 2011
BSR58LT1G - 60MHz

Tekway DST1202B hw0 100/200MHz
J/SST201 - P1KJF (P1) marked

Rigol E hw58
PMBFJ308 - 6U marked

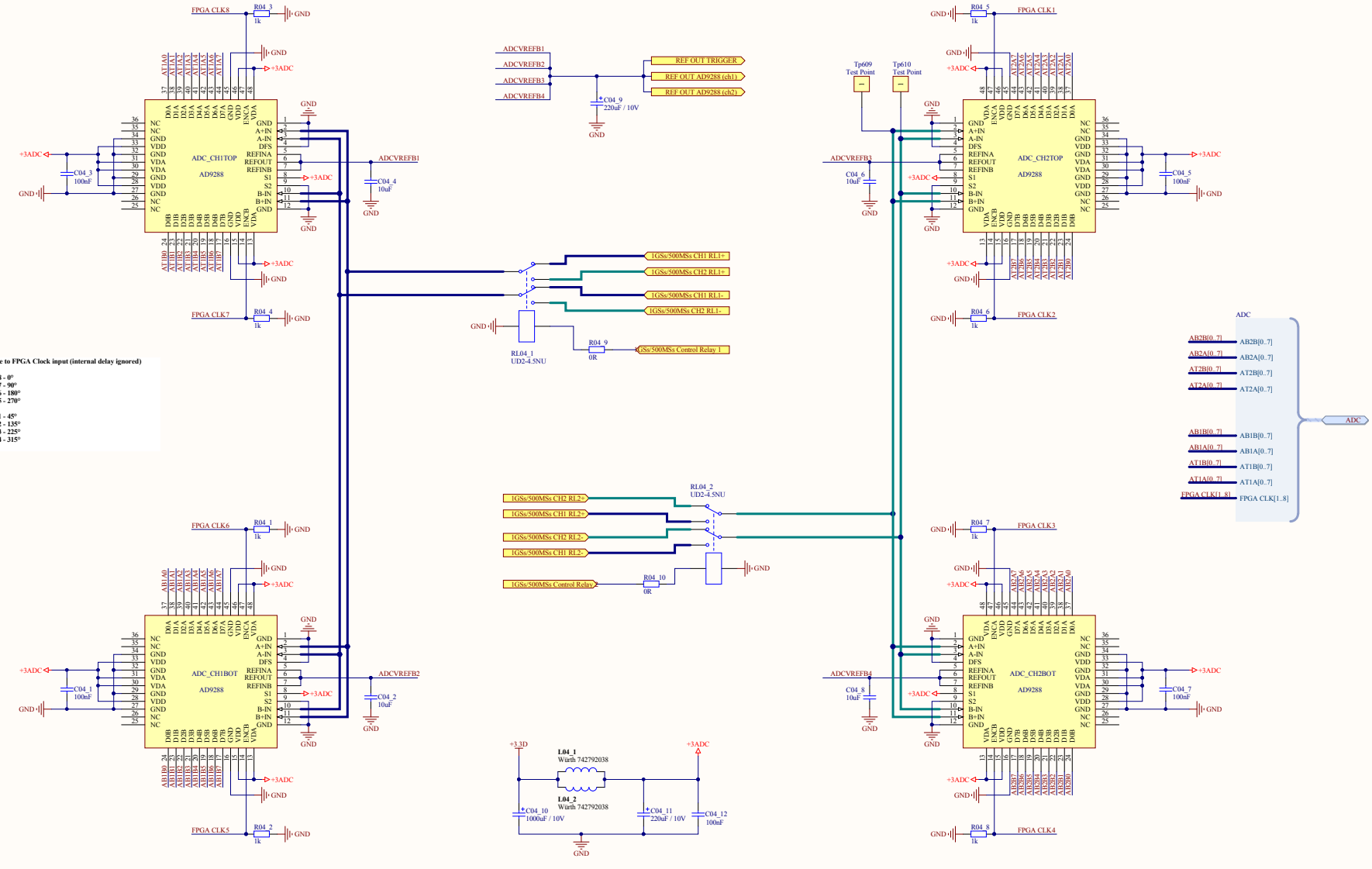
Rigol CA
2SK508 - K51 marked

ATTEN CML
2SK508 - K52 marked



J300
EXT TRIG BNC
RL03_1
UD2-4.5NU
EXT_EXT/5
Trigger_Range1/5_Relay
OP4-A
TLC272CPW
OP4-B
TLC272CPW
OFFSET4-TRG
Q03_2
MMBTH10LT1
Q03_3
BC846B
Q03_4
BC846B
TG_AC50
TRG-CH2+
TRG-CH1+
TRG-CH2-
TRG-CH1-
REF OUT TRIGGER
U03_1
LMH6574MA
R03_33
82R - 200MHz, 100R - 60/100MHz
Voltcraft DSO1062D - 82R
OP6-C
TLV274C
Q03_5
MMBT2907A (2F)
MMBT3906 (2A)
U03_3A
74HC4053
U03_3B
74HC4053
Q03_6
MMBTH10LT1
OP5-A
TLV274C
Q03_7
BC846B
U03_4
ADCMP562BRQ
OFFSET2-TRG
OFFSET1-TRG
HYSB
HYSA
TRIGGER
TG2P
TG2M
TG1M
TG1P
TV_CompSync
TV_OddEven
U03_5
LM1881N
D03_3
BAV70W
U03_3C
74HC4053
U03_3D
74HC4053
U03_2 (595-2)
SN74HC595N
INDATA3
INCLK
INRCLK
J500
1kHz OUT
D03_4
BAV99
Q03_11
S8050LT1 or MMBT2222A
CPLDBUS
INDATA
INCLK
INRCLK
INLTCH1
INLTCH2
SELFCAL
CALOUT
OFFSET3-TRG
OP5-B
TLV274C
OP5-C
TLV274C
Q03_10
BC846B
Q03_8
MMBT2907A (2F)
MMBT3906 (2A)
Q03_9
MMBT2907A (2F)
MMBT3906 (2A)
Würth 742792038

ADC Circuit

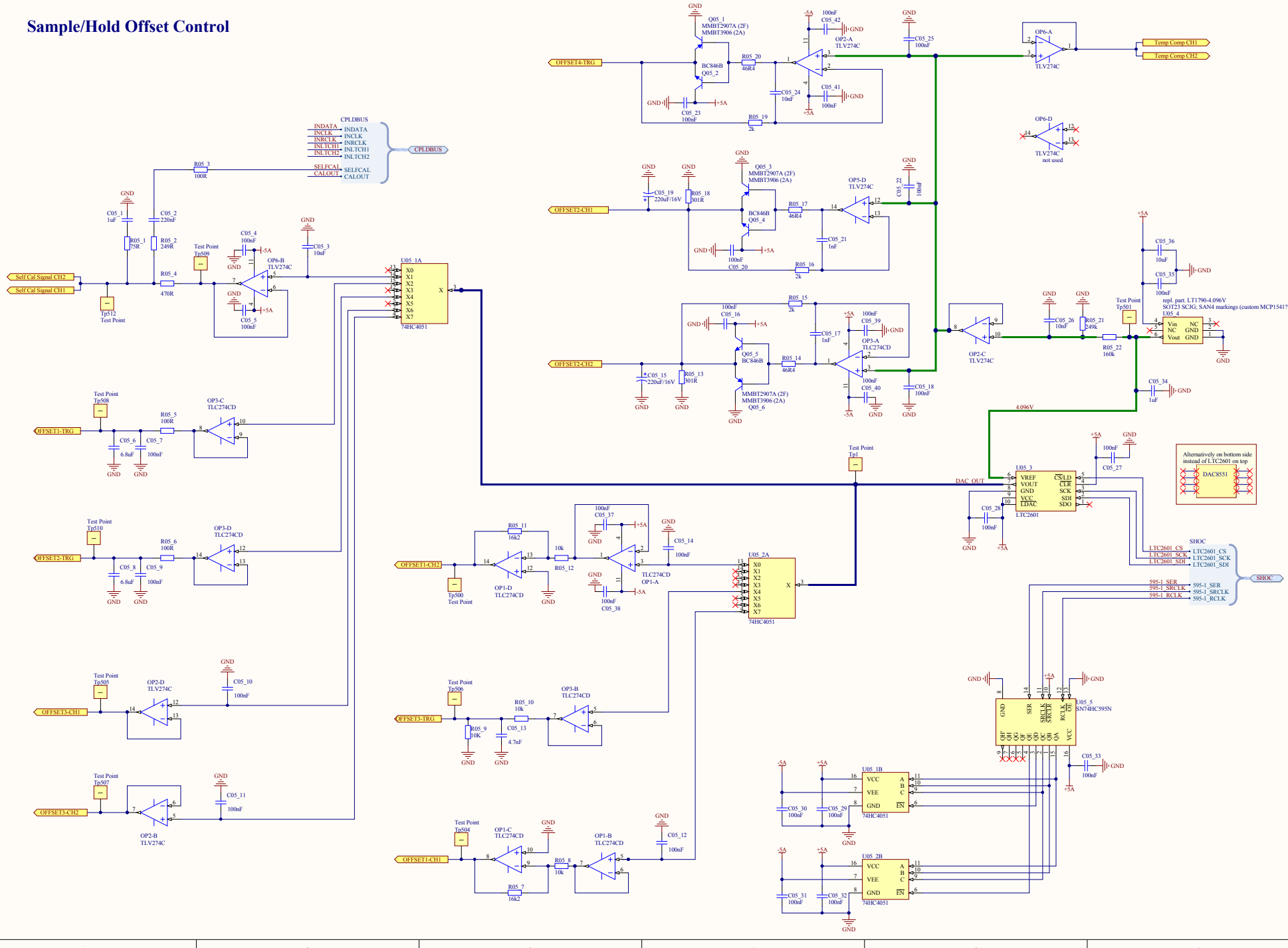


Clocks relative to FPGA Clock input (internal delay ignored)

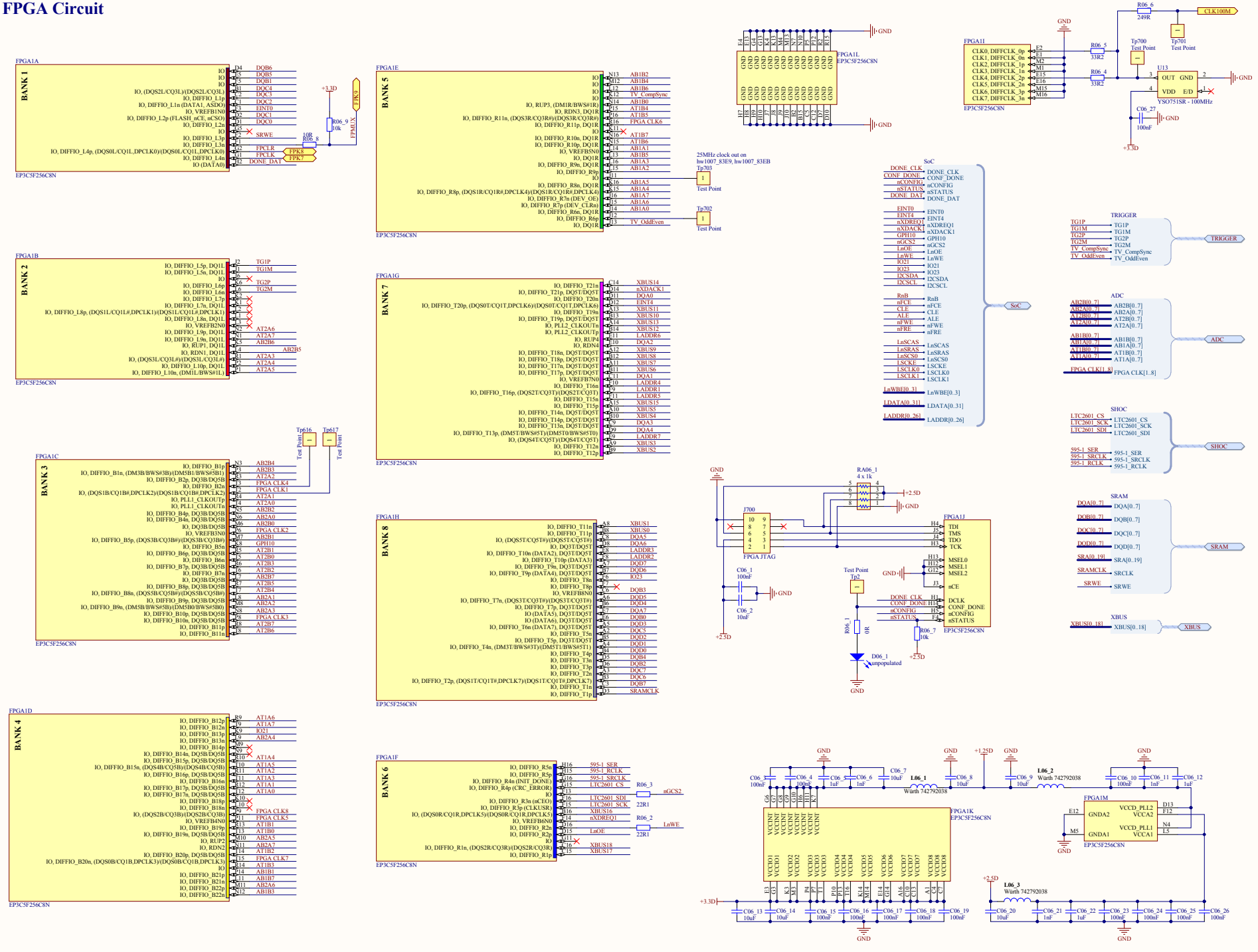
FPGA Clock 8 - 0°
FPGA Clock 7 - 90°
FPGA Clock 6 - 180°
FPGA Clock 5 - 270°

FPGA Clock 1 - 45°
FPGA Clock 2 - 135°
FPGA Clock 3 - 225°
FPGA Clock 4 - 315°

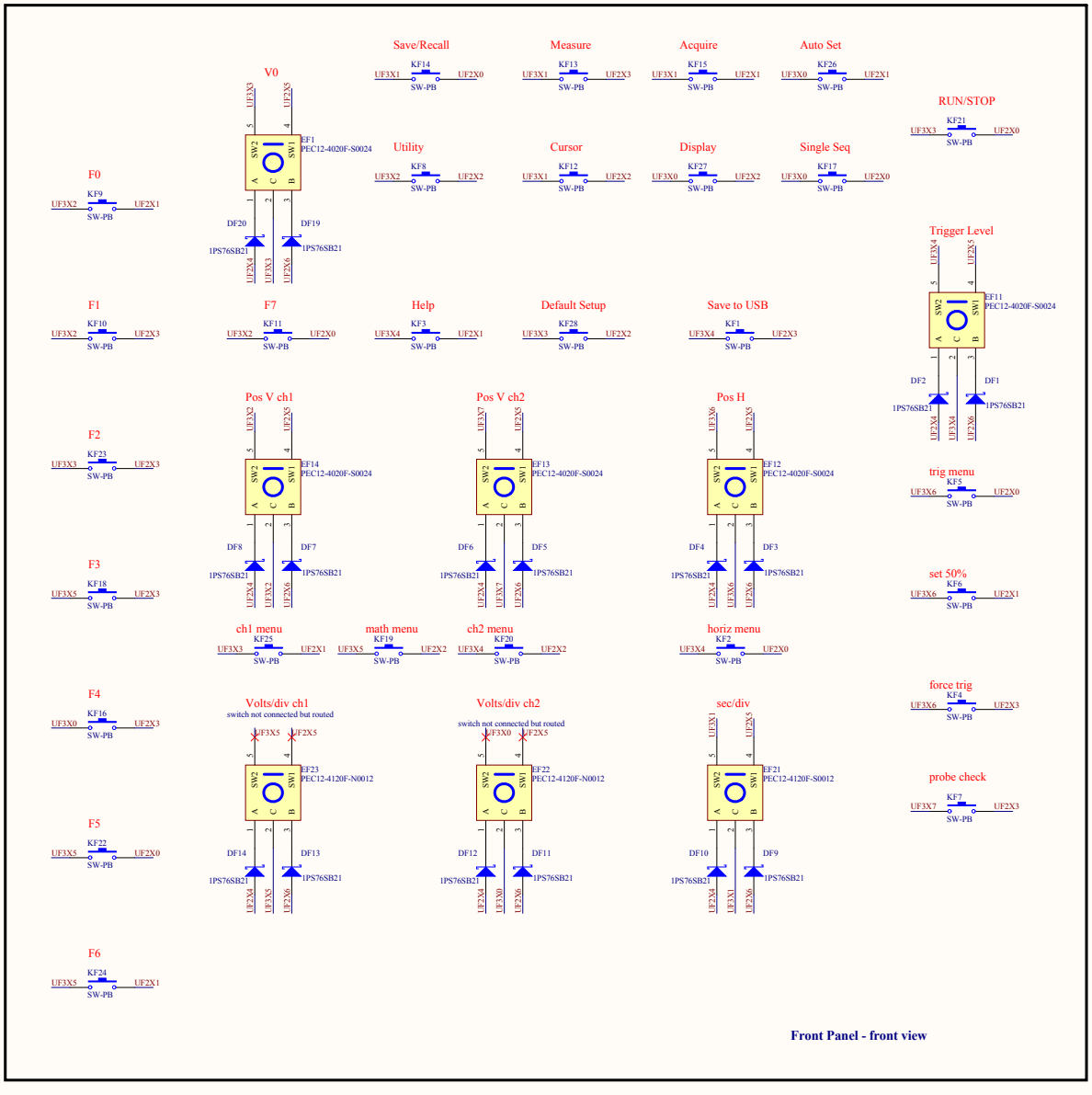
Sample/Hold Offset Control

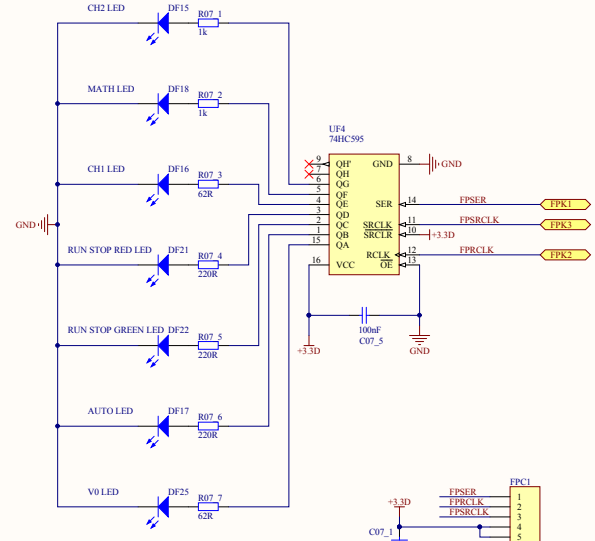


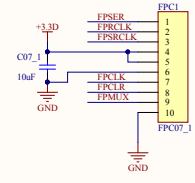
FPGA Circuit

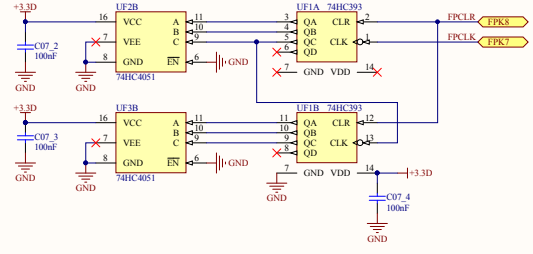


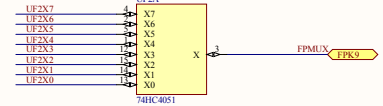
Front Panel Circuit

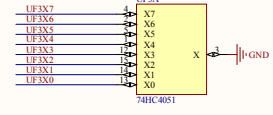




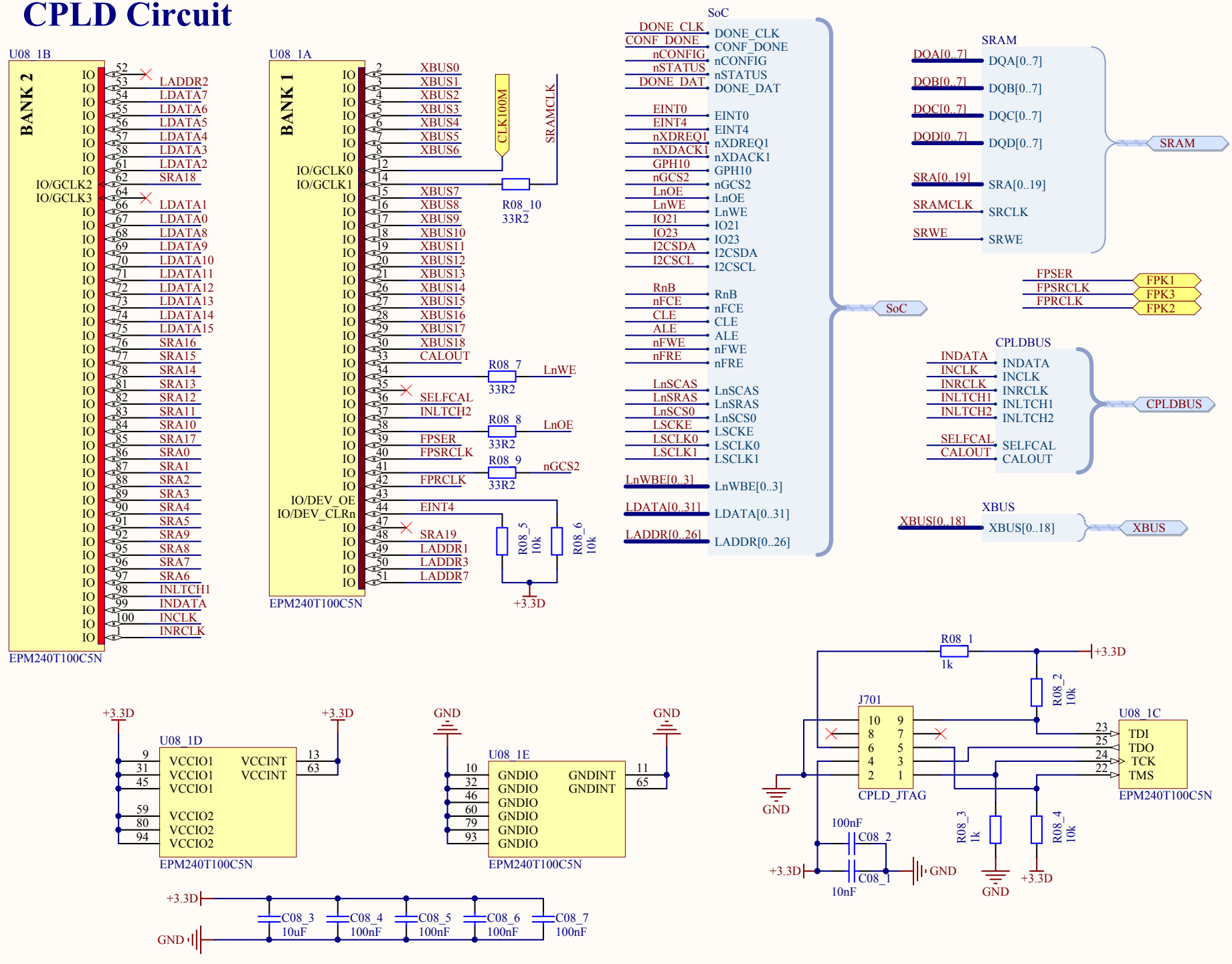




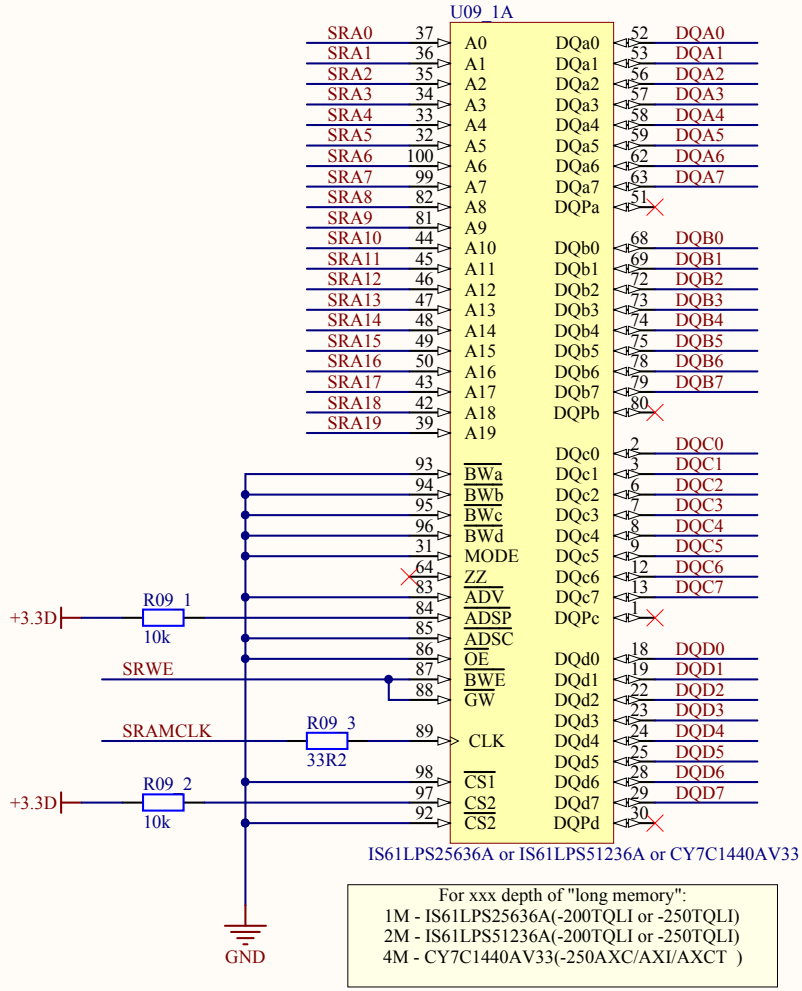


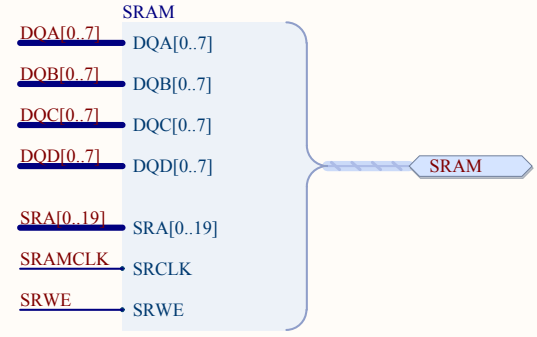


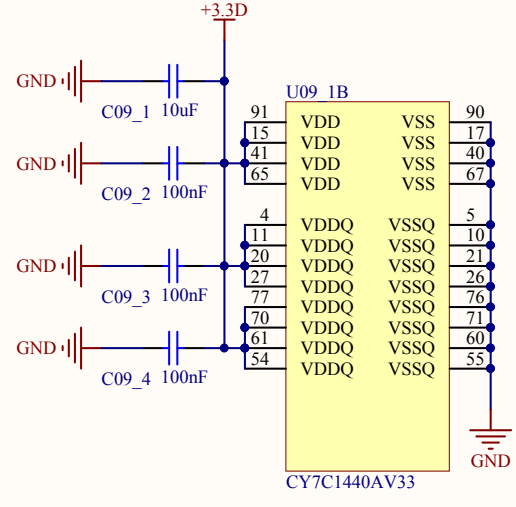
CPLD Circuit

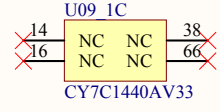


SRAM Circuit

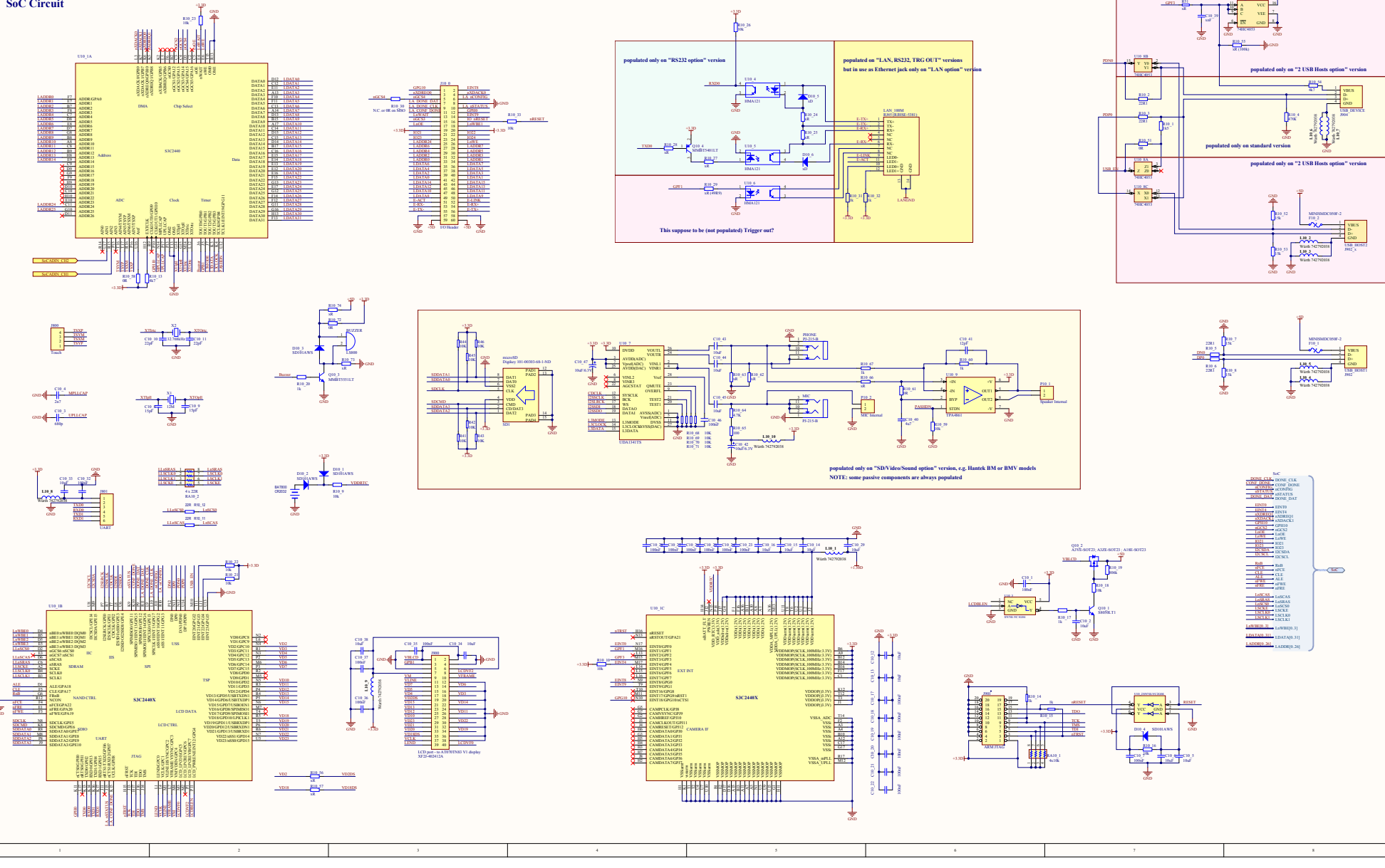




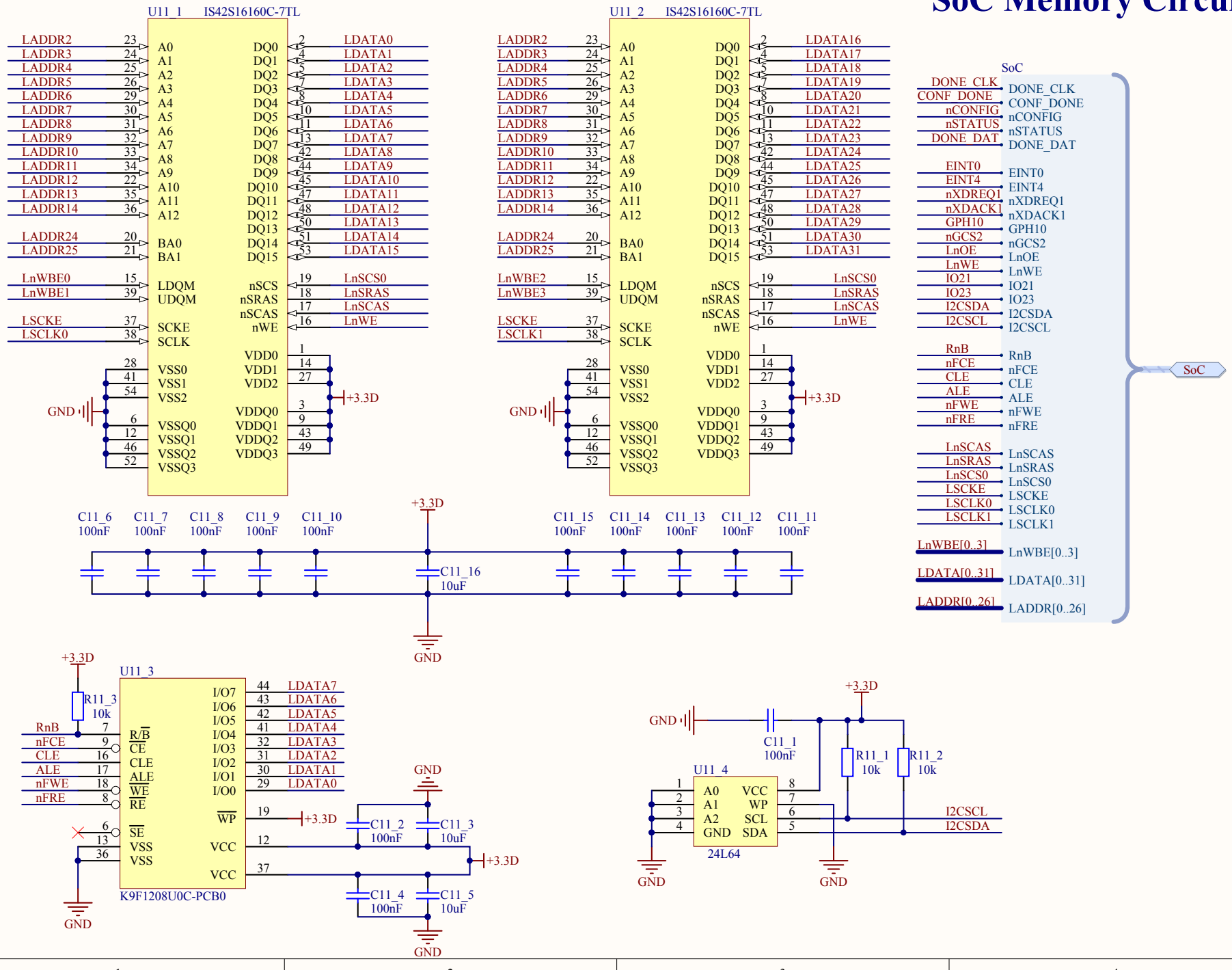




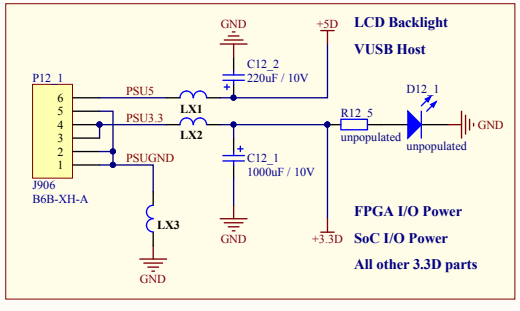
SoC Circuit

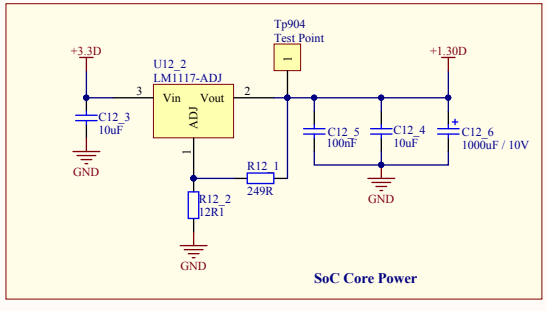

populated only on "RS232 option" version
populated on "LAN, RS232, TRG OUT" versions
but in use as Ethernet jack only on "LAN option" version
This suppose to be (not populated) Trigger out?
populated only on "2 USB Hosts option" version
populated only on standard version
populated only on "2 USB Hosts option" version
populated only on "SD/Video/Sound option" version, e.g. Hantek BM or BMV models
NOTE: some passive components are always populated
S3C2440
S3C2440X
SoC

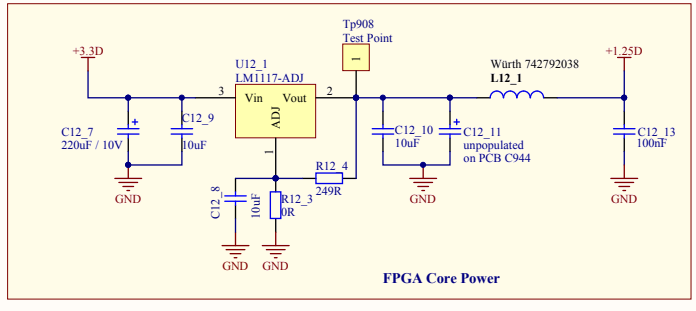
SoC Memory Circuit

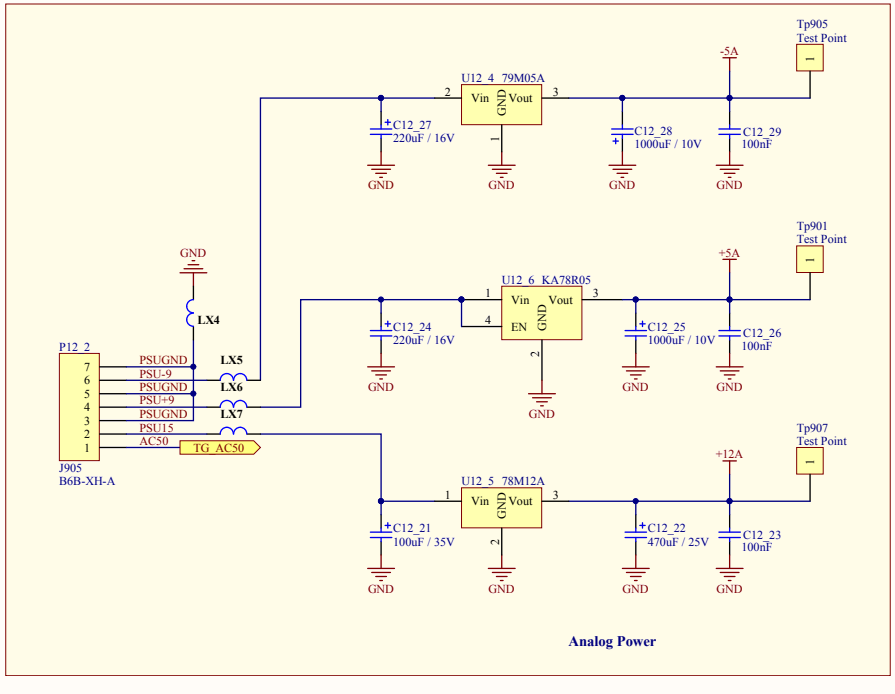


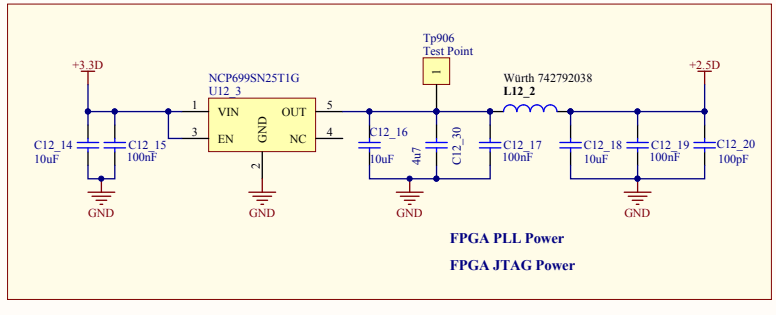
Power Distribution Circuit

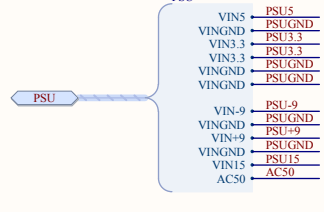


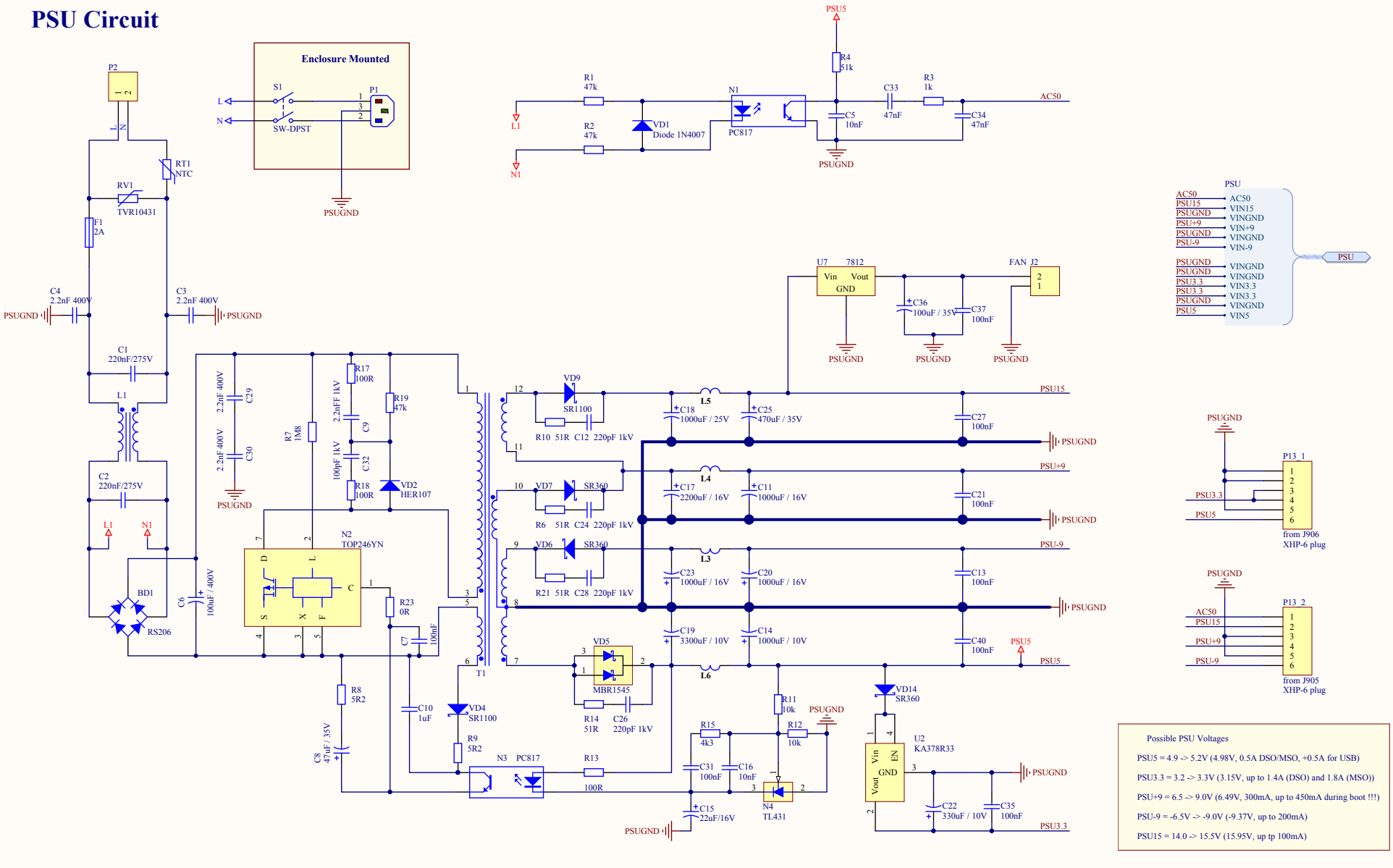




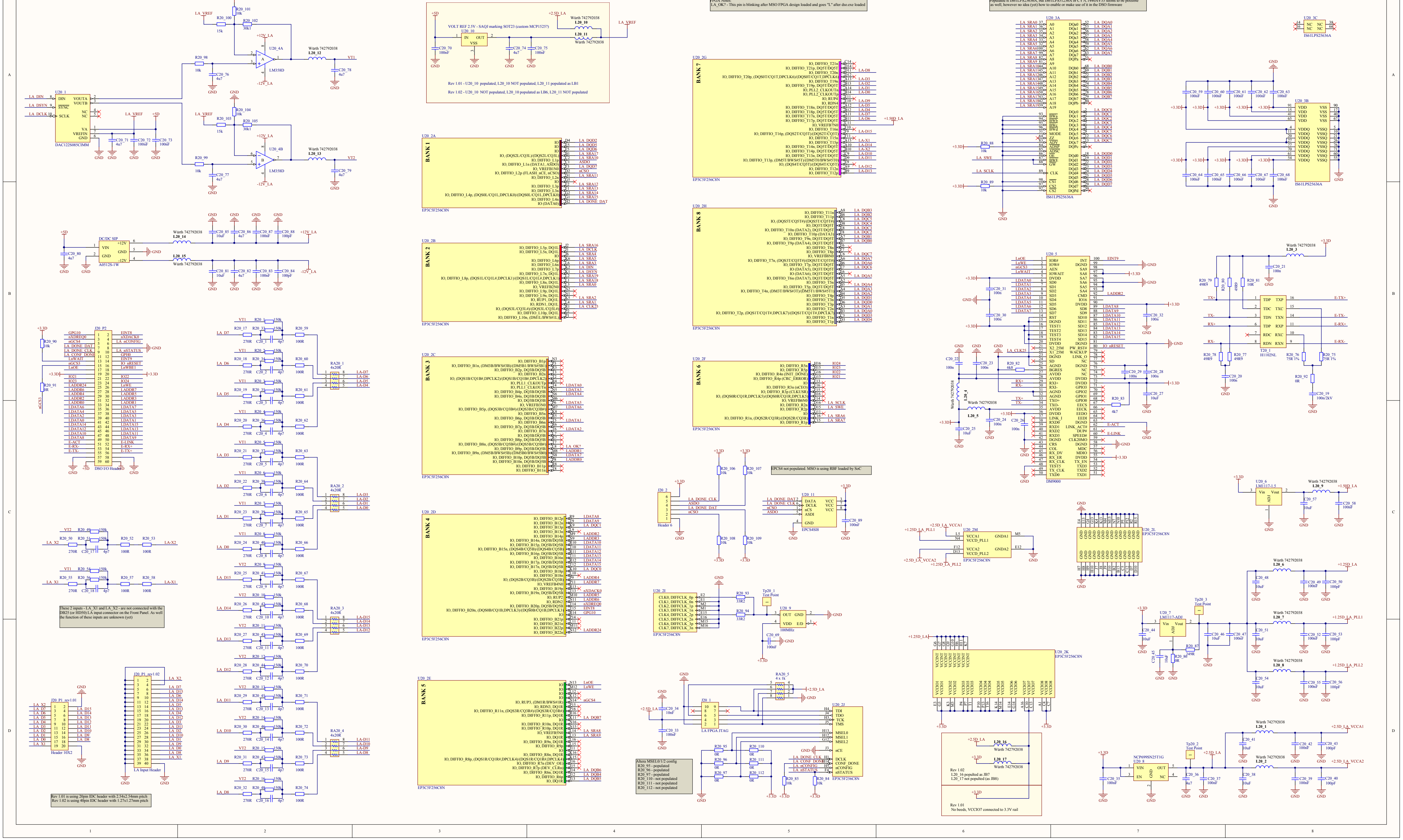




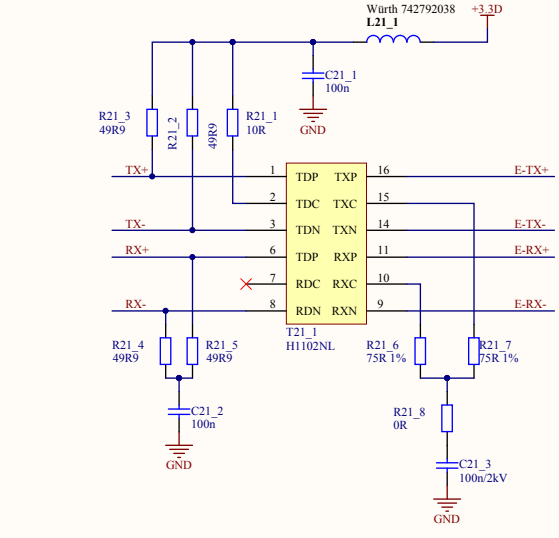


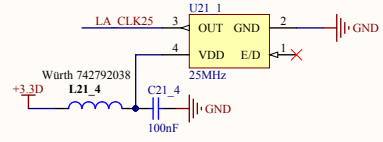

PSU Circuit
Enclosure Mounted
P2
S1
SW-DPST
P1
L
N
PSUGND
RT1
NTC
RV1
TVR10431
F1
2A
C4
2.2nF 400V
C3
2.2nF 400V
C1
220nF/275V
L1
C2
220nF/275V
BD1
RS206
C6
100uF / 400V
C29
C30
R7
1M8
R17
100R
R18
100R
2.2nF 1kV
C9
100pF 1kV
C32
R19
47k
VD2
HER107
N2
TOP246YN
R23
0R
C7
100nF
R8
5R2
C10
1uF
C8
47uF / 35V
VD4
SR1100
R9
5R2
T1
PSU5
R1
47k
R2
47k
VD1
Diode 1N4007
N1
PC817
R4
51k
C5
10nF
C33
47nF
R3
1k
C34
47nF
AC50
U7
7812
Vin
Vout
GND
C36
100uF / 35V
C37
100nF
FAN
J2
VD9
SR1100
R10 51R C12 220pF 1kV
C18
1000uF / 25V
L5
C25
470uF / 35V
C27
100nF
PSU15
VD7
SR360
R6 51R C24 220pF 1kV
C17
2200uF / 16V
L4
C11
1000uF / 16V
C21
100nF
PSU+9
VD6
SR360
R21 51R C28 220pF 1kV
C23
1000uF / 16V
L3
C20
1000uF / 16V
C13
100nF
PSU-9
C19
3300uF / 10V
C14
1000uF / 10V
C40
100nF
PSU5
L6
VD5
MBR1545
R14
51R
C26
220pF 1kV
R11
10k
R12
10k
R15
4k3
C31
100nF
C16
10nF
N3
PC817
R13
100R
N4
TL431
C15
22uF/16V
VD14
SR360
U2
KA378R33
Vin
EN
GND
Vout
C22
330uF / 10V
C35
100nF
PSU3.3
PSU
AC50
PSU15
PSUGND
PSU+9
PSUGND
PSU-9
PSUGND
PSUGND
PSU3.3
PSU3.3
PSUGND
PSU5
VIN15
VINGND
VIN+9
VINGND
VIN-9
VINGND
VINGND
VIN3.3
VIN3.3
VINGND
VIN5
P13_1
from J906
XHP-6 plug
P13_2
from J905
XHP-6 plug
Possible PSU Voltages
PSU5 = 4.9 -> 5.2V (4.98V, 0.5A DSO/MSO, +0.5A for USB)
PSU3.3 = 3.2 -> 3.3V (3.15V, up to 1.4A (DSO) and 1.8A (MSO))
PSU+9 = 6.5 -> 9.0V (6.49V, 300mA, up to 450mA during boot !!!)
PSU-9 = -6.5V -> -9.0V (-9.37V, up to 200mA)
PSU15 = 14.0 -> 15.5V (15.95V, up tp 100mA)

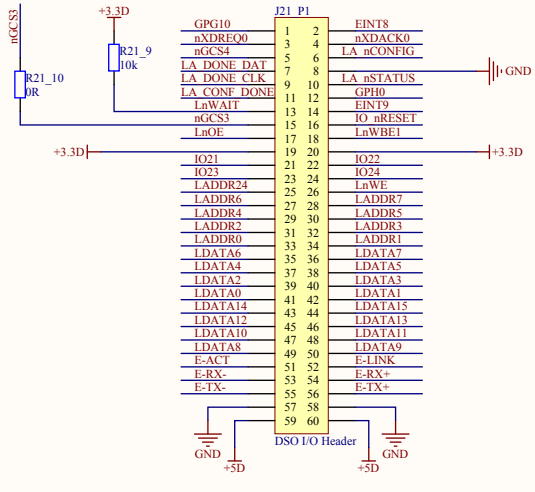
Option MSO (LAN/LA PCB)

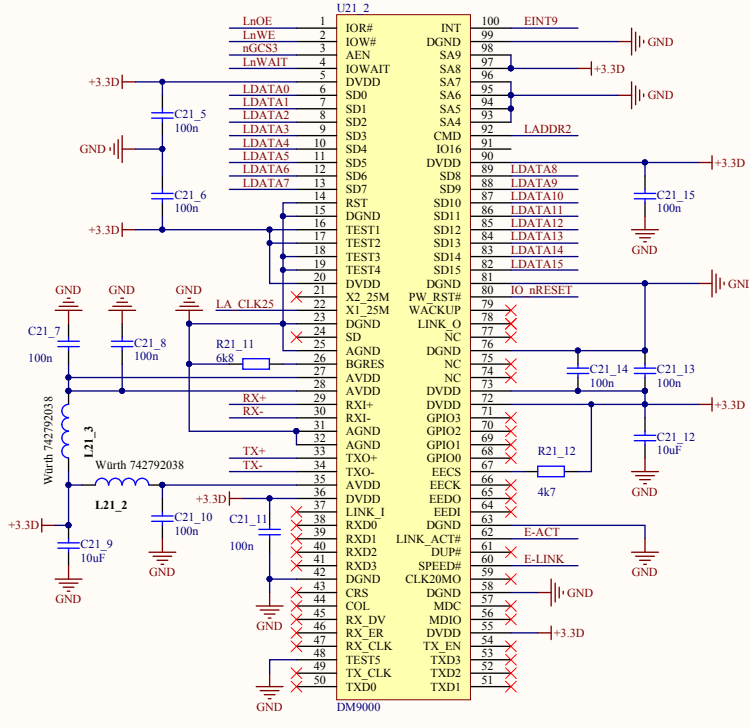


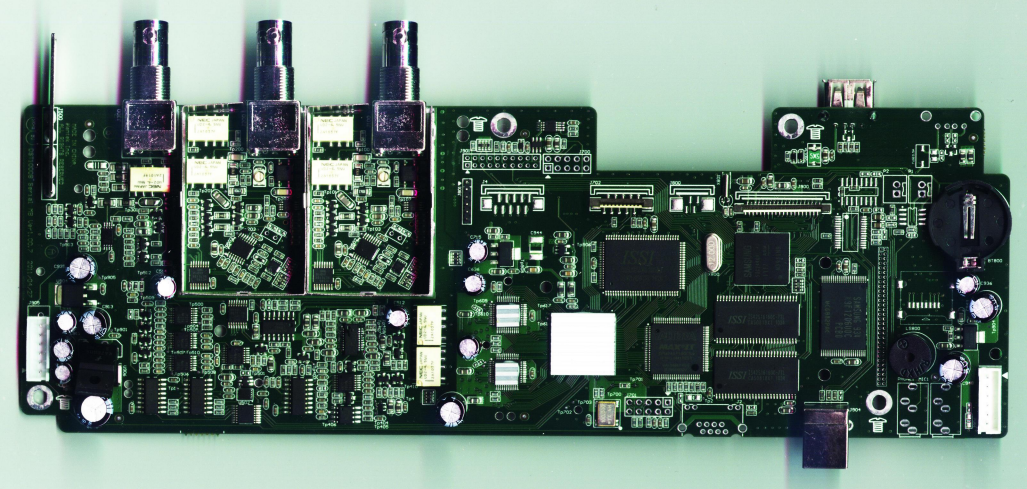
Option LAN

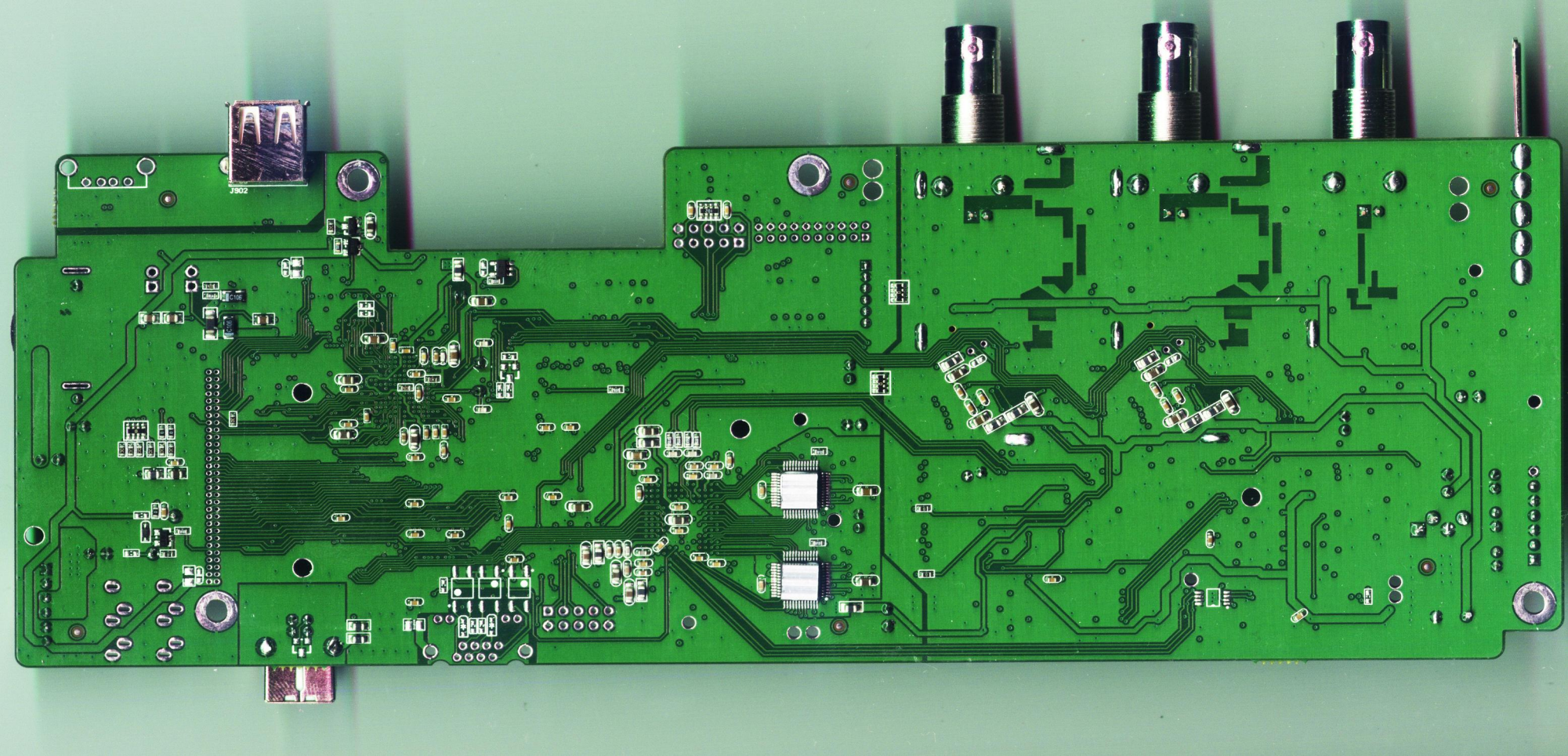

Würth 742792038
L21_1
+3.3D
C21_1
100n
GND
R21_3
49R9
R21_2
49R9
R21_1
10R
TX+
TX-
RX+
RX-
TDP TXP
TDC TXC
TDN TXN
TDP RXP
RDC RXC
RDN RXN
E-TX+
E-TX-
E-RX+
E-RX-
T21_1
H1102NL
R21_4
49R9
R21_5
49R9
R21_6
75R 1%
R21_7
75R 1%
C21_2
100n
R21_8
0R
C21_3
100n/2kV


U21_1
LA_CLK25
OUT GND
VDD E/D
25MHz
GND
Würth 742792038
L21_4
+3.3D
C21_4
100nF


J21_P1
nGCS3
+3.3D
R21_9
10k
R21_10
0R
GPG10
nXDREQ0
nGCS4
LA_DONE_DAT
LA_DONE_CLK
LA_CONF_DONE
LnWAIT
nGCS3
LnOE
EINT8
nXDACK0
LA_nCONFIG
LA_nSTATUS
GPH0
EINT9
IO_nRESET
LnWBE1
IO21
IO23
LADDR24
LADDR6
LADDR4
LADDR2
LADDR0
LDATA6
LDATA4
LDATA2
LDATA0
LDATA14
LDATA12
LDATA10
LDATA8
E-ACT
E-RX-
E-TX-
IO22
IO24
LnWE
LADDR7
LADDR5
LADDR3
LADDR1
LDATA7
LDATA5
LDATA3
LDATA1
LDATA15
LDATA13
LDATA11
LDATA9
E-LINK
E-RX+
E-TX+
GND
+5D
DSO I/O Header


U21_2
LnOE
LnWE
nGCS3
LnWAIT
LDATA0
LDATA1
LDATA2
LDATA3
LDATA4
LDATA5
LDATA6
LDATA7
IOR#
IOW#
AEN
IOWAIT
DVDD
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
RST
DGND
TEST1
TEST2
TEST3
TEST4
DVDD
X2_25M
X1_25M
DGND
SD
AGND
BGRES
AVDD
AVDD
RXI+
RXI-
AGND
AGND
TXO+
TXO-
AVDD
DVDD
LINK_I
RXD0
RXD1
RXD2
RXD3
DGND
CRS
COL
RX_DV
RX_ER
RX_CLK
TEST5
TX_CLK
TXD0
INT
DGND
SA9
SA8
SA7
SA6
SA5
SA4
CMD
IO16
DVDD
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
DGND
PW_RST#
WACKUP
LINK_O
NC
DGND
NC
NC
DVDD
DVDD
GPIO3
GPIO2
GPIO1
GPIO0
EECS
EECK
EEDO
EEDI
DGND
LINK_ACT#
DUP#
SPEED#
CLK20MO
DGND
MDC
MDIO
DVDD
TX_EN
TXD3
TXD2
TXD1
EINT9
LADDR2
LDATA8
LDATA9
LDATA10
LDATA11
LDATA12
LDATA13
LDATA14
LDATA15
IO_nRESET
E-ACT
E-LINK
DM9000
+3.3D
GND
C21_5
100n
C21_6
100n
C21_7
100n
C21_8
100n
C21_9
10uF
C21_10
100n
C21_11
100n
C21_12
10uF
C21_13
100n
C21_14
100n
C21_15
100n
R21_11
6k8
R21_12
4k7
LA_CLK25
RX+
RX-
TX+
TX-
Würth 742792038
L21_3
Würth 742792038
L21_2

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