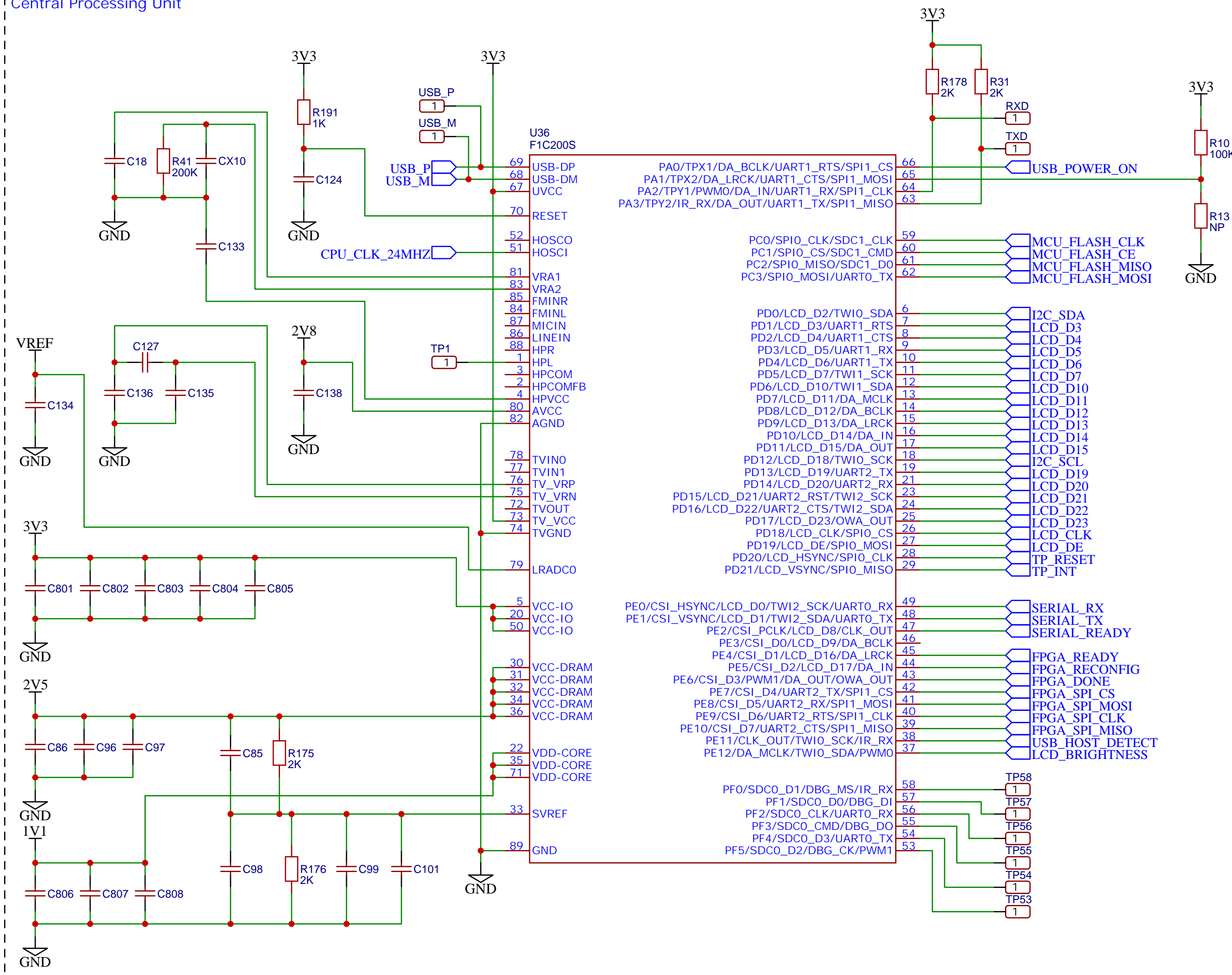
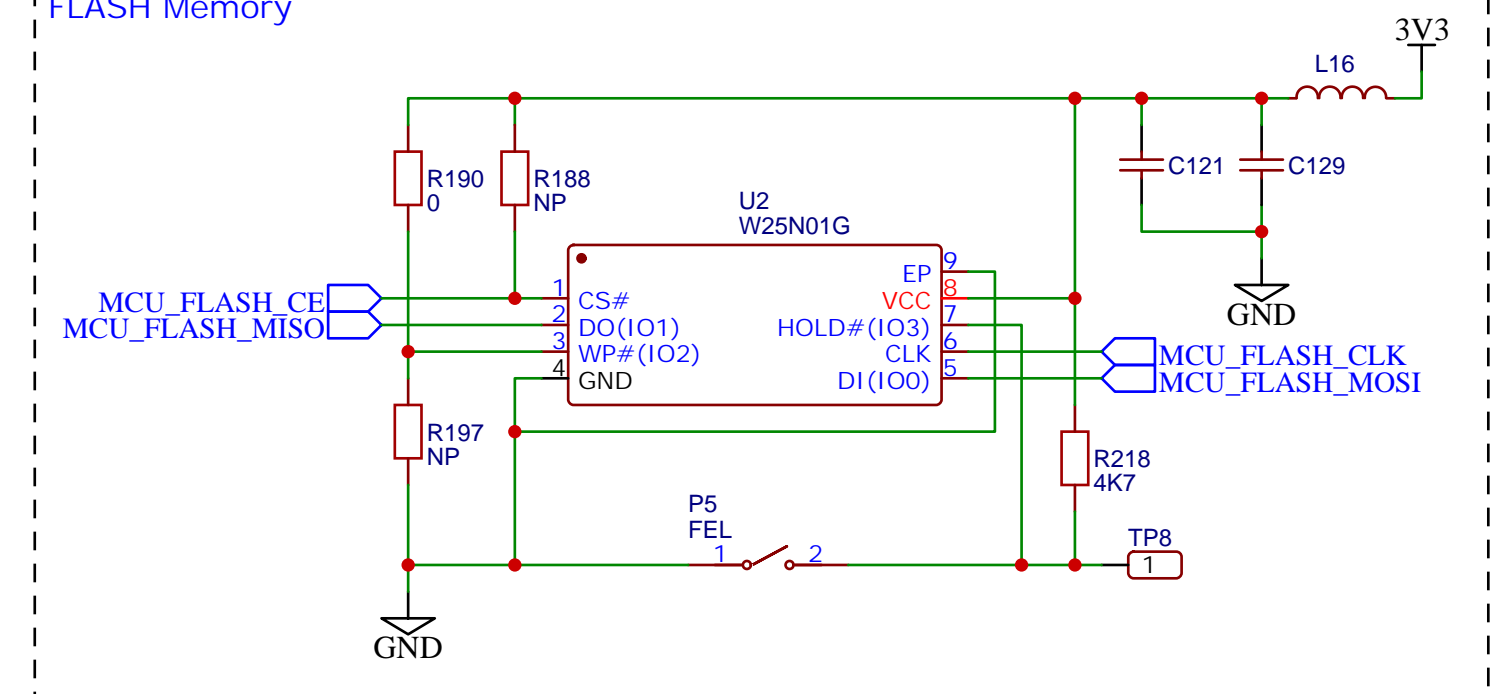


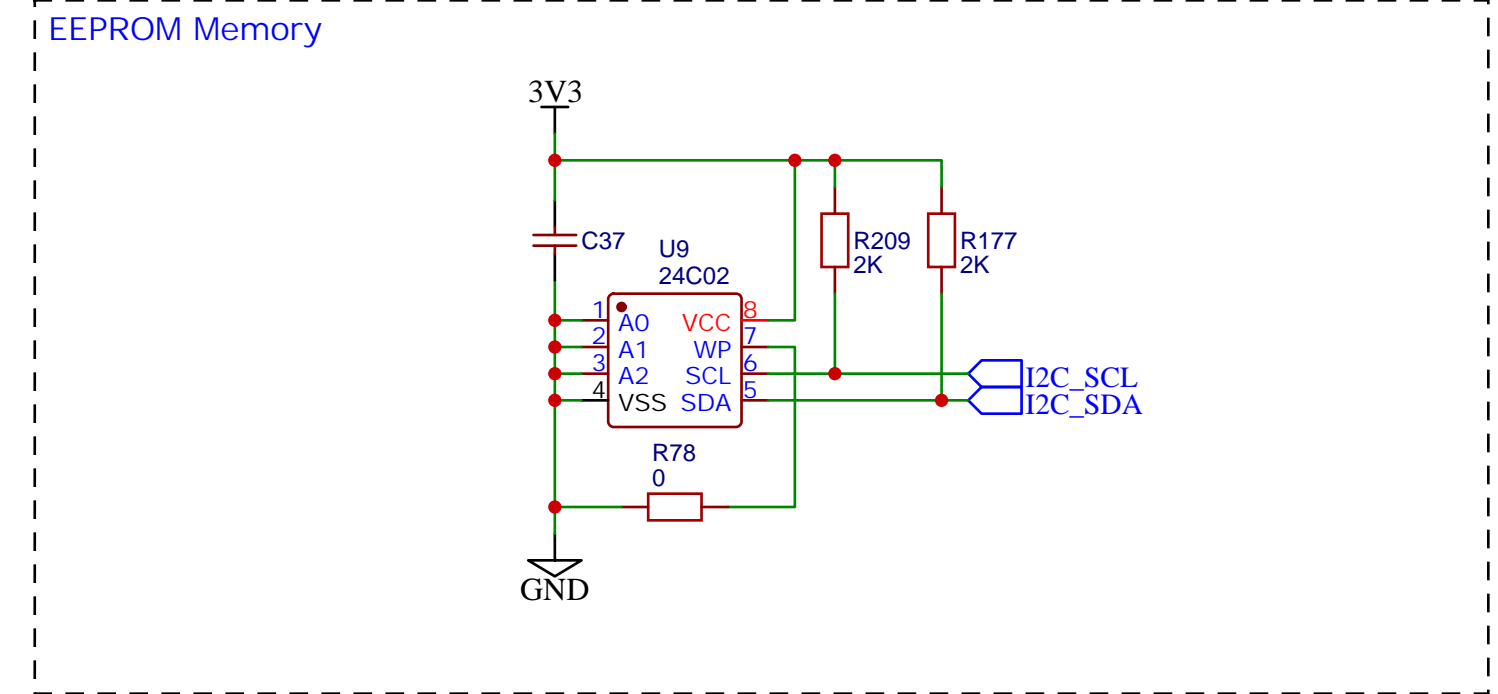
Central Processing Unit



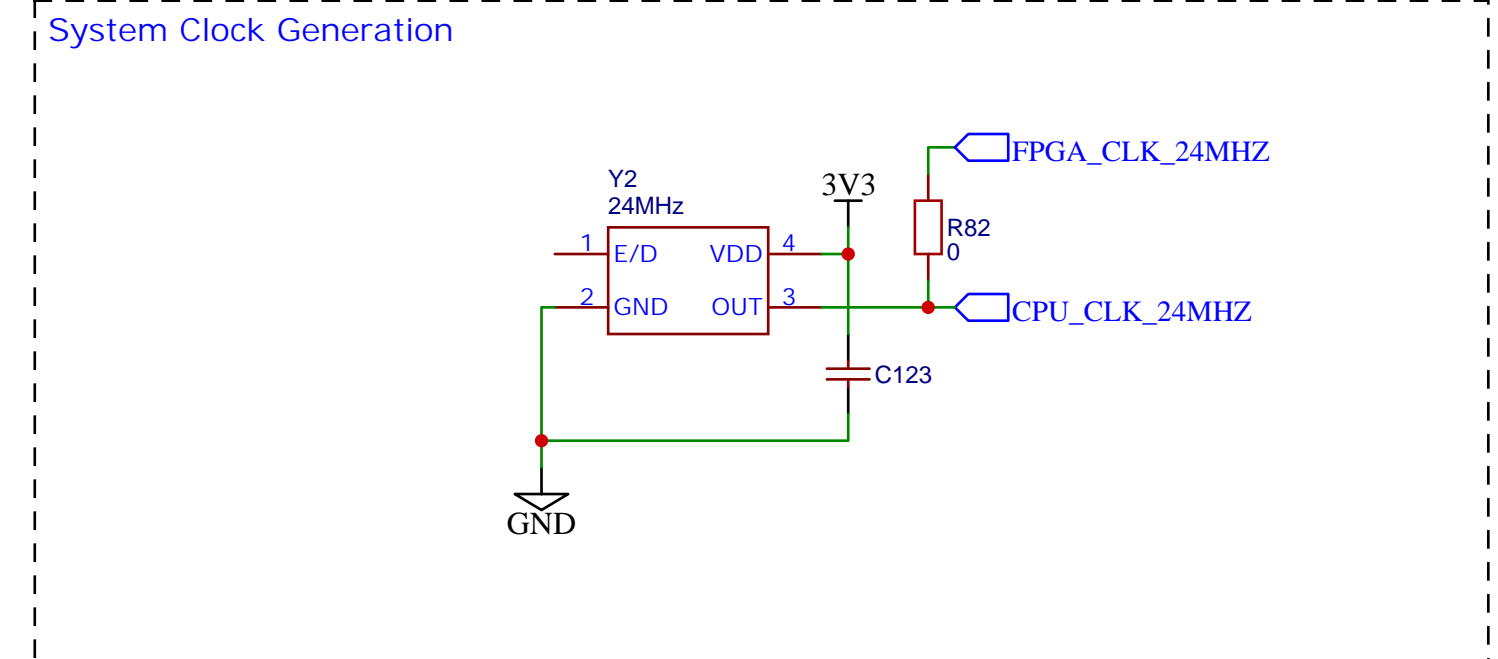
FLASH Memory

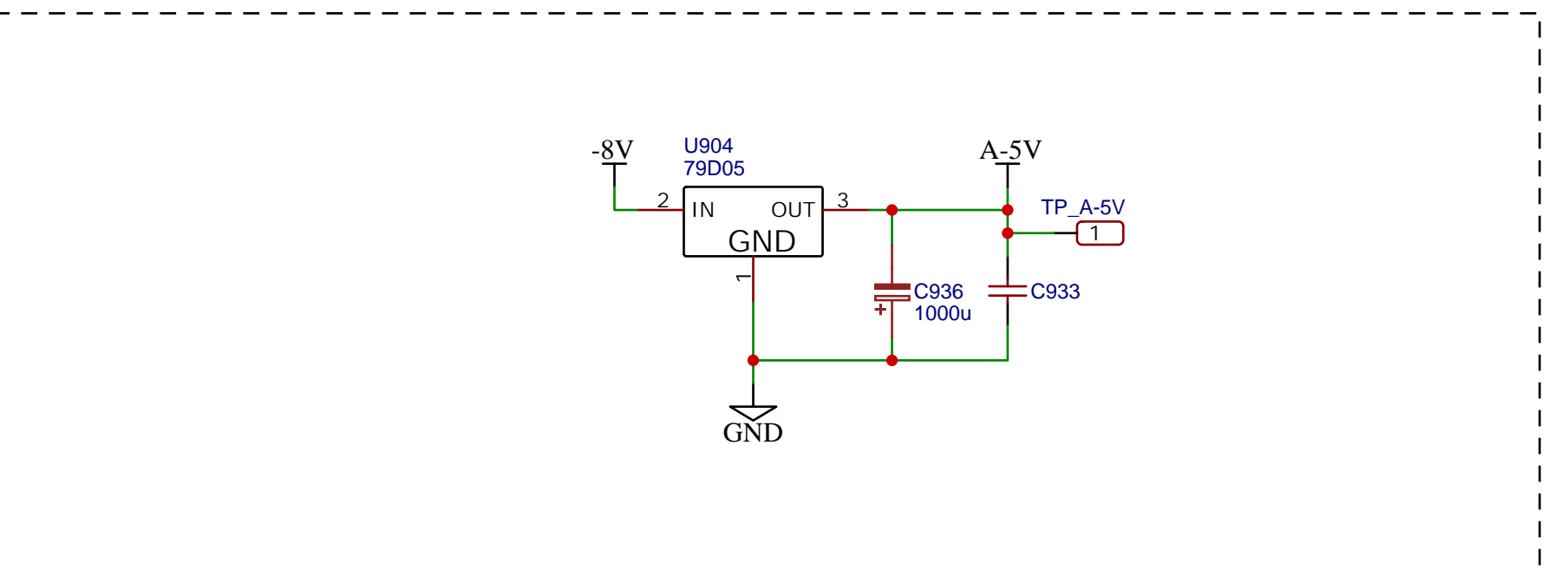
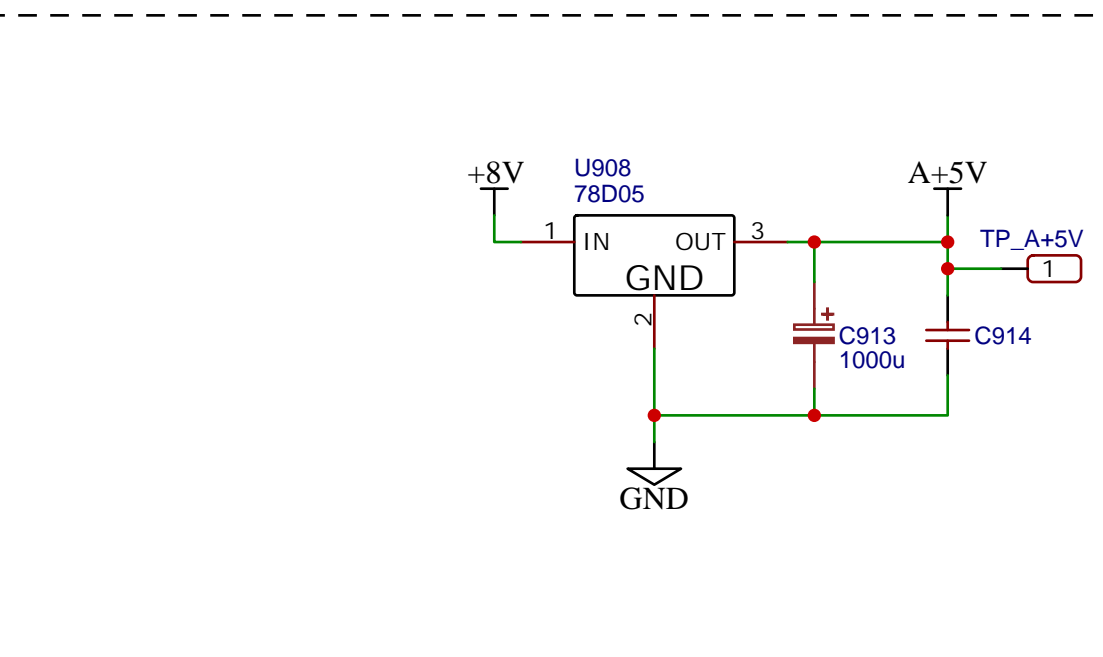
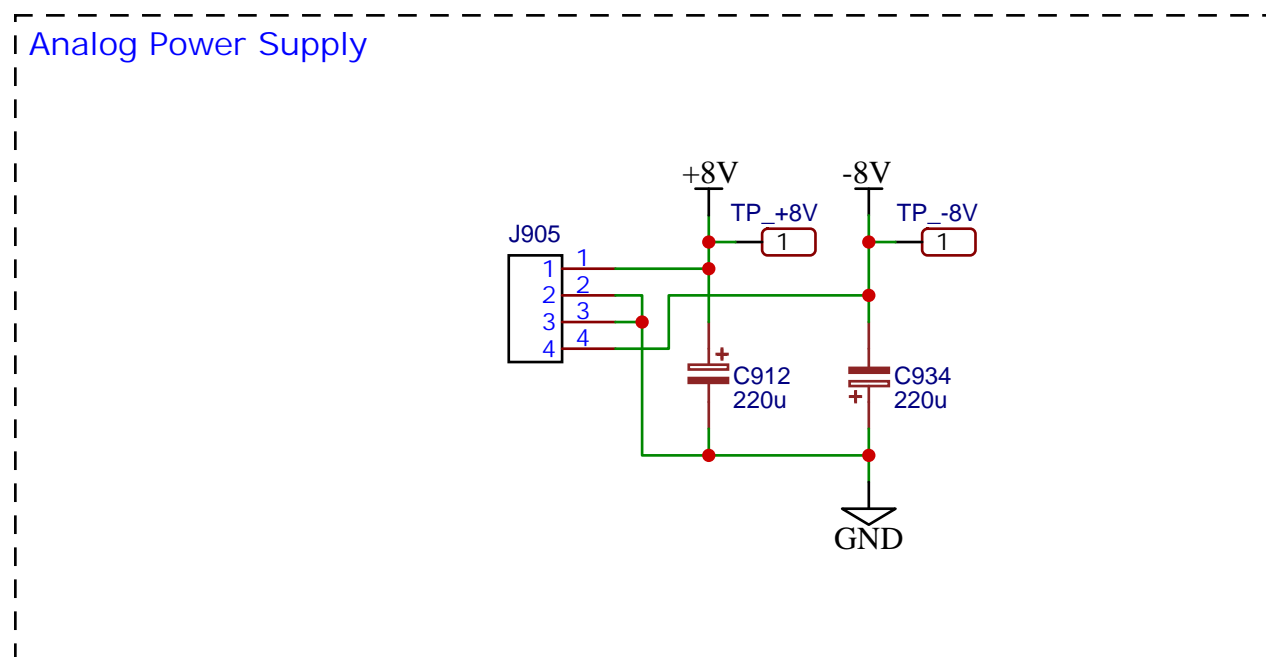
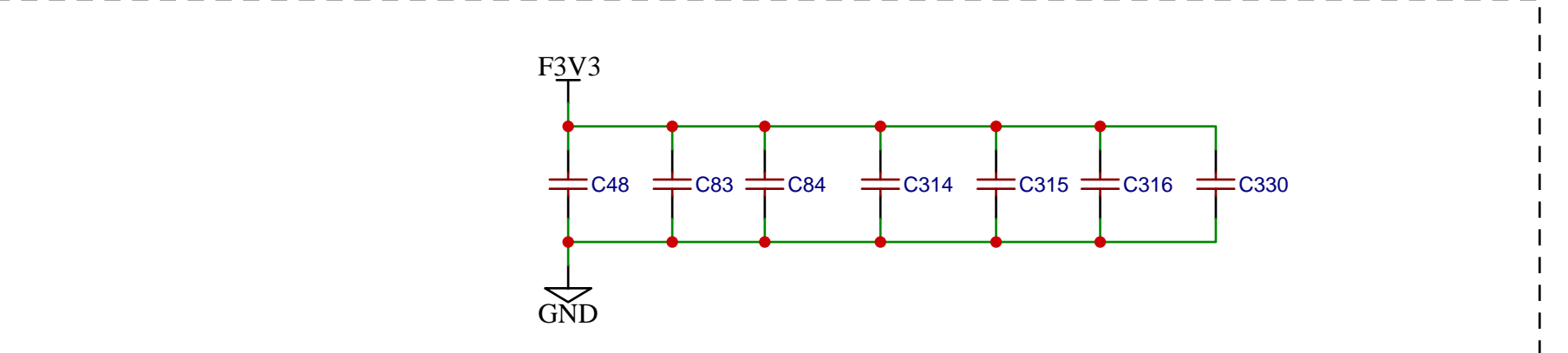
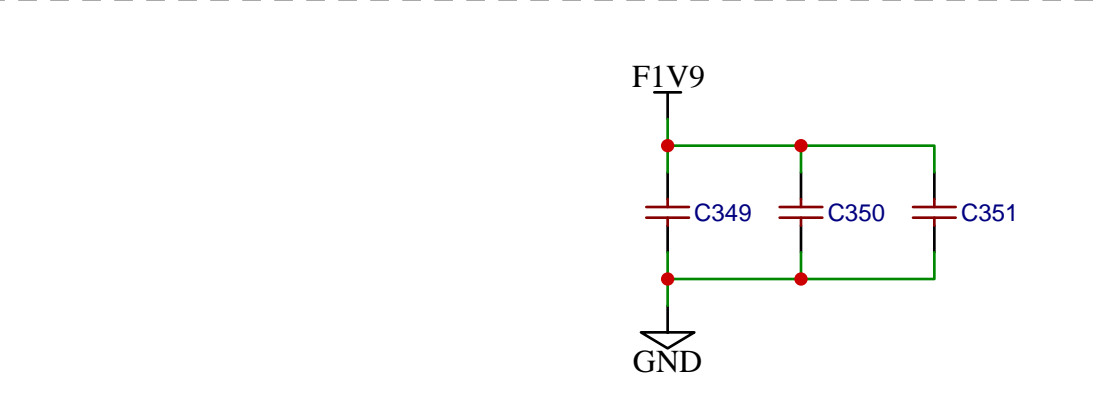
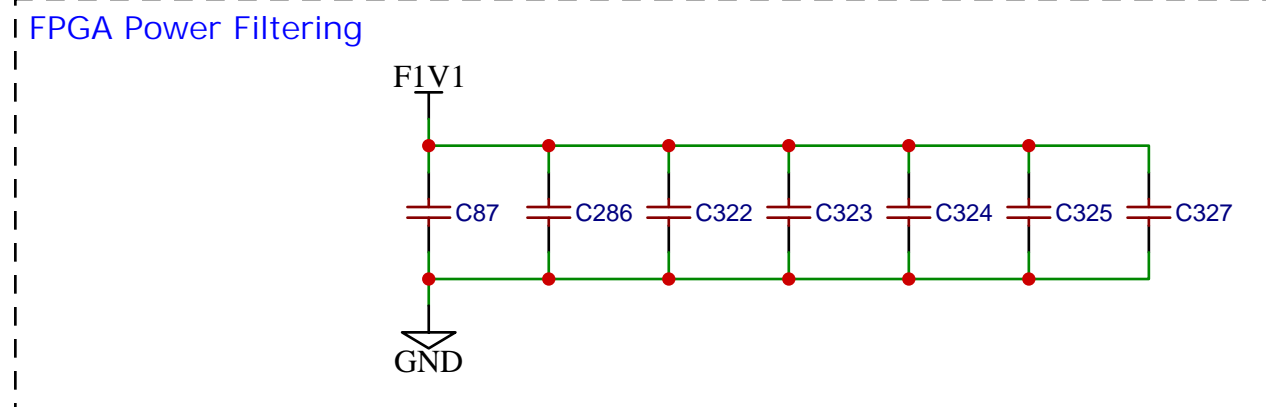
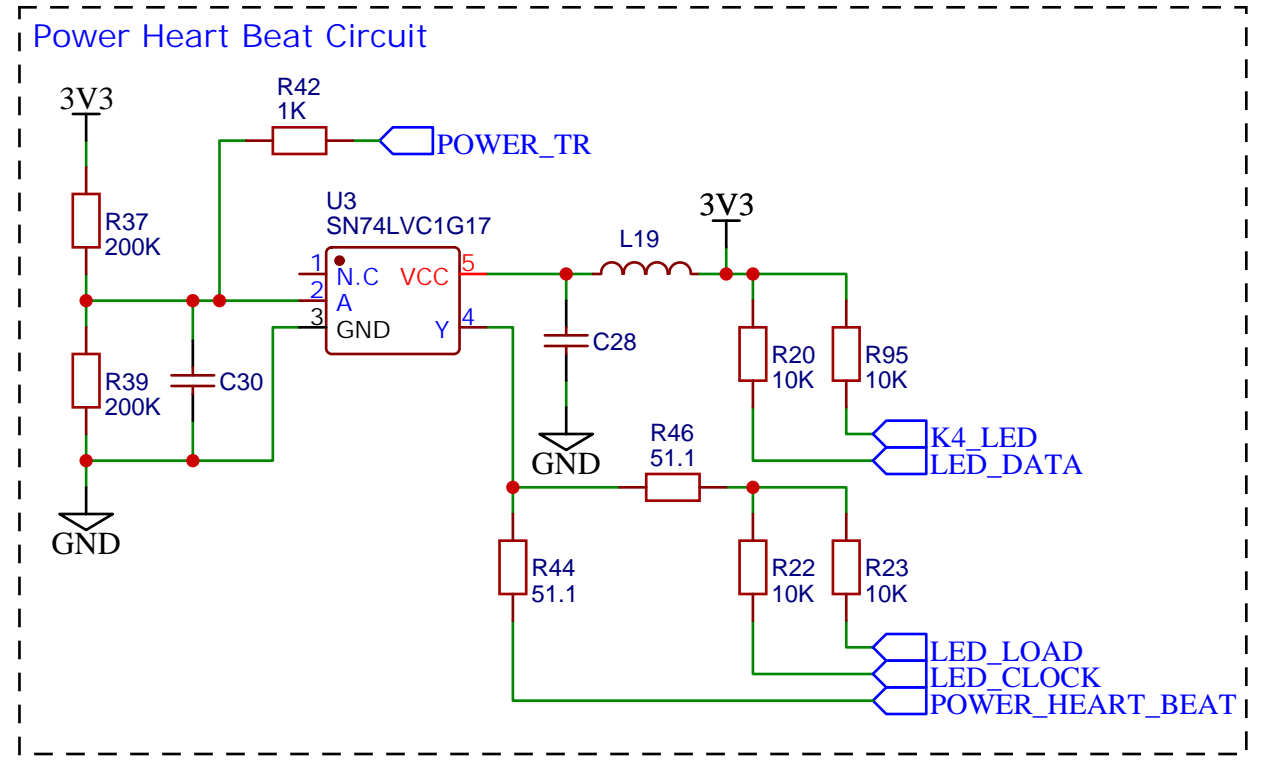
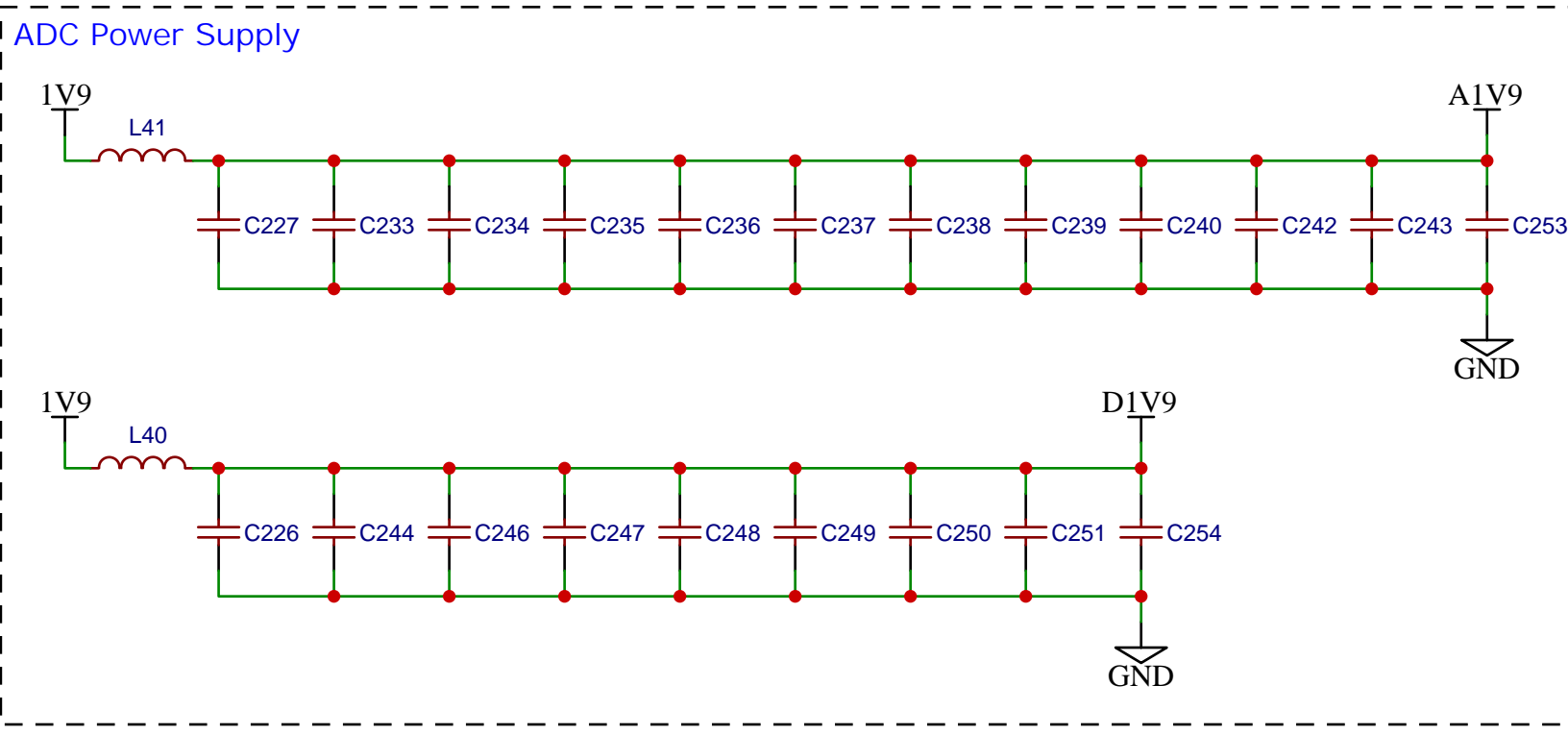
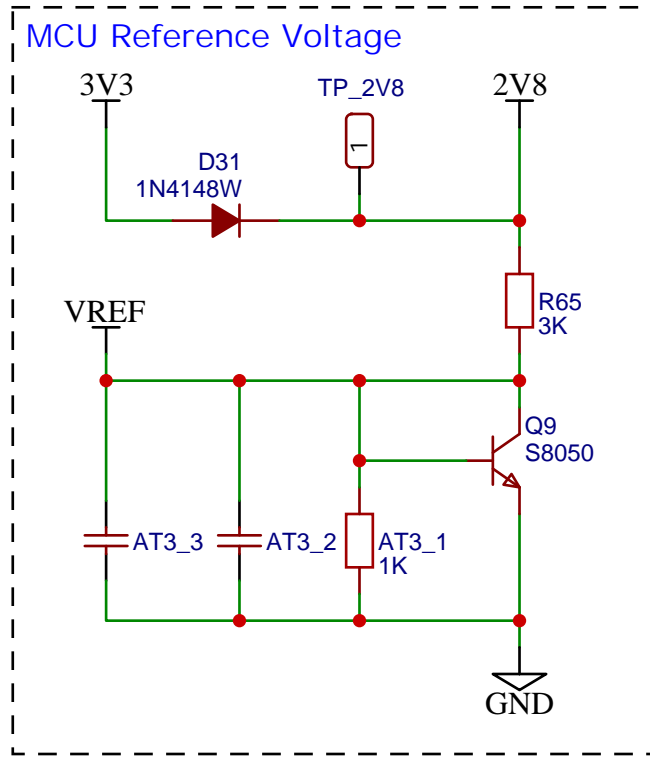
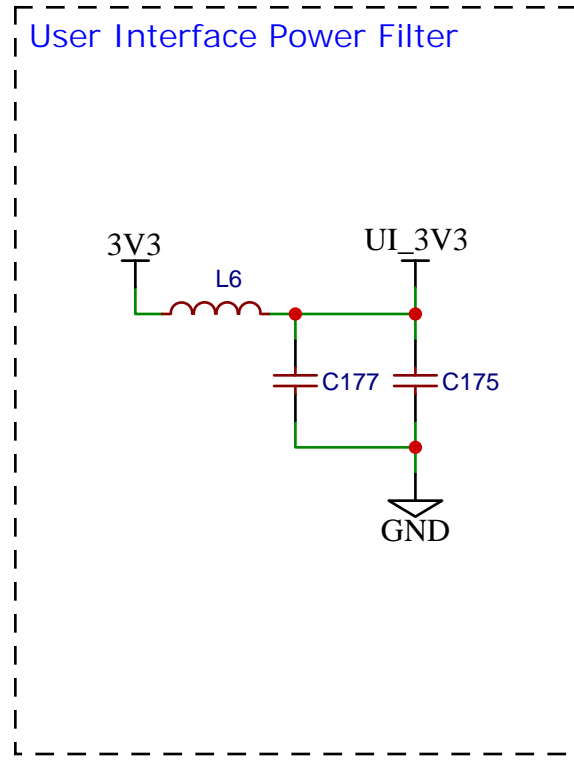
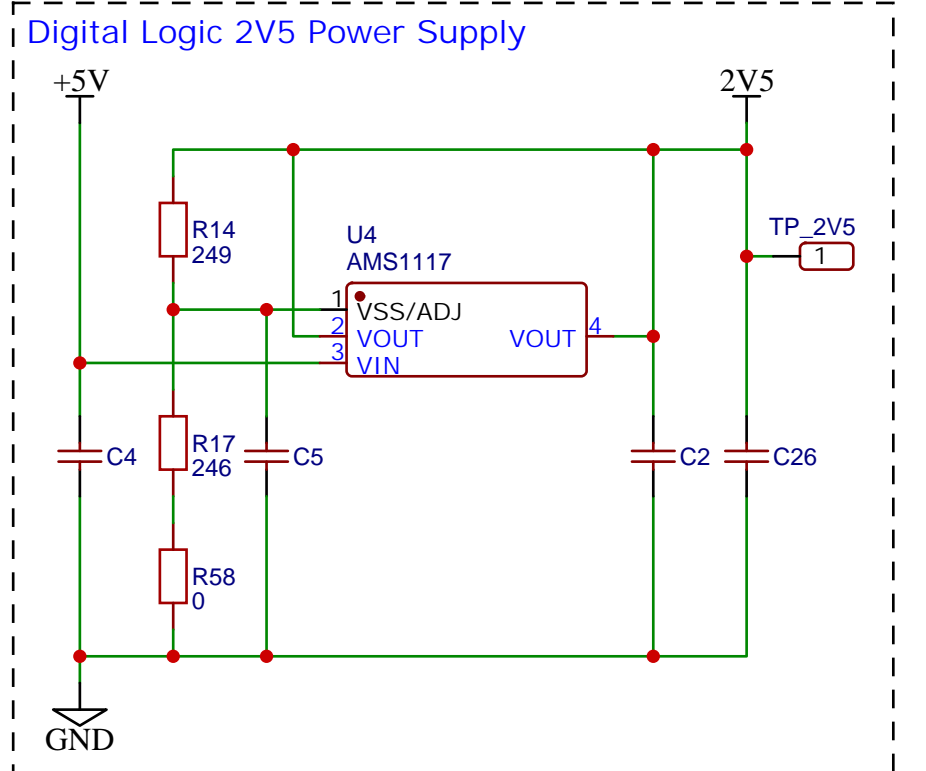
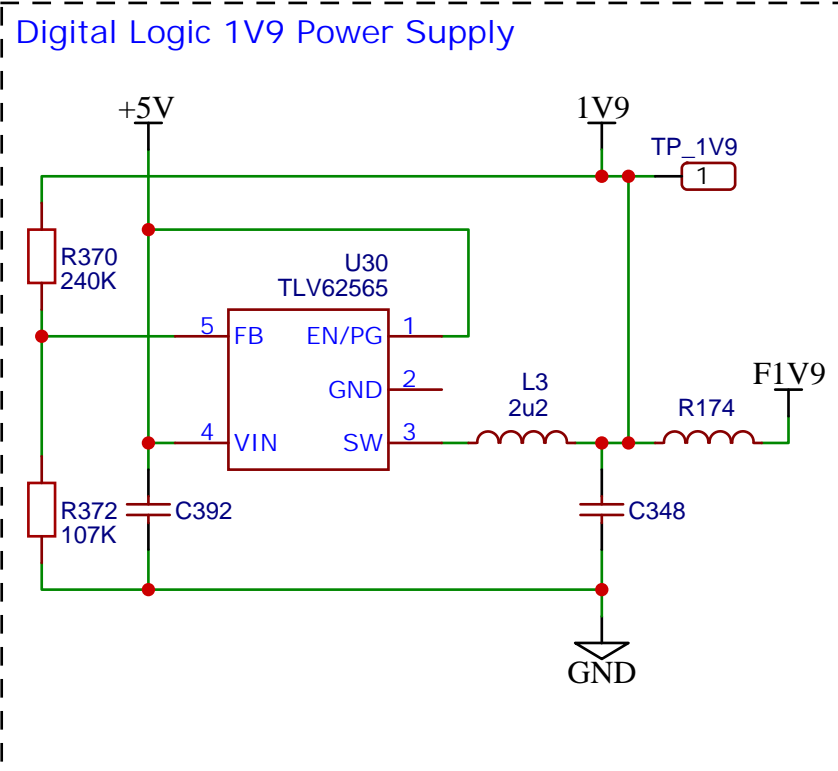
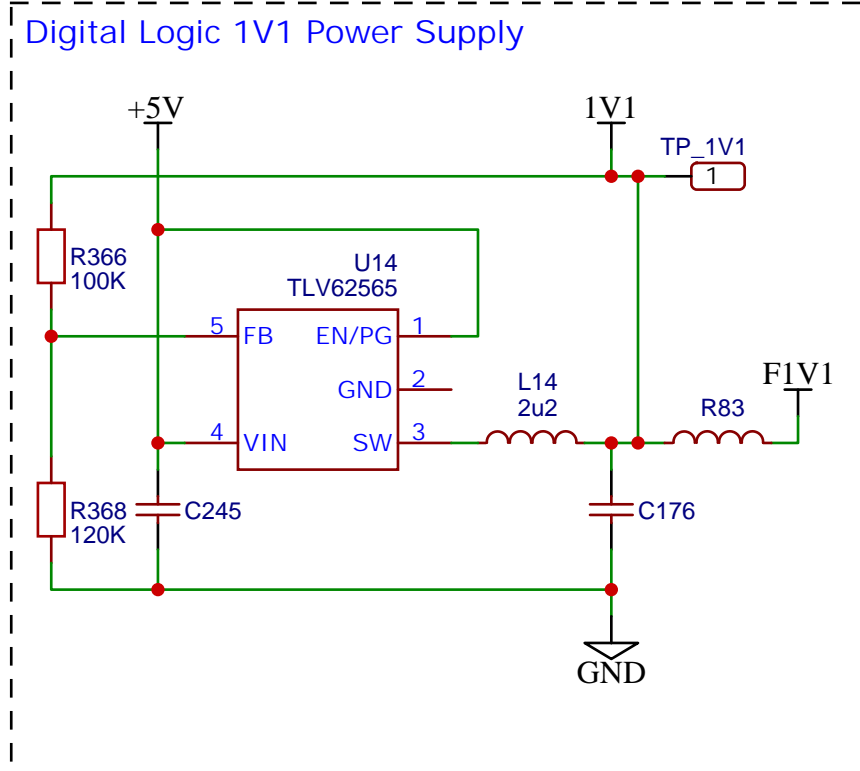
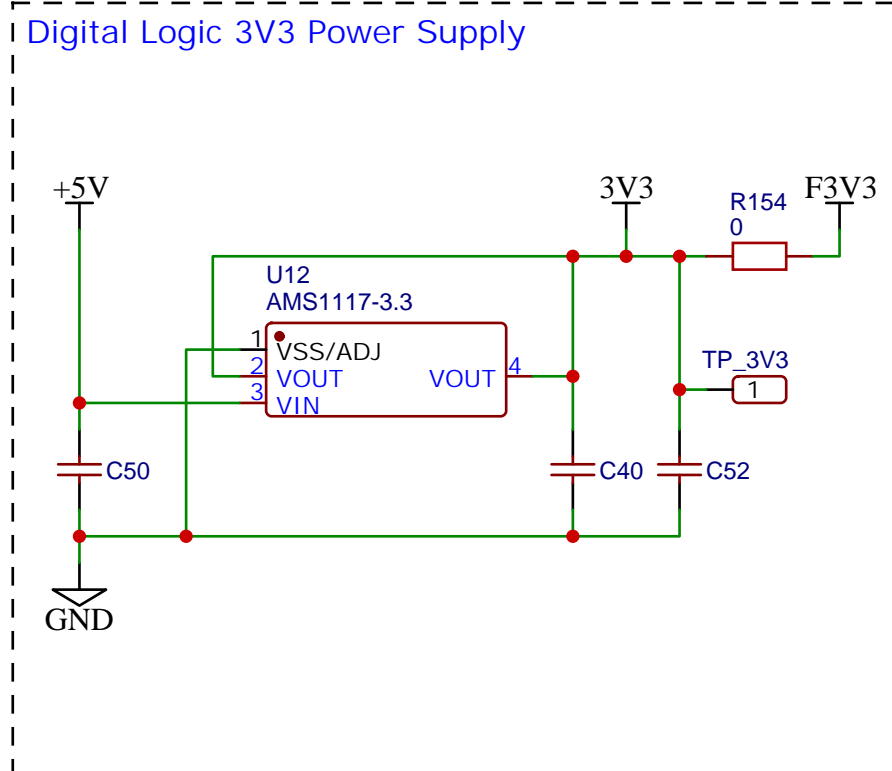
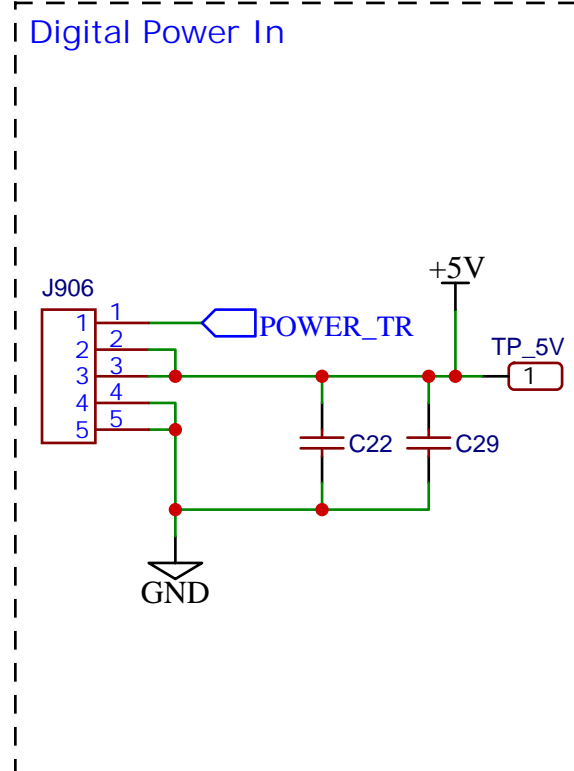


EEPROM Memory

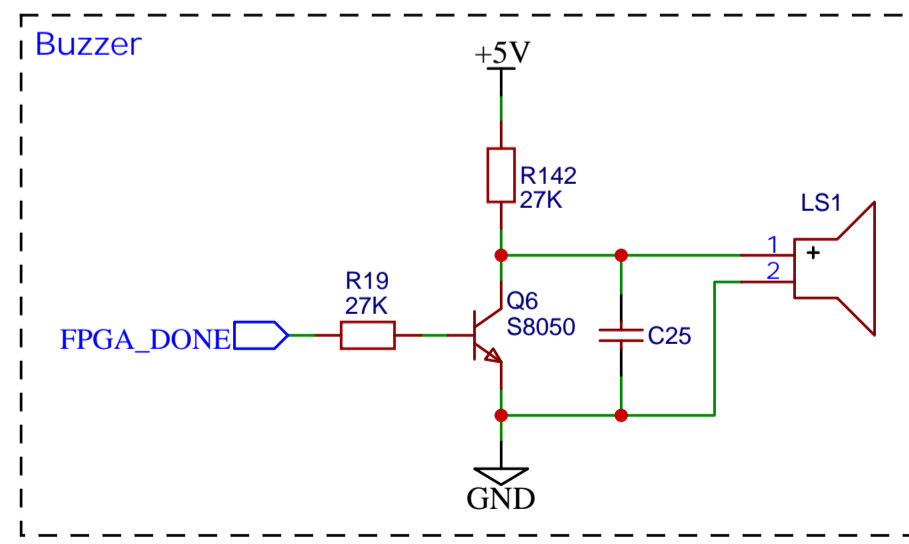
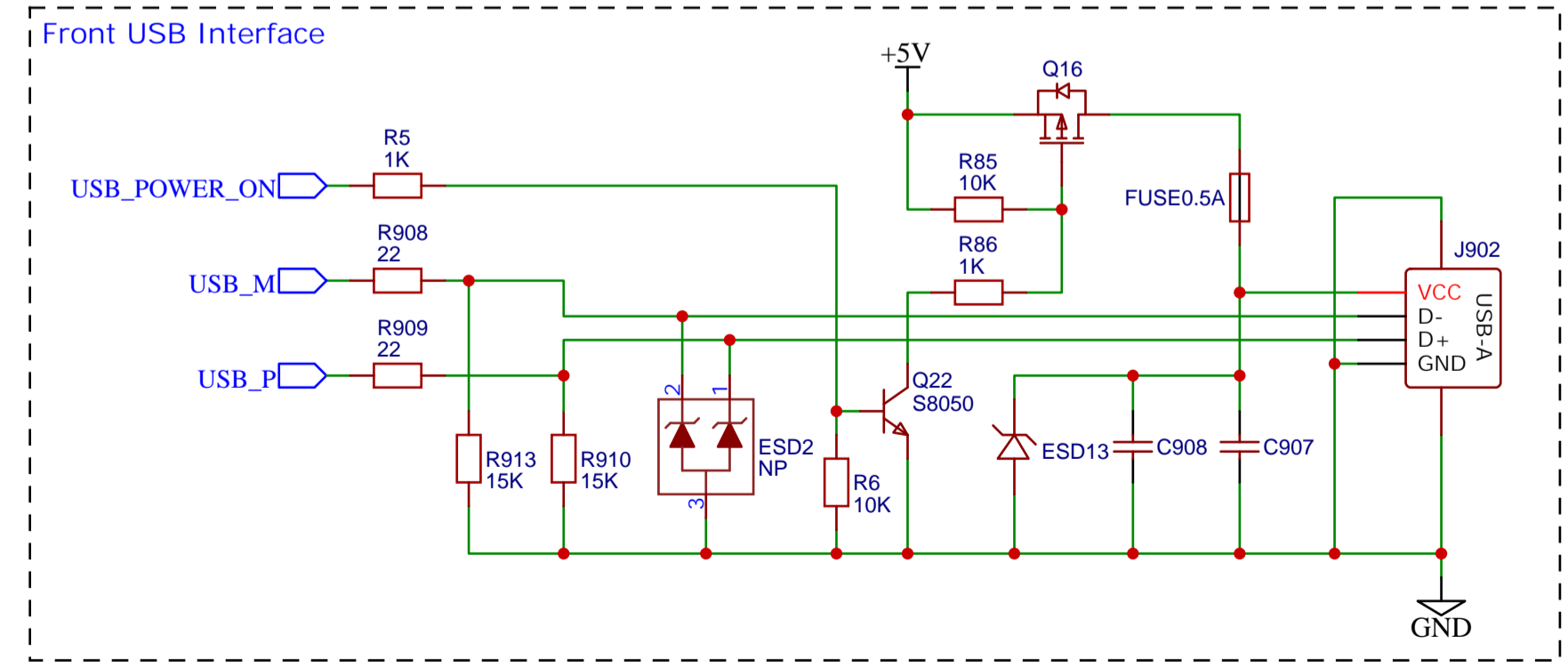
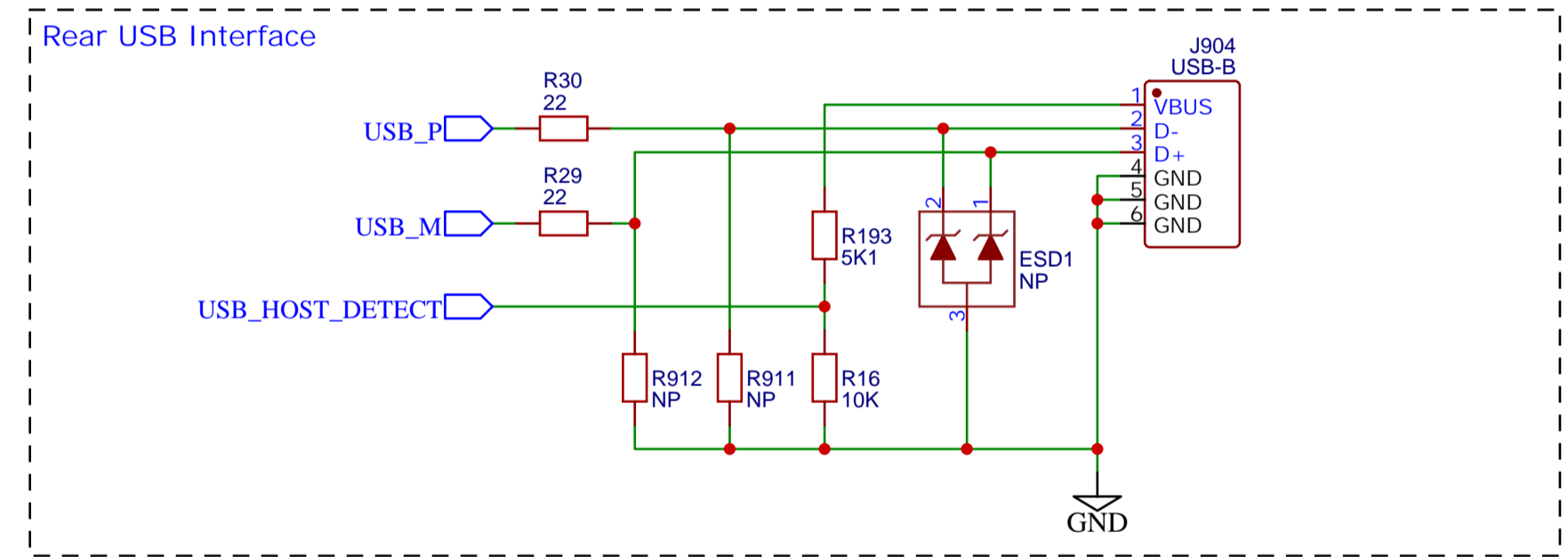
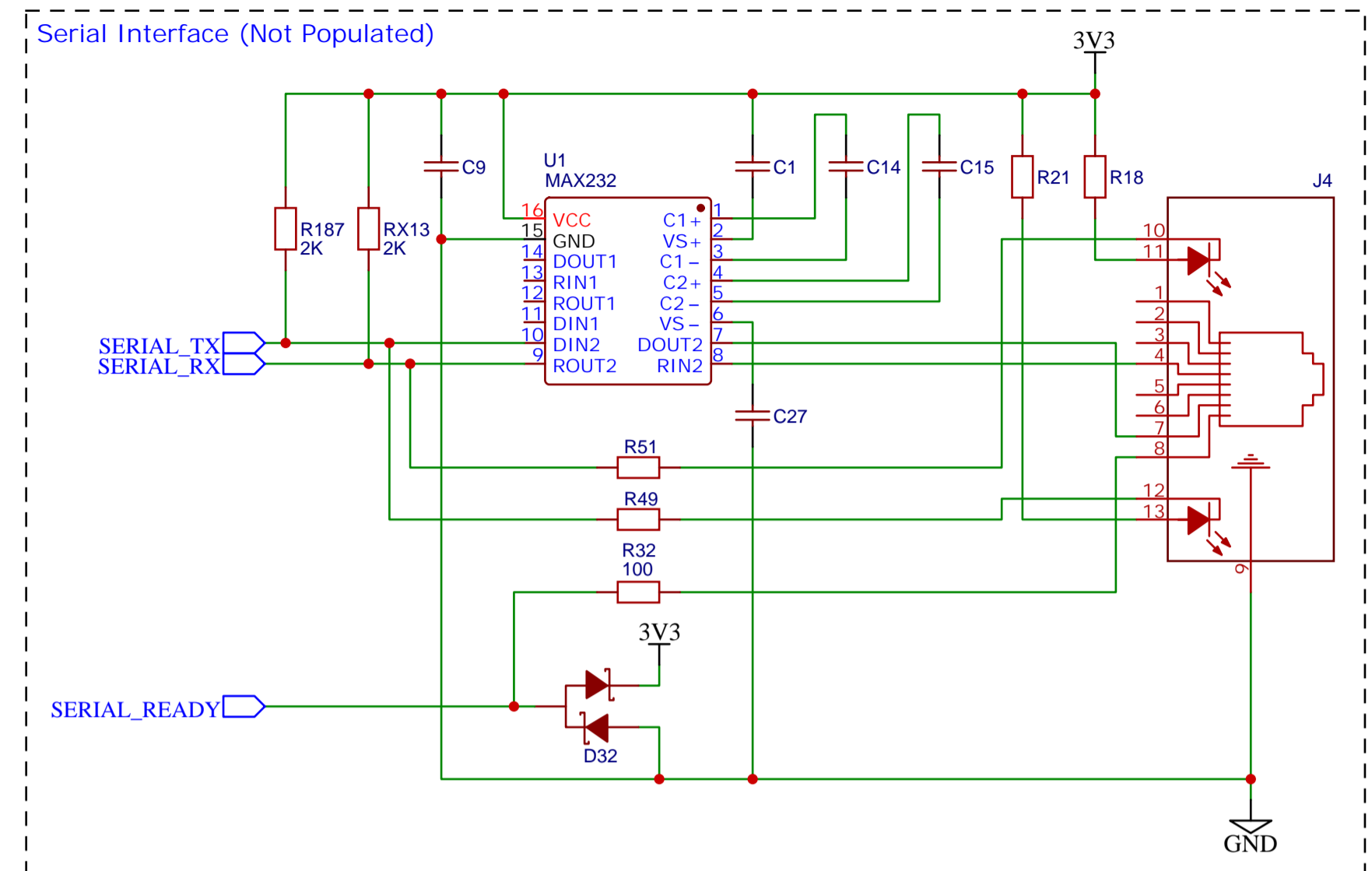
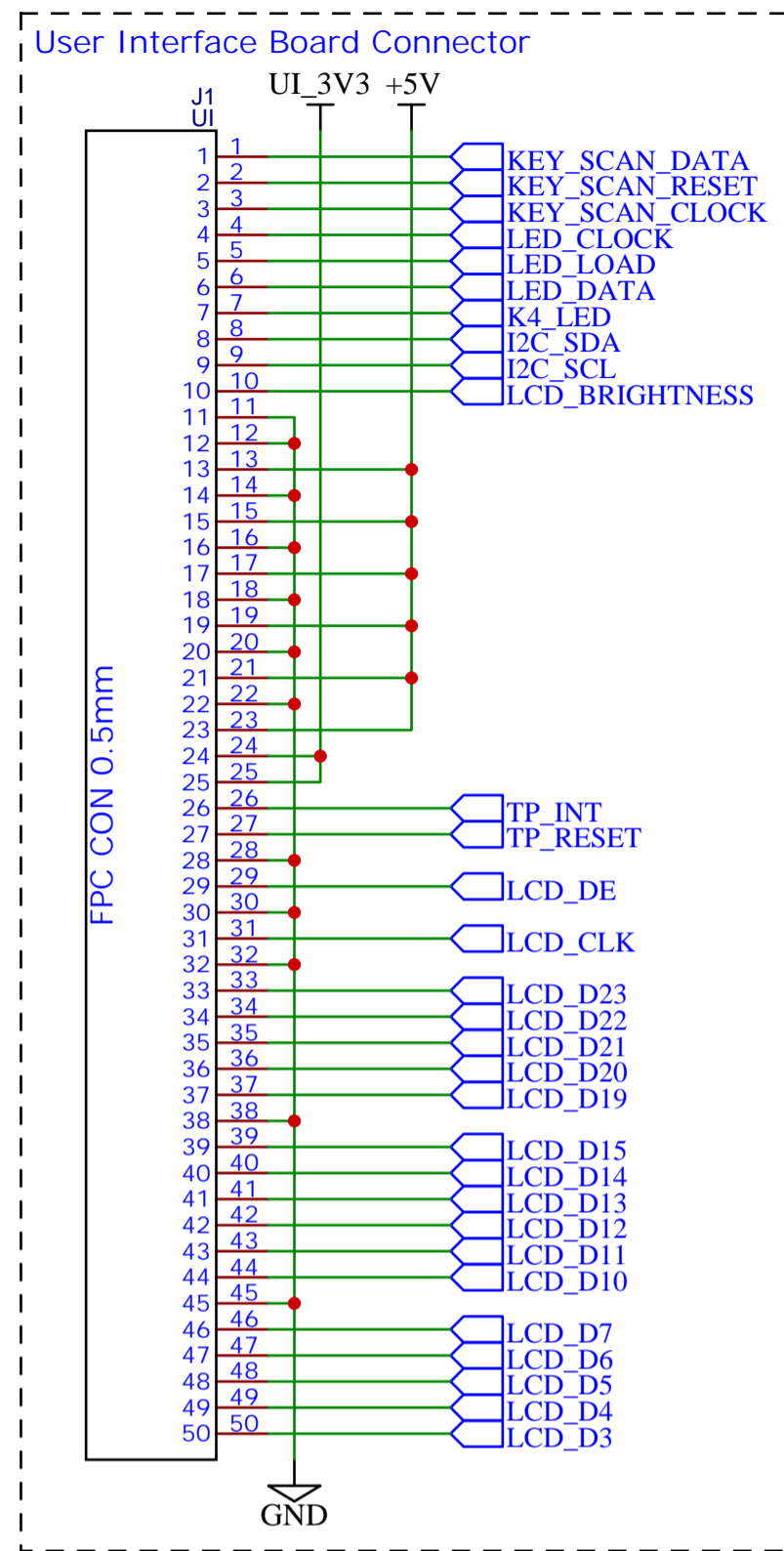


System Clock Generation

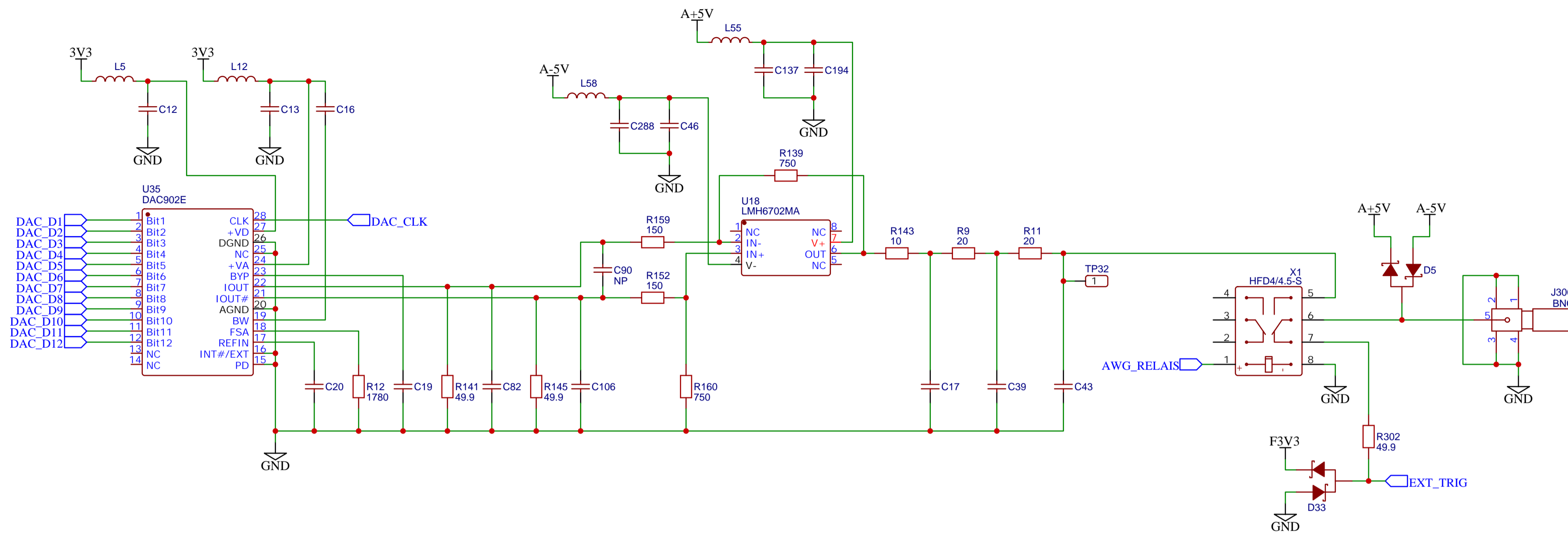




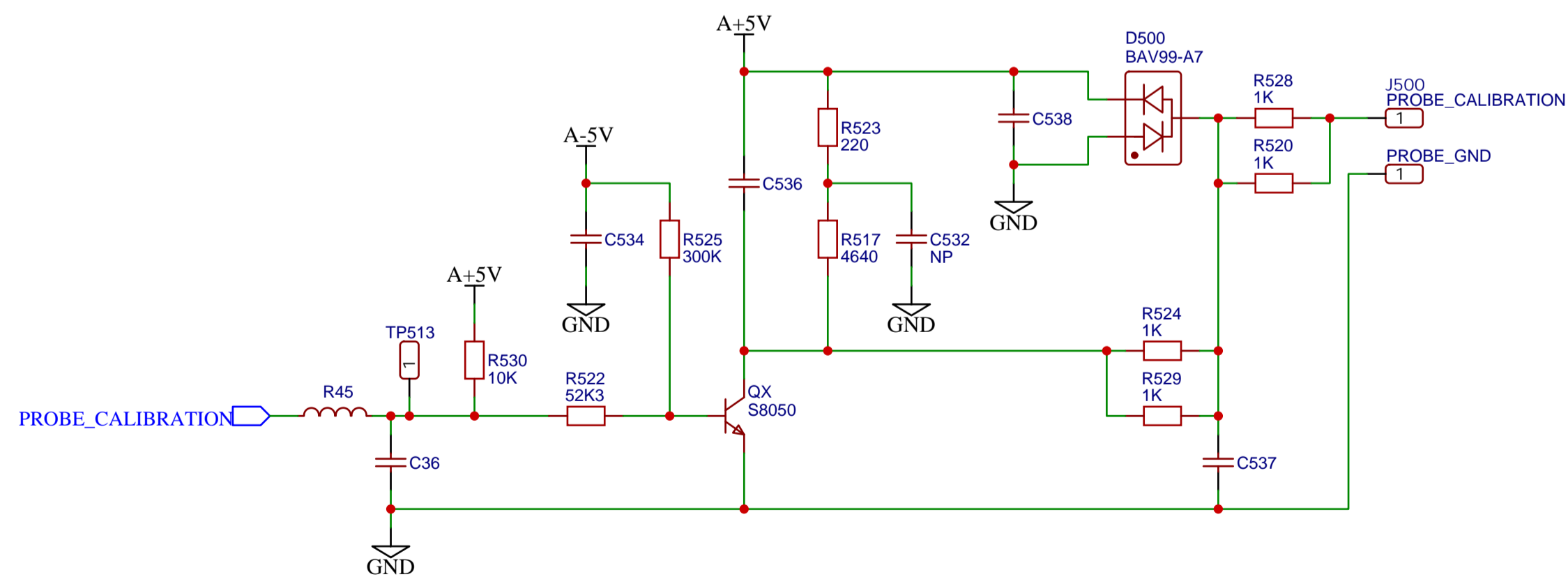
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Company:	EasyEDA	Sheet:	8/8
Date:	2022-06-26	Drawn By:	



Waveform Generator And Trigger Input

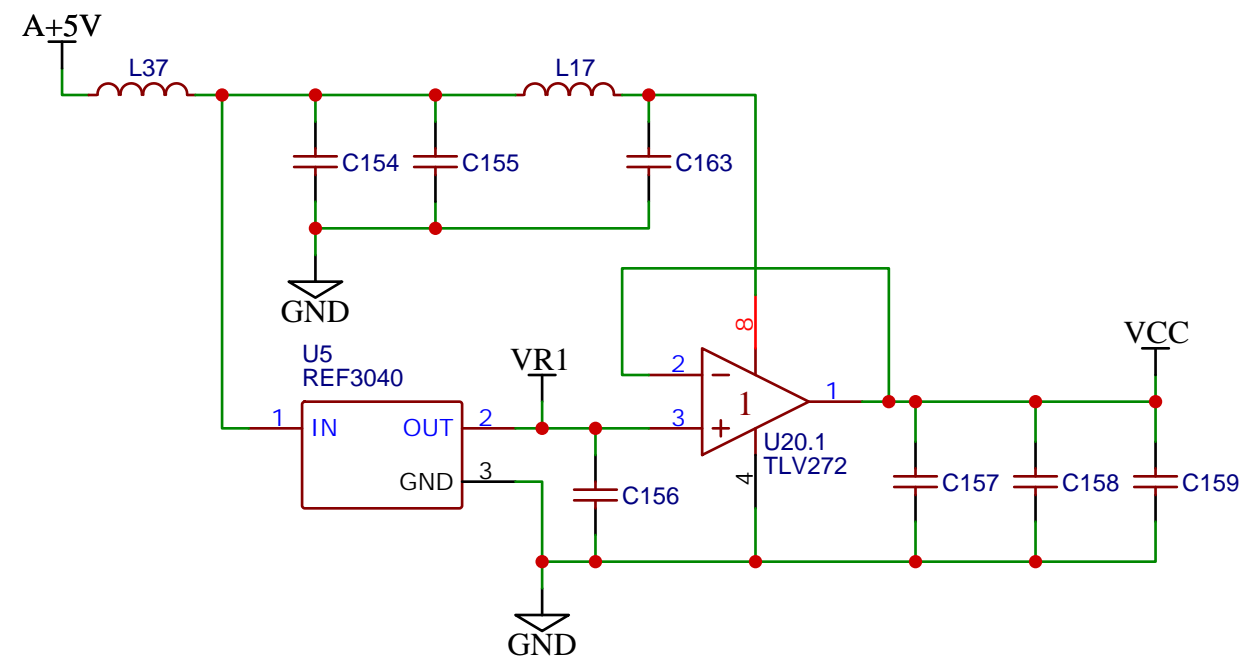


Probe Calibration Signal

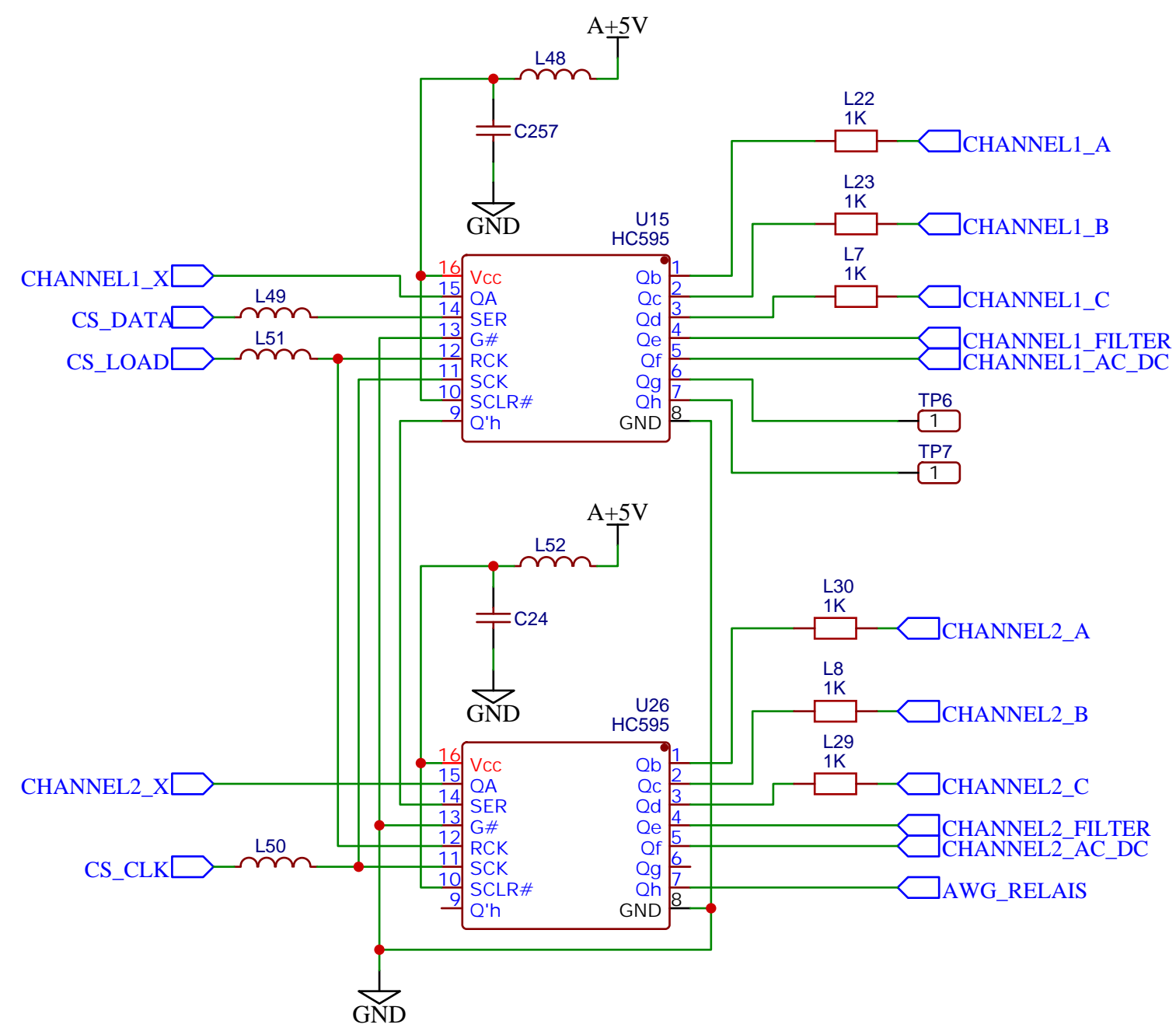


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EasyEDA	Company:	Sheet: 6/8	
	Date:	2022-06-29	Drawn By:

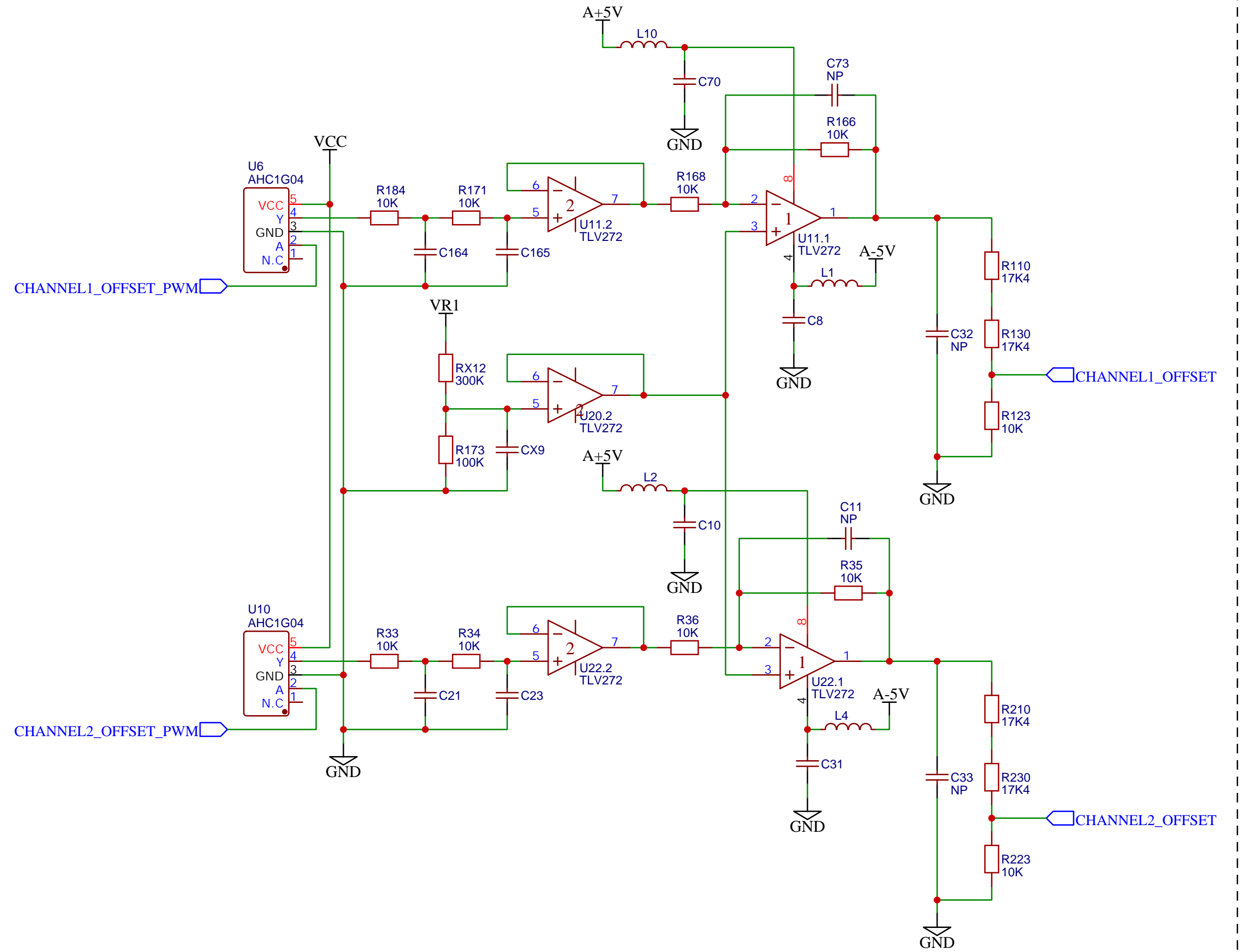
Offset Signal Buffers Power Supply

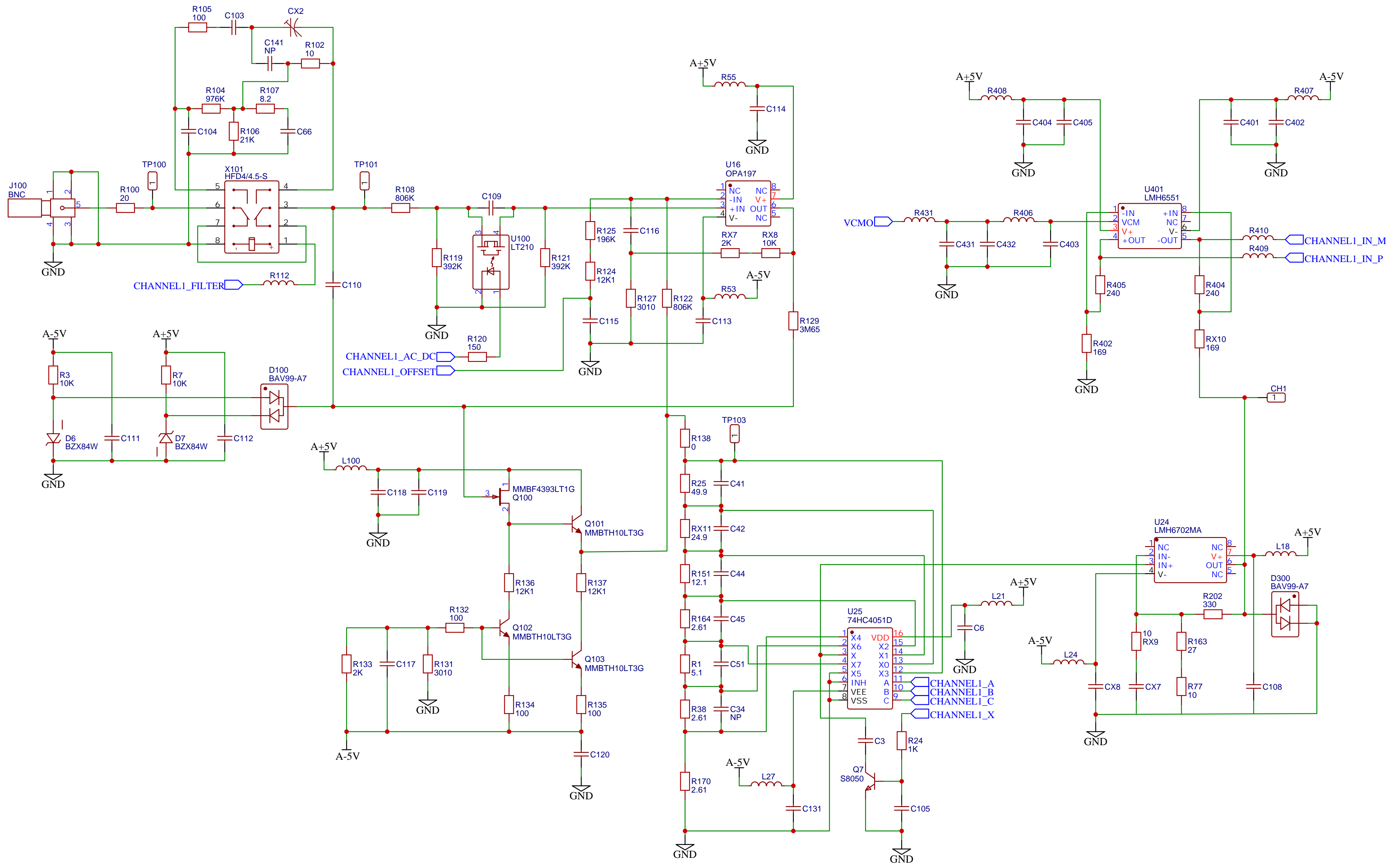


Channel Control Signals

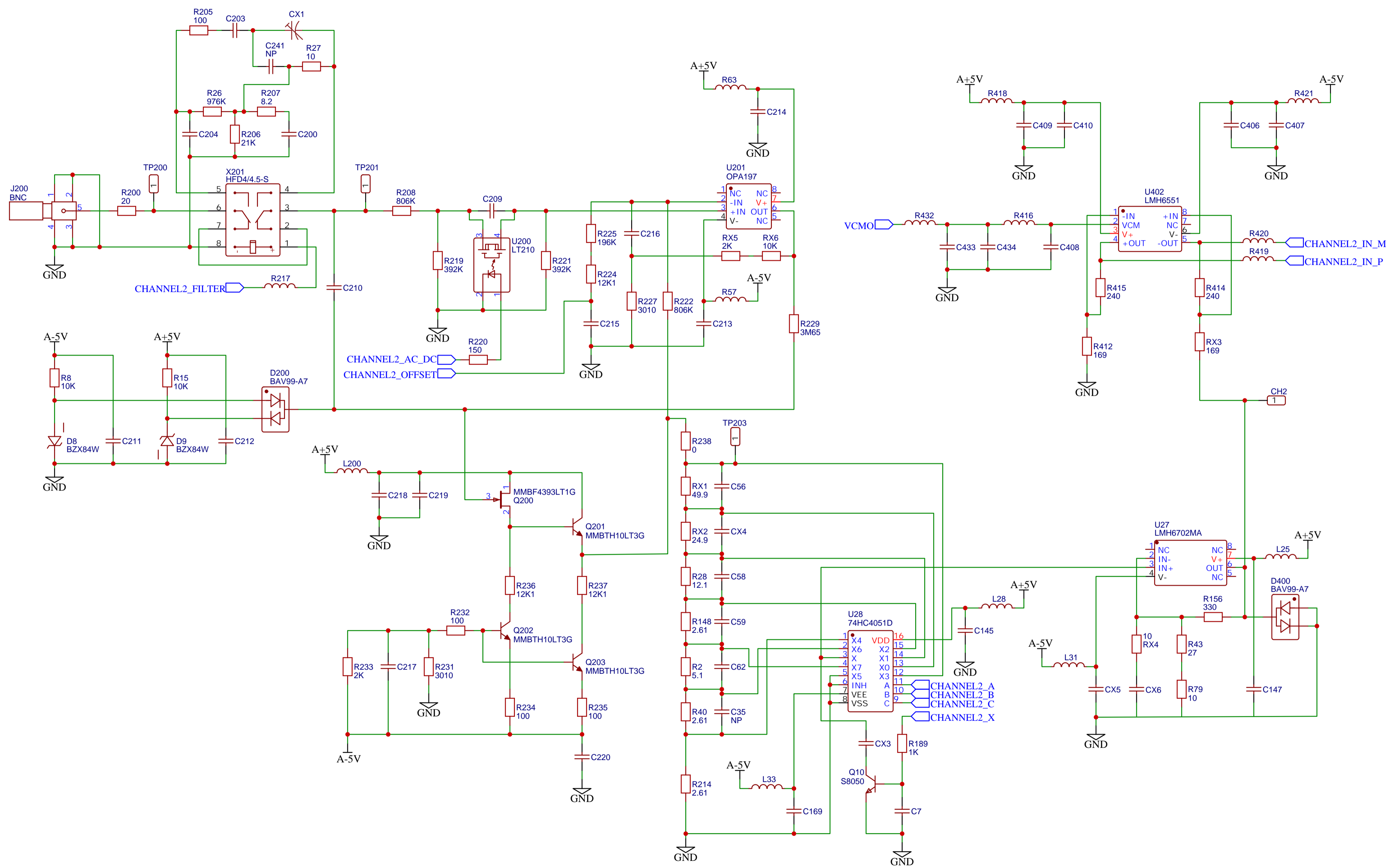


Offset Signals





TITLE: Main Board (Channel 1)		REV: 1.0
Company: EasyEDA		Sheet: 4/8
Date: 2022-06-30		Drawn By:



TITLE: Main Board (Channel 2)		REV: 1.0
Company: EasyEDA		Sheet: 5/8
Date: 2022-07-04		Drawn By: