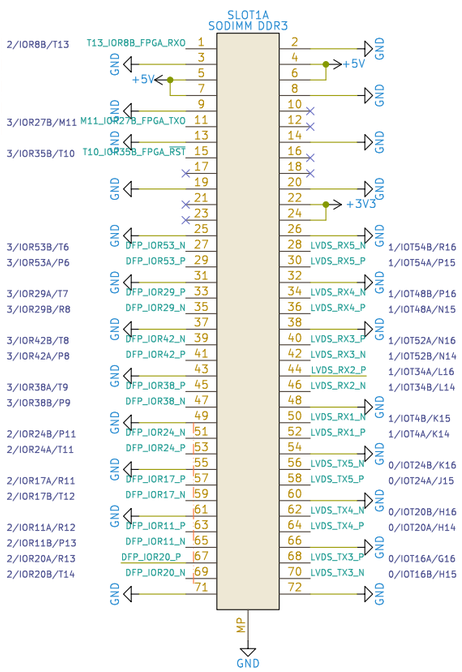
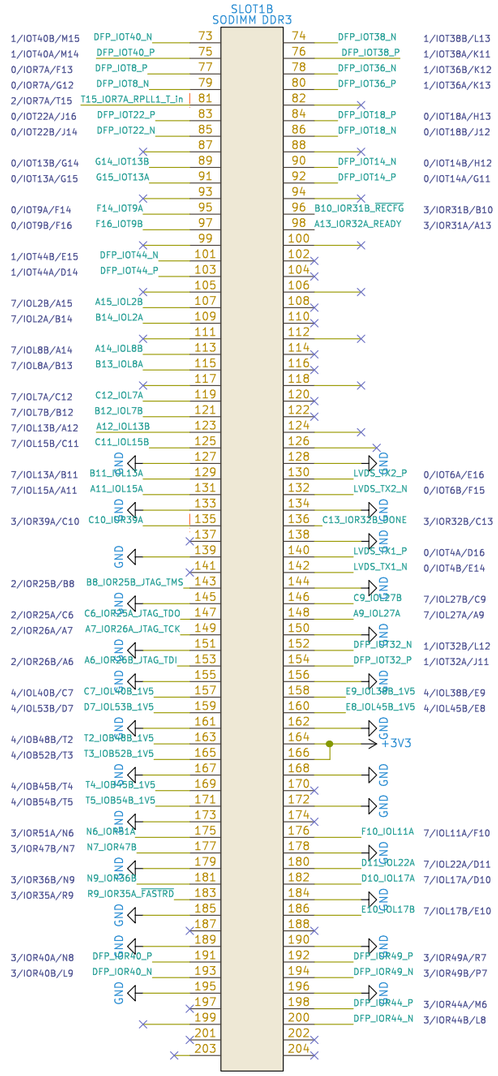
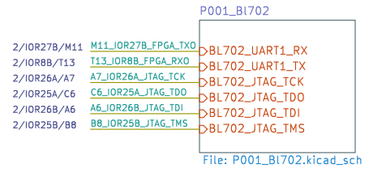
Tang Nano 20K Dock

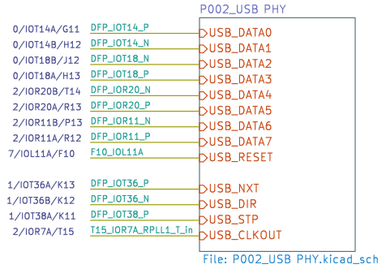
Revision History

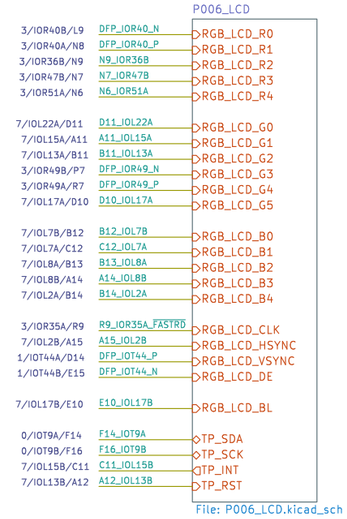
Version	Date	Change Note
7101	2022/02/21	First edition

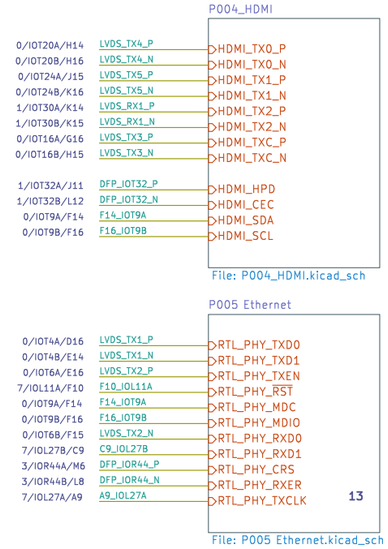


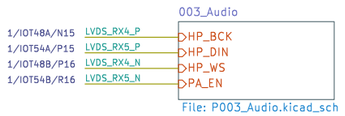


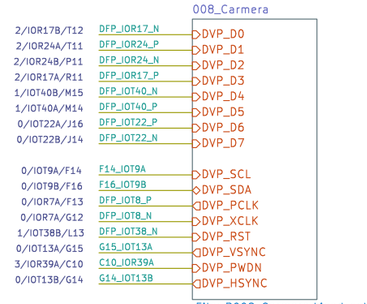


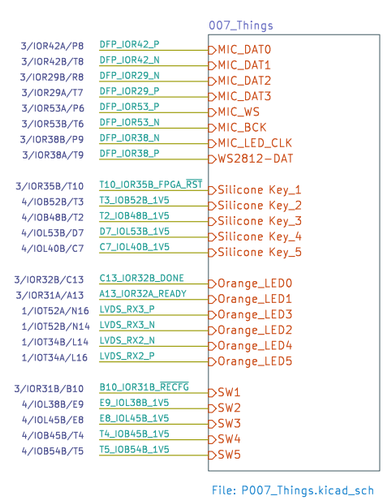












A Compact&Economical FPGA Edge AI Computing Solution

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Sheet: /

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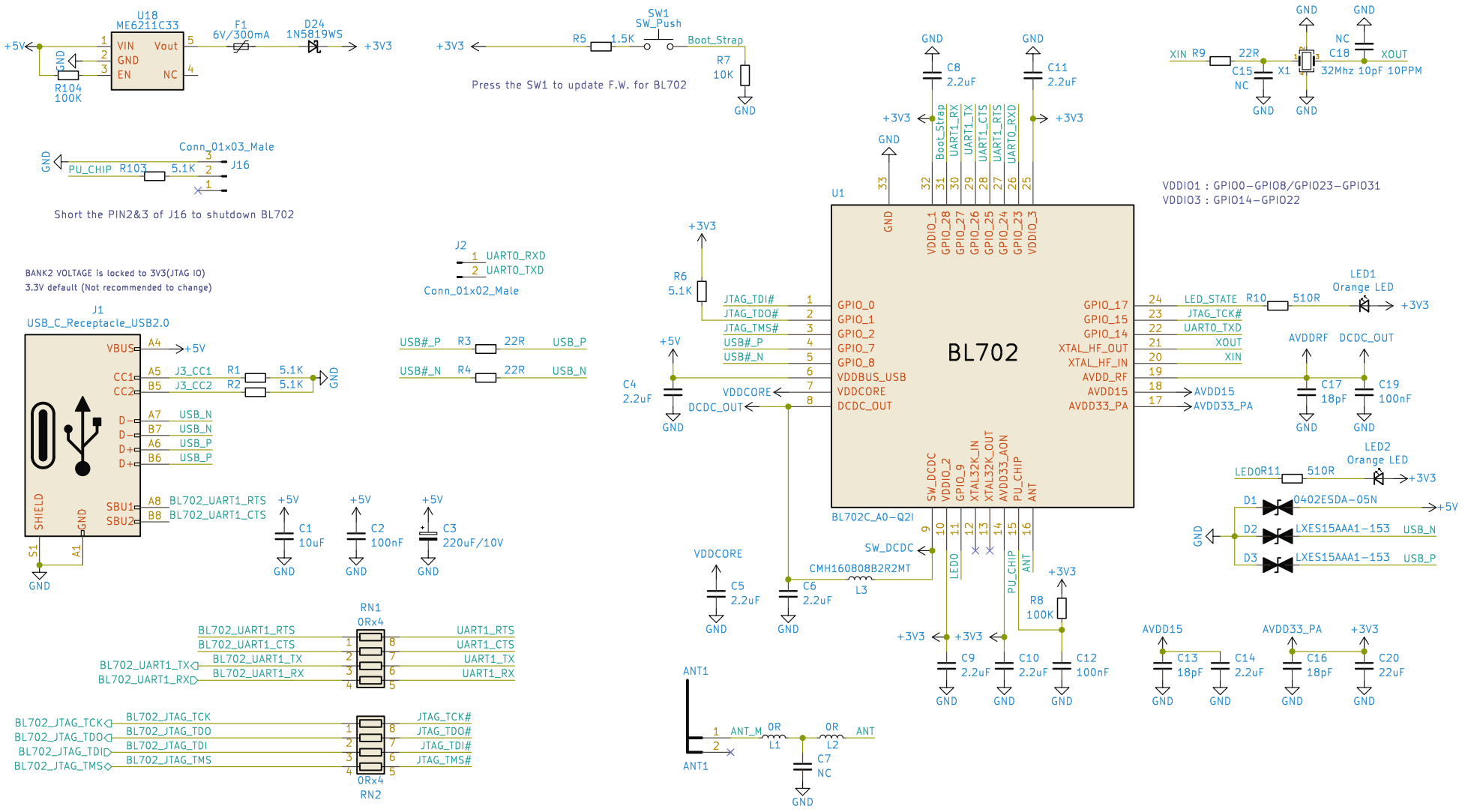
Size: A3	Date: 2022-10-30	**Rev: 1.00b**
KiCad E.D.A. kicad (6.99.0-1732-g4cd48cd5c9)		Id: 1/9


U18
ME6211C33
VIN
GND
EN
Vout
NC
F1
6V/300mA
D24
1N5819WS
+5V
+3V3
R104
100K
SW1
SW_Push
R5
1.5K
Boot_Strap
R7
10K
Press the SW1 to update F.W. for BL702
Conn_01x03_Male
J16
PU_CHIP R103
5.1K
Short the PIN2&3 of J16 to shutdown BL702
BANK2 VOLTAGE is locked to 3V3(JTAG IO)
3.3V default (Not recommended to change)
J1
USB_C_Receptacle_USB2.0
VBUS
CC1
CC2
D-
D+
SHIELD
SBU1
SBU2
J3_CC1
J3_CC2
R1
R2
5.1K
USB_N
USB_P
BL702_UART1_RTS
BL702_UART1_CTS
C1
10uF
C2
100nF
C3
220uF/10V
J2
UART0_RXD
UART0_TXD
Conn_01x02_Male
USB#_P
USB#_N
R3
R4
22R
USB_P
USB_N
RN1
0Rx4
BL702_UART1_TX
BL702_UART1_RX
UART1_RTS
UART1_CTS
UART1_TX
UART1_RX
BL702_JTAG_TCK
BL702_JTAG_TDO
BL702_JTAG_TDI
BL702_JTAG_TMS
JTAG_TCK#
JTAG_TDO#
JTAG_TDI#
JTAG_TMS#
RN2
Remove the RN2 to use External JTAG
U1
BL702
BL702C_A0-Q2I
GPIO_0
GPIO_1
GPIO_2
GPIO_7
GPIO_8
VDDBUS_USB
VDDCORE
DCDC_OUT
GPIO_17
GPIO_15
GPIO_14
XTAL_HF_OUT
XTAL_HF_IN
AVDD_RF
AVDD15
AVDD33_PA
SW_DCDC
VDDIO_2
GPIO_9
XTAL32K_IN
XTAL32K_OUT
AVDD33_AON
PU_CHIP
ANT
JTAG_TDI#
JTAG_TDO#
JTAG_TMS#
R6
5.1K
C4
2.2uF
C8
2.2uF
C11
2.2uF
Boot_Strap
UART1_RX
UART1_TX
UART1_CTS
UART1_RTS
UART0_RXD
VDDIO_1
GPIO_28
GPIO_27
GPIO_26
GPIO_25
GPIO_24
GPIO_23
VDDIO_3
VDDIO1 : GPIO0-GPIO8/GPIO23-GPIO31
VDDIO3 : GPIO14-GPIO22
XIN R9
22R
C15
NC
X1
C18
NC
XOUT
32Mhz 10pF 10PPM
LED1
Orange LED
LED_STATE
R10
510R
LED0R11
LED2
Orange LED
D1
D2
D3
0402ESDA-05N
LXES15AAA1-153
C17
18pF
C19
100nF
AVDDRF
DCDC_OUT
VDDCORE
C5
2.2uF
C6
2.2uF
CMH160808B2R2MT
L3
R8
100K
C9
2.2uF
C10
2.2uF
C12
100nF
C13
18pF
C14
2.2uF
C16
18pF
C20
22uF
ANT1
ANT_M
0R
L1
L2
C7
NC
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Shenzhen Sipeed Technology Co,Ltd.
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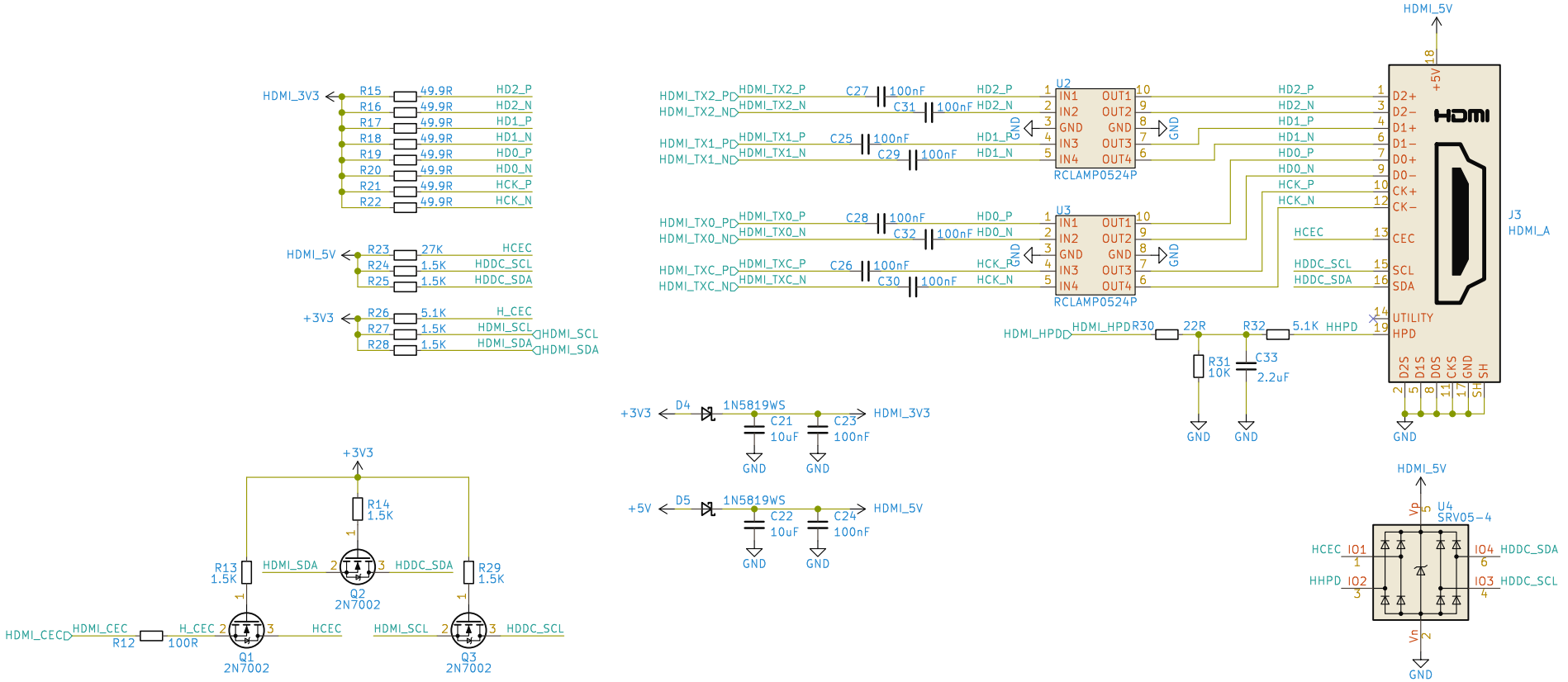
Size: A4
Date: 2022-09-01
Rev: 1.00a
KiCad E.D.A. kicad (6.99.0-1732-g4cd48cd5c9)
Id: 2/9

HDMI_TX/RX



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Shenzhen Sipeed Technology Co,Ltd.

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Size: A4	Date: 2022-09-01	**Rev: 1.00a**
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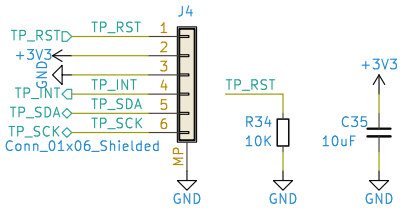
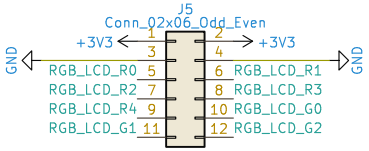
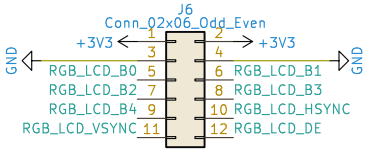
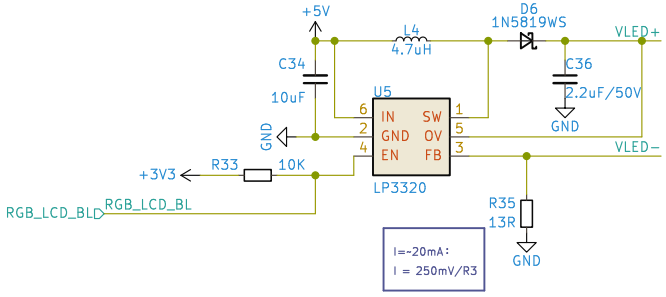
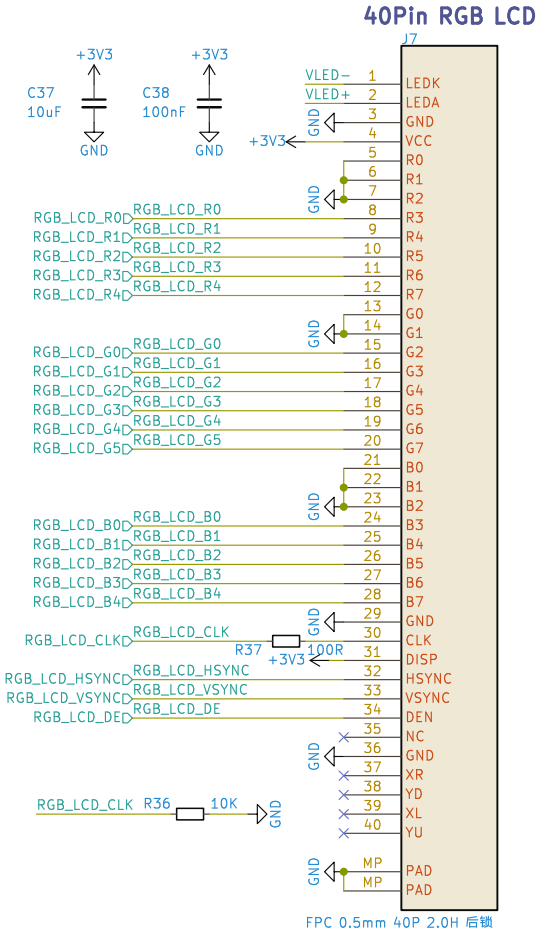
RGB LCD











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Title: Tang_Primer_20K-Dock_3709

Size: A4	Date: 2022-09-01	**Rev: 1.00a**
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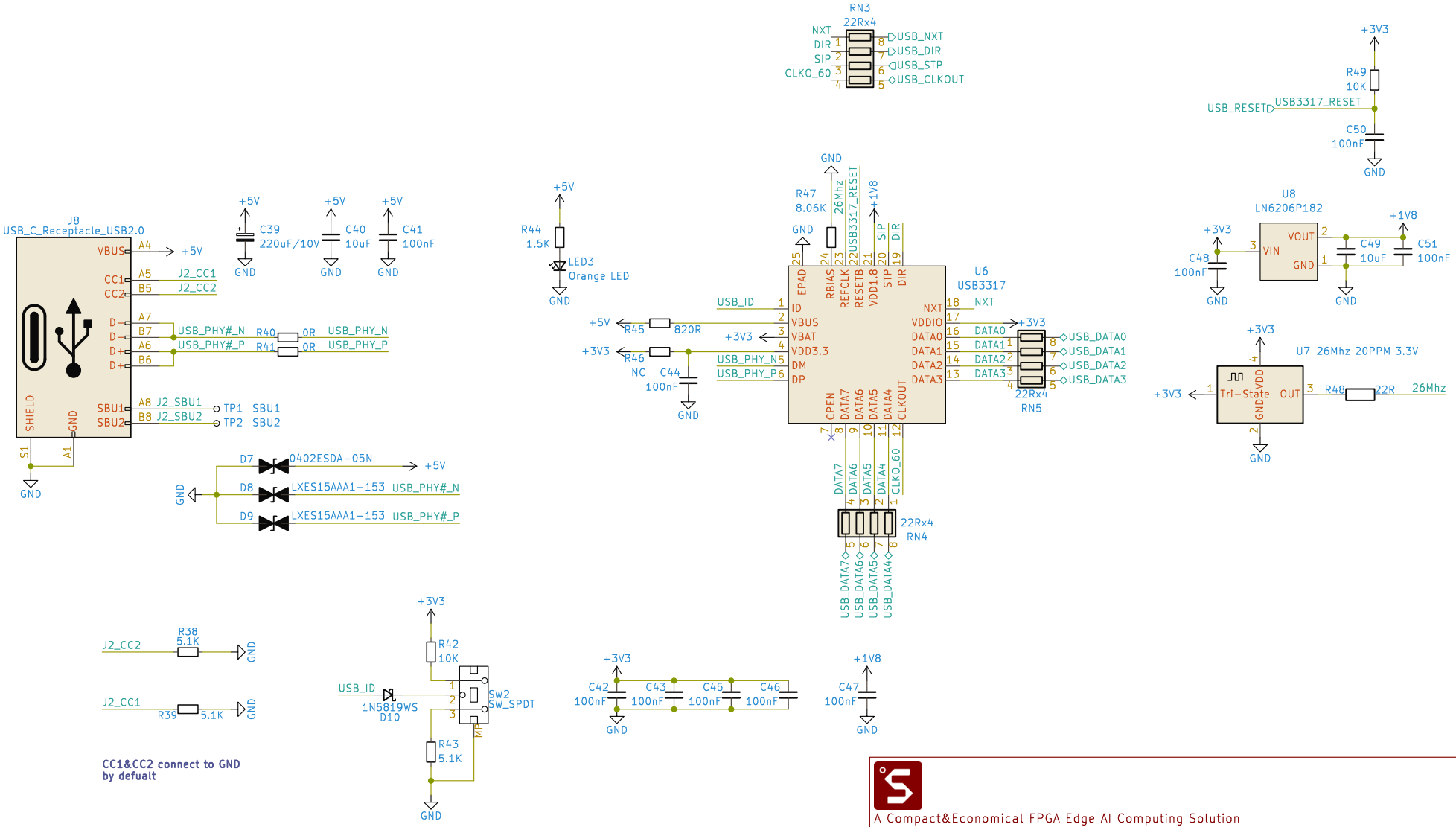
USB 2.0 PHY-IN BANK7



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Shenzhen Sipeed Technology Co,Ltd.

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Size: A4	Date: 2022-09-01	**Rev: 1.00a**
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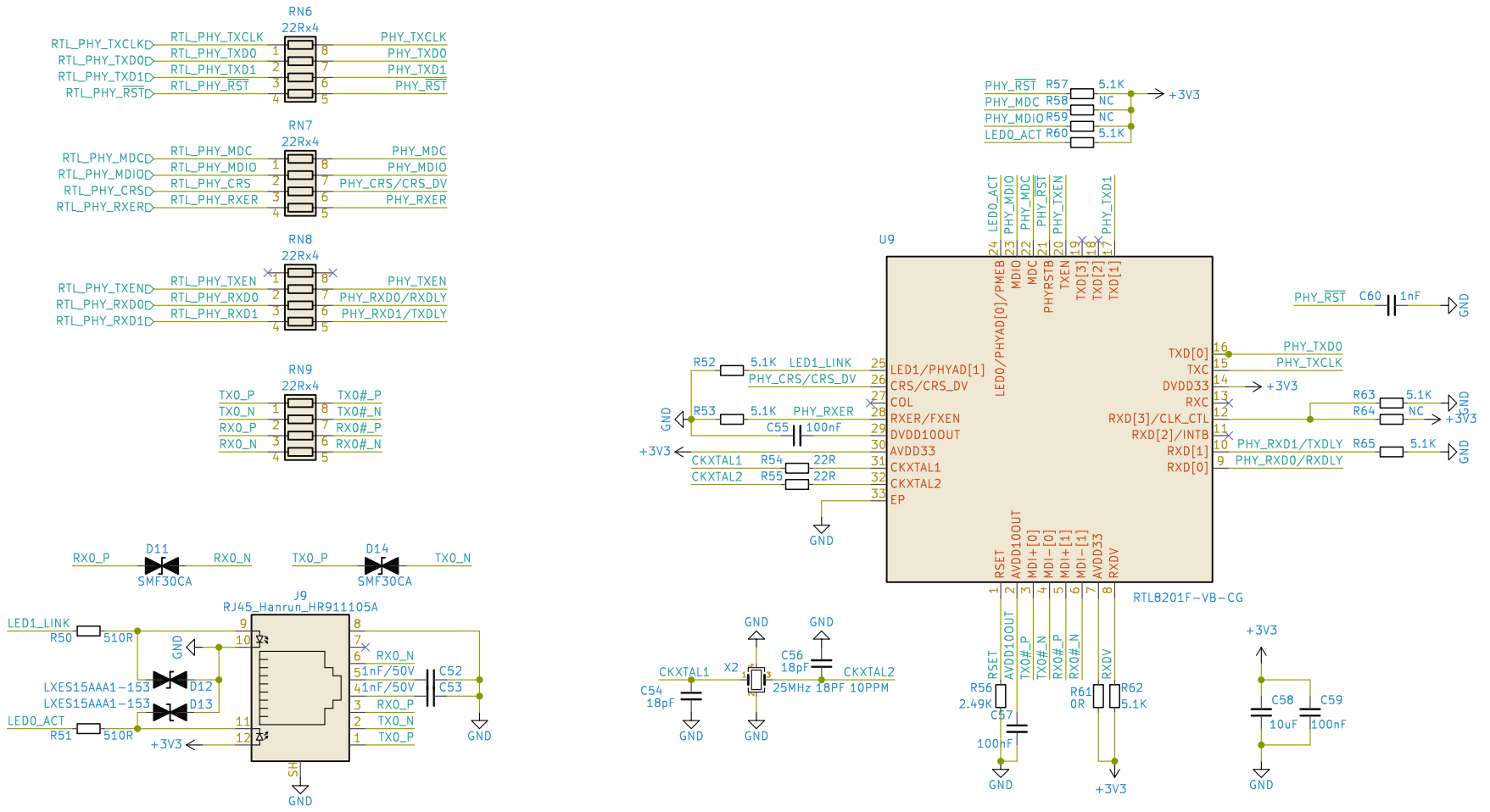

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Shenzhen Sipeed Technology Co,Ltd.

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Size: A4	Date: 2022-09-01	**Rev: 1.00a**
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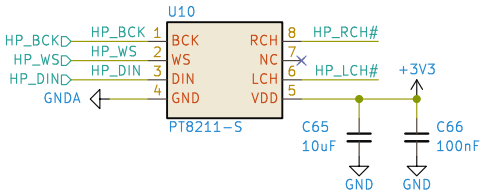
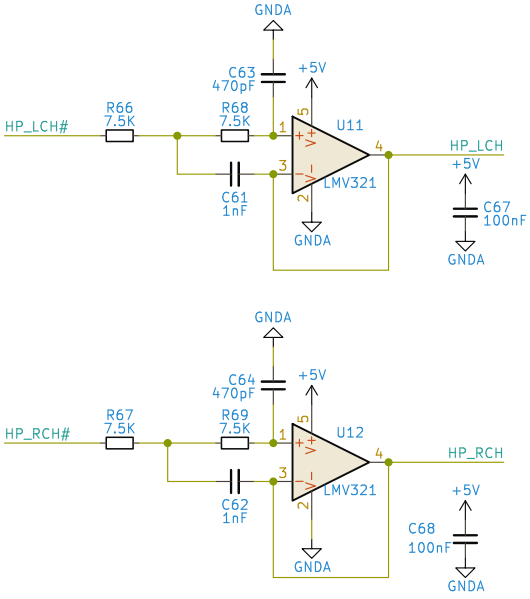
Audio

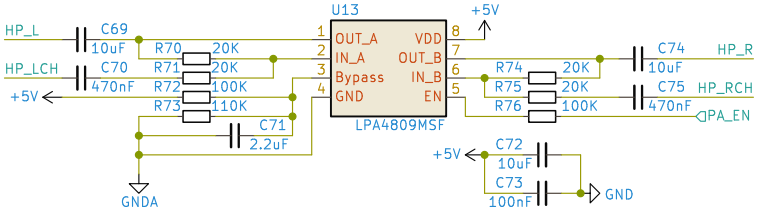
STEREO DAC



Low-Pass Filter



HEADPHONE AMP.



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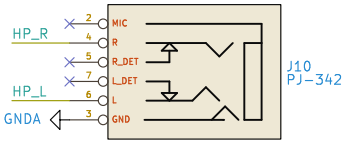

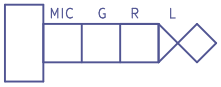

When the jack is unpluged, L/R_DET is connected to L/R.

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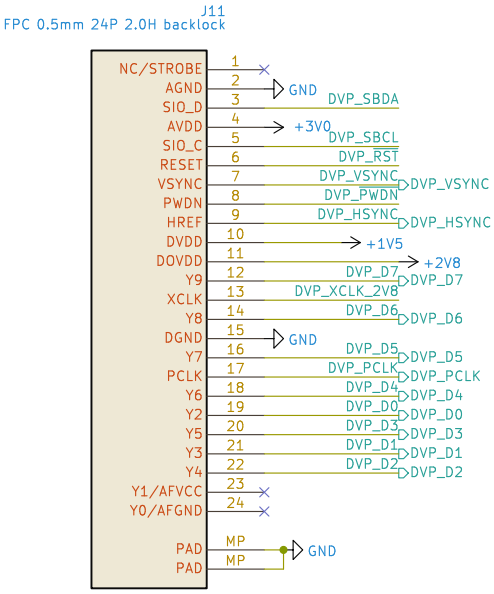
Sheet: /003_Audio/

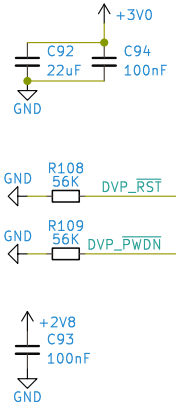
File: P003_Audio.kicad_sch

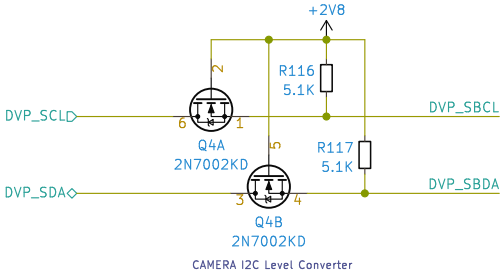
Title: Tang_Primer_20K-Dock_3709

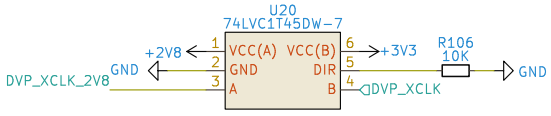
Size: A4	Date: 2022-09-01	**Rev: 1.00a**
KiCad E.D.A. kicad (6.99.0-1732-g4cd48cd5c9)		Id: 8/9

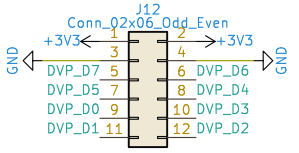
DVP Carmera

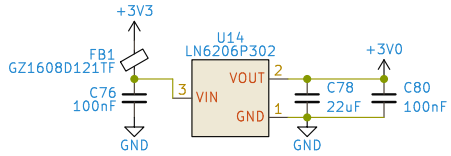


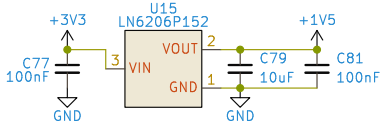


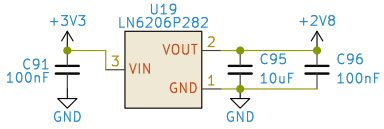












NOTICE:
DOVDD refers to I/O Bank voltage

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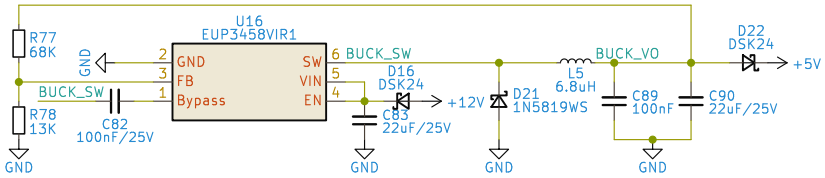
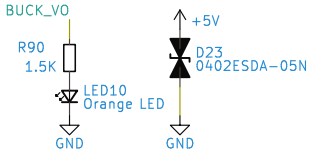
Sheet: /008_Carmera/
File: P008_Carmera.kicad_sch

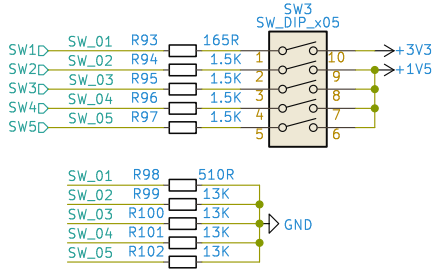
Title: Tang_Primer_20K-Dock_3709

Size: A4	Date: 2022-09-01	**Rev: 1.00a**
KiCad E.D.A. kicad (6.99.0-1732-g4cd48cd5c9)		Id: 9/9

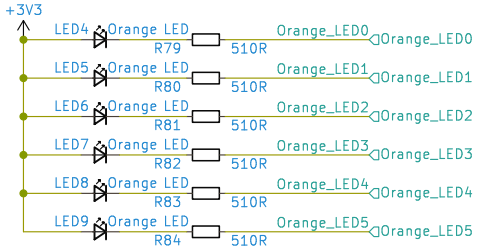
DC-IN BUCK



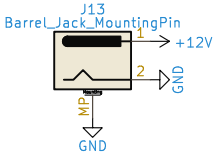


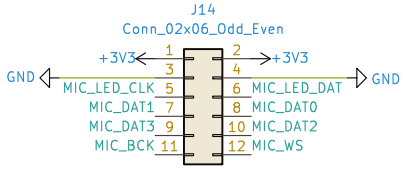


LED x 6

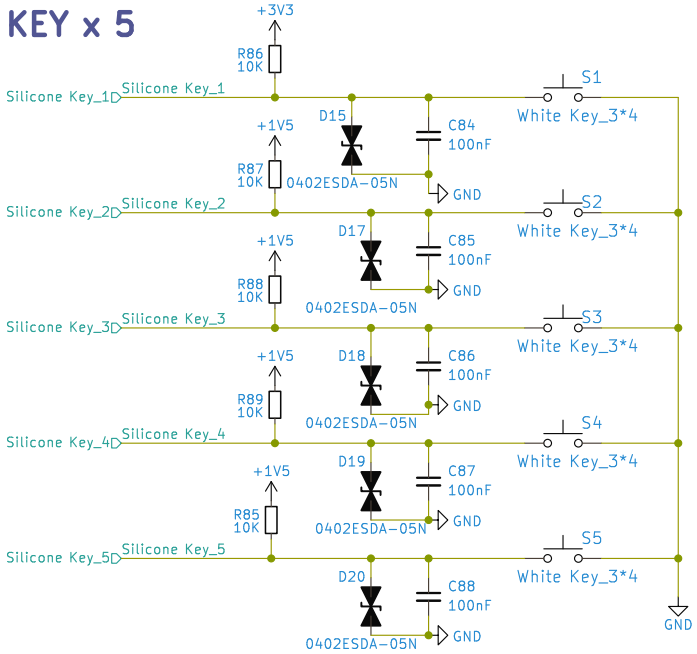


DC-IN JACK

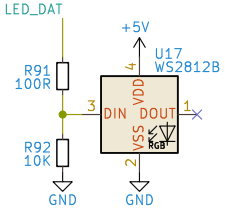




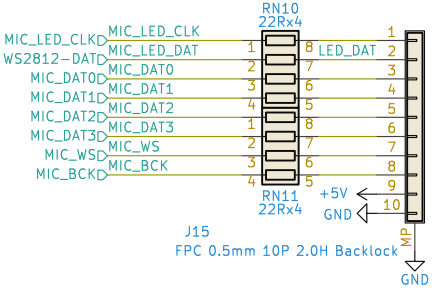
KEY x 5



WS2812B



MIC Array Conn.



A Compact&Economical FPGA Edge AI Computing Solution

Shenzhen Sipeed Technology Co,Ltd.

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Size: A4	Date: 2022-09-01	**Rev: 1.00a**
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