




Gowin Software Quick Start Guide

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Revision History

Date	Version	Description
05/07/2020	1.0E	Initial version published.
09/07/2020	1.1E	<ul style="list-style-type: none">● RTL schematic added.● File encryption added.● Tcl command added.
10/21/2020	1.1.1E	Use GowinSynthesis [®] as an example to describe synthesis.
06/10/2021	1.2E	<ul style="list-style-type: none">● Synplify Pro removed.● MIPI IP in the design modified.
11/02/2021	1.3E	Some descriptions updated.

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1 About This Guide

1.1 Purpose

This manual uses MIPI as an example to introduce Gowin Software and aims to help you get familiar with the usage and improve the design efficiency.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- [SUG100](#), Gowin Software User Guide
- [SUG935](#), Gowin Design Physical Constraints User Guide
- [SUG101](#), Gowin Design Timing Constraints User Guide
- [SUG114](#), Gowin Analyzer Oscilloscope User Guide
- [SUG282](#), Gowin Power Analyzer User Guide
- [SUG502](#), Gowin Programmer User Guide
- [SUG550](#), GowinSynthesis User Guide
- [SUG755](#), Gowin HDL Schematic Viewer User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
PnR	Place & Route
GAO	Gowin Analyzer Oscilloscope
GPA	Gowin Power Analyzer
AO Core	Analysis Oscilloscope Core

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Design Flow

Gowin Software is available in Windows and Linux. It supports GUI running mode and commands running mode. Take the GUI running mode in Windows and MIPI design as an instance to introduce quick start of Gowin Software.

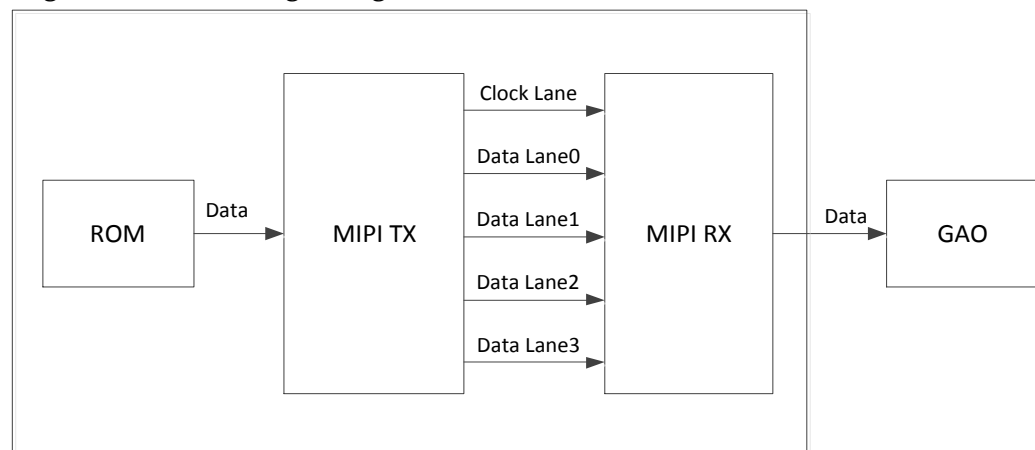
The design uses FloorPlanner to add physical constraints, uses Timing Constraints Editor to add timing constraints, uses GAO to add GAO config file and to capture data, GPA to add GPA config file, and Programmer to download bitstream.

2.2 Design Diagram

Gowin MIPI D-PHY TX RX IP applies to the serial display interface and serial camera interface for receiving or transmitting the image or video data. MIPI D-PHY provides its physical layer definition.

The design integrates MIPI RX Advance IP and MIPI TX Advance IP. pROM provides data for MIPI TX Advance. MIPI TX Advance transmits data and MIPI RX Advance receives data. GAO captures the data received by MIPI RX Advance to verify MIPI RX Advance and MIPI TX Advance. The design diagram is as shown in Figure 2-1 .

Figure 2-1 MIPI Design Diagram



3 Quick Start

3.1 Create a New Project

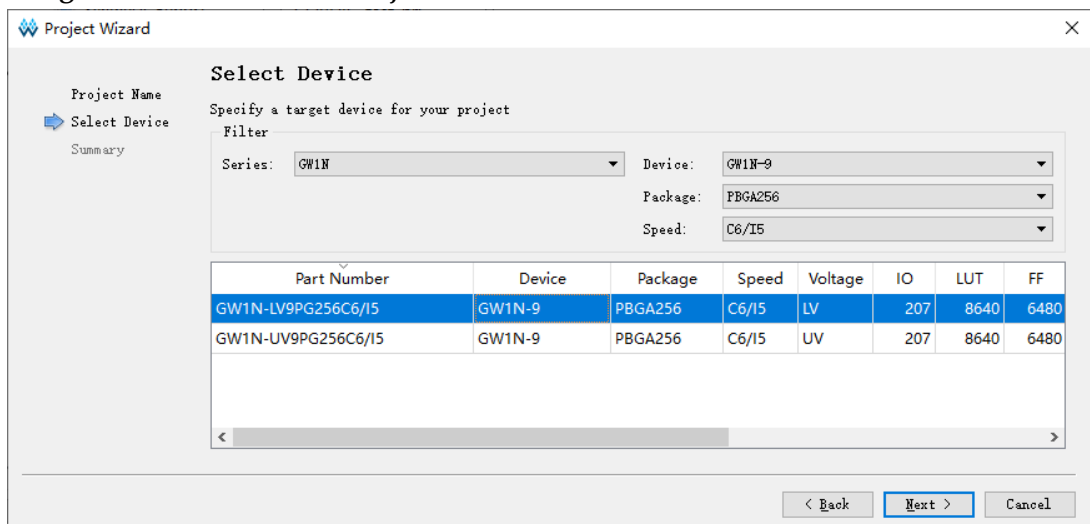
3.1.1 Create a New Project

Open Gowin Software and click "Start Page > Quick Start > New Project" to create a new project named as MIPI_RX_TX_Advance. The device selected is as shown in Figure 3-1.

- Series: GW1N
- Device: GW1N-9
- Package: PBGA256
- Speed: C6/I5
- Part Number: GW1N-LV9PG256C6/I5

Click "Next" until the project creation completed. For the details, please refer to [SUG100](#), Gowin Software User Guide.

Figure 3-1 Create a New Project



After the project is created, the impl and src folders are generated under the project creation path, as shown in Figure 3-2. impl contains synthesis and PnR files and src contains the source files.

Figure 3-2 Project Directory

Name	Date modified	Type	Size
impl	6/10/2021 17:17	File folder	
src	6/10/2021 17:17	File folder	
MIPI_RX_TX_Advance.gprj	6/10/2021 17:07	GPRJ File	1 KB
MIPI_RX_TX_Advance.gprj.user	6/10/2021 17:17	USER File	3 KB

3.1.2 Generate MIPI D-PHY IP

Click "Tools > IP Core Generator" to open the IP Core Generator window. Double-click "Interface and Interconnect > MIPI RX Advance" to open the IP Customization dialog box to configure as required. The MIPI RX Advance configuration in this design is shown in Figure 3-3. Then click "OK" to generate MIPI RX Advance IP.

Figure 3-3 MIPI RX Advance Configuration

Options

MIPI D-PHY Mode: 1:8 1:16

CLK IO TYPE: TLVDS ELVDS MIPI IO MIPI COMB IO

D-PHY Lane0 Lane0 IO TYPE:

D-PHY Lane1 Lane1 IO TYPE:

D-PHY Lane2 Lane2 IO TYPE:

D-PHY Lane3 Lane3 IO TYPE:

Data0 Before Lane Alignment HS DATA0 IO Delay Value

Data1 Before Lane Alignment HS DATA1 IO Delay Value

Data2 Before Lane Alignment HS DATA2 IO Delay Value

Data3 Before Lane Alignment HS DATA3 IO Delay Value

LP mode on clock lane

LP mode on data lane 0 LP mode on data lane 1

LP mode on data lane 2 LP mode on data lane 3

Turns on byte alignment Turns on lane alignment

D-PHY RX using external Clock

Generation Config

Disable I/O Insertion

After generation, IP design files and simulation files are generated

under the IP creation path, as shown in Figure 3-4.

- .v file is an IP design file, encrypted.
- _tmp.v is an IP design template file.
- .vo file is an IP simulation model file, unencrypted.
- .ipc file is an IP configuration file. The user can load the file to modify the configuration.
- temp contains the files required to generate the IP.
- The doc, model, sim, and tb contain the simulation files: readme text, simulation model, simulation script, and testbench.

Note!

At present, for some IPs, the created path still generates doc, model, sim, and tb folders, indicating readme text, simulation model, simulation script, and testbench simulation file. The IP directory is subject to IP Core Generator in use.

Figure 3-4 MIPI RX Advance IP Directory

Name	Date modified	Type	Size
temp	6/10/2021 17:17	File folder	
mipi_rx_advance.ipc	6/10/2021 13:42	IPC File	1 KB
mipi_rx_advance.v	6/10/2021 13:43	V File	427 KB
mipi_rx_advance.vo	6/10/2021 13:43	VO File	734 KB
mipi_rx_advance_tmp.v	6/10/2021 13:43	V File	2 KB

Double-click MIPI TX Advance to open the IP Customization dialog box to configure as required. The MIPI TX Advance configuration in this design is shown in Figure 3-5. Then click "OK" to generate MIPI TX Advance IP.

Figure 3-5 MIPI TX Configuration

Options

MIPI D-PHY Mode: 8:1 16:1

D-PHY CLK CLK IO TYPE: ELVDS

D-PHY Lane0 Lane0 IO TYPE: ELVDS

D-PHY Lane1 Lane1 IO TYPE: ELVDS

D-PHY Lane2 Lane2 IO TYPE: ELVDS

D-PHY Lane3 Lane3 IO TYPE: ELVDS

LP mode on clock lane

LP mode on data lane 0 LP mode on data lane 1

LP mode on data lane 2 LP mode on data lane 3

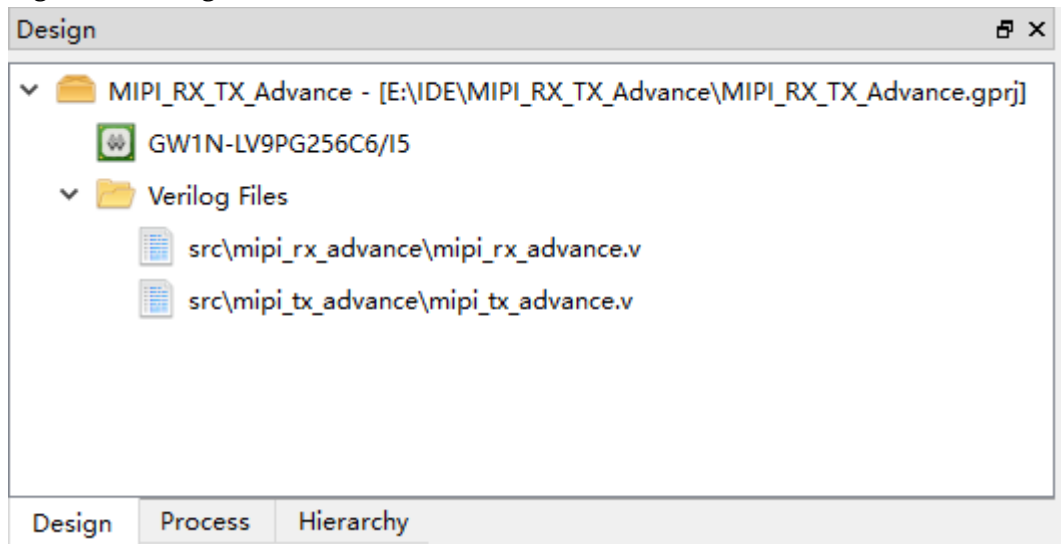
DPHY TX with Internal PLL

PLL Reference Clock: 50MHz

Generation Config

Disable I/O Insertion

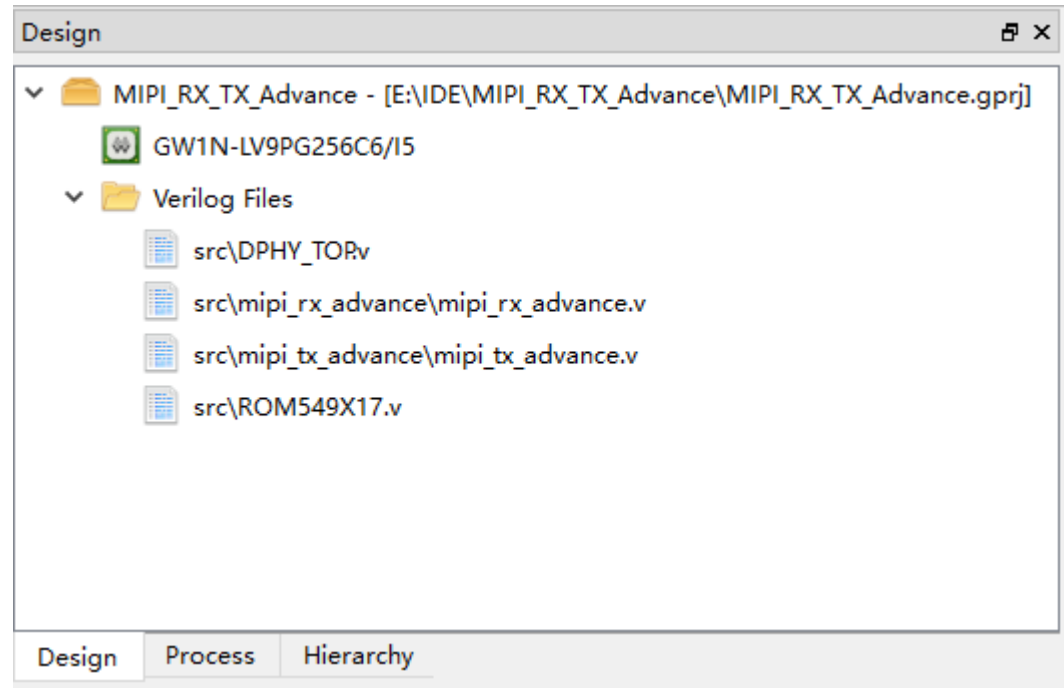
After MIPI RX Advance and MIPI TX Advance IPs generated, the Design window is as shown in Figure 3-6.

Figure 3-6 Design Window

3.1.3 Load File

In order to test MIPI RX Advance and MIPI TX Advance, some design files need to be loaded or created, as shown in Figure 3-7.

Figure 3-7 Load Files



3.1.4 RTL Schematic

After the source file is loaded, you can view the design schematic by clicking "Tools > Schematic Viewer" to help you better understand the logic. For details, see [SUG755](#), Gowin HDL Schematic Viewer User Guide.

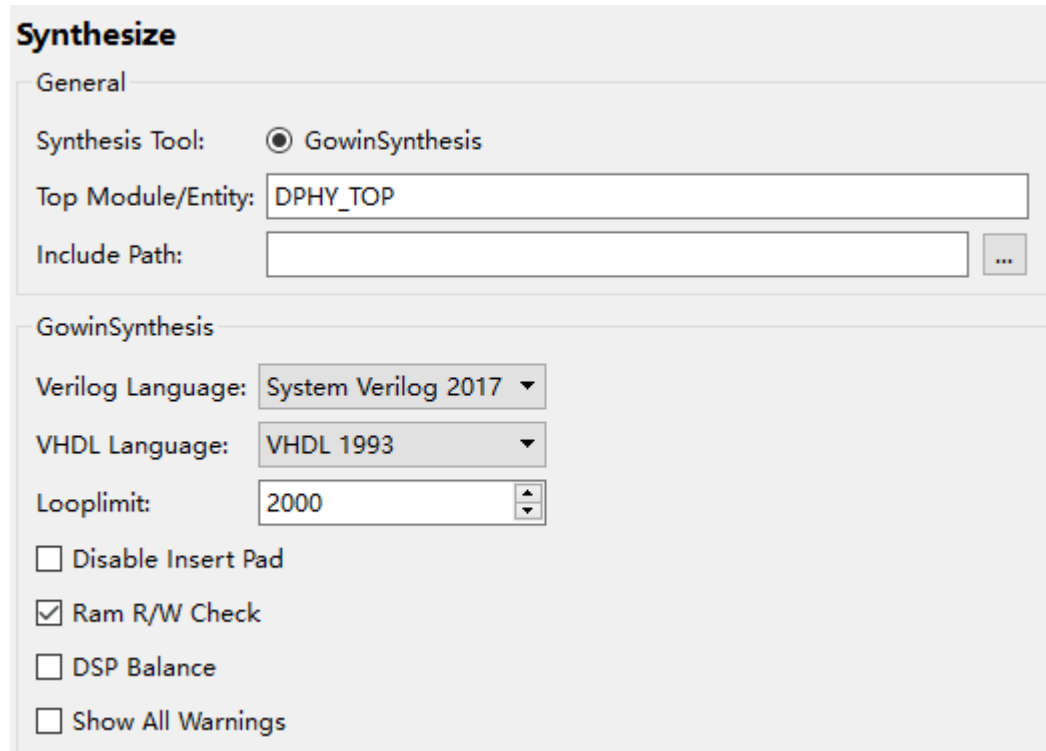
3.2 Use GowinSynthesis® to Synthesize

3.2.1 Configuration

Select "Process > Synthesize > Configuration" to open Configurations dialog box. For details, refer to [SUG550](#), GowinSynthesis User Guide.

The top module/entity is DPHY_TOP, as shown in Figure 3-8.

Figure 3-8 Synthesis Configuration



Synthesize

General

Synthesis Tool: GowinSynthesis

Top Module/Entity:

Include Path: ...

GowinSynthesis

Verilog Language:

VHDL Language:

Looplimit:

Disable Insert Pad

Ram R/W Check

DSP Balance

Show All Warnings

In addition, you can add some attributes and instructions to the source file to control synthesis. For the details, see [SUG550](#), GowinSynthesis User Guide. As shown in Figure 3-9, in this design, a specific net is retained without optimization during the synthesis by using the `/* synthesis syn_keep=1 */` attribute.

Figure 3-9 Attributes and Instructions of GowinSynthesis

```

417 `ifdef GEN_MIPI_RX_16
418     reg [63:0] data_in;
419     reg [15:0] data0, data1, data2, data3;
420     reg [15:0] dout, dout1;
421     reg [15:0] data_cntr;
422     reg hactive_flag_RX;
423
424     wire [1:0] lp_clk_out, lp_data0_out;
425     wire [1:0] lp_data1_out, lp_data2_out, lp_data3_out;
426
427     wire [15:0] data_out3, data_out2, data_out1, data_out0;
428     wire D0_delay, D1_delay, D2_delay, D3_delay;
429     reg [63:0] data_out reg;
430     wire clk_byte_out /* synthesis syn_keep=1 */;
431     wire sclk_tx ;
432 `endif

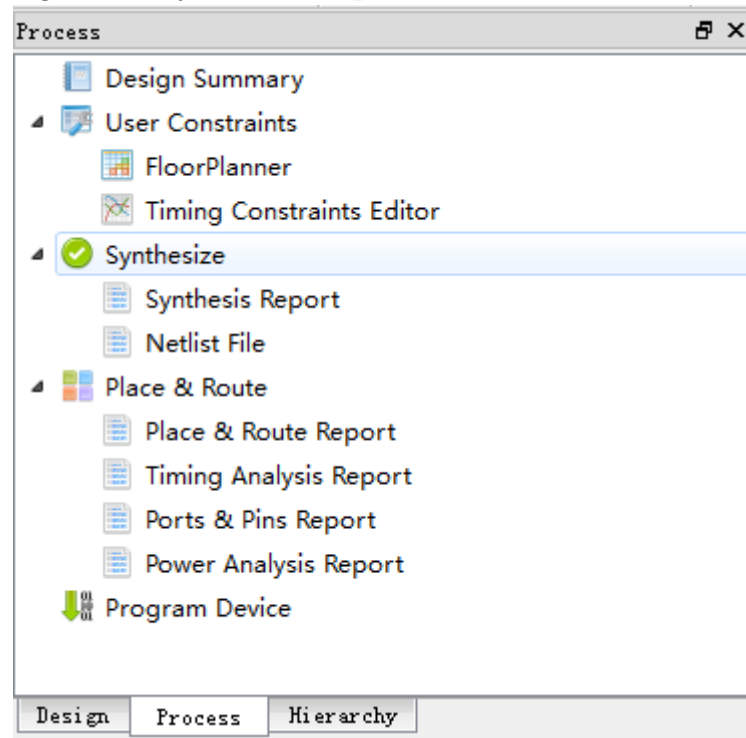
```

3.2.2 Synthesize

After synthesis configuration, you can start to synthesize.

Double-click "Synthesize" in Process window to synthesize, as shown in Figure 3-10. When the icon changes to "✔", you can double-click Synthesis Report to view the report and double-click Netlist File to view the netlist file.

Figure 3-10 Synthesis Completed



After synthesis, the gwsynthesis folder is generated under the \impl path. The folder contains all the files and folders generated in synthesis, as shown in Figure 3-11.

Figure 3-11 gwsynthesis Directory

Name	Date modified	Type	Size
MIPI_RX_TX_Advance.log	6/10/2021 15:09	LOG File	4 KB
MIPI_RX_TX_Advance.prj	6/10/2021 15:09	PRJ File	2 KB
MIPI_RX_TX_Advance.vg	6/10/2021 15:09	VG File	464 KB
MIPI_RX_TX_Advance_syn.rpt.html	6/10/2021 15:09	360 se HTML Doc...	29 KB
MIPI_RX_TX_Advance_syn_resource.html	6/10/2021 15:09	360 se HTML Doc...	3 KB
MIPI_RX_TX_Advance_syn_rsc.xml	6/10/2021 15:09	XML Document	1 KB

3.3 Physical Constraints

After synthesis, you can use FloorPlanner or write manually to add physical constraints. In this design, FloorPlanner is selected. For more details, please refer to the [SUG935](#), Gowin Design Physical Constraints User Guide

3.3.1 Create New Physical Constraints

Click "Process > User Constraints > FloorPlanner" to open FloorPlanner, which supports I/O, Primitive, and Group physical constraints. This design only adds I/O constraints and uses it as an instance.

You can create I/O constraints in I/O Constraints window. Drag the port row to be constrained in the Netlist or I/O Constraints window to a specific location in the Package View or Chip Array view. After finished, the port location displays in the IOB, as shown in Figure 3-12.

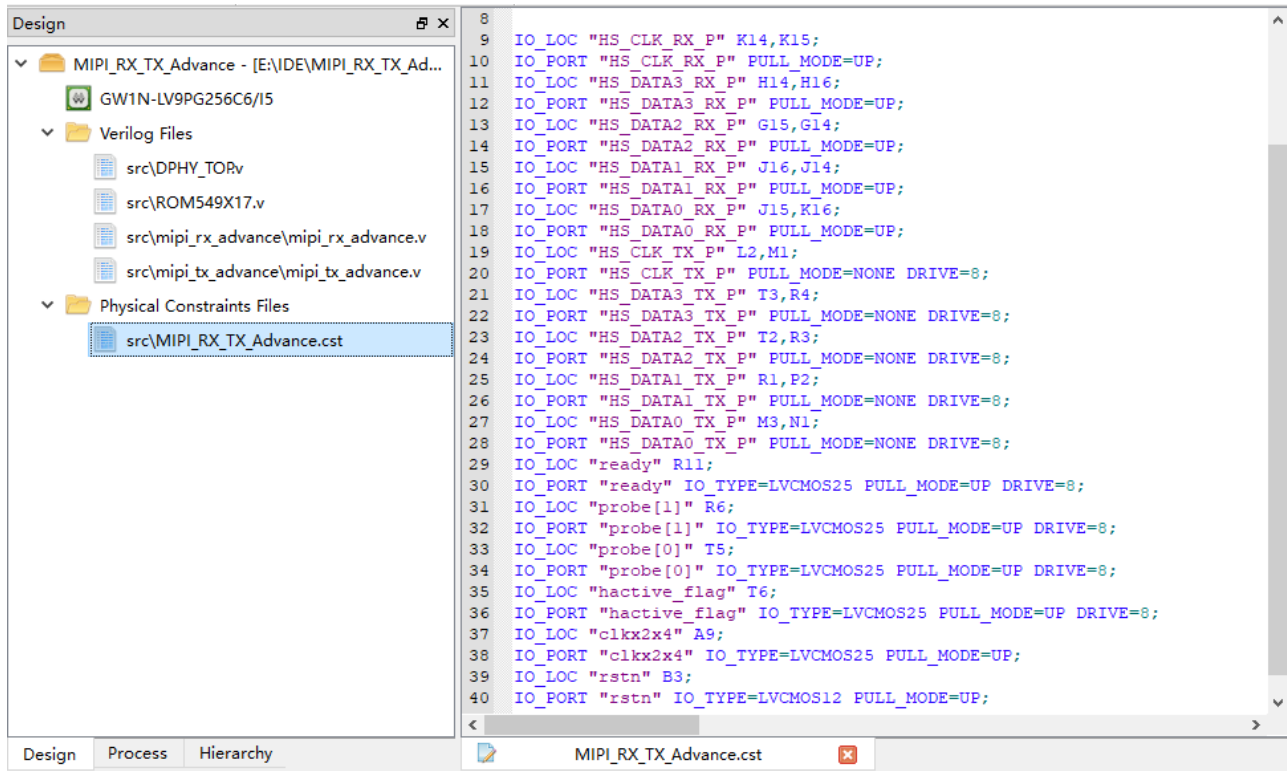
Figure 3-12 I/O Constraints

	Port	Direction	Diff Pair	Location	Bank	Exclusive	IO Type
1	HS_CLK_RX_P	input	HS_CLK_RX_N	K14,K15	0	False	LVCNOS33D
2	HS_CLK_TX_P	output	HS_CLK_TX_N	L2,M1	2	False	LVCNOS33D
3	HS_DATA0_RX_P	input	HS_DATA0_RX_N	J15,K16	0	False	LVCNOS33D
4	HS_DATA0_TX_P	output	HS_DATA0_TX_N	M3,N1	2	False	LVCNOS33D
5	HS_DATA1_RX_P	input	HS_DATA1_RX_N	J16,J14	0	False	LVCNOS33D
6	HS_DATA1_TX_P	output	HS_DATA1_TX_N	R1,P2	2	False	LVCNOS33D
7	HS_DATA2_RX_P	input	HS_DATA2_RX_N	G15,G14	0	False	LVCNOS33D

After constraints finished, click "Save" to generate physical constraints

files as shown in Figure 3-13.

Figure 3-13 Physical Constraints Display



In PnR, if there is no physical constraints file, the PnR will be automatically performed. If there is a physical constraint file, the PnR will be performed according to the physical constraints file.

3.3.2 Modify Physical Constraints

After physical constraints files generated, you can modify the constraints by FloorPlanner. Click "Save" to finish.

3.4 Timing Constraint

After synthesis, you can use Timing Constraints Editor or write manually to add timing constraints. In this design, Timing Constraints Editor is selected. For more details, please refer to [SUG101](#), Gowin Design Timing Constraints Guide.

3.4.1 Create New Timing Constraints

Click "Process > User Constraints > Timing Constrains Editor" to open Timing Constrains Editor, which supports clock, I/O and timing report constraints. This design adds clock and timing report constraints and uses them as instances.

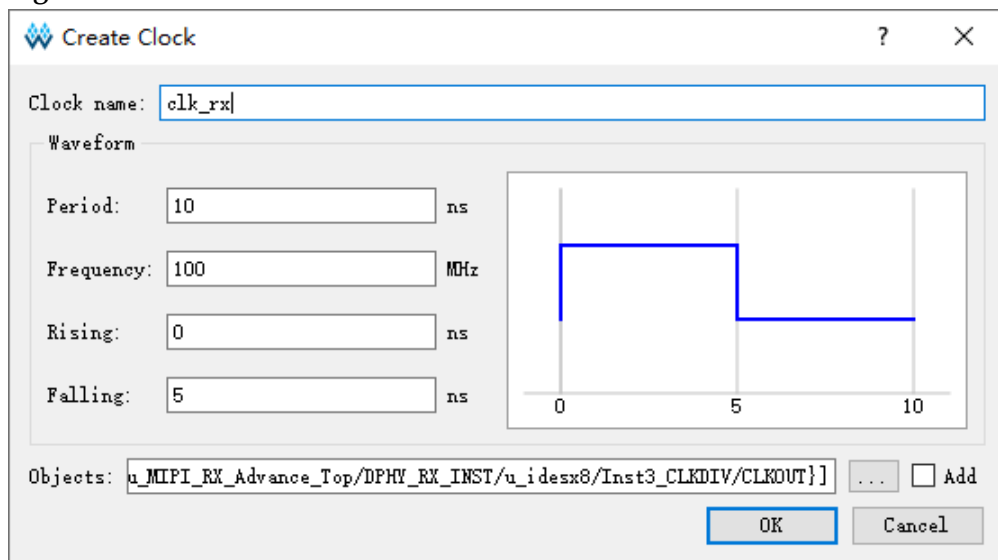
Clock Constraints

- Select "Timing Constraints > Clocks" and right-click to select "Create Clock" as shown in Source Object: get_pins
{ u_MIPI_RX_Advance_Top/DPHY_RX_INST/u_idesx8/Inst3_CLKDIV/CLKOUT}

Figure 3-14. The constraints are as follows:

- Clock name: clk_rx
- Period: 10
- Rising: 0
- Falling: 5
- Source Object: get_pins
{ u_MIPI_RX_Advance_Top/DPHY_RX_INST/u_idesx8/Inst3_CLKDIV/CLKOUT}

Figure 3-14 Clock Constraints



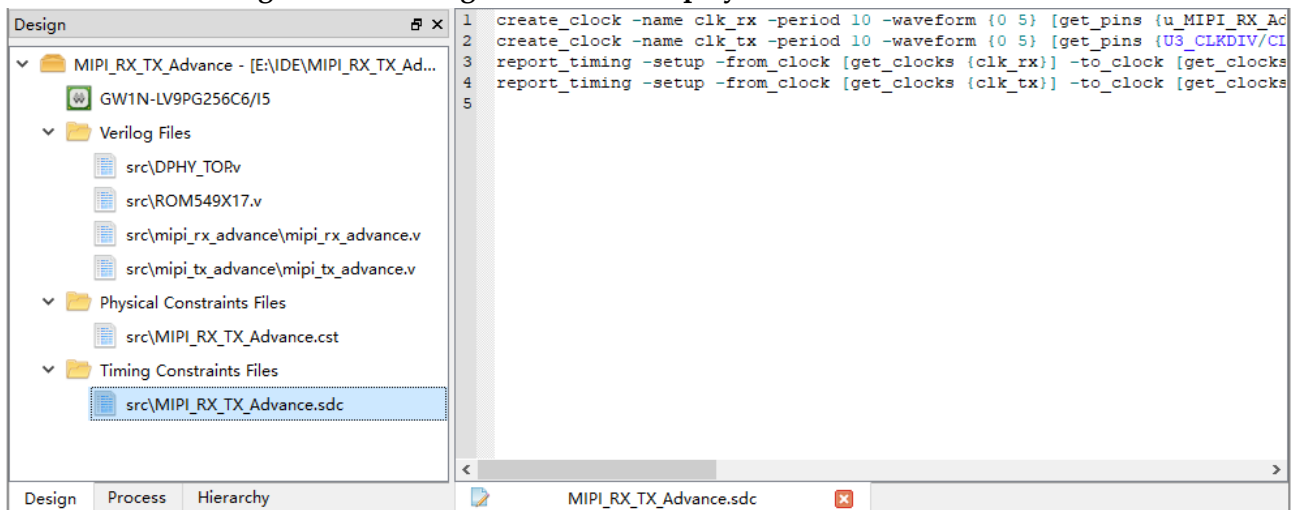
Timing Report Constraint

Select "Timing Constraints > Report > Report Timing" and right-click to select "Create Report". You can configure parameters in Report Timing dialog box. The max.setup path is 100, as shown in Figure 3-15.

Figure 3-15 Timing Report Constraints

After constraints is finished, click "Save" to generate timing constraints, as shown in Figure 3-16.

Figure 3-16 Timing Constraints Display



In PnR, if there is no timing constraints file, the PnR will be automatically performed. If there is a timing constraint file, the PnR will be performed according to the timing constraints file.

3.4.2 Modify Timing Constraints

After timing constraints files are generated, you can modify the constraints by Timing Constraints Editor. Click "Save" to finish.

3.5 GAO Configuration

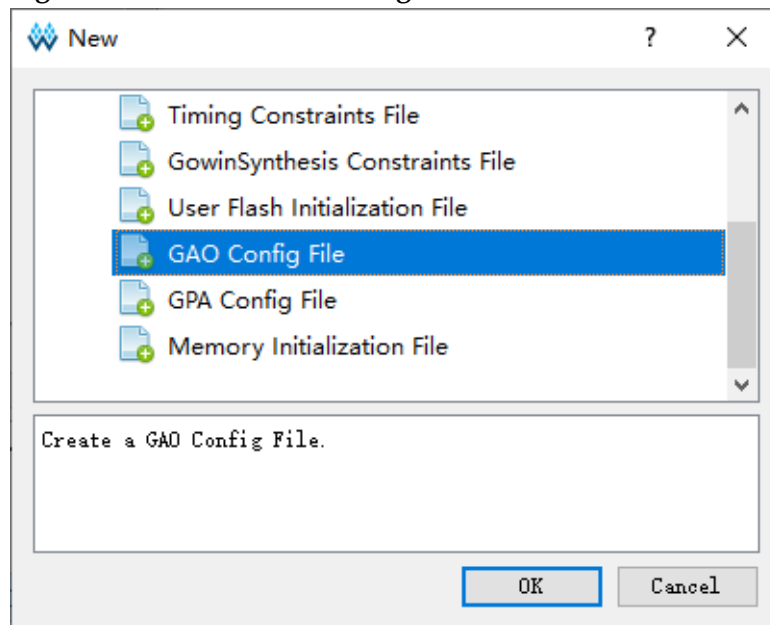
After synthesis, you can create GAO config file to capture data and verify the design. Gowin Software provides Standard Mode GAO and Lite Mode GAO. For the usage, see [SUG114](#), Gowin Analyzer Oscilloscope User Guide.

This design uses Standard Mode GAO and takes it as an instance.

3.5.1 Create Standard Mode GAO Config File

Select "Design > New File..." to open "New" dialog box, and select "GAO Config File" in "New", as shown in Figure 3-17. Click "OK". Select For Post-Synthesis Netlist in Type, Standard in Mode. Click "Next". The file name is MIPI_RX_TX. Then click "Next" until finished.

Figure 3-17 Create GAO Config File



3.5.2 Configure Standard Mode GAO

After file created, you can configure the number of AO cores, trigger options and capture options. The trigger options include match unit, trigger port, match type and expressions; The capture options include sample clock, capture, capture utilization and capture signals. In this design the number of AO cores is 1 and the trigger options and capture options configuration are shown in Figure 3-18 and Figure 3-19.

Figure 3-18 Trigger Options Configuration

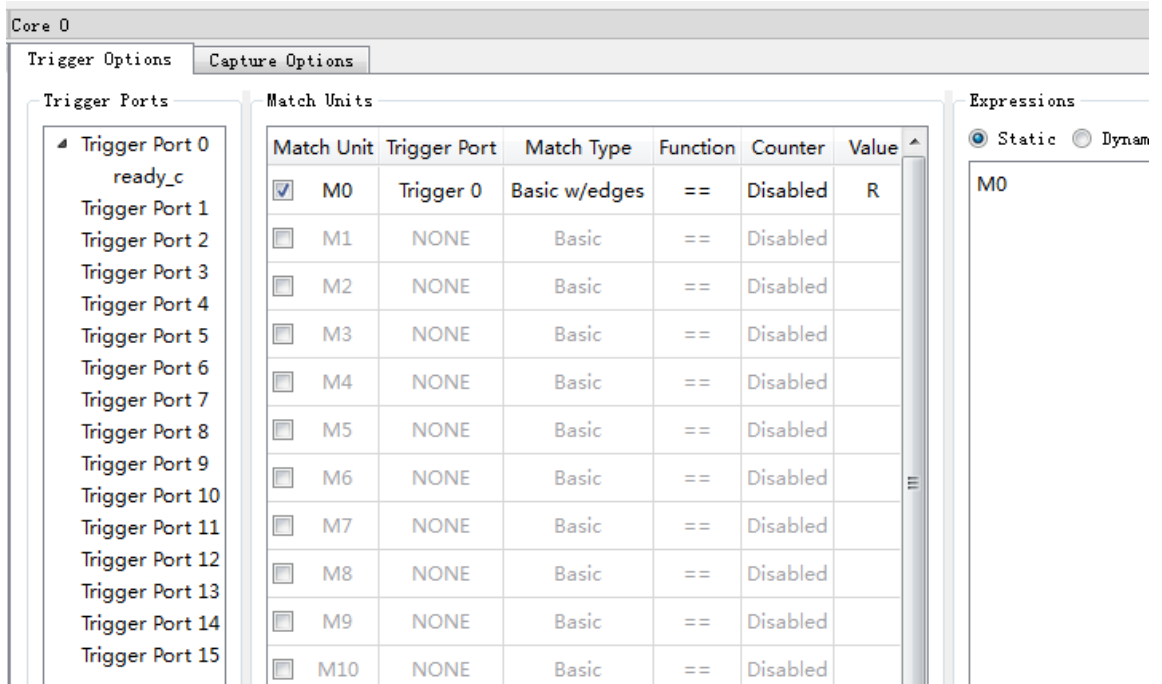
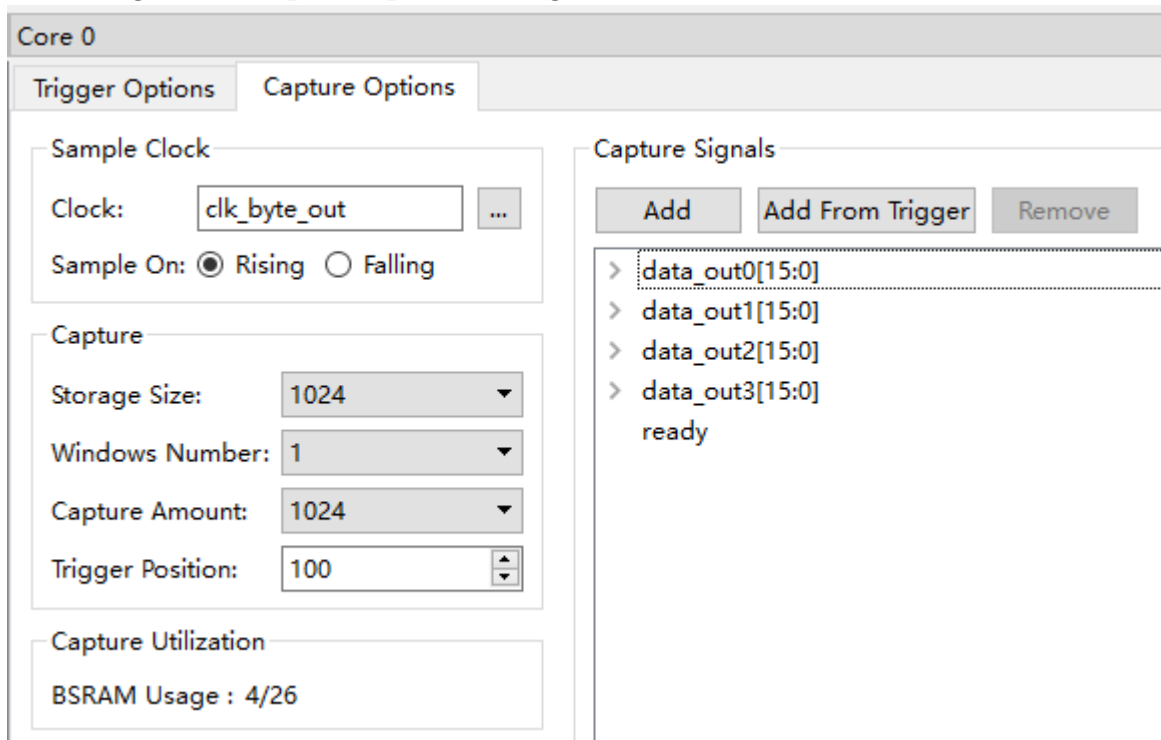
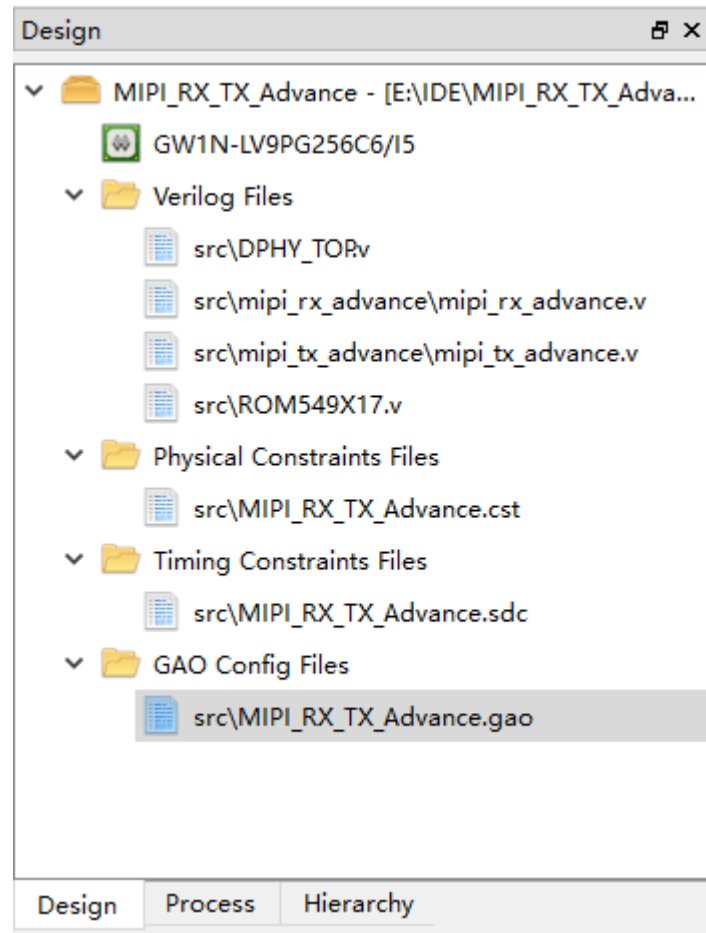


Figure 3-19 Capture Options Configuration



After configuration, click "Save" to finish and the design window is as shown in Figure 3-20.

Figure 3-20 GAO Config Files

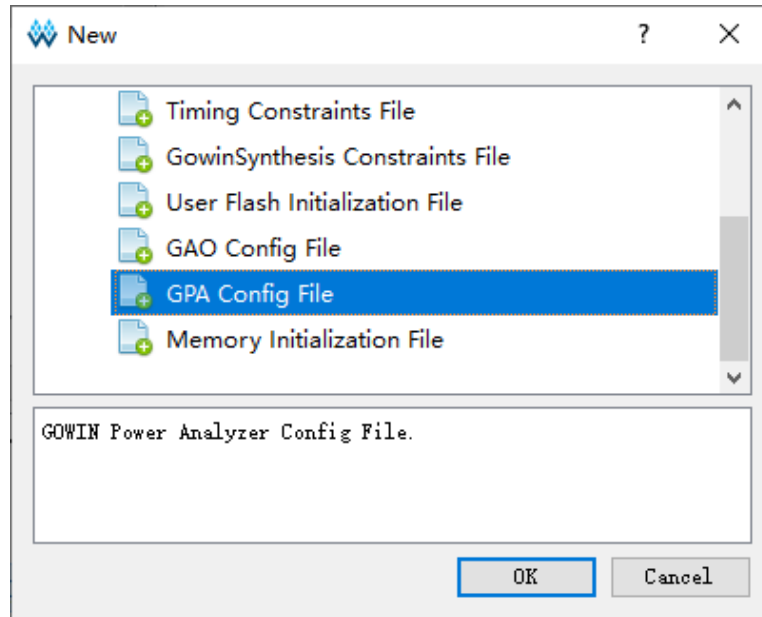


3.6 GPA Configuration

After synthesis, you can create a GPA config file to analyze power. For the usage, please refer to [SUG282](#), Gowin Power Analyzer User Guide.

3.6.1 Create GPA Config File

Select "Design > New File..." to open "New" dialog box, and select "GPA Config File" in "New", as shown in Figure 3-21. Click "OK". The file name is MIPI_RX_TX_Advance, and the file is under src by default. Then click "OK" to finish.

Figure 3-21 Create GPA Config File

3.6.2 Configure GPA

After GPA config file is created, configure General Setting, Rate Setting and Clock Setting.

- General Setting includes the parameters of device, package, speed grade, temperature grade, thermal impedance, and voltage.
- Rate Setting is used to configure signal transition rate. You can set transition rate of IO or Net, or use the default value.
- Clock Setting is used to configure clock and enable features of BSRAM, I/O and DFF.

General Setting

In this design, the general setting is configured as follows: commercial temperature, 25°C ambient temperature, no heat sink, VCCX 3.3V and VCC 1.2V, as shown in Figure 3-22.

Figure 3-22 General Setting Configuration

General Setting Rate Setting Clock Setting

Device

Device: GW1N-LV9PG256C6/I5

Operating Condition: COMMERCIAL Process: TYPICAL

Environment

Ambient Temperature: 25.000°C

Custom Theta JA: 25.000°C/W

Heat Sink

None Low Profile Medium Profile High Profile Custom

Air-flow: 0 (LFM)

Custom Theta SA: 25.000°C/W

Board Thermal Model

None Custom Typical

Board Temperature: 25.000°C (-40°C-100°C)

Custom Theta JB: 25.000°C/W

Voltage

VCC: 1.200V

VCCX: 3.300V

MIPI_RX_TX_Advance.gpa

Rate Setting

In this design, the transition rate of clkx2x4 is 50% and the remaining signals use the default value, as shown in Figure 3-23.

Figure 3-23 Rate Setting Configuration

General Setting Rate Setting Clock Setting

Net Rate

% transition/s

Name	Value
clkx2x4	50.00%

VCD File

Instance	File Name	File Type
----------	-----------	-----------

Filter glitch on VCD file

Default Rate Setting

Default Rate used for IO input signals: 12.50 %

Default Rate used for remaining signals

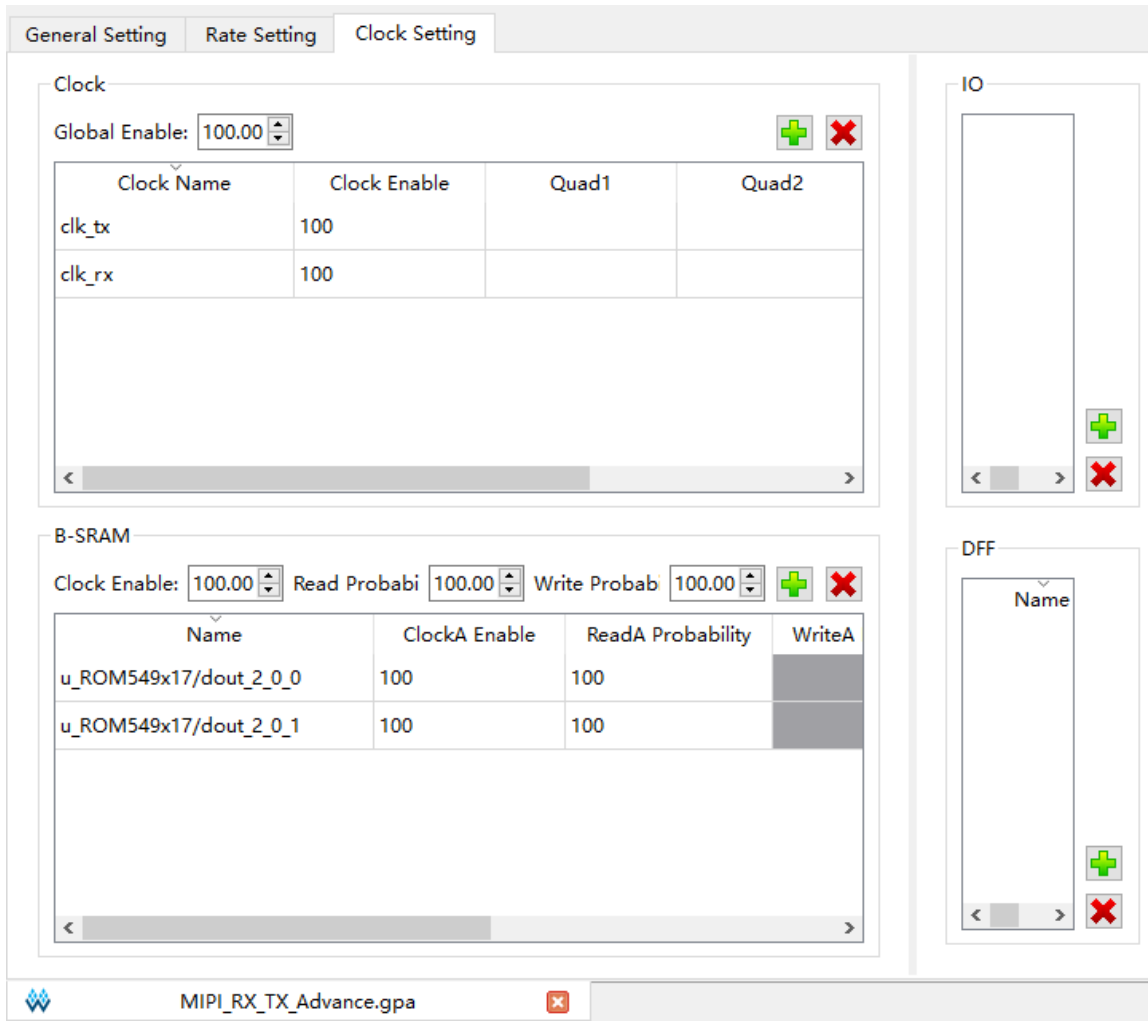
Default Value: 12.50 %

MIPI_RX_TX_Advance.gpa

Clock Setting

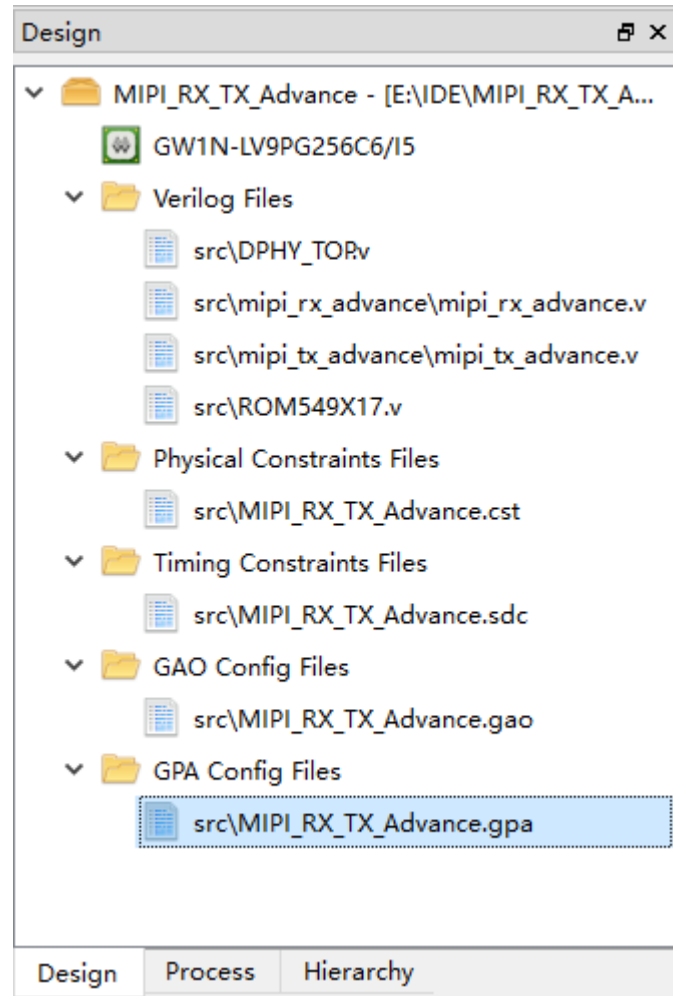
In this design, the clock is created in the timing analysis. The pROM clock enable and read enable used in this design is specified by BSRAM, and the rest are not set, as shown in Figure 3-24.

Figure 3-24 Clock Setting Configuration



After configuration, click "Save" to finish and the design window is as shown in Figure 3-25.

Figure 3-25 GPA Config Files



In PnR, if there is no GPA config file, the PnR will be automatically performed. If there is a GPA config file, the PnR will be performed according to the GPA config file.

3.7 Place & Route

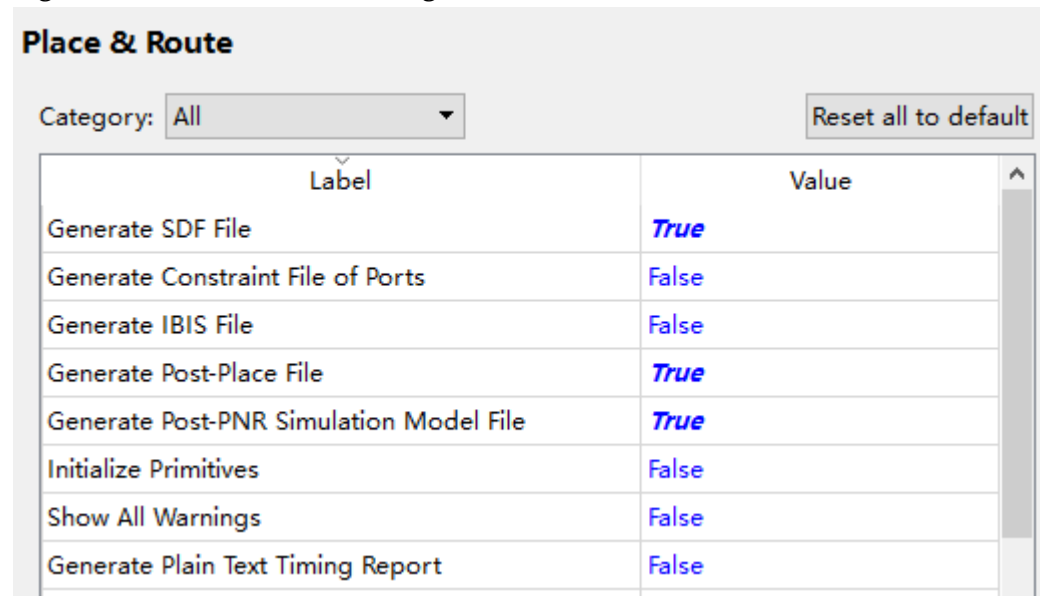
After synthesis and the creation of physical constraints files, timing constraints file, GAO config file, GPA config file as required, you can start PnR.

3.7.1 Configuration

Select "Process > Place & Route > Configuration" to open Configurations to configure General, Dual-Purpose and Bitstream. For the details, see [SUG100](#), Gowin Software User Guide.

In this design, Generate SDF File, Generate Post-Place File and Generate Post-PNR Simulation Model File are configured to True. Place input register to IOB, Place output register to IOB and Place inout register to IOB are configured to False, and the rest use default values, as shown in Figure 3-26.

Figure 3-26 Place & Route Configuration

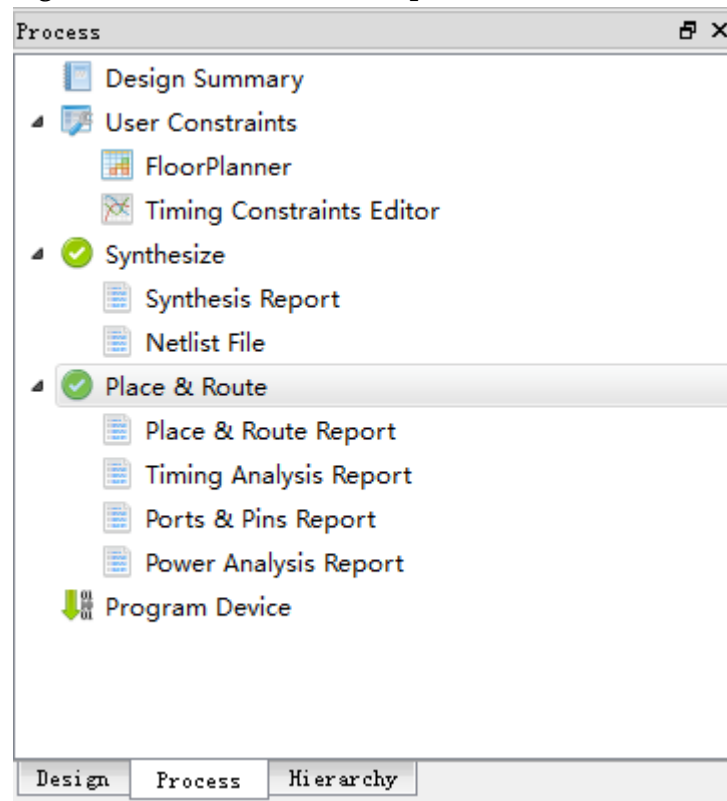


3.7.2 Run PnR

After configuration, you can run PnR.

Double-click Place & Route in Process window to start PnR based on physical constraints, timing constraints, GAO config, GPA config. After PnR, the icon before the Place & Route changes to "✔", as shown in Figure 3-27.

Figure 3-27 Place & Route Completed



After finishing PnR, the pnr folder is generated under the project creation path \impl, as shown in Figure 3-28. The folder contains all the files generated in PnR, including the bitstream file, the netlist file after PnR, and the output reports. For the details, refer to [3.11 Output Files](#).

Figure 3-28 PnR Directory

Name	Date modified	Type	Size
ao_0.bin	6/10/2021 16:08	BIN File	435 KB
ao_0.binx	6/10/2021 16:08	BINX File	435 KB
ao_0.fs	6/10/2021 16:08	FS File	3,476 KB
cmd.do	6/10/2021 16:08	DO File	1 KB
device.cfg	6/10/2021 16:58	CFG File	1 KB
MIPI_RX_TX_Advance.bin	6/10/2021 15:32	BIN File	435 KB
MIPI_RX_TX_Advance.binx	6/10/2021 15:32	BINX File	435 KB
MIPI_RX_TX_Advance.db	6/10/2021 16:08	Data Base File	48 KB
MIPI_RX_TX_Advance.fs	6/10/2021 15:32	FS File	3,476 KB
MIPI_RX_TX_Advance.log	6/10/2021 16:08	LOG File	2 KB
MIPI_RX_TX_Advance.pin.html	6/10/2021 16:08	360 se HTML Doc...	57 KB
MIPI_RX_TX_Advance.posp	6/10/2021 16:08	POSP File	1 KB
MIPI_RX_TX_Advance.power.html	6/10/2021 16:08	360 se HTML Doc...	9 KB
MIPI_RX_TX_Advance.rpt.html	6/10/2021 16:08	360 se HTML Doc...	64 KB
MIPI_RX_TX_Advance.rpt.txt	6/10/2021 16:08	TXT File	48 KB
MIPI_RX_TX_Advance.sdf	6/10/2021 16:08	SDF File	2,356 KB
MIPI_RX_TX_Advance.timing_paths	6/10/2021 16:08	TIMING_PATHS File	53 KB
MIPI_RX_TX_Advance.tr.html	6/10/2021 16:08	360 se HTML Doc...	1 KB
MIPI_RX_TX_Advance.vo	6/10/2021 16:08	VO File	1,098 KB
MIPI_RX_TX_Advance_tr_cata.html	6/10/2021 16:08	360 se HTML Doc...	9 KB
MIPI_RX_TX_Advance_tr_content.html	6/10/2021 16:08	360 se HTML Doc...	1,230 KB

If the project contains the GAO config file, after PnR, gao file is generated under the project creation path \impl, as shown in Figure 3-29:

- ao_0 contains the parameter files of the AO core.
- ao_control contains the parameter files of the control AO core.
- gao.v is the netlist file GAO post-synthesis, encrypted.
- gw_gao_top.v is the top of GAO, connecting ao, ao_control and jtag modules.
- The other files are generated during GAO synthesis.

Figure 3-29 GAO Directory

Name	Date modified	Type	Size
ao_0	6/10/2021 17:17	File folder	
ao_control	6/10/2021 17:17	File folder	
gao.v	6/10/2021 15:35	V File	269 KB
gao_std.prj	6/10/2021 15:35	PRJ File	2 KB
gw_gao_top.v	6/10/2021 15:35	V File	7 KB

3.8 Timing Optimization

After finishing PnR, you can use FloorPlanner to modify physical constraints and key path to help users realize timing closure to achieve timing optimization. For more details, see [SUG935](#), Gowin Design Physical Constraints User Guide

A place file and a timing path file are needed for timing optimization when using FloorPlanner, and these two files are automatically generated in PnR.

3.8.1 Timing Analysis

After finishing PnR, a timing report will be generated. If the max.frequency does not meet requirements, as shown in Figure 3-30, the timing can be optimized by FloorPlanner.

Figure 3-30 Max. Frequency

Max Frequency Summary:						
NO.	Clock Name	Constraint	Actual Fmax	Logic Level	Entity	
1	clk_rx	100.000(MHz)	97.734(MHz)	5	TOP	
2	clk_tx	100.000(MHz)	177.943(MHz)	1	TOP	
3	u_MIP1_RX_Advance_Top/DPHY_RX_INST/HS_CLK	100.000(MHz)	113.980(MHz)	2	TOP	
4	u_gw_jtag/tck_pad_i	50.000(MHz)	62.647(MHz)	5	TOP	

3.8.2 Adjust Key Path

Start FloorPlanner and the place file and the timing paths file will be loaded automatically, the setup and hold of the timing path in the Netlist window are as shown in Figure 3-31. You can highlight a path by changing "Chip Array" to "Show Place View > All Instance", as shown in Figure 3-32.

Figure 3-31 Timing Path

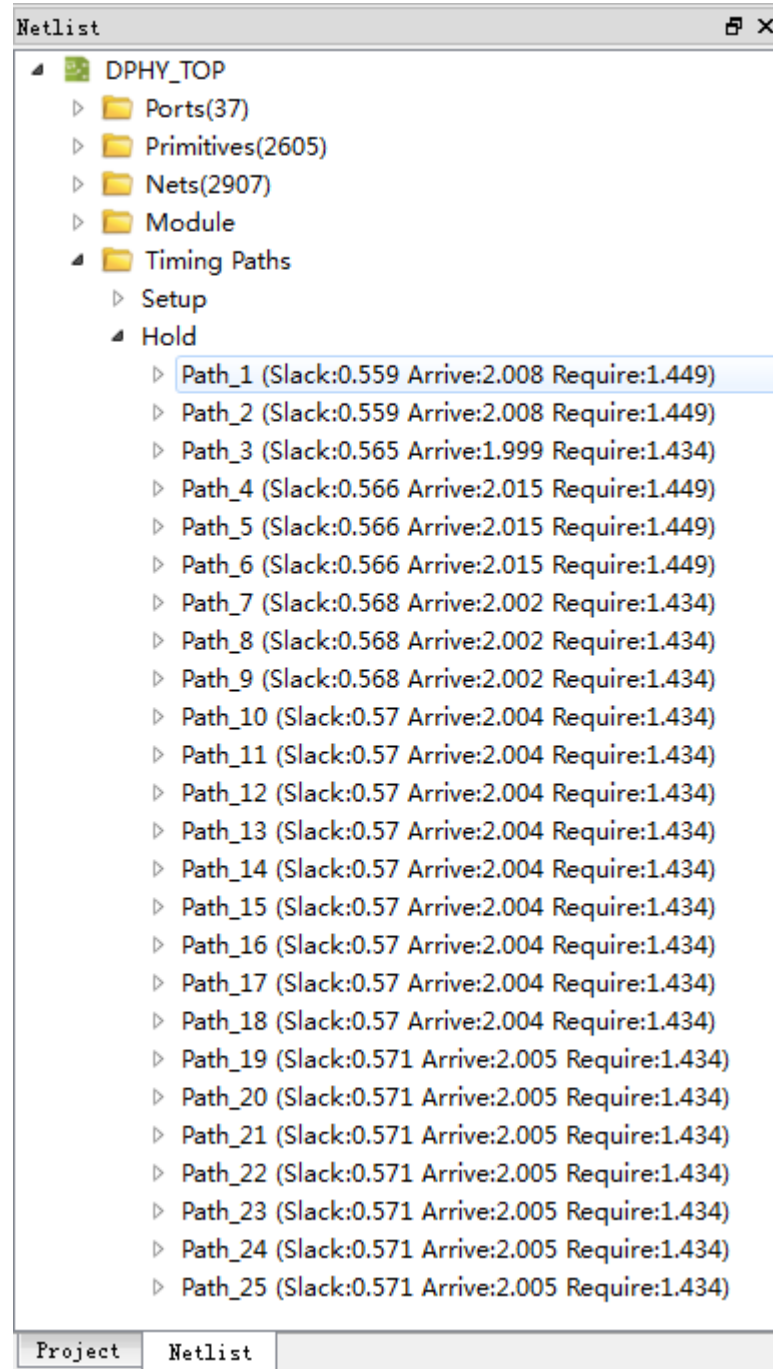
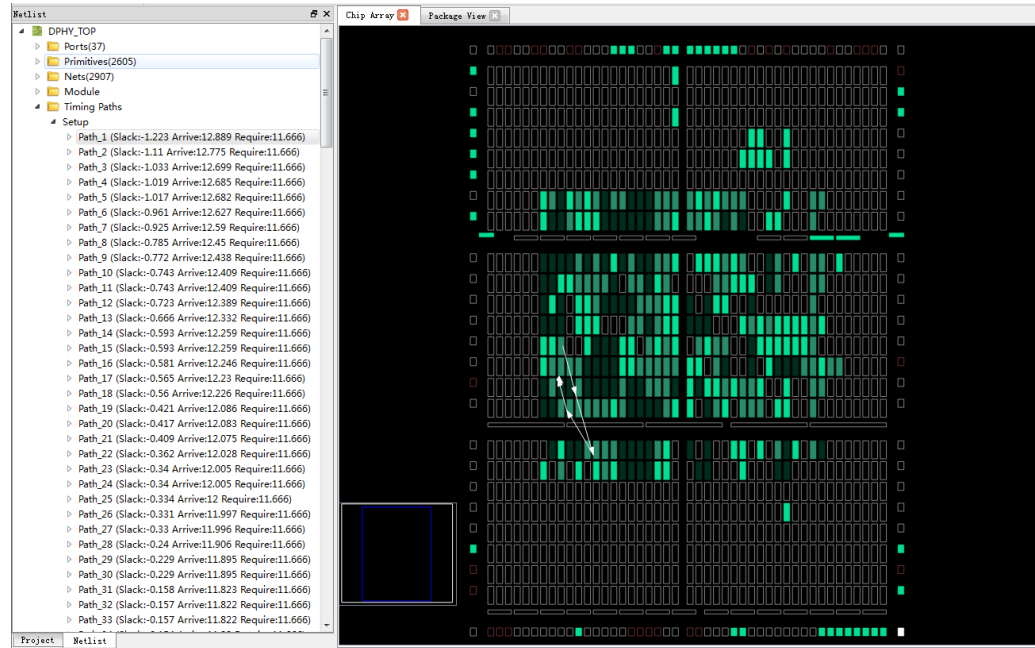
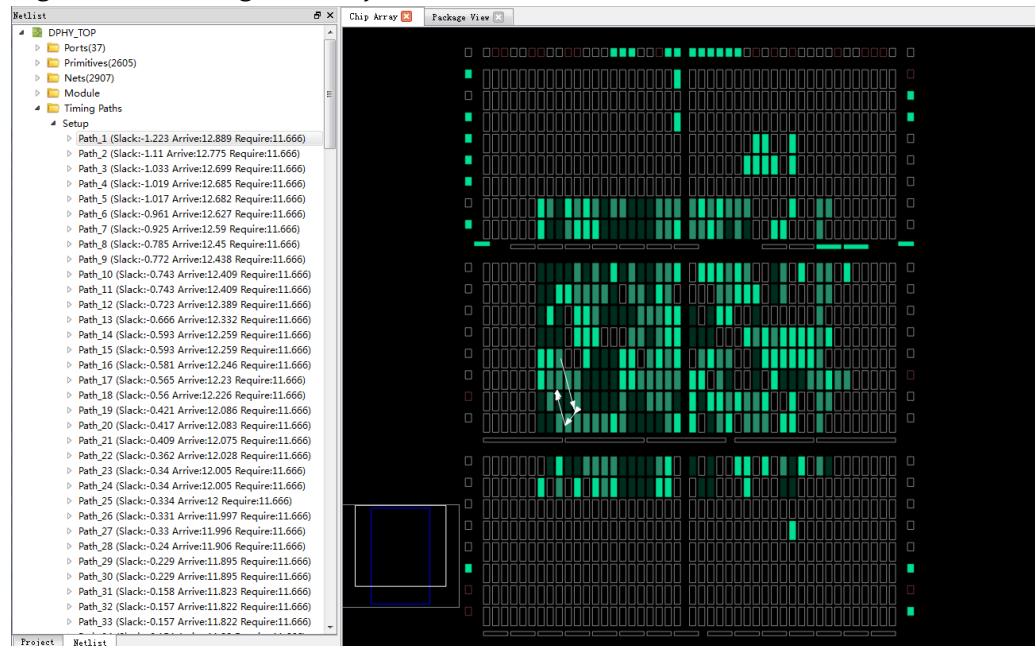


Figure 3-32 Timing Path Highlighted



After adjustment, click "Save" to finish, as shown in Figure 3-33. After this adjustment, the timing optimization can be continued if the max. frequency still does not meet the design requirements.

Figure 3-33 Timing Path Adjusted

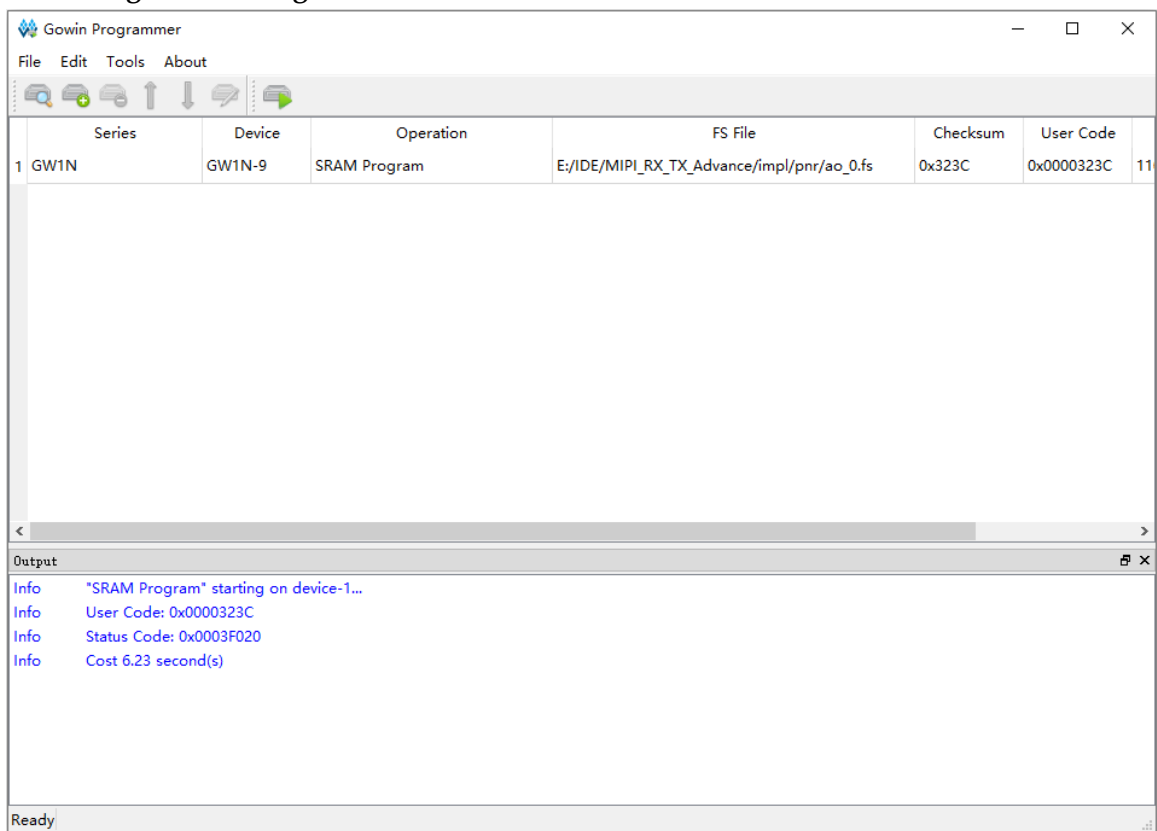


3.9 Download Bitstream

After optimization, the design can meet the timing requirements. Run Place & route again to generate the bitstream file and download it with Programmer to verify the design. For the usage, please see [SUG502](#), Gowin Programmer User Guide.

Select "Process > Program Device" to open Programmer, and the programmer automatically identifies the bitstream file. After the development board is ready, click "Program/Configure" to download the bitstream to the development board. Figure 3-34 shows the completion of the bitstream download.

Figure 3-34 Programmer

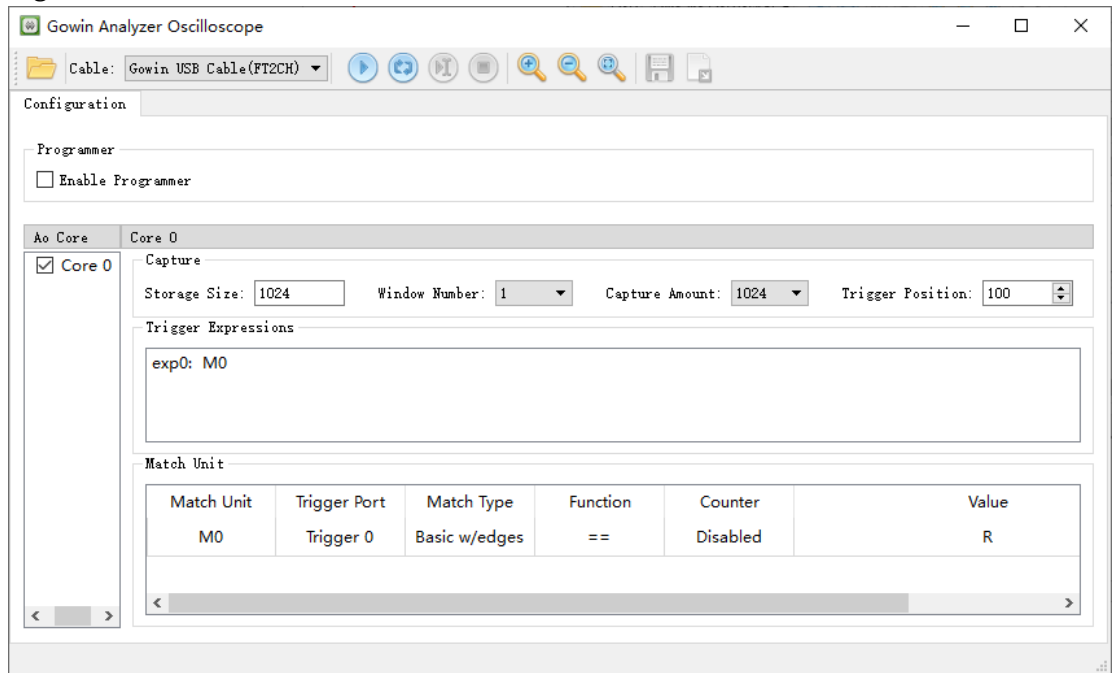


3.10 GAO Captures Data

After the bitstream is downloaded, you can use GAO to verify the design. For the usage, refer to the [SUG114](#), Gowin Analyzer Oscilloscope User Guide.

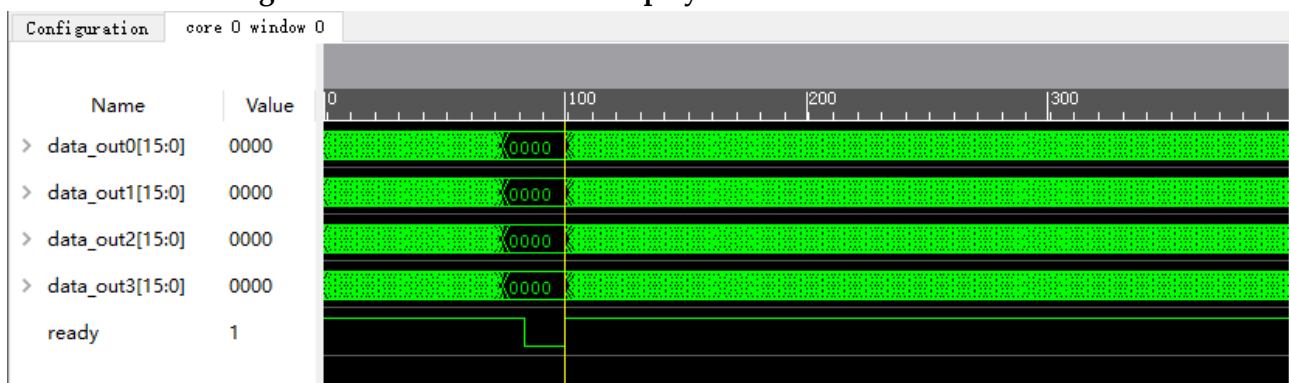
Click the GAO icon in the Gowin Software toolbar to open the GAO interface, which automatically identifies the GAO config file, as shown in Figure 3-35.

Figure 3-35 GAO Interface



Click the Start icon in the GAO interface to capture data. After finishing capturing data, GAO interface generates a window to display the waveform, as shown in Figure 3-36. The window supports cursor, zoom-out and so on so as to facilitate you to analyze the data.

Figure 3-36 GAO Waveform Display



3.11 Output Files

3.11.1 Place & Route Report

The Place & Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the file suffix .rpt.html. Check the *.rpt.html file for further details.

Double-click "Place & Route Report" in the Process window to open Place & Route report, as shown in Figure 3-37.

For the details, refer to 6.2 Place & Route Report of [SUG100](#) Gowin Software User Guide.

Figure 3-37 Place & Route Report

PnR Details

Place & Route Process	Running placement: Placement Phase 0: CPU time = 0h 0m 0.187s, Elapsed time = 0h 0m 0.181s Placement Phase 1: CPU time = 0h 0m 0.079s, Elapsed time = 0h 0m 0.08s Placement Phase 2: CPU time = 0h 0m 0.375s, Elapsed time = 0h 0m 0.37s Placement Phase 3: CPU time = 0h 0m 1s, Elapsed time = 0h 0m 1s Placement Phase GAO: CPU time = 0h 0m 0.047s, Elapsed time = 0h 0m 0.047s Total Placement: CPU time = 0h 0m 2s, Elapsed time = 0h 0m 2s
Total Time and Memory Usage	Running routing: Routing Phase 0: CPU time = 0h 0m 0s, Elapsed time = 0h 0m 0.001s Routing Phase 1: CPU time = 0h 0m 0.281s, Elapsed time = 0h 0m 0.283s Routing Phase 2: CPU time = 0h 0m 0.843s, Elapsed time = 0h 0m 0.836s Routing Phase GAO: CPU time = 0h 0m 0.558s, Elapsed time = 0h 0m 0.56s Total Routing: CPU time = 0h 0m 2s, Elapsed time = 0h 0m 2s Generate output files: CPU time = 0h 0m 3s, Elapsed time = 0h 0m 3s
	CPU time = 0h 0m 6s, Elapsed time = 0h 0m 6s, Peak memory usage = 275ME

Resource

Resource Usage Summary:

Resource	Usage	Utilization
Logic	1540/8640	17%
--LUT,ALU,ROM16	1540(1531 LUT, 9 ALU, 0 ROM16)	-
--SSRAM(RAM16)	0	-
Register	837/7104	11%
--Logic Register as Latch	0/6480	0%
--Logic Register as FF	837/6480	12%

3.11.2 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes port types, attributes, and locations, etc. The generated file is saved with the .pin.html suffix. Check the .pin.html file for further details.

Double-click Ports & Pins Report in the Process window to open Ports & Pins Report, as shown in Figure 3-38.

For the details, refer to 6.3 Ports & Pins Report of [SUG100](#), Gowin Software User Guide.

Figure 3-38 Ports & Pins Report

Pin Details

Pinout by Port Name:

Port Name	Diff Pair	Loc./Bank	Constraint	Dir.	Site	IO Type	Drive	Pull Mode
HS_CLK_RX_P	HS_CLK_RX_N	K14,K15/0	Y	in	I0T29	LVCMOS33D	NA	UP
HS_DATA3_RX_P	HS_DATA3_RX_N	H14,H16/0	Y	in	I0T23	LVCMOS33D	NA	UP
HS_DATA2_RX_P	HS_DATA2_RX_N	G15,G14/0	Y	in	I0T17	LVCMOS33D	NA	UP
HS_DATA1_RX_P	HS_DATA1_RX_N	J16,J14/0	Y	in	I0T25	LVCMOS33D	NA	UP
HS_DATA0_RX_P	HS_DATA0_RX_N	J15,K16/0	Y	in	I0T27	LVCMOS33D	NA	UP
rstn		B3/2	Y	in	I0B12[A]	LVCMOS12	NA	UP
clkx2x4		A9/3	Y	in	I0L9[A]	LVCMOS25	NA	UP
HS_CLK_TX_P	HS_CLK_TX_N	L2,M1/2	Y	out	I0B29	LVCMOS33D	8	NONE
HS_DATA3_TX_P	HS_DATA3_TX_N	T3,R4/2	Y	out	I0B45	LVCMOS33D	8	NONE
HS_DATA2_TX_P	HS_DATA2_TX_N	T2,R3/2	Y	out	I0B43	LVCMOS33D	8	NONE
HS_DATA1_TX_P	HS_DATA1_TX_N	R1,P2/2	Y	out	I0B41	LVCMOS33D	8	NONE
HS_DATA0_TX_P	HS_DATA0_TX_N	M3,N1/2	Y	out	I0B39	LVCMOS33D	8	NONE
hactive_flag		T6/1	Y	out	I0R25[B]	LVCMOS25	8	UP
probe[0]		T5/1	Y	out	I0R27[A]	LVCMOS25	8	UP
probe[1]		R6/1	Y	out	I0R27[B]	LVCMOS25	8	UP
ready		R11/1	Y	out	I0R3[A]	LVCMOS25	8	UP

All Package Pins:

Loc./Bank	Signal	Dir.	Site	IO Type	Drive	Pull Mode	PCI Clamp	Hysteresis
I15/3	-	in	I0T2[A]	LVCMOS18	NA	IUP	NA	NONE

3.11.3 Timing Report

The timing report includes setup check, hold check, recovery time check, removal time check, min. clock pulse check, max. fan out path, Place & Route congestion report, etc. by default. The timing report also includes the max. frequency report.

Double-click Timing Analysis Report in the Process window to open the timing analysis report for the project, as shown in Figure 3-39.

For the details, please refer to [SUG940](#), Gowin Design Timing Constraints User Guide.

Figure 3-39 Timing Report

Timing Messages

Report Title	Gowin Timing Analysis Report
Design File	E:\IDE\MIP1_RX_TX\mpl\synthesize\rev_1\MIP1_RX_TX.vm
Physical Constraints File	E:\IDE\MIP1_RX_TX\src\MIP1_RX_TX.cst
Timing Constraint File	E:\IDE\MIP1_RX_TX\src\MIP1_RX_TX.sdc
GOWIN version	V1.9.7Beta
Part Number	GW1N-LV9PG256C6/I5
Device	GW1N-9
Created Time	Mon Sep 07 16:56:05 2020
Legal Announcement	Copyright (C)2014-2020 Gowin Semiconductor Corporation. All rights reserved.

Timing Summaries

STA Tool Run Summary:

Setup Delay Model	Slow 1.14V 85C
Hold Delay Model	Fast 1.26V 0C
Numbers of Paths Analyzed	3785
Numbers of Endpoints Analyzed	3982
Numbers of Falling Endpoints	1
Numbers of Setup Violated Endpoints	0
Numbers of Hold Violated Endpoints	0

3.11.4 Power Analysis Report

The Power Analysis Report helps you evaluate the basic power consumption of your design.

Double-click Power Analysis Report in the Process window to open the power analysis report as shown in Figure 3-40.

For the details, please refer to chapter 4 Power Analysis Report of [SUG282](#), Gowin Power Analysis User Guide.

Figure 3-40 Power Analysis Report

Power Summary

- Power Messages
- Power Summary
 - Power Information
 - Thermal Information
 - Configure Information
 - Supply Information
- Power Details
 - Power By Block Type
 - Power By Hierarchy
 - Power By Clock Domain

Power Information:

Total Power (mW)	32.529
Quiescent Power (mW)	3.686
Dynamic Power (mW)	28.843

Thermal Information:

Junction Temperature	25.330
Theta JA	10.200
Max Allowed Ambient Temperature	84.670

Configure Information:

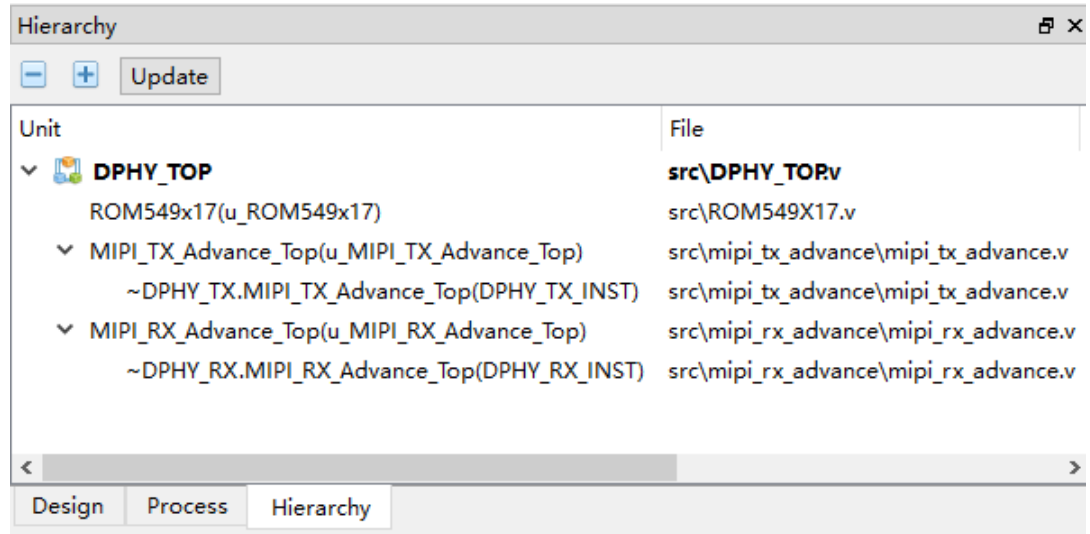
Default IO Toggle Rate	0.125
Default Remain Toggle Rate	0.125
Use Vectorless Estimation	false
Filter Glitches	false
Related Vcd File	
Related Saif File	
Use Custom Theta JA	false
Air Flow	LFM_0
Heat Sink	None
Use Custom Theta SA	false
Board Thermal Model	None
Use Custom Theta TD	false

3.12 File Encryption

3.12.1 Source File Encryption

When you need to encrypt and protect source files, you can encrypt the selected module and its sub modules in Hierarchy window, as shown in Figure 3-41. For details, see [SUG100](#), Gowin Software User Guide.

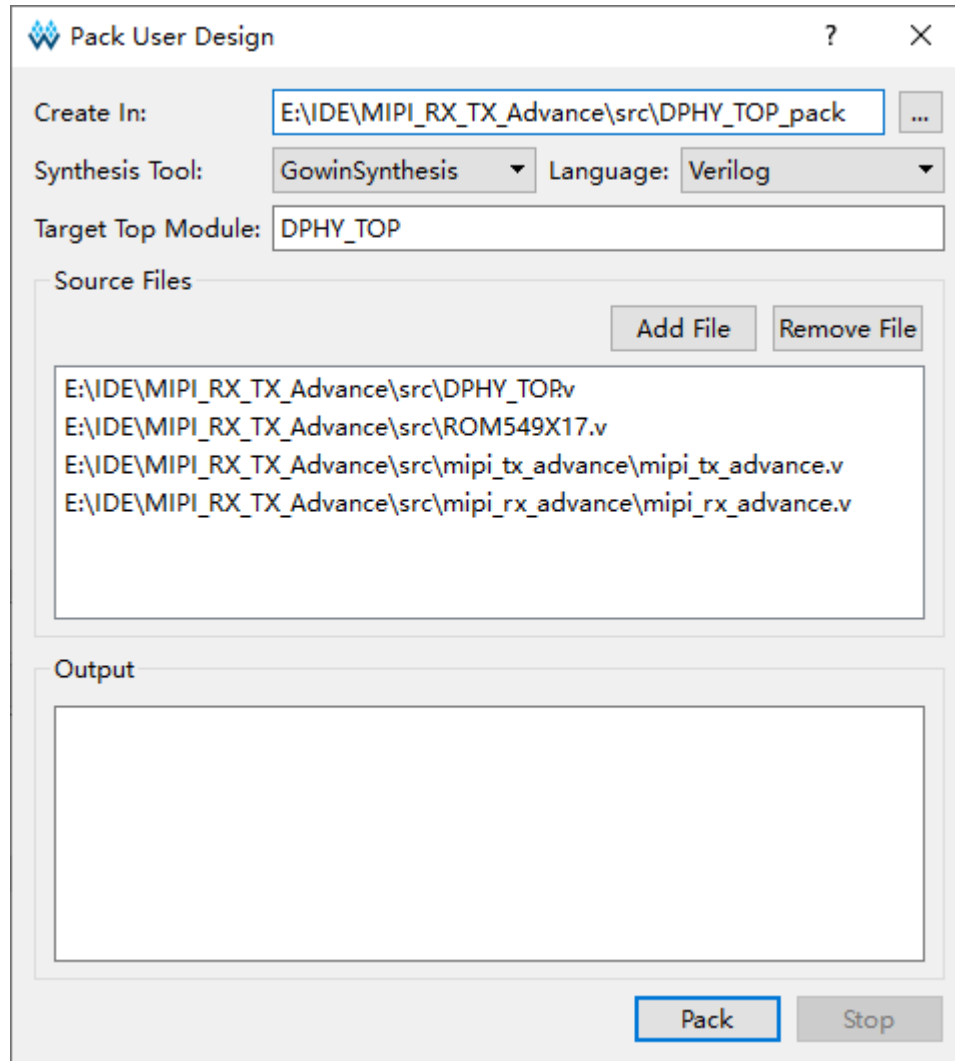
Figure 3-41 Hierarchy Window



Take module DPHY_TOP as an example to introduce the file encryption.

You can right-click DPHY_TOP in the Hierarchy window and select "Pack User Design" in the right-click list to open the dialog box, as shown in Figure 3-42.

Figure 3-42 Pack User Design Dialog Box



Select DPHY_TOP as the top module. Click "Pack" to start encryption. The relevant information will be printed in the Output window.

After the encryption, two files are generated under the destination path (E:\IDE\MIPI_RX_TX_Advance\src\DPHY_TOP_pack):
DPHY_TOP_gowin.vp and DPHY_TOP_sim.v.

- DPHY_TOP_gowin.vp: Encrypted files that can be used by others.
- DPHY_TOP_sim.v: Flattened synthesized plaintext netlist file that can be used for simulation.

3.12.2 Simulation File Encryption

The simulation file provided by Gowin is plaintext. In order to protect the simulation file, it can be encrypted by using a third-party simulation software, such as Modelsim and VCS, and the license of the tool needs to be obtained. Here it uses DPHY_TOP_sim.v as an example to introduce the encryption.

Encryption by Modelsim

When using Modelsim, the steps to encrypt the simulation file are as follows:

1. Add macro ``protect` and ``endprotect` before and after the encrypted in the simulation file `DPHY_TOP_sim.v`;
2. Run command: `vlog +protect DPHY_TOP_sim.v`;
3. After running the command, `DPHY_TOP_sim.vp` is generated in the work library, which is the encrypted file of `DPHY_TOP_sim.v` that can be used for Modelsim simulation.

Encryption by VCS

When using VCS, the steps to encrypt the simulation file are as follows:

1. Add macro ``protect128` and ``endprotect128` before and after the encrypted in the simulation file `DPHY_TOP_sim.v`;
2. Run command: `vcs +v2k -protect128 DPHY_TOP_sim.v`;
3. After running the command, `DPHY_TOP_sim.vp` is generated under the current path, which is the encrypted file of `DPHY_TOP_sim.v` that can be used for VCS simulation.

4 Tcl

The previous chapters introduce the way to implement the entire design process by using GUI. Gowin Software also provides tcl commands for some settings. Take MIPI design in Windows as an example to introduce the usage of tcl commands. For the details, see Appendix A of [SUG100](#), Gowin Software User Guide.

4.1 Tcl Execution

4.1.1 Tcl Editing Window

At the bottom of the Console page is the tcl editing window, where you can enter the tcl commands and press Enter to run, as shown in Figure 4-1.

Figure 4-1 Tcl Editing Window

```
Generate file "E:\IDE\MIPI_RX_TX_Advance\impl\pnr\MIPI_RX_TX_Advance.rpt.html" completed
Generate file "E:\IDE\MIPI_RX_TX_Advance\impl\pnr\MIPI_RX_TX_Advance.rpt.txt" completed
Generate file "E:\IDE\MIPI_RX_TX_Advance\impl\pnr\MIPI_RX_TX_Advance.vo" completed
Generate file "E:\IDE\MIPI_RX_TX_Advance\impl\pnr\MIPI_RX_TX_Advance.tr.html" completed
Generate file "E:\IDE\MIPI_RX_TX_Advance\impl\pnr\MIPI_RX_TX_Advance.posp" completed
Thu Jun 10 16:08:46 2021
```

```
% run pnr
```

Console Message

4.1.2 Tcl Command Line

Start command: `\x.x\IDE\bin\gw_sh.exe [script file]` under the installation directory

The First Way: enter `gw_sh.exe` to start. This mode executes in the same way as the Tcl editing window, executing tcl commands one by one, as shown in Figure 4-2.

Figure 4-2 Tcl Command Line

```
*** GOWIN Tcl Command Line Console ***
% add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/DPHY_TOP.v"
add new file: "E:/IDE/MIPI_RX_TX_Advance/src/DPHY_TOP.v"
% add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/ROM549X17.v"
add new file: "E:/IDE/MIPI_RX_TX_Advance/src/ROM549X17.v"
%
```

The Second Way: use `gw_sh.exe [script file]` to execute the script file. Tcl script file can contain all the supported tcl commands, such as, device, design file, option, and run information, and tcl script file is shown in Figure 4-3. Tcl script file can be generated by handwriting or `saveto` command, but `saveto` command The tcl script file can be generated by hand or by `saveto` command, but the `saveto` command does not include the run command when generating the tcl script, so you can add the run command if needed.

Figure 4-3 Tcl Script File

```

1 add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/DPHY_TOP.v"
2 add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/ROM549X17.v"
3 add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/mipi_rx_advance/mipi_rx_advance.v"
4 add_file -type verilog "E:/IDE/MIPI_RX_TX_Advance/src/mipi_tx_advance/mipi_tx_advance.v"
5 add_file -type cst "E:/IDE/MIPI_RX_TX_Advance/src/MIPI_RX_TX_Advance.cst"
6 add_file -type sdc "E:/IDE/MIPI_RX_TX_Advance/src/MIPI_RX_TX_Advance.sdc"
7 set_device GW1N-LV9PG256C6/I5 -name GW1N-9
8 set_option -synthesis_tool gowinsynthesis
9 set_option -output_base_name MIPI_RX_TX_Advance
10 set_option -top_module DPHY_TOP
11 set_option -verilog_std sysv2017
12 set_option -gen_sdf 1
13 set_option -gen_posp 1
14 set_option -gen_sim_netlist 1
15 set_option -ireg_in_iob 0
16 set_option -oreg_in_iob 0
17 set_option -ioreg_in_iob 0
18 run all

```

4.2 Tcl Quick Start

As tcl command line executes in the same way as the Tcl editing window, the following uses tcl editing window as an example to introduce how to use it.

4.2.1 rm_file

`rm_file` is used to remove files. For example, use this tcl command to remove ROM549X17.v and DPHY_TOP.v from the project: `rm_file src/ROM549X17.v src/DPHY_TOP.v`

After running the command, the Console will display the prompt for removing files, and these two files will be removed from the Design window.

4.2.2 add_file

`add_file` is used to add files. Here it will use tcl to add the removed files to the project.

Add ROM549X17.v and DPHY_TOP.v

```
add_file src/ROM549X17.v src/DPHY_TOP.v
```

After running the command, the Console will display the prompt for adding files, and these two files will appear in the Design window.

4.2.3 set_file_enable

`set_file_enable` is used to set whether a file can be used. Here it will use tcl to set DPHY_TOP.v disable/enable.

Modify DPHY_TOP.v to disable

```
Set_file_enable src/DPHY_TOP.v false
```

After running the command, the Console will display the prompt for disabling the file and DPHY_TOP.v file is grayed out in Design window.

Modify DPHY_TOP.v to enable

```
Set_file_enable src/DPHY_TOP.v true
```

After running the command, the Console will display the prompt for enabling the file and DPHY_TOP.v file is available in Design window.

4.2.4 set_option

set_option is used to set options in the project. Here it will use tcl to configure synthesis and PnR.

- Select GowinSynthesis
set_option -synthesis_tool gowinsynthesis
- Set TOP Module/Entity to DPHY_TOP
set_option -top_module DPHY_TOP
- Set Generate SDF File to True
set_option -gen_sdf 1
- Set Generate Post-Place File to True
set_option -gen_posp 1
- Set Generate Post-PNR Simulation Model File to True
set_option -gen_sim_netlist 1
- Set Place input register to IOB to False
set_option -ireg_in_iob 0
- Set Place output register to IOB to False
set_option -oreg_in_iob 0
- Set Place inout register to IOB to False
set_option -ioreg_in_iob 0

4.2.5 run

Run is used to run a flow or all flows. Here it will use tcl to run synthesis and PnR flows.

- Run synthesis
Run syn
- Run PnR
Run pnr

4.2.6 set_device

set_device is used to set the target device. Here it will use tcl to set GW1N-9C, GW1N-LV9PG256C6/I5 as the target device.

Set GW1N-9C, GW1N-LV9PG256C6/I5 as the target device.

```
Set_device -name GW1N-9C GW1N-LV9PG256C6/I5
```

After running the command, the Console will display the device information.

4.2.7 saveto

saveto is used to save the current data to the tcl script, including device, design file, and options, but no run information. Save the data as mipi.tcl, and you can run with command line gw_sh.exe mipi, as shown below.

Save the current data to mipi.tcl

```
saveto mipi.tcl
```

After running the command, the mipi.tcl file is generated on the path where the project files are located.

