Gowin IP Core Generator

User Guide

SUG284-2.1E,05/14/2020

Disclaimer

Revision History

Date	Version	Description
03/07/2017	1.0E	Initial version published.
01/30/2018	1.2E	● GW1NR-4, GW1N-6, GW1N-9 and GW1NR-9 supported; ● BSRAM updated; ● DSP updated; ● PLL updated; ● User Flash updated.
08/25/2018	1.3E	● GW1N-2B, GW1N-4B, GW1N-6ES, GW1N-9ES, GW1NR-4B, GW1NR-9ES, GW1NS-2,GW1NS-2C supported; ● DDR3, DDR3 PHY added; ● PLL updated; ● OSC updated; ● User Flash updated; ● Interface optimized; ● CORDIC, Complex Multiplier and DIVIDER added;
10/26/2018	1.4E	● GW1NZ-1 and GW1NSR-2C supported; ● I3C and SPMI hard core added.
11/15/2018	1.5E	● GW1NSR-2 supported; ● GW1N-6ES, GW1NS-9ES and GW1NR-9ES removed;
02/12/2019	1.6E	● RiscV N25 and CAN added; ● PSRAM、DDRx、MIPI updated;
02/25/2019	1.7E	● Basic FIR Filter, FD Adaptive Filter, Integer Multiply Divider, NLMS Adaptive Filter, XCORR and Triple Speed Ethernet MAC added; ● Interface optimized (Add to Current Project option removed).
05/17/2019	1.8E	● GW1N-1S supported; ● PSRAM Memory Interface 2CH, Advanced FIR Filter, Gowin_EMPU_M1, HyperRAM Memory Interface added; ● Shadow Memory, including RAM16S, RAM16SDP and ROM16 added; ● MIPI, DDR, DDR2, DDR3 and GOWIN_EMPU updated.
11/28/2019	1.9E	● GW1NS-4, GW1NRF-4B, GW1NSE-2C, GW1NSER-4C, GW1NSR-4, GW1NSR-4C supported; ● Users can select Synplify Pro or GowinSynthesis as the synthesis tool; ● Classification of Soft IP Core adjusted; ● BandGap, rPLL, PLLVR, DPB, DPBX9, SDPB, SDPBX9, rSDP, rSDPX9, rROM, rROMX9, pROM, pROMX9 added in Hard Module; ● Remarks of the preferred primitives added.
03/10/2020	2.0E	● GW2A-18C, GW2AR-18C, and GW2A-55C supported; ● CLKDIV, CLKDIV2, DLLDLY, DCS, DQCE and DHCEN added in Hard Module;
05/14/2020	2.1E	● Document structure updated; ● DLL removed.

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1 About This Guide

1.1 Purpose

This guide describes the usage of IP Core Generator in Gowin software to help users realize complex designs in a more convenient way. Gowin software supports both Linux and Windows operating systems. The software screen shots and the supported products listed in this guide are based on the versionWindows 1.9.6 Beta. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com

1. SUG100, Gowin Software User Guide
2. SUG283, Gowin Primitive User Guide.

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology that are employed in this guide.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
IP Core	Intellectual Property Core
DPB/DPBX9	Dual Port
SP/SPX9	Single Port
SDPB/SDPBX9	Semi Dual Port
pROM/pROMX9	Read Only Memory
PADD	PADD
MULT	MULT
rPLL	PLL
PLLVR	Phase-locked Loop
OSC	On Chip Oscillator
SPMI	System Power Management Interface

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction

The IP Core Generator in Gowin software is used to generate instance components and soft IPs that users can call to implement required functions. The IP Core Generator includes the Hard Module associated with primitives and the Soft IP Core.

2.2 Features

IP Core Generator has following features:

- Supports soft IP core, hard module information preview;
- Supports customized soft IP core and hard module;
- Supports hard module instance generation;
- Supports to save configuration automatically;
- Supports the selection of synthesis tool and IP generation code language;
- Some soft IP supports to generate incentive files automatically;
- Supports to display available IPs by selecting device.

3 Usage

Select "Tools > IP Core Generator" in the menu bar or click "  " in the tool bar to open the IP Core Generator interface, as shown in Figure 3-1.

The interface includes two parts:

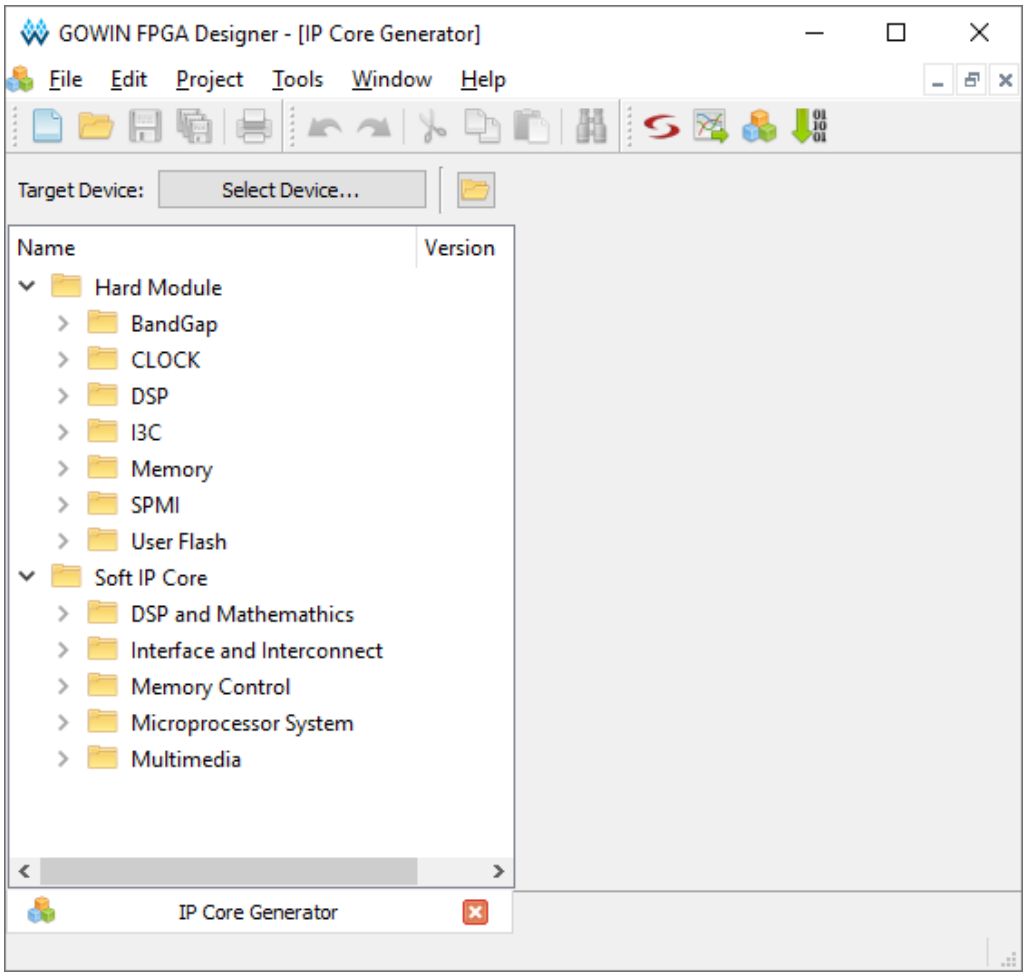
- The Hard Module associated with primitives;
- The Soft IP Core.

The Hard Module includes BandGap, CLOCK, DSP, I3C, Memory, SPMI and User Flash, etc;

Soft IP Core includes DSP and Mathematics, Interface and Interconnect, Memory Control, Microprocessor System, Multimedia, etc.

This guide aims to introduce the use of the Hard Module. For the use of the Soft IP Core, refer to the related manuals at official website.

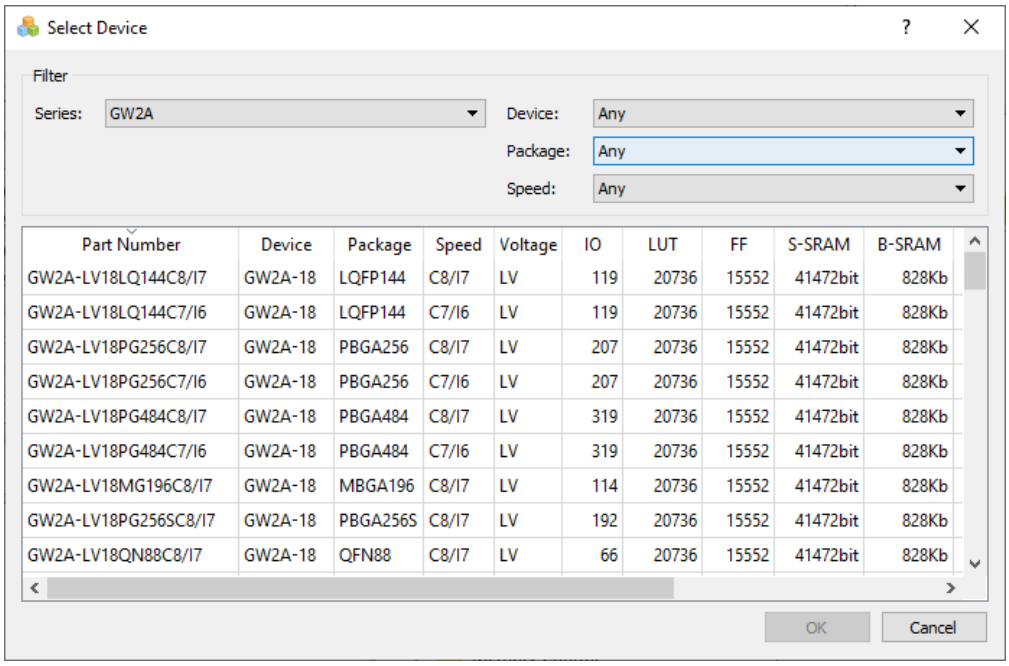
Figure 3-1 IP Core Generator Interface



It will introduce two options here: "Target Device" and "  ".

"Target Device": Configure device. Click the right box and "Select Device" dialog box pops up, as shown in Figure 3-2. You can select device from "Target Device" drop-down list. Double-click the highlighted IP to open the IP Customization dialog box, and you can also see the target device in File configuration box of in IP Customization interface.

Figure 3-2 Select Device



After device is selected, the IP Core Generator will automatically determine whether the module is supported according to the device.

- If supported, the module name is highlighted. Double-click to open the IP Customization. As shown in Figure 3-3, users can configure IP. After the configuration is completed, click "OK" to generate IP. The configuration interface of each IP will be introduced in chapter 3.
- The IP modules that are displayed in grey are not supported.

"  " can be used to open the configured IP core files. These can be edited according to the user requirements. Click the icon to open the "Select IP Config File" dialog box, and then select the IP Core Config file ".ipc". You can configure parameters and the file path cannot be changed, as shown in Figure 3-4.

Figure 3-3 IP Customization

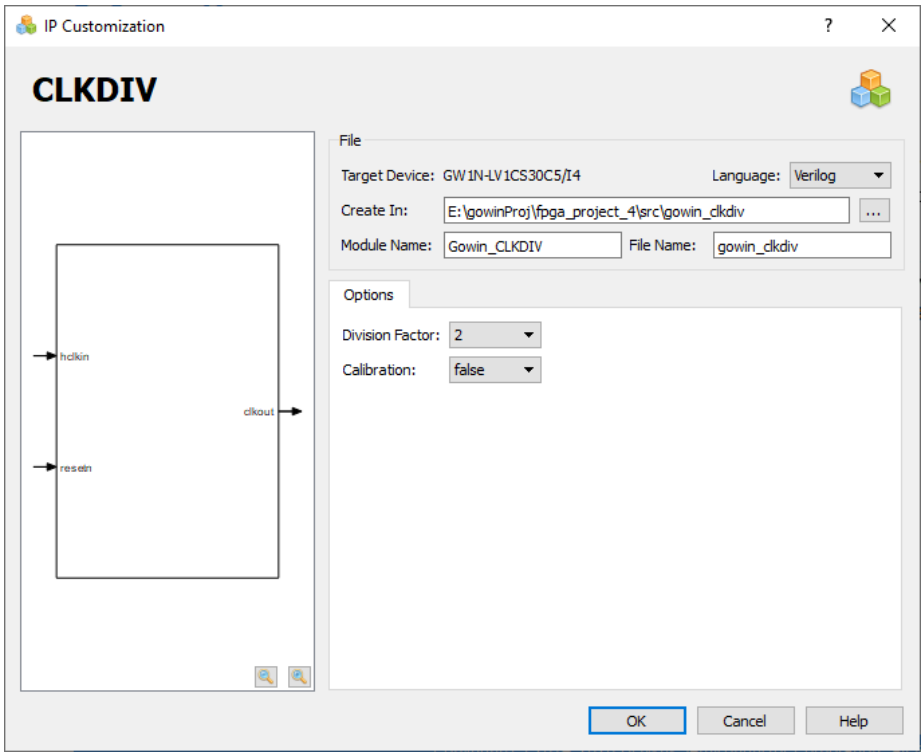
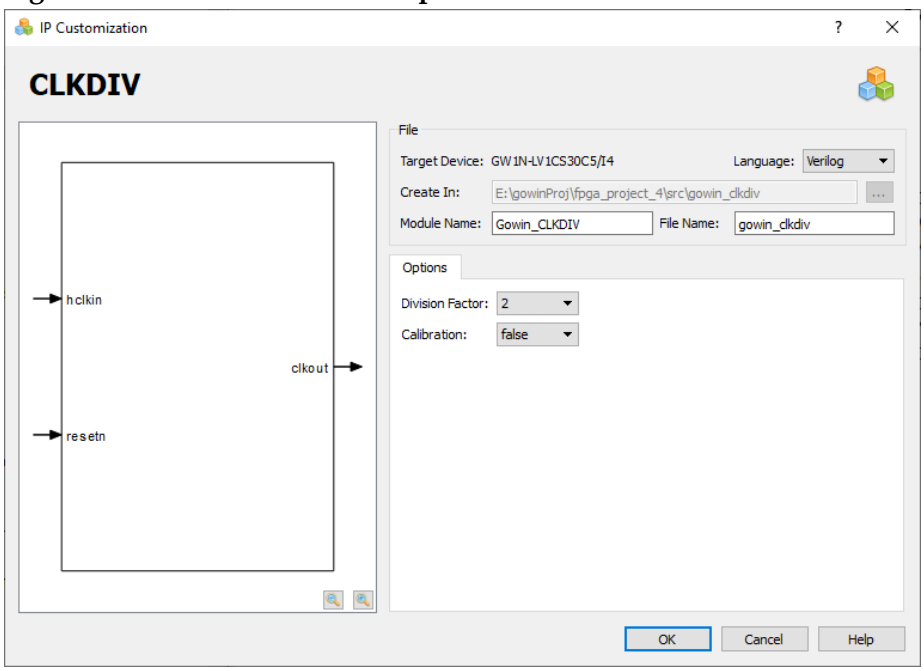


Figure 3-4 IP Customization of .ipc File



Note!

The path "Create In" can not be changed.

3.1 Block Memory

Currently, Block Memory (BSRAM) supports Single Port, Semi-dual Port, Dual-port and ROM.

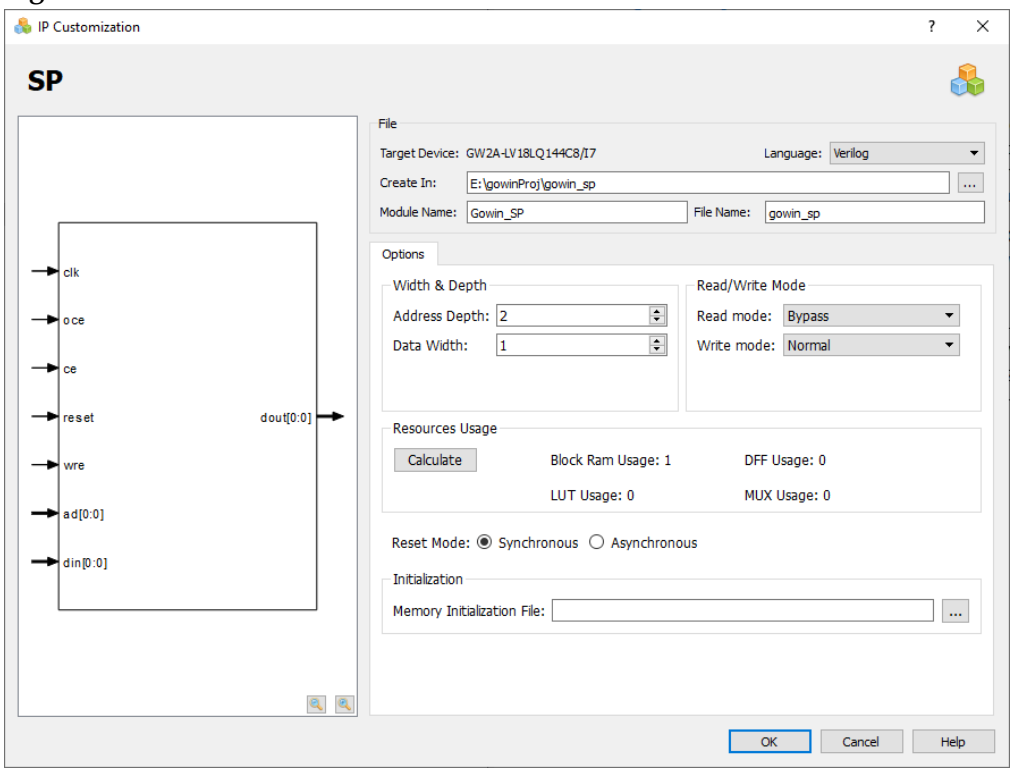
3.1.1 SP

SP is a single port block memory that can be implemented by SP and SPX9. Click "SP" on the IP Core Generator, and a brief introduction to the SP will be displayed.

IP Configuration

Double-click "SP", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-5.

Figure 3-5 IP Customization of SP



1. File

   The File displays the basic information related to the SP;

   - Target Device: Display configured device;
   - Language: Hardware description language used to generate the IP design files. Click the drop-down list to select the language, including Verilog and VHDL.
   - Module Name: The module name of the generated IP design files. Enter the module name in the text box. Module name cannot be the same as the primitive name. If it is the same, an error will be reported.

- File Name: The name of the generated IP design files. Enter the file name in the text box.
- Create In: The path in which the generated IP files will be stored. Enter the target path in the box or select the target path by clicking the option.

2. Options The Options is used to configure single-port block memory by users, as shown in Figure 3-5.
   - Width & Depth: Configure SP address depth and data width. If the configuration cannot be implemented by one module, multiple modules will be used to implement the current configuration;
   - Resource Usage: Calculate and display the resource usage of Block Ram, DFF, LUT, and MUX;
   - Read/Write Mode: Configure Read/Write mode.
   - SP supports the following modes:
     - Two Read modes: Bypass and Pipeline;
     - Three Write modes: Normal, Write-Through, Read-before-Write.
     - Reset Mode: support synchronous or asynchronous;
   - Initialization: Configure the INIT value of SP. Initialization value is written in the initialization file in Binary, Hex or Address Hex formats. The initialization file can be generated by manual writing or clicking "File > New > Memory Initialization File". For the details, please refer SUG100, Gowin Software User Guide.
3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-5.
   - "Address Depth" affects the bit-width of Address; "Data Width" affects the bit-width of input and output.
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_sp.v" file is a complete Verilog module to generate instance SP, and it is generated according to the IP configuration;
- "gowin_sp_tmp.v" is the instance template file;
- "gowin_sp.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

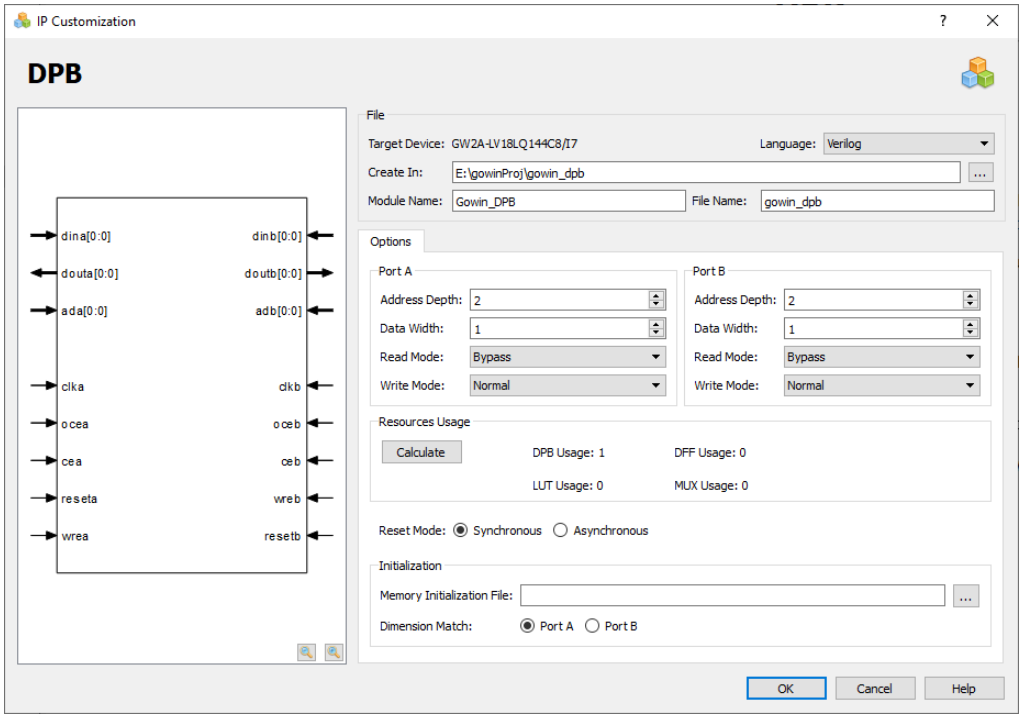
3.1.2 DP

DP is a dual port block memory that can be implemented by DPB and DPX9B. Click "DPB" on the IP Core Generator, and a brief introduction to the DPB will be displayed.

IP Configuration

Double-click "DPB" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-6.

Figure 3-6 IP Customization of DPB



1. The File displays the basic information related to the DP, as shown in Figure 3-6. The DPB file configuration box is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure dual-port block memory by users, as shown in Figure 3-6.
   - DP Options configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1SP > Options.
   - Pay attention to the follows before DPB configuration:
     - The address depth, data width, and read/write mode of DPB Port A and Port B can be configured independently.
     - The address depth and data width of DPB Port A and Port B must be same because Port A and Port B read or write the same memory.

- The data width in the Memory initialization File should be consistent with the data width of the port specified in the "Dimension Match".

Note!

- If the address depth*data width of Port A and Port B is different, an error prompt will pop up.
- If the data width is different, the Init value of generated DPB instance is 0 by default, and an Error will pop up:
  Error (MG2105): Initial.'width is unequal to user's width.

3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-6;
   - "Address Depth" of port A and port B affects the bit-width of Address; "Data Width" affects the bit-width of input and output.
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_dpb.v" file is a complete Verilog module to generate instance DPB, and it is generated according to the IP configuration;
- "gowin_dpb_tmp.v" is the instance template file;
- "gowin_dpb.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

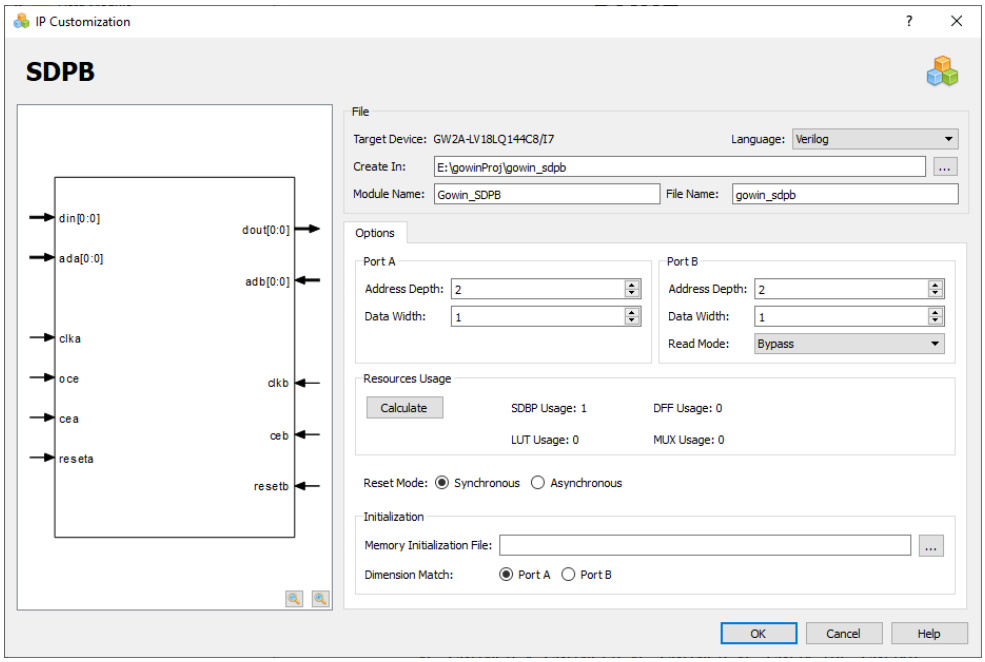
3.1.3 SDP

SDP is a semi-dual port block memory that can be implemented by SDPB and SDPX9B. Click "SDPB" on the IP Core Generator, and a brief introduction to the SDPB will be displayed.

IP Configuration

Double-click the "SDPB" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-7.

Figure 3-7 IP Customization of SDPB



1. File
   - The File displays the basic information related to the SDP;
   - The SDPB file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure semi-dual port block memory by users, as shown in Figure 3-7.
   - SDPB options configuration boxis similar to that of SP. For the detailed configuration instructions, please refer to 3.1 Block Memory > 3.1.1 SP > Options.

Note!

- SDPB only supports Port A write and Port B read; You can configure Port B Read Mode to Bypass or Pipeline in Read Mode;
- The address depth and data width of SDPB Port A and Port B can be configured independently.
- The address depth and data width of SDPB Port A and Port B must be same because Port A and Port B read or write the same memory. If not, an Error prompt will pop up.
- The date width in Memory initialization File should be consistent with the data width of the port selected by "Dimension Match". If not, the Init. value of generated SDPB instance is 0 by default, and an Error prompt will pop up:
  Error (MG2105): Initial value's width is unequal to user's width.

3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-7;
   - "Address Depth" of Port A affects the bit-width of Address, and

"Data Width" of Port A affects the bit-width of input; "Address Depth" of Port B affects the bit-width of Address, and "Data Width" of Port B affects the bit-width of output.

4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_sdpb.v" file is a complete Verilog module to generate instance SDPB, and it is generated according to the IP configuration;
- "gowin_sdpb_tmp.v" is the instance template file;
- ."gowin_sdpb.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

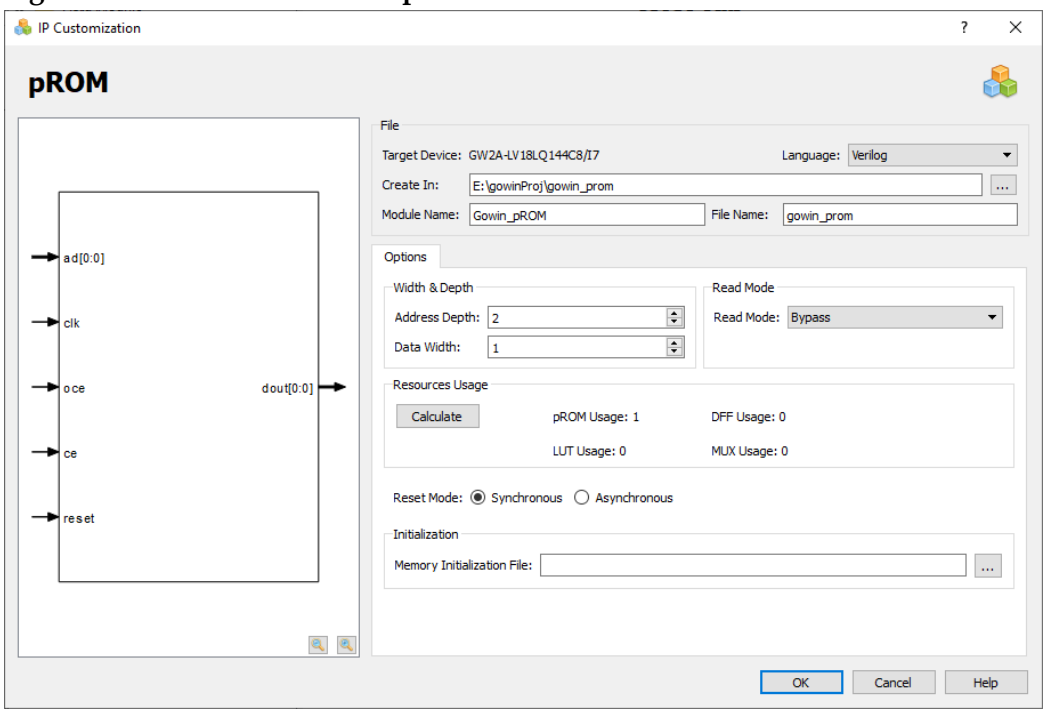
3.1.4 ROM

ROM is a read-only block memory that can be implemented by pROM and pROMX9. Click "pROM" on the IP Core Generator, and a brief introduction to the pROM will be displayed.

IP Configuration

Double-click the "pROM" to open the "IP Customization" window. This includes "File", "Options", ports diagram, and the "Help", as shown in Figure 3-8.

Figure 3-8 IP Customization of pROM



1. File
   - The File displays the basic information related to the ROM;
   - The pROM file configuration is similar to that of SP. For the detais, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure read-only memory by users, as shown in Figure 3-8.
   - pROM Options configuration is similar to that of SP. For the detailed configuration instructions, please refer to 3.1 Block Memory > 3.1.1 SP > Options.

Note!

- pROM only supports read; Read mode can be Bypass or Pipeline;
- The date width in Memory initialization File should be consistent with the data width configured. If not, the Init value of generated pROM instance is 0 by default, and an Error will pop up:
  Error (MG2105): Initial values' width is unequal to user's width option.

3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-8;
   - "Address Depth" affects the bit-width of Address; "Data Width" affects the bit-width of the output.
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_prom.v" file is a complete Verilog module to generate instance ROM, and it is generated according to the IP configuration;
- "gowin_prom_tmp.v" is the instance template file;
- ."gowin_prom.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with an .vhd suffix.

3.2 Shadow Memory

Shadow Memory (SSRAM) module can implement RAM16S (single-port mode), RAM16SDP (semi-dual-port mode), and ROM16 (read-only mode).

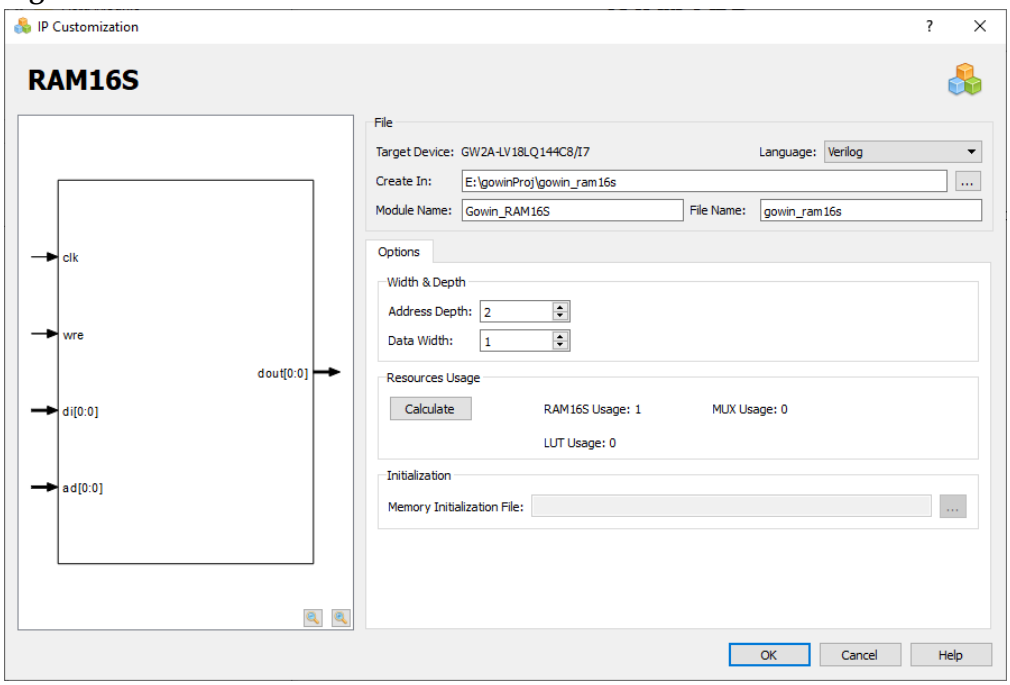
3.2.1 RAM16S

RAM16S is a single port shadow memory that can be implemented by RAM16S1, RAM16S2, RAM16S4. Click "RAM16S" on the IP Core Generator, and a brief introduction to RAM16S will be displayed.

IP Configuration

Double-click "RAM16S" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-9.

Figure 3-9 IP Customization of RAM16S



1. File
   - The File displays the basic information related to the RAM16S;
   - The RAM16S file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure RAM16S by users, as shown in Figure 3-9.
   - RAM16S Options configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1SP > Options.
3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-9;
   - "Address Depth" affects the bit-width of Address; "Data Width" affects the bit-width of the input and output.

4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_ram16s.v" file is a complete Verilog module to generate instance ROM16S, and it is generated according to the IP configuration;
- "gowin_ram16s_tmp.v" is the instance template file;
- "gowin_ram16s.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

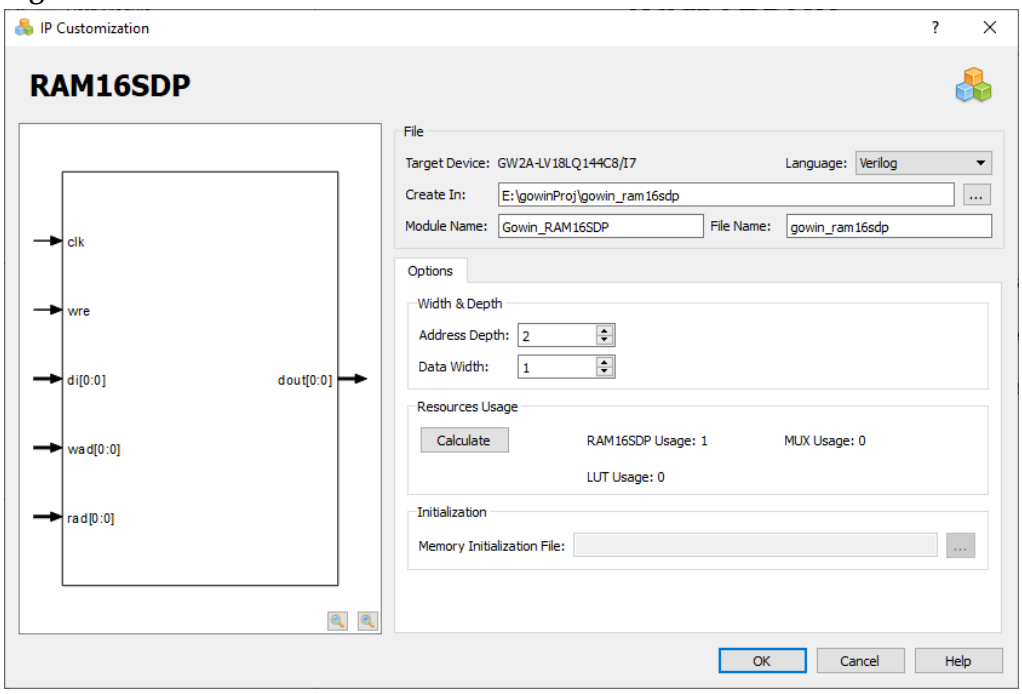
3.2.2 RAM16SDP

RAM16SDP is a semi-dual port shadow memory that can be implemented by RAM16SDP1, RAM16SDP2 and RAM16SDP4. Click "RAM16SDP" on the IP Core Generator, and a brief introduction to "RAM16SDP" will be displayed.

IP Configuration

Double-click the "RAM16SDP" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-10.

Figure 3-10 IP Customization of RAM16SDP



1. File
   - The File displays the basic information related to the RAM16SDP;
   - The RAM16SDP file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure RAM16SDP by users, as shown in Figure 3-10.
   - RAM16SDP options configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > Options.
3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-10;
   - "Address Depth affects the bit-width of Address; "Data Width" affects the bit-width of input and output.
4. Help
   Click "Help" to open the IP Core configuration information . The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_ram16sdp.v" file is a complete Verilog module to generate instance ROM16SDP, and it is generated according to the IP configuration;
- "gowin_ram16sdp_tmp.v" is the instance template file;
- "gowin_ram16sdp.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

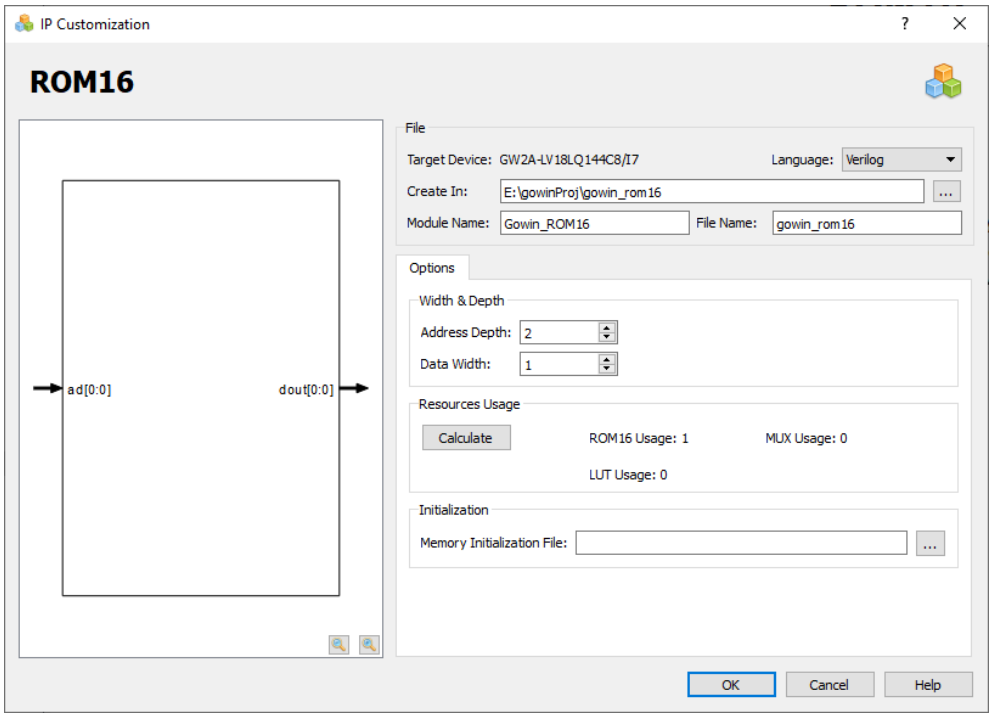
3.2.3 ROM16

ROM16 is a read only memory. Click "ROM16" on the IP Core Generator, and a brief introduction to "RAM16" will be displayed.

IP Configuration

Double-click the "ROM16" to open the "IP Customization" window. This includes "File", "Options", ports diagram, and the "Help".

Figure 3-11 IP Customization of ROM16



1. File
   - The File displays the basic information related to the RAM16;
   - The ROM16 file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure RAM16 by users, as shown in Figure 3-11.
   - ROM16 Options configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP> Options.
3. Ports Diagram
   - The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-11;
   - "Address Depth" affects the bit-width of Address; "Data Width" affects the bit-width of the output.
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_rom16.v" file is a complete Verilog module to generate instance ROM16, and it is generated according to the IP configuration;
- "gowin_ram16_tmp.v" is the instance template file;

- "gowin_rom16.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

3.3 DSP

DSP module supports five types of Gowin Primitive: ALU54, MULT, MULTADDALU, MULTALU and PADD.

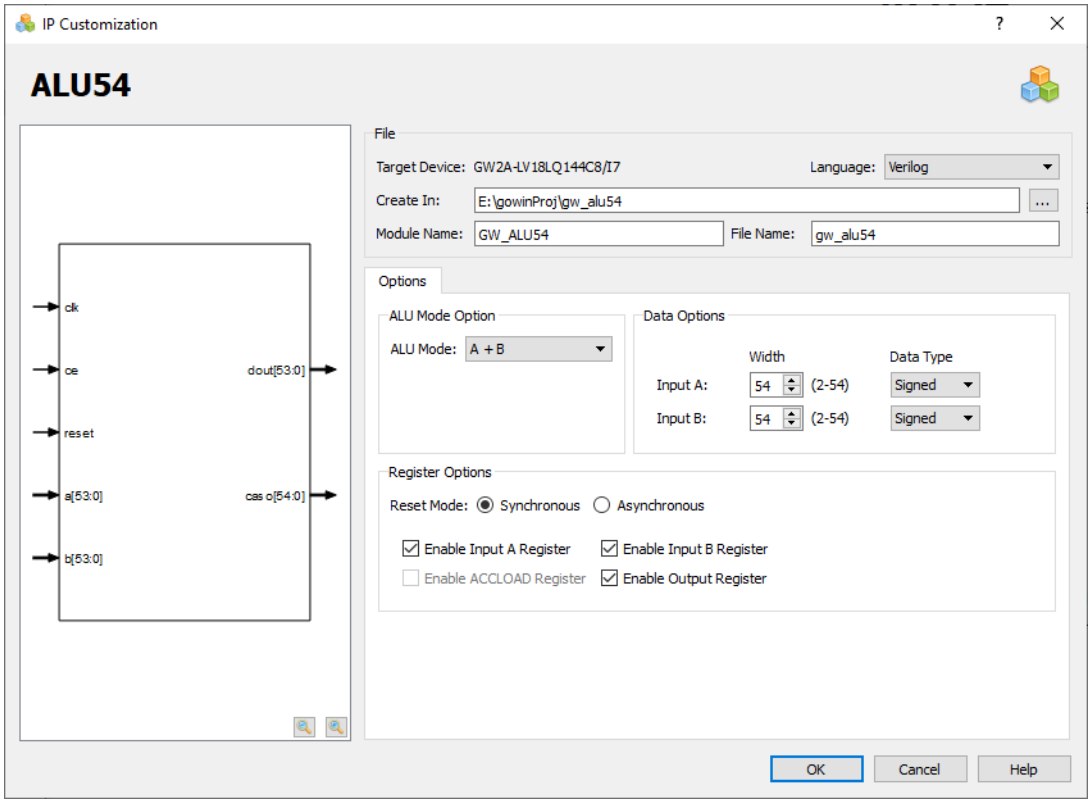
3.3.1 ALU54

ALU54 can be used to implement 54-bit arithmetic and logical operations. Click "ALU54" on the IP Core Generator, and a brief introduction to "ALU54" will be displayed.

IP Configuration

On the IP Core Generator interface, double-click "ALU54" to open the "IP Customization" window, as shown in Figure 3-12. This includes "File", "Options", ports diagram, and the "Help".

Figure 3-12 IP Customization of ALU54



1. File
   - The File displays the basic information related to the ALU54;
   - The ALU54 file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.

2. Options

The Options is used to configure ALU54 by users, as shown in Figure 3-12.

- ALU Mode Option: Allows users to select the operation modes. The MULTADDALU can be configured in the following operation modes:
  - A + B；
  - A – B；
  - Accum + A + B；
  - Accum + A – B；
  - Accum - A + B；
  - Accum - A – B；
  - B + CASI；
  - Accum + B + CASI；
  - Accum - B + CASI；
  - A + B + CASI；
  - A - B + CASI；
- Data Options: Allows users to configure data.
  - Configure ALU54 input data width. The data width of input port A/B can be configured as 1-54 bit;
  - Output width adjusts automatically according to the input width;
  - Data Type: Can be configured as signed or unsigned.
- Register Options: Allows users to configure registers operation mode.
  - Reset Mode: Synchronous or asynchronous;
  - Enable Input A Register: Allows users to enable or disable Input A register;
  - Enable Input B Register: Allows users to enable or disable Input B register;
  - Enable ACCLOAD Register: Allows users to enable or disable ACCLOAD register;
  - Enable Output Register: Allows users to enable or disable Output register.

3. The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-12;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_alu54.v" file is a complete Verilog module to generate instance ROM16, and it is generated according to the IP configuration;
- "gw_alu54_tmp.v" is the instance template file;
- "gw_alu54.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

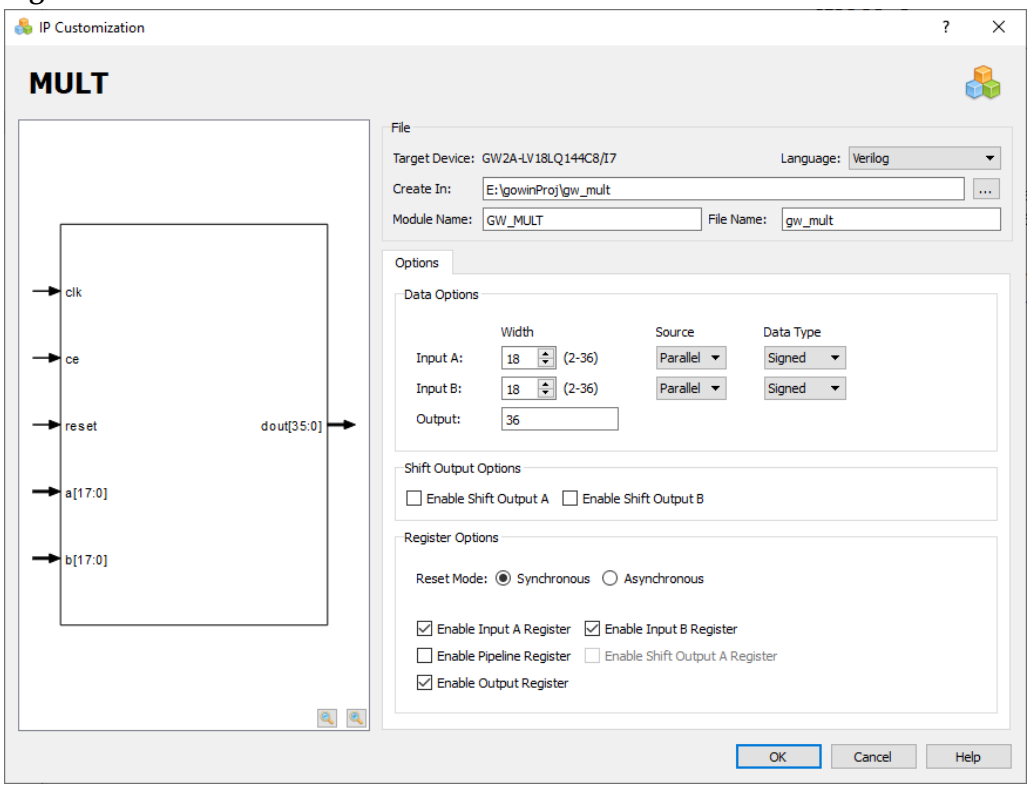
3.3.2 MULT

MULT can be configured as a multiplier. Click "MULT" on the IP Core Generator, and a brief introduction to the MULT will be displayed.

IP Configuration

Double-click "MULT" to open the "IP Customization" window, as shown in Figure 3-13. This includes "File", "Options", ports diagram, and "Help".

Figure 3-13 IP Customization of MULT



1. File
   - The File displays the basic information related to the MULT;
   - The MULT file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.

2. Options
   - The Options is used to configure MULT by users, as shown in Figure 3-13.
   - Data Options: Allows users to configure data options.
     - The maximum data width of the input ports (Input A Width/ Input B Width) is 36;
     - Output width adjusts automatically according to input width and generates MULT9X9, MULT18X18, or MULT36X36 according to the width during the instance.
     - Input A/B can be set as Parallel, Shift.
     - The data type can be configured as Unsigned or Signed.
   - Shift Output Options: Allows users to select whether to enable shift out. This option can be checked when both Input A width and Input B width are less than or equal to 18.

   Note!

   If either Input A width or Input B width is greater than 18, the Shift Output Options will be grayed.

   - Register Options: It is similar to that of ALU54. Please refer to the Options in 3.3.1 ALU54 for details.
3. The ports diagram is based on the current IP Core configuration. The input/output number of and bit-width update in real time based on the "Options" configuration, as shown in Figure 3-13;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_mult.v" file is a complete Verilog module to generate instance MULT, and it is generated according to the IP configuration;
- "gw_mult_tmp.v" is the instance template file;
- "gw_mult.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

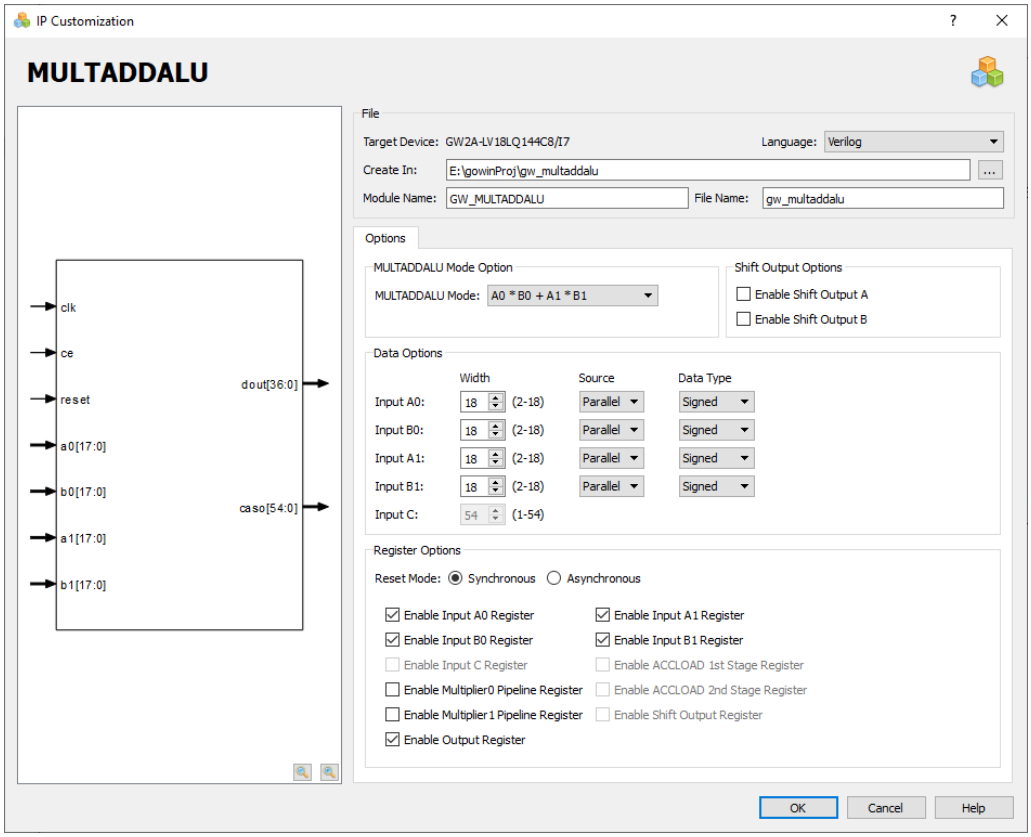
3.3.3 MULTADDALU

MULTADDALU can implement the sum of two 18x18 multipliers. Click "MULT" on the IP Core Generator, and a brief introduction to the MULTADDALU will be displayed.

IP Configuration

Double-click the "MULTADDALU" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-14.

Figure 3-14 IP Customization of MULTADDALU



1. File
   - The File displays the basic information related to the MULTADDALU;
   - The MULTADDALU file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   The Options is used to configure MULTADDALU by users, as shown in Figure 3-14.
   - MULTADDALU Mode Option: Allows users to select the operation modes. The MULTADDALU can be configured in the following operation modes:
     - A0*B0 + A1*B1
     - A0*B0 - A1*B1
     - A0*B0 + A1*B1 + C
     - A0*B0 + A1*B1 - C
     - A0*B0 - A1*B1 + C

- A0*B0 - A1*B1 - C
- Accum + A0*B0 + A1*B1
- Accum + A0*B0 - A1*B1
- A0*B0 + A1*B1 + CASI
- A0*B0 - A1*B1 + CASI；

- The Data Options and Register Options is similar to those of MULT. For the details, please refer to 3.3.2 MULT.

3. The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Data Options" and "Register Options" configuration, as shown in Figure 3-14;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_multaddalu.v" file is a complete Verilog module to generate instance MULTADDALU, and it is generated according to the IP configuration;
- "gw_multaddalu_tmp.v" is the instance template file;
- "gw_multaddalu.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

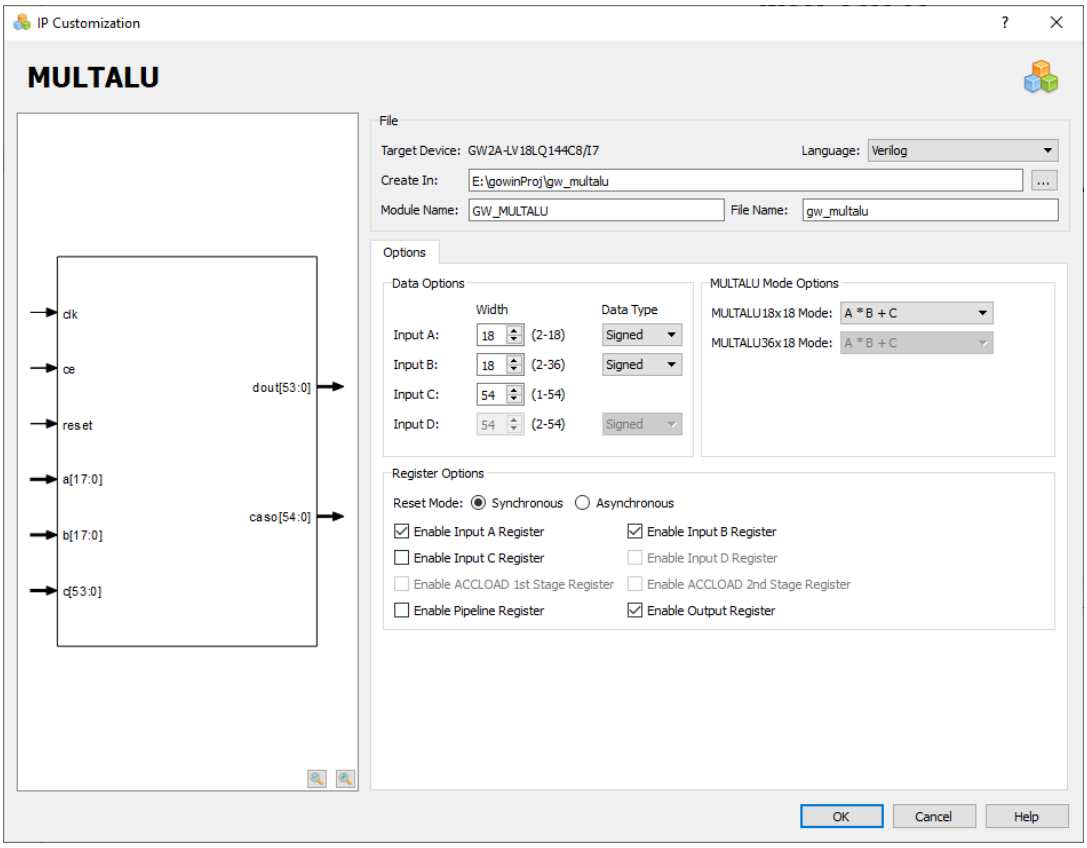
3.3.4 MULTALU

MULTALU can implement the Multiplier ALU mode. Click "MULTALU" on the IP Core Generator, and a brief introduction to the MULTALU will be displayed.

IP Configuration

Double-click "MULTALU" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-15.

Figure 3-15 IP Customization of MULTALU



1. File
   - The File displays the basic information related to the MULTALU;
   - The MULTALU file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   The Options is used to configure MULTALU by users, as shown in Figure 3-15.
   - MULTALU can generate two modules according to the input port width: MULTALU36X18 or MULTALU18X18. When the Input A width and Input B width are less than or equal to 18, the MULTALU36X18 mode will be grayed-out, and MULTALU18X18 mode can be configured as follows:
     - A*B + C
     - A*B - C
     - Accum + A*B + C
     - Accum + A*B - C
     - Accum - A*B + C
     - Accum - A*B - C
     - A*B + CASI
     - Accum + A*B + CASI

  - Accum - A*B + CASI
  - A*B + D + CASI
  - A*B - D + CASI
- When Input B width is greater than 18, the MULTALU18X18 mode will be grayed out, and the MULTALU36X18 mode can be configured as follows:
  - A*B + C
  - A*B - C
  - Accum + A*B
  - A*B + CASI
- The MULTALU Data Options and Register Options are similar to those of MULT. For the details, please refer to 3.3.2MULT.

3. The ports diagram is based on the current IP Core configuration. The input/output bit-width updates in real time based on the "Options" configuration, as shown in Figure 3-15;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_multtalu.v" file is a complete Verilog module to generate instance MULTALU, and it is generated according to the IP configuration;
- "gw_multtalu_tmp.v" is the instance template file;
- "gw_multtalu.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

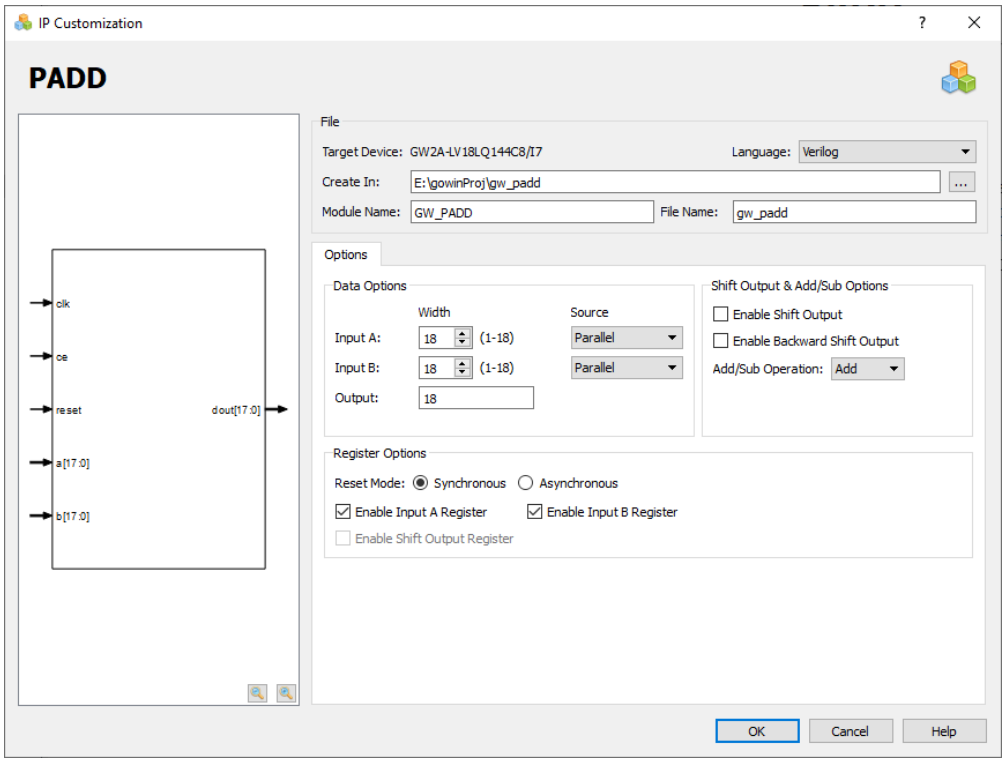
3.3.5 PADD

PADD can be configured as a pre-adder, pre-subtracter, or shifter. Click "PADD" on the IP Core Generator, and a brief introduction to the PADD will be displayed.

IP Configuration

Double-click the "PADD" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-16.

Figure 3-16 IP Customization of PADD



1. File
   - The File displays the basic information related to the PADD;
   - The PADD file configuration is similar to that of SP. For the details, please refer to 3.1Block Memory > 3.1.1SP> File.
2. Options
   The Options is used to configure PADD by users, as shown in Figure 3-16.
   - Data Options: Allows users to configure data options.
     - The maximum data width of the input ports (Input A Width/ Input B Width) is 18;
     - The output width automatically adjusts according to the input width, and the width determines whether PADD9 or PADD18 are generated during instance.
     - Input A Source: Users can select Parallel A or Shift;
     - Input B Source: Users can select Parallel or Backward Shift.
   - Shift Output and Add/Sub Options: Allows users to enable or disable Shift Output, Backward Shift Output, and add/sub operation.
     - Check "Enable Shift Output" to enable shift output;
     - Check "Enable Backward Shift Output" to enable backward shift output;
     - Configure "Add/Sub Operation" to perform add/sub operation.

- Register Options: Allows users to configure registers operation mode.
  - Reset Mode: Sets whether the reset mode is synchronous or asynchronous;
  - Enable Input A Register: Allows users to enable or disable Input A register;
  - Enable Input B Register: Allows users to enable or disable Input B register;
  - Enable Output Register: Allows users to enable or disable Output register.

3. The ports diagram is based on the current IP Core configuration. The input/output number of and bit-width update in real time based on the "Options" configuration, as shown in Figure 3-16;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_padd.v" file is a complete Verilog module to generate instance PADD, and it is generated according to the IP configuration;
- "gw_padd_tmp.v" is the instance template file;
- "gw_padd.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

3.4 CLOCK

The CLOCK module currently supports nine types of Gowin Primitive: rPLL, PLLVR, OSC, CLKDIV, CLKDIV2, DCS, DHCEN, DLLDLY and DQCE.

3.4.1 PLL

Based on the "clkin" input, PLL adjusts the clock phase, duty cycle, and frequency (multiplication and division) to output different phases and frequencies. Click "rPLL" on the IP Core Generator, IP a brief introduction to the IP will be displayed.

The formulas of rPLL output calculation are as follows:

1. $f_{CLKOUT} = (f_{CLKIN}*FDIV)/IDIV$
2. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
3. $f_{VCO} = f_{CLKOUT}*ODIV$

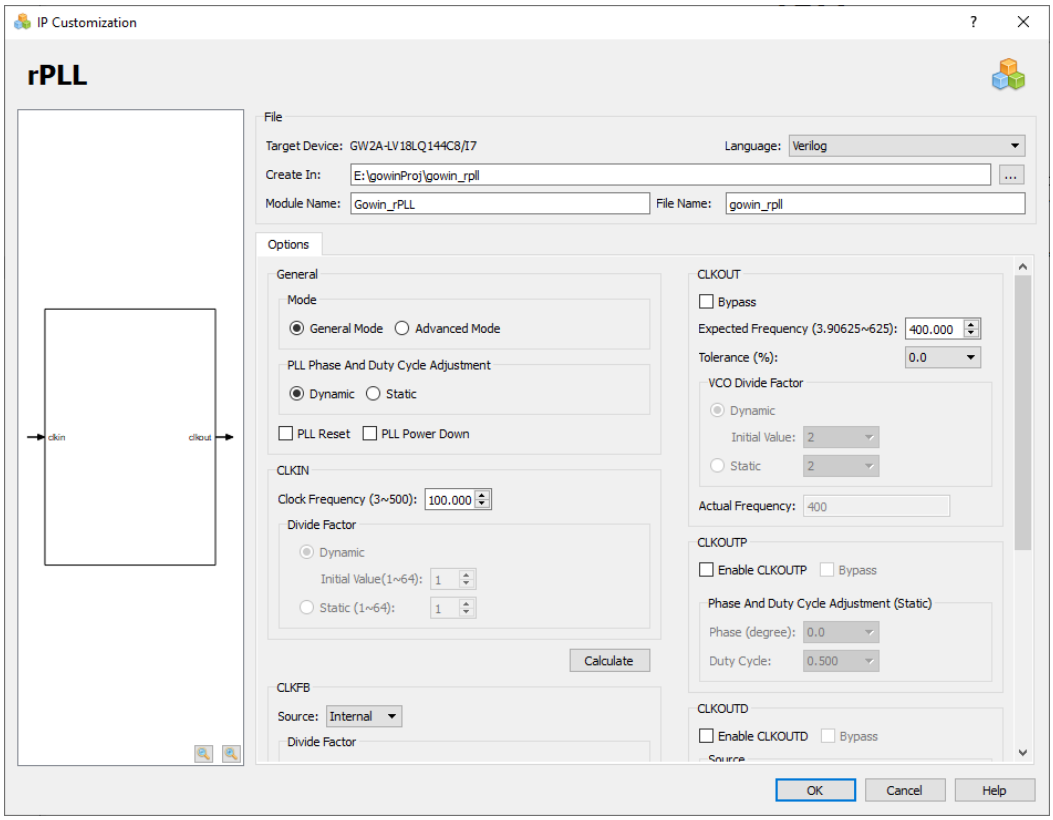
Note!

- f_{CLKIN}: The frequency of input clock CLKIN;
- f_{CLKOUT}: The frequency of output clock CLKOUT;
- $f_{CLKOUTD}$: The frequency of output clock CLKOUTD, and CLKOUTD is the clock "CLKOUT" after division.
- f_{VCO}: VCO oscillation frequency.

IP Configuration

Double-click the "rPLL" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-17.

Figure 3-17 IP Customization of rPLL



1. File
   - The File displays the basic information related to the PLL;
   - The rPLL file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   The Options is used to configure PLL by users, as shown in Figure 3-17.
   - General: Users can select "General Mode" or "Advanced Mode", select "Static Mode" or "Dynamic Mode" for PLL phase and duty cycle, and enable or disable PLL Reset.
     - Mode: "General Mode" or "Advanced Mode".

  - PLL Phase And Duty Cycle Adjustment: "Static" Mode or "Dynamic" Mode.
  - "PLL Reset": Disable or enable PLL Reset.
  - "PLL Power Down": Configure the rPLL in power-saving mode.

- CLKIN: Allows users to set input clock frequency, divide factor, and IDESEL Reset.
  - Clock Frequency: Specify the frequency. The frequency range is determined by the device selected.
  - Divide Factor: Allows users to set the Divide Factor as "Dynamic" or "Static" in Advanced mode. In Static mode, Divide Factor value can be set as a specific value, which ranges from 1 to 64. If the CLKOUT frequency is not in the range required by the device, an error prompt will pop up when the user clicks "Calculate" or "OK" ; If the frequency of CLKIN/IDIV is not in the range required by the device, an error prompt will pop up when the user clicks "Calculate" or "OK".
- CLKFB: Allows users to configure the source and divide factor of rPLL.
  - Source: Internal or External;
  - Divide Factor: Allows users to set the Divide Factor as "Dynamic" or "Static" in advanced mode. In static mode, Divide Factor value can be set as a specific value, which ranges from 1 to 64. If the configuration is invalid, an error prompt will pop up when the user clicks"Calculate" or "OK".
- Enable LOCK: Allows users to enable LOCK.
- CLKOUT: Allows users to configure the expected frequency, VCO, tolerance and actual frequency.
  - Bypass: Allows users to enable/disable clkout bypass;
  - Expected Frequency: Set the output clock expected frequency in general mode. The frequency range is determined by the device selected.
  - Tolerance(%): Set a tolerance for the CLKOUT expected frequency and actual frequency calculated.
  - VCO Divide Factor: Allows users to set Divide Factor as "Dynamic" or "Static" in advanced mode. In static mode, the Divide Factor value can be set as a specific value, and the range is 2/4/8/16/32/48/64/80/96/112/128. If the configuration is invalid, an error prompt will be displayed when the user clicks "Calculate" or "OK".
  - Actual Frequency: The actual frequency that can be generated automatically.
- CLKOUTP: Allows users to set Phase And Duty Cycle Adjustment

and enable/disable CLKOUTP.

- Enable CLKOUTP: Enable/disable CLKOUTP;
- Bypass: Allows users to enable/disable CLKOUTP bypass;
- Phase And Duty Cycle Adjustment (Static): Configure (Phase [degree]) and (Duty Cycle [*1/16]) in static mode;

- CLKOUTD: Allows users to specify the source, expected frequency, and divide factor of the clock divider, and enable/disable CLKOUTD Reset.
  - Enable CLKOUTD: Used to enable/disable CLKOUTD;
  - Bypass: Allows users to enable/disable CLKOUTD bypass;
  - Source: Select the source of CLKOUTD as "CLKOUT" or "CLKOUTP";
  - Expected Frequency: Set the output clock frequency in General mode. The frequency range is determined by the device selected.
  - Tolerance(%): Set a tolerance for the CLKOUTD expected frequency and actual frequency calculated.
  - Divide Factor (2~128): Select the divide factor from the drop-down list in advanced mode. Only even between 2 and 128 can be selected. If an odd is set, an error prompt will be displayed when the user clicks "OK".
  - Actual Frequency: The actual frequency that can be generated automatically.
- CLKOUTD3: Allows users to set the source of CLKOUTD3.
  - Enable CLKOUTD3: Enable/disable CLKOUTD3;
  - Source: Select the source of CLKOUTD3 as "CLKOUT" or "CLKOUTP";
- Calculate: Calculate whether the current configuration is valid.
  - Calculate Divide Factor settings based on the input/output frequency in general mode. If the actual frequency is different to the expected frequency, an Error prompt will pop up and the invalid value will be marked in red.
  - Calculate Divide Factor settings based on the input/output frequency in advanced mode If the calculated results are invalid, an Error prompt will pop up and the invalid value will be marked in red.

3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-17;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_rpll.v" file is a complete Verilog module to generate instance rPLL, and it is generated according to the IP configuration;
- "gowin_rpll_tmp.v" is the instance template file;
- "gowin_rpll.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

3.4.2 PLLVR

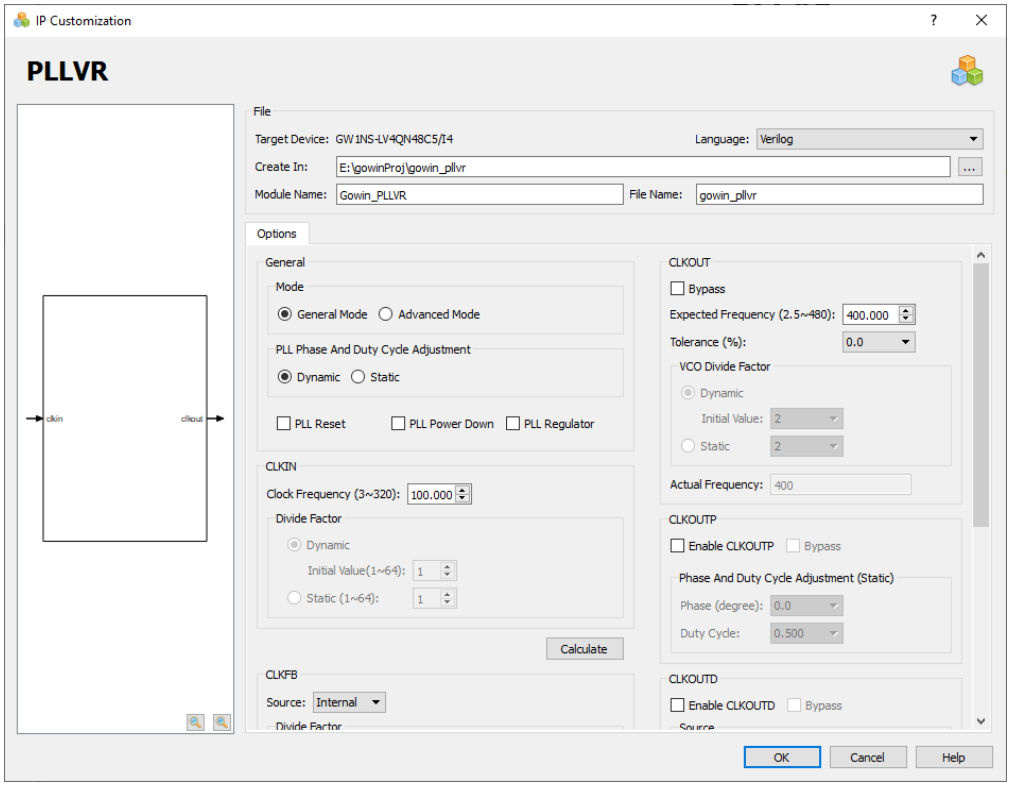
PLLVR is only available for GW1NS-4, GW1NS-4C, GW1NSR-4, GW1NSR-4C and GW1NSER-4C. Click "PLLVR" on the IP Core Generator, and a brief introduction to the PLLVR will be displayed.

PLLVR output data calculation formula is the same as the one of PLL, please refer to 3.4 CLOCK > 3.4.1 PLL.

IP Configuration

Double-click the "PLLVR" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-18.

Figure 3-18 IP Customization of PLLVR



1. File
   - The File displays the basic information related to the PLLVR;
   - The PLLVR file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure PLLVR by users, as shown in Figure 3-18.
   - PLLVR Options configuration is similar to that of rPLL. For the details, please refer to 3.4 CLOCK > 3.4.1 PLL > Options. PLL Regulater option is added.
3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-18;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_pllvr.v" file is a complete Verilog module to generate instance PLLVR, and it is generated according to the IP configuration;
- "gowin_pllvr_tmp.v" is the instance template file;
- "gowin_pllvr.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

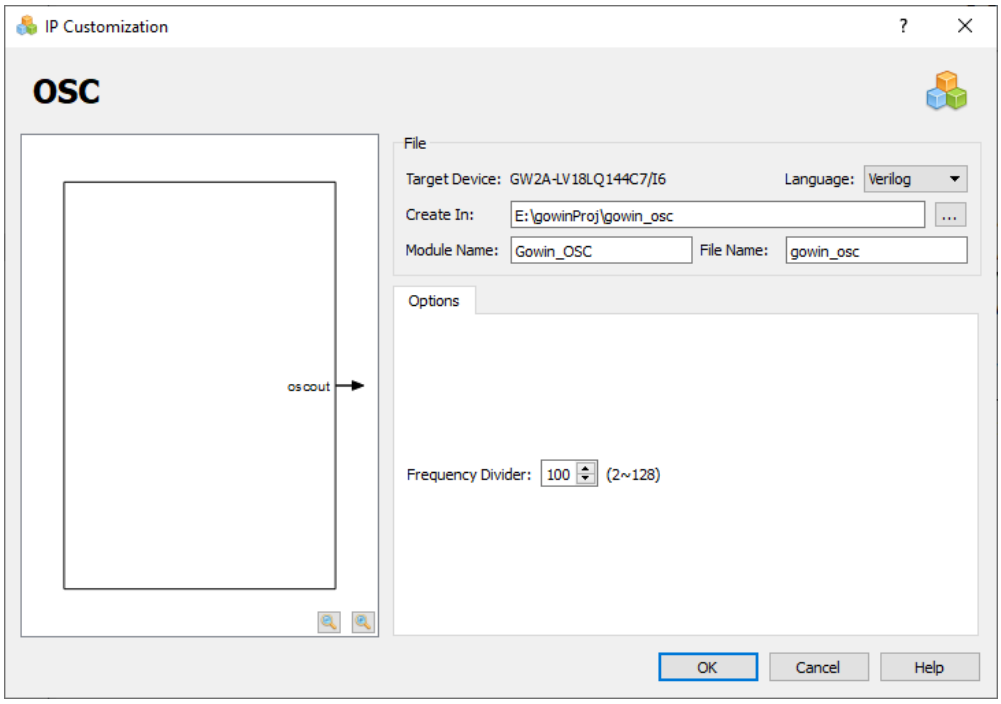
3.4.3 OSC

Click OSC on the IP Core Generator, and a brief introduction to the OSC will be displayed.

IP Configuration

Double-click "OSC", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-19.

Figure 3-19 IP Customization of OSC



1. File
   - The File displays the basic information related to the PLLVR;
   - The OSC file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.

Note!

Different devices can generate different OSC, you can see SUG283, Gowin Primitives User Guide.

2. Options
   - The Options is used to configure OSC by users, as shown in Figure 3-19.
   - Frequency Divider: Allows users to select any even number between 2 and 128.
3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-19;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_osc.v" file is a complete Verilog module to generate instance OSC, and it is generated according to the IP configuration;
- "gowin_osc_tmp.v" is the instance template file;

- "gowin_osc.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

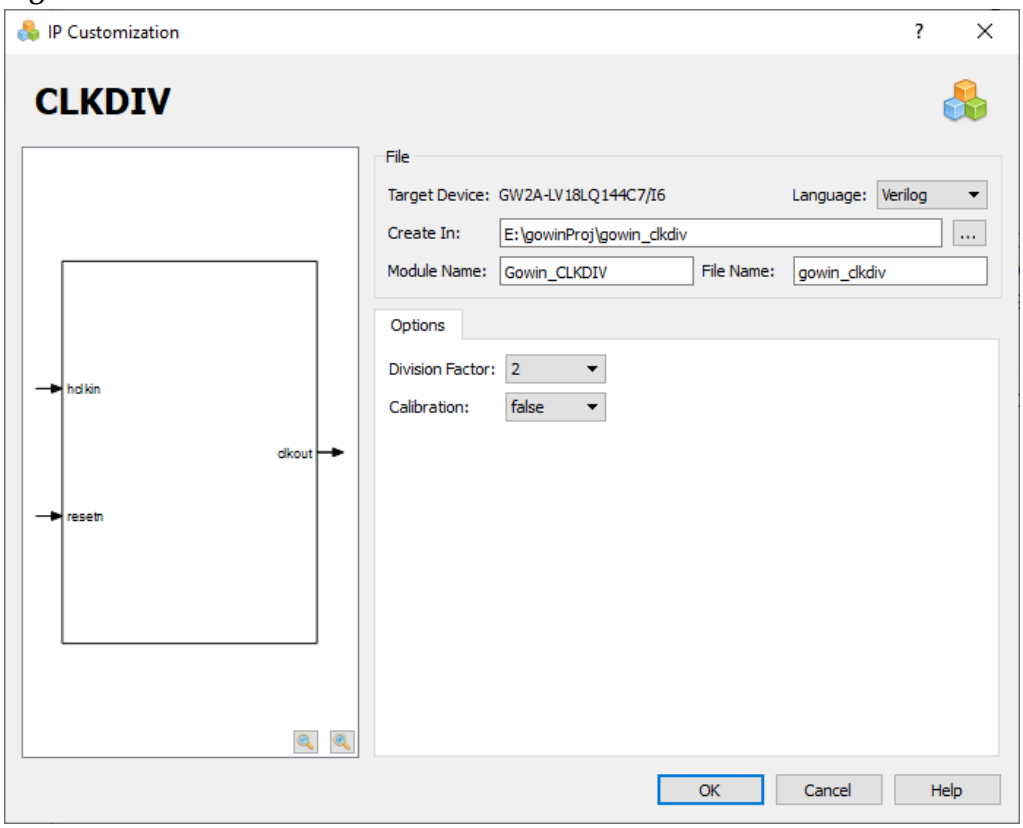
3.4.4 CLKDIV

Click CLKDIV on the IP Core Generator, and a brief introduction to the CLKDIV will be displayed.

IP Configuration

Double-click "CLKDIV", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-20.

Figure 3-20 IP Customization of CLKDIV



1. File
   - The File displays the basic information related to the CLKDIV;
   - The CLKDIV file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure CLKDIV by users, as shown in Figure 3-20.
   - Division Factor: Division factor

- Calibration: Enable/disable calibration

3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-20;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_clkdiv.v" file is a complete Verilog module to generate instance CLKDIV, and it is generated according to the IP configuration;
- "gowin_clkdiv_tmp.v" is the instance template file;
- "gowin_clkdiv.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

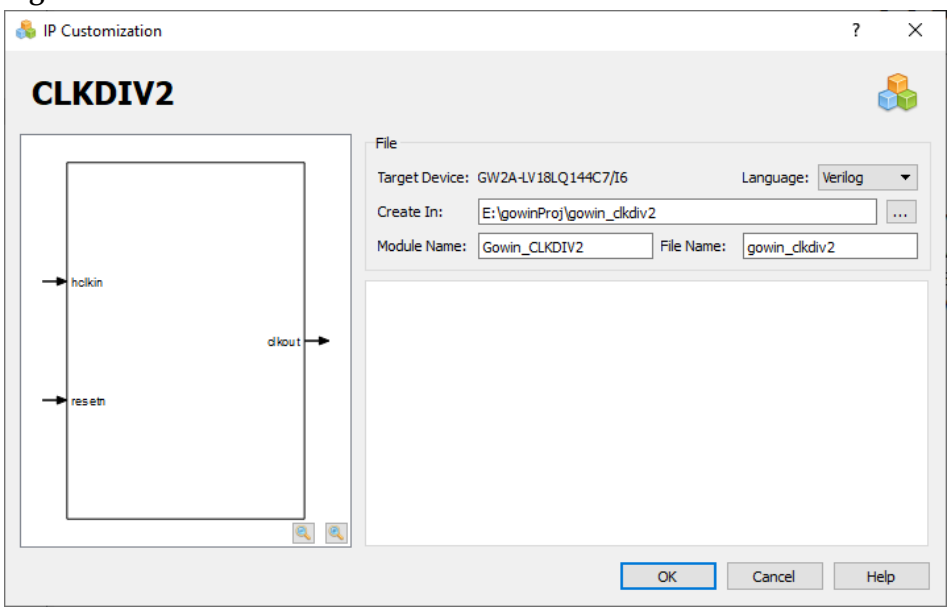
3.4.5 CLKDIV2

Click CLKDIV2 on the IP Core Generator, and a brief introduction to the CLKDIV2 will be displayed.

IP Configuration

Double-click "CLKDIV2", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-21.

Figure 3-21 IP Customization of CLKDIV2



1. File

- The File displays the basic information related to the CLKDIV2;
- The CLKDIV2 file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.

2. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-21;
3. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_clkdiv2.v" file is a complete Verilog module to generate instance ROM16, and it is generated according to the IP configuration;
- "gowin_clkdiv2_tmp.v" is the instance template file;
- "gowin_clkdiv2.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

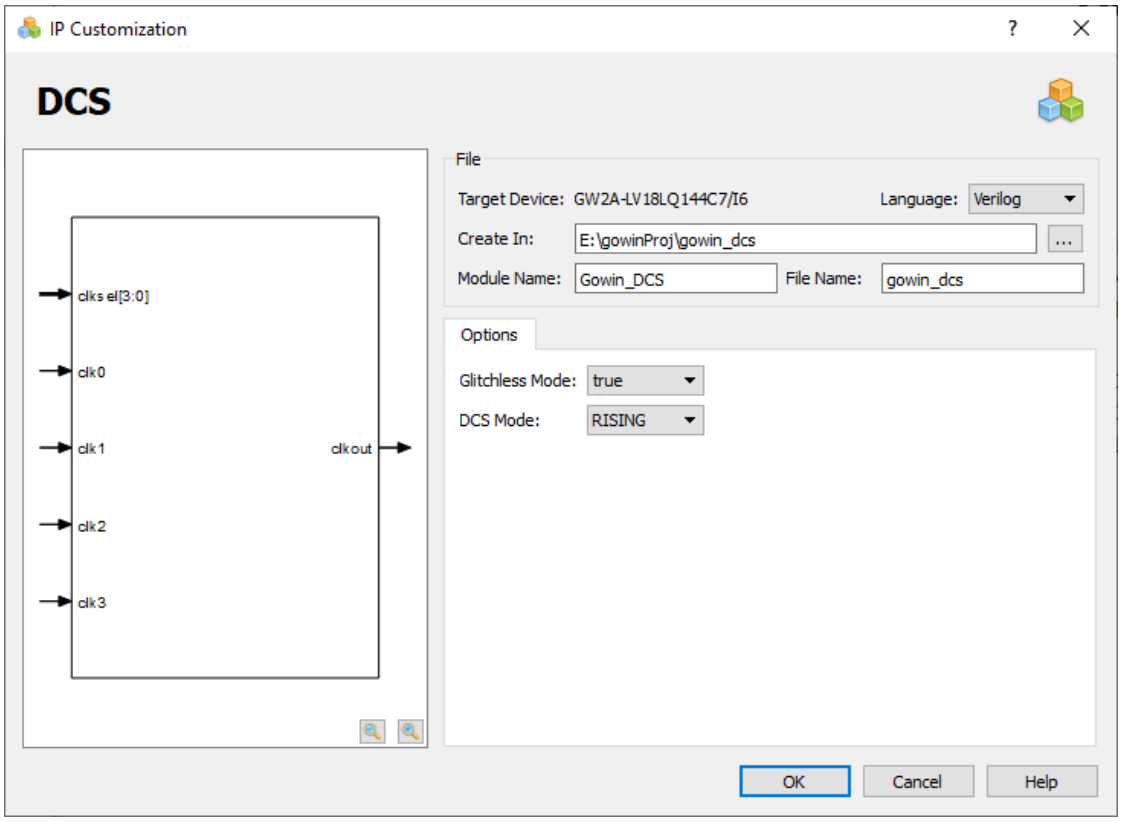
3.4.6 DCS

Click DCS on the IP Core Generator, and a brief introduction to the DCS will be displayed.

IP Configuration

Double-click "DCS", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-22.

Figure 3-22 IP Customization of DCS



1. File
   - The File displays the basic information related to the DCS;
   - The DCS file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure DCS by users, as shown in Figure 3-22.
   - Glitchless Mode: Enable/disable Glitchless
   - DCS Mode: Set DCS mode;
3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-22;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_dcs.v" file is a complete Verilog module to generate instance DCS, and it is generated according to the IP configuration;
- "gowin_dcs_tmp.v" is the instance template file;

- "gowin_dcs.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

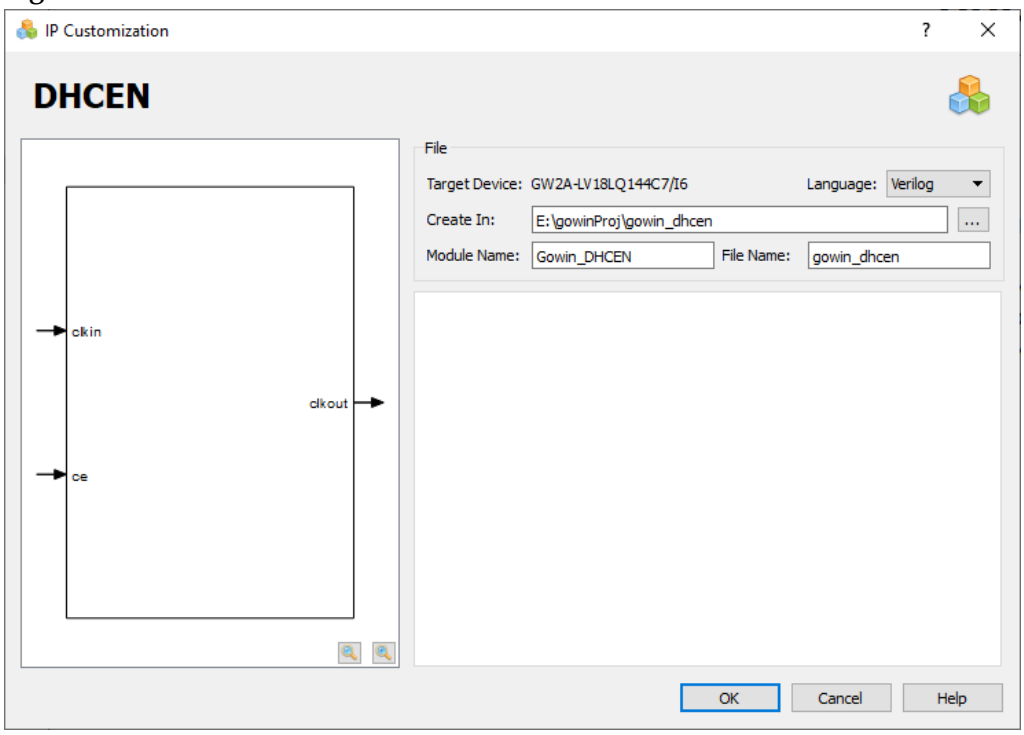
3.4.7 DHCEN

Click DHCENon the IP Core Generator, and a brief introduction to the DHCEN will be displayed.

IP Configuration

Double-click "DHCEN", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-23.

Figure 3-23 IP Customization of DHCEN



1. File
   - The File displays the basic information related to the DHCEN;
   - The DHCEN file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-23;
3. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_dhcen.v" file is a complete Verilog module to generate instance DHCEN, and it is generated according to the IP configuration;
- "gowin_dhcen_tmp.v" is the instance template file;
- "gowin_dhcen.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

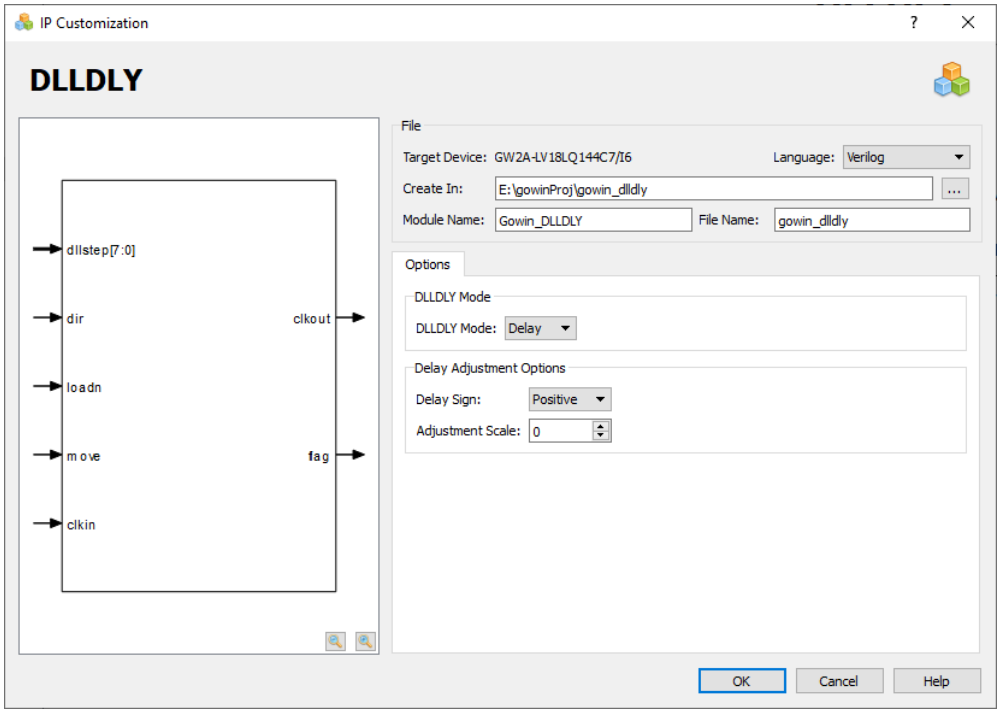
3.4.8 DLLDLY

Click DLLDLY on the IP Core Generator, and a brief introduction to the DLLDLY will be displayed.

IP Configuration

Double-click "DLLDLY", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-24.

Figure 3-24 IP Customization of DLLDLY



1. File
   - The File displays the basic information related to the DLLDLY;
   - The DLLDLY file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options

- The Options is used to configure DLLDLY by users, as shown in Figure 3-24.
- DLLDLY Mode: Set DLLDLY mode;
- Delay Sign: Set the sign of delay;
- Adjustment Scale: Delay adjustment.

3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-24;
4. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_dlldly.v" file is a complete Verilog module to generate instance DLLDLY, and it is generated according to the IP configuration;
- "gowin_dlldly_tmp.v" is the instance template file;
- "gowin_dlldly.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

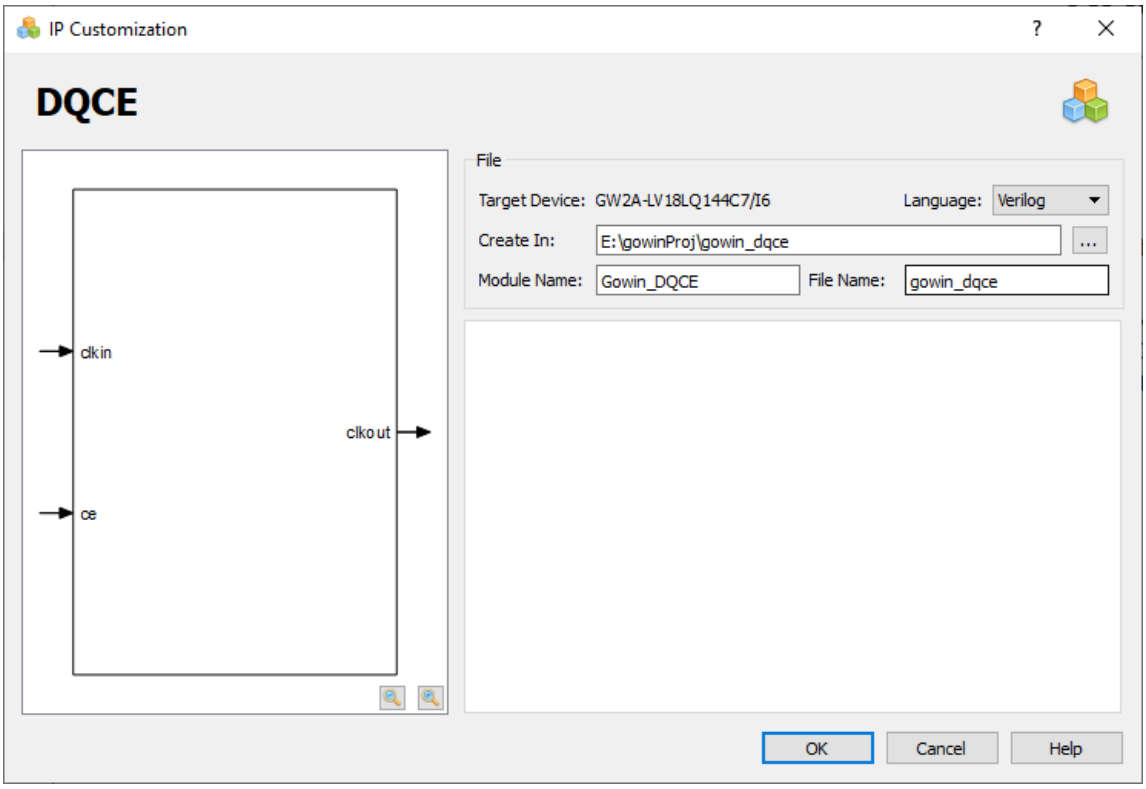
3.4.9 DQCE

Click DQCE on the IP Core Generator, and a brief introduction to the DQCE will be displayed.

IP Configuration

Double-click "DQCE", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-25.

Figure 3-25 IP Customization of DQCE



1. File
   - The File displays the basic information related to the DQCE;
   - The DQCE file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-25;
3. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_dqce.v" file is a complete Verilog module to generate instance DQCE, and it is generated according to the IP configuration;
- "gowin_dqce_tmp.v" is the instance template file;
- "gowin_dqce.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

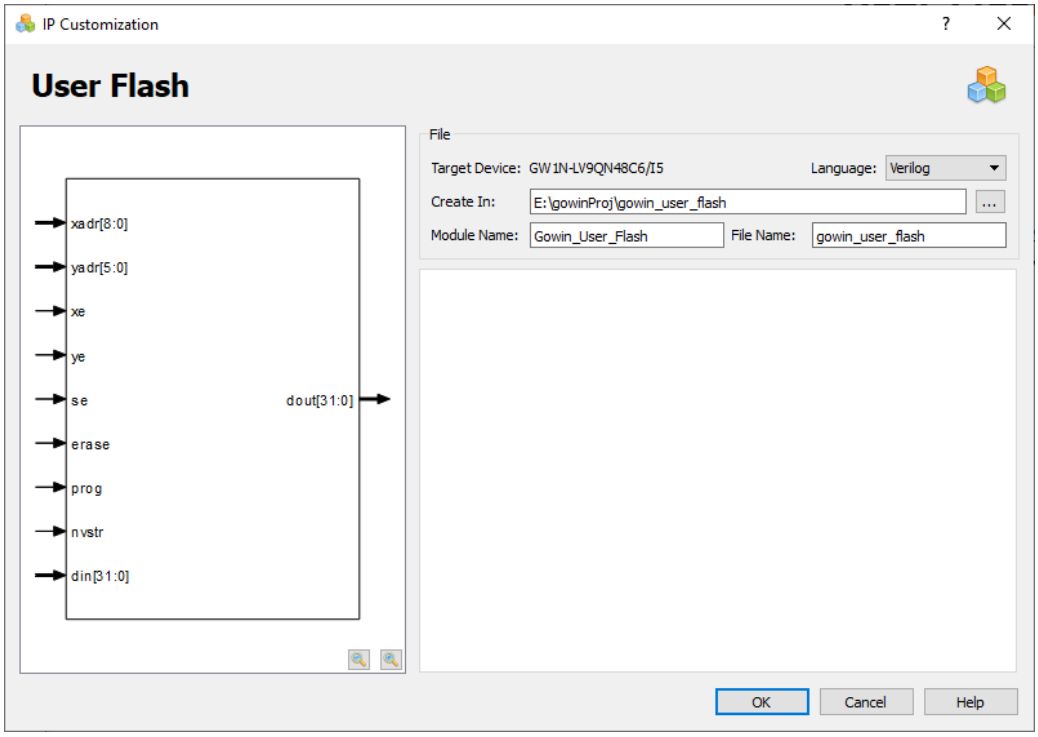
3.5 User Flash

User Flash is the user flash memory. Click "User Flash" on the IP Core Generator page. A brief introduction to the User Flash will be displayed.

IP Configuration

Double-clicking on "User Flash", and the "IP Customization" window opens as shown in Figure 3-26. This displays the "File" configuration and port Display diagram.

Figure 3-26 IP Customization of User Flash



1. File
   - The File displays the basic information related to the User Flash.
   - The User Flash file configuration is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.

Note!

- Different devices can generate different User Flash, you can refer to SUG283, Gowin Primitives User Guide.

2. The ports configuration diagram displays the current IP Core configuration result, and User Flash input bit-width updates in real time based on the target device, as shown in Figure 3-26.
3. Help Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the

"File Name".

- "gowin_user_flash.v" file is a complete Verilog module to generate instance User Flash, and it is generated according to the IP configuration;
- "gowin_user_flash_tmp.v" is the instance template file;
- "gowin_user_flash.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

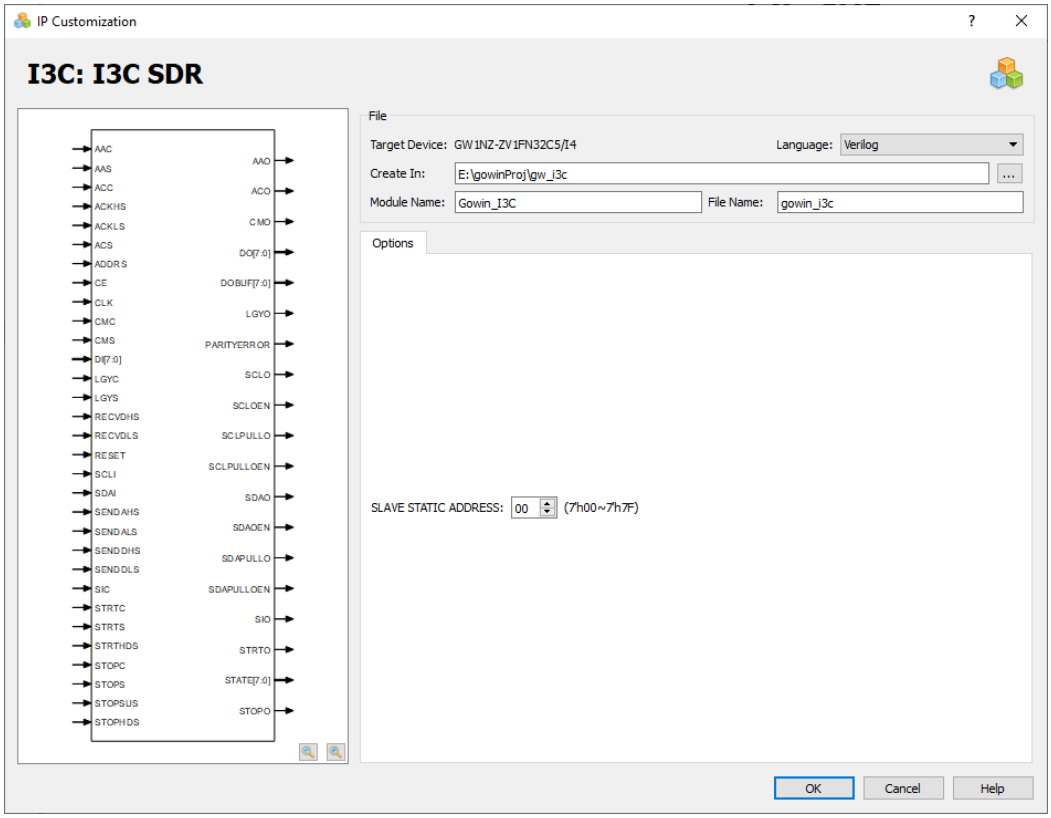
3.6 I3C

I3C supports high-speed, low-power, and other critical features that are currently covered by I²C and SPI. The I3C IP provides registers for users to control and realize specific functions. Click "I3C > I3C SDR" on the "IP Core Generator" page. A brief introduction to the I3C SDR will be displayed.

IP Configuration

Double-click "I3C SDR", and the "IP Customization" window pops up. This includes the "File", "Options", port diagram, and "Help", as shown in Figure 3-27.

Figure 3-27 IP Customization of I3C



1. File

- The File displays the basic information related to the I3C.
- The I3C file configuration is similar to that of SP. For the detailed configuration instructions, please refer to 3.1 Block Memory > 3.1.1 SP > File.

2. Options
   - The Options is used to configure I3C by users, as shown in Figure 3-27.
   - SLAVE STATIC ADDRESS: Specify the static address of the Slave.
3. The ports diagram is based on the IP Core configuration. The input/output number updates in real time based on the "Options" configuration, as shown in Figure 3-27;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_i3c.v" file is a complete Verilog module to generate instance I3C, and it is generated according to the IP configuration;
- "gw_i3c_tmp.v" is the instance template file;
- "gw_i3c.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

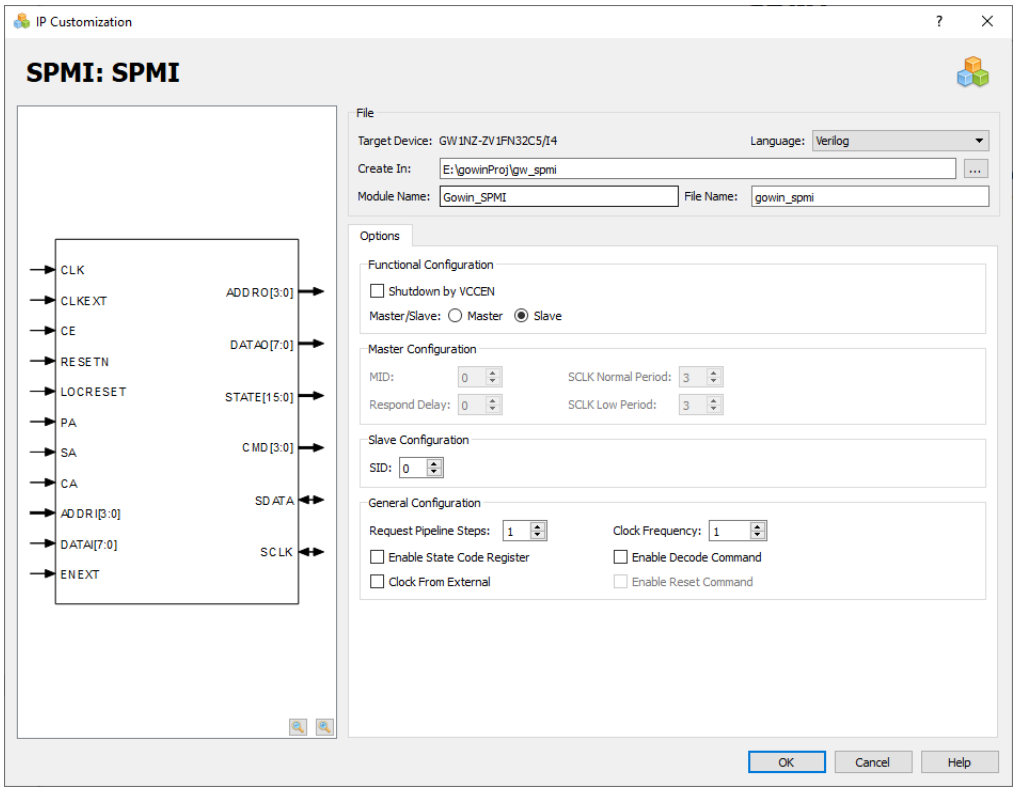
3.7 SPMI

SPMI Hard Core is a two-wire serial interface and it can make integrated Power Controller (PC) of a System-on-Chip (SoC) processor system connect with one or more voltage regulation systems of Power Management Integrated Circuits (PMIC). SPMI enables systems to dynamically adjust the supply and substrate bias voltages of the voltage domains inside the SoC using a single SPMI bus. Click "SPMI" on the IP Core Generator, and a brief introduction to the SPMI will be displayed.

IP Configuration

Double-click the "SPMI" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-28.

Figure 3-28 IP Customization of SPMI



1. File
   - The File displays the basic information related to SPMI.
   - The SPMI file configuration box is similar to that of SP. For the details, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. Options
   - The Options is used to configure SPMI by users, as shown in Figure 3-28.
   - Functional Configuration：
     - Shutdown by VCCEN：Shutdown by external pin VCCEN If this option is checked, the communication function of SPMI will be disabled.
     - Master/Slave: Set SPMI as Master or Slave.
   - Master Configuration:
     - MID: Master ID. The range is 0-3, and default value is 0.
     - Respond Delay: Set the response delay.
     - SCLK Normal Period: Set SCLK period in normal mode.
     - SCLK Normal Period: Set SCLK period in low mode.
   - Slave Configuration:
     SID: Slave ID.
   - General configuration:

- Enable State Code Register: Enable or disable the state code register. If "Enable State Code Register" is checked, the output state code will pass a register.
- Request Pipeline Steps: Set the sampling delay step of the request signal.
- Enable Decode Command: Enable or disable decode. If "Enable Decode Command" is checked, SPMI will decode the reset, sleep, shutdown, and wakeup.
- Enable Decode Command: Enable or disable reset.
- Clock From External: Enable or disable the external clock.
- Clock Frequency: System clock frequency.

3. The ports diagram is based on the current IP Core configuration, as shown in Figure 3-28;
4. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information" and "Options".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gw_spmi.v" file is a complete Verilog module to generate instance SPMI, and it is generated according to the IP configuration;
- "gw_spmi_tmp.v" is the instance template file;
- "gw_spmi.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.

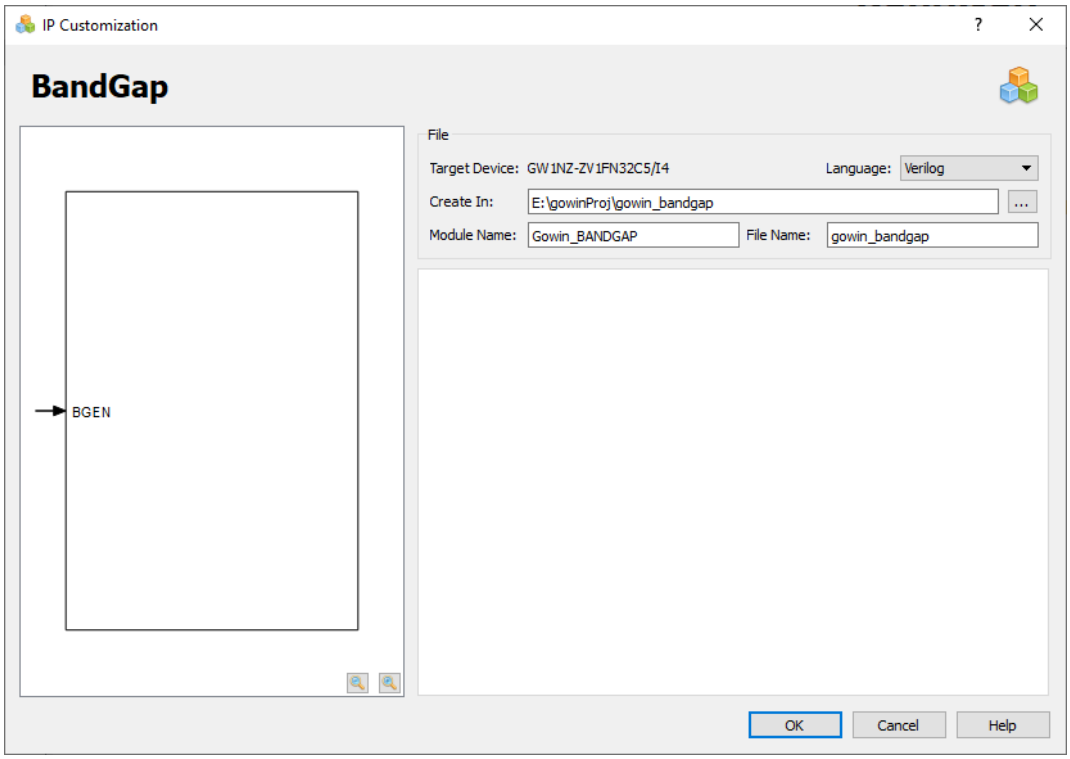
3.8 BandGap

BandGap provides a constant voltage and current for certain modules in the chip. If BandGap is closed, certain modules such as OSC, PLL, PLL, and FLASH will not work, reducing device power consumption. Click "BandGap" on the IP Core Generator, and a brief introduction to the BandGap will be displayed.

IP Configuration

Double-click the "BandGap" to open the "IP Customization" window. This includes the "File", "Options", ports diagram, and the "Help", as shown in Figure 3-29.

Figure 3-29 IP Customization of BandGap



1. File
   - The File displays the basic information related to BandGap.
   - The BandGap file configuration is similar to that of SP. For the detailed configuration, please refer to 3.1 Block Memory > 3.1.1 SP > File.
2. The ports diagram is based on the current IP Core configuration, as shown in Figure 3-29;
3. Help
   Click "Help" to open the IP Core configuration information. The Help page displays "Information".

Generated Files

After configuration, it will generate three files that are named after the "File Name".

- "gowin_bandgap.v" file is a complete Verilog module to generate instance BandGap, and it is generated according to the IP configuration;
- "gowin_bandgap_tmp.v" is the instance template file;
- "gowin_bandgap.ipc" file is IP configuration file. The user can load the file to configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.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