



## KL05 Sub-Family Data Sheet

Supports: MKL05Z8VFK4,  
MKL05Z16VFK4, MKL05Z32VFK4,  
MKL05Z8VLC4, MKL05Z16VLC4,  
MKL05Z32VLC4, MKL05Z8VFM4,  
MKL05Z16VFM4, MKL05Z32VFM4,  
MKL05Z16VLF4, MKL05Z32VLF4

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 48 MHz ARM® Cortex-M0+ core
- Memories and memory interfaces
  - Up to 32 KB program flash memory
  - Up to 4 KB RAM
- Clocks
  - 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
  - Multi-purpose clock source
- System peripherals
  - Nine low-power modes to provide power optimization based on application requirements
  - 4-channel DMA controller, supporting up to 63 request sources
  - COP Software watchdog
  - Low-leakage wakeup unit
  - SWD interface and Micro Trace buffer
  - Bit Manipulation Engine (BME)
- Security and integrity modules
  - 80-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - 12-bit SAR ADC
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- Timers
  - Two 2-channel Timer/PWM (TPM)
  - Periodic interrupt timers
  - 16-bit low-power timer (LPTMR)
  - Real-time clock
- Communication interfaces
  - One 8-bit SPI module
  - I2C module
  - One low power UART module

## KL05P48M48SF1



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preliminary  
General Business Information



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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [www.freescale.com](http://www.freescale.com) and perform a part number search for the following device numbers: PKL05 and MKL05

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KL##	Kinetis family	<ul style="list-style-type: none"> <li>KL05</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = Cortex-M0+</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>8 = 8 KB</li> <li>16 = 16 KB</li> <li>32 = 32 KB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>

*Table continues on the next page...*

## Terminology and guidelines

Field	Description	Values
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• V = -40 to 105</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• FK = 24 QFN (4 mm x 4 mm)</li><li>• LC = 32 LQFP (7 mm x 7 mm)</li><li>• FM = 32 QFN (5 mm x 5 mm)</li><li>• LF = 48 LQFP (7 mm x 7 mm)</li></ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"><li>• 4 = 48 MHz</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li><li>• (Blank) = Trays</li></ul>

## 2.4 Example

This is an example part number:

MKL05Z8VLC4

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

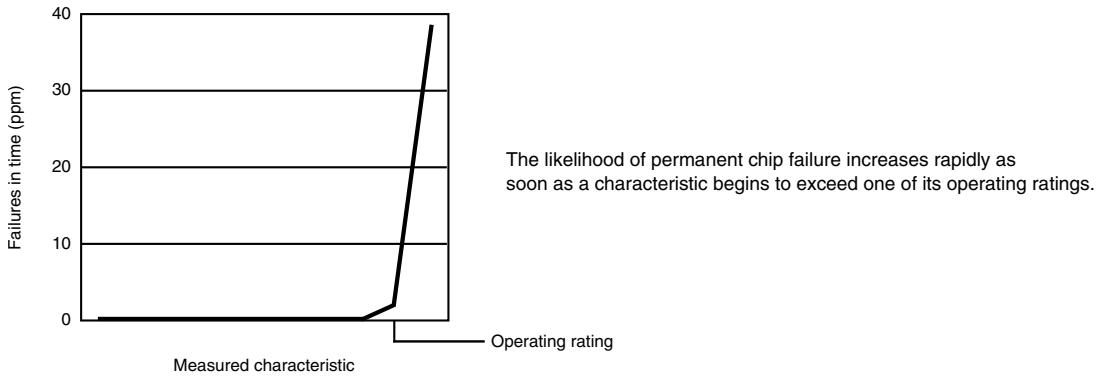
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

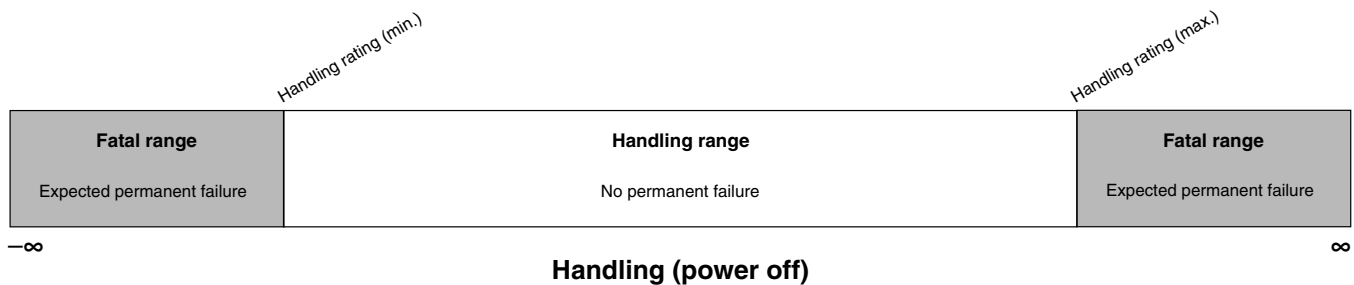
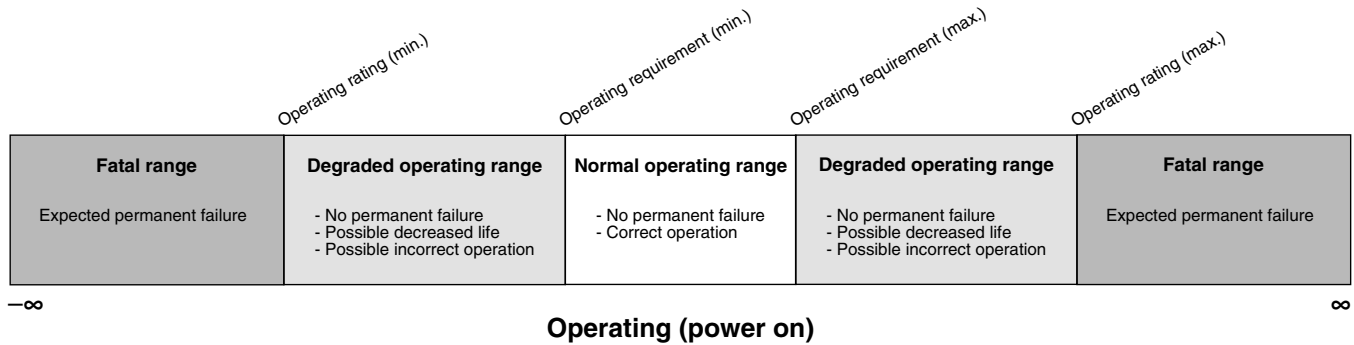
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



### 3.6 Relationship between ratings and operating requirements



### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

#### 3.8.1 Example 1

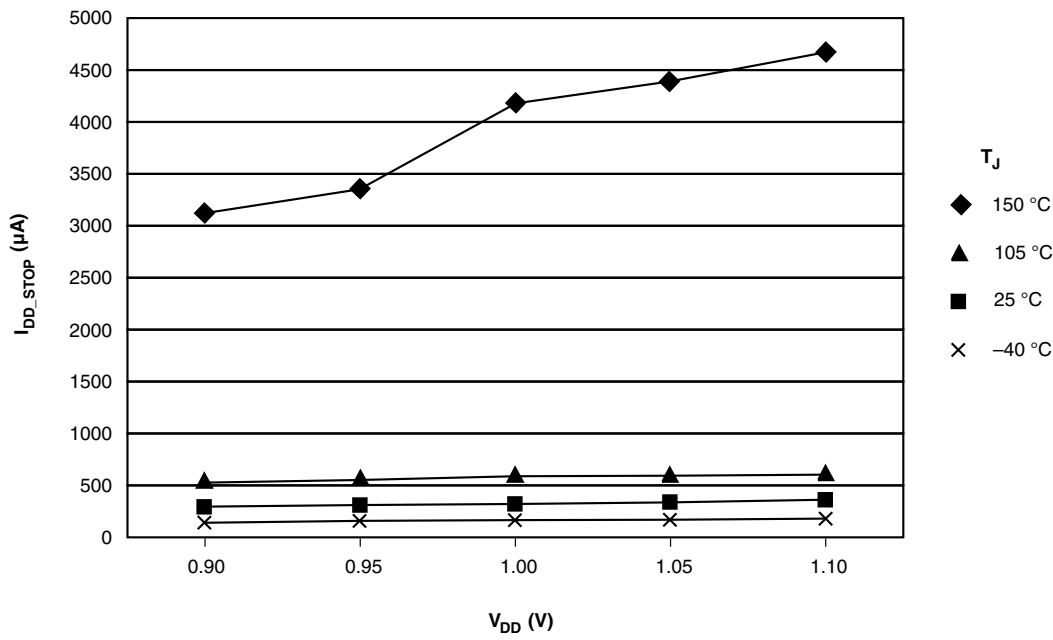
This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	μA

#### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

## Ratings



## 3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.



## 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

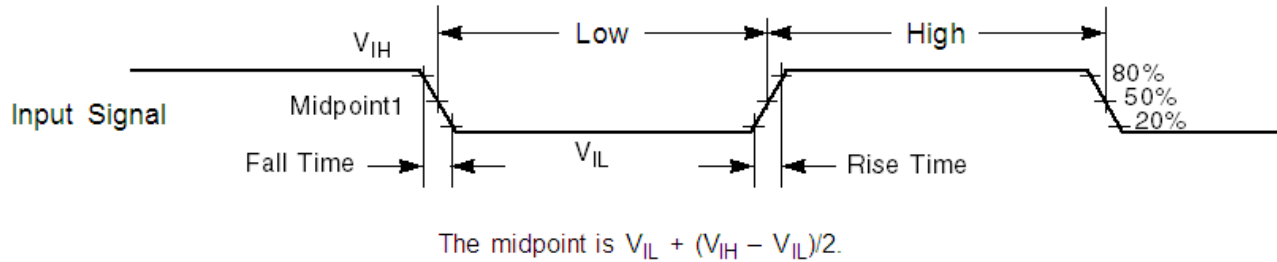
Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	Digital supply voltage	-0.3	3.8	V
I <sub>DD</sub>	Digital supply current	—	120	mA
V <sub>DIO</sub>	Digital pin input voltage (except $\overline{\text{RESET}}$ )	-0.3	V <sub>DD</sub> + 0.3	V
V <sub>AIO</sub>	Analog pins <sup>1</sup> and $\overline{\text{RESET}}$ pin input voltage	-0.3	V <sub>DD</sub> + 0.3	V
I <sub>D</sub>	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V <sub>DDA</sub>	Analog supply voltage	V <sub>DD</sub> - 0.3	V <sub>DD</sub> + 0.3	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assumes:

1. output pins
  - have  $C_L=30\text{pF}$  loads,
  - are slew rate disabled, and
  - are normal drive strength

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	

Table continues on the next page...

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$I_{ICIO}$	I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3V</math> (Negative current injection)</li> <li><math>V_{IN} &gt; V_{DD}+0.3V</math> (Positive current injection)</li> </ul>	-3 —	— +3	mA	1
$I_{ICcont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> <li>Positive current injection</li> </ul>	-25 —	— +25	mA	
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	

1. All analog pins are internally clamped to  $V_{SS}$  and  $V_{DD}$  through ESD protection diodes. If  $V_{IN}$  is greater than  $V_{AIO\_MIN}$  ( $=V_{SS}-0.3V$ ) and  $V_{IN}$  is less than  $V_{AIO\_MAX}$  ( $=V_{DD}+0.3V$ ) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$ . Select the larger of these two calculated resistances.

## 5.2.2 LVD and POR operating requirements

**Table 2.  $V_{DD}$  supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
$V_{LVDH}$	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
$V_{LVW1H}$	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
$V_{LVW2H}$	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
$V_{LVW3H}$	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
$V_{LVW4H}$	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
$V_{LVW1L}$	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
$V_{LVW2L}$	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
$V_{LVW3L}$	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
$V_{LVW4L}$	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	

Table continues on the next page...

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

## 5.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — Normal drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -5 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -1.5 mA</li> </ul>	V <sub>DD</sub> - 0.5 V <sub>DD</sub> - 0.5	— —	V V	1
V <sub>OH</sub>	Output high voltage — High drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -18 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -6 mA</li> </ul>	V <sub>DD</sub> - 0.5 V <sub>DD</sub> - 0.5	— —	V V	1
I <sub>OHT</sub>	Output high current total for all ports	—	100	mA	
V <sub>OL</sub>	Output low voltage — Normal drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OL</sub> = 5 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OL</sub> = 1.5 mA</li> </ul>	— —	0.5 0.5	V V	1
V <sub>OL</sub>	Output low voltage — High drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OL</sub> = 18 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OL</sub> = 6 mA</li> </ul>	— —	0.5 0.5	V V	1
I <sub>OLT</sub>	Output low current total for all ports	—	100	mA	
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range	—	1	μA	2
I <sub>IN</sub>	Input leakage current (per pin) at 25 °C	—	0.025	μA	2
I <sub>IN</sub>	Input leakage current (total all pins) for full temperature range	—	41	μA	2
I <sub>OZ</sub>	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R <sub>PU</sub>	Internal pullup resistors	20	50	kΩ	3

1. PTA12, PTA13, PTB0 and PTB1 I/O have both high drive and normal drive capability selected by the associated PTX\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V<sub>DD</sub> = 3.6 V
3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

**Table 4. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	$\mu s$	
	• VLLS0 $\rightarrow$ RUN	—	95	115	$\mu s$	
	• VLLS1 $\rightarrow$ RUN	—	93	115	$\mu s$	
	• VLLS3 $\rightarrow$ RUN	—	42	53	$\mu s$	
	• LLS $\rightarrow$ RUN	—	4	4.6	$\mu s$	
	• VLPS $\rightarrow$ RUN	—	4	4.4	$\mu s$	
	• STOP $\rightarrow$ RUN	—	4	4.4	$\mu s$	

## 5.2.5 Power consumption operating behaviors

**Table 5. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUNCO}$	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	—	4.1	TBD	mA	2
$I_{DD\_RUN}$	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	—	5.1	TBD	mA	2

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 125 °C</li> </ul> </li> </ul>	—	6.4	TBD	mA	2, 3,
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	3.0	TBD	mA	2
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.3	TBD	mA	2
I <sub>DD_PSTOP2</sub>	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.3	TBD	mA	2
I <sub>DD_VLPRCO</sub>	Very low power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	154	TBD	μA	4
I <sub>DD_VLPR</sub>	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	185	TBD	μA	4
I <sub>DD_VLPR</sub>	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	237	TBD	μA	4, 3
I <sub>DD_VLPW</sub>	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	118	TBD	μA	4

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_STOP</sub>	Stop mode current <ul style="list-style-type: none"> <li>at 3.0 V</li> <li>at 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	308	TBD	μA	
		—	325	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
I <sub>DD_VLPS</sub>	Very-low-power stop mode current <ul style="list-style-type: none"> <li>at 3.0 V</li> <li>at 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	2.5	TBD	μA	
		—	6.2	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
I <sub>DD_LLS</sub>	Low leakage stop mode current <ul style="list-style-type: none"> <li>at 3.0 V</li> <li>at 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.8	TBD	μA	
		—	4.0	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current <ul style="list-style-type: none"> <li>at 3.0 V</li> <li>at 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.3	TBD	μA	
		—	3.2	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current <ul style="list-style-type: none"> <li>at 3.0 V</li> <li>at 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	0.7	TBD	μA	
		—	2.7	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) <ul style="list-style-type: none"> <li>• at 3.0 V</li> <li>• at 25 °C</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	386	TBD	nA	
		—	2350	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) <ul style="list-style-type: none"> <li>• at 3.0 V</li> <li>• at 25 °C</li> <li>• at 50 °C</li> <li>• at 70 °C</li> <li>• at 85 °C</li> <li>• at 105 °C</li> </ul>	—	183	TBD	nA	5
		—	2193	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		
		—	TBD	TBD		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for FEI mode.
3. Incremental current consumption from peripheral activity is not included.
4. MCG configured for BLPI mode.
5. No brownout

**Table 6. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHz</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHz</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>EREFSTEN4MHz</sub>	External 4MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA

*Table continues on the next page...*



**Table 6. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>EREFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
		440	490	540	560	570	580	
	VLLS1	490	490	540	560	570	680	
	VLLS3	510	560	560	560	610	680	
	LLS	510	560	560	560	610	680	
	VLPS							
	STOP							
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>RTC</sub>	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							μA
	MCGIRCLK (4MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4MHz external crystal)	214	237	246	254	260	268	
I <sub>TPM</sub>	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							μA
	MCGIRCLK (4MHz internal reference clock)	86	86	86	86	86	86	
	OSCERCLK (4MHz external crystal)	235	256	265	274	280	287	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA

Table continues on the next page...

**Table 6. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	μA

### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

TBD

**Figure 2. Run mode supply current vs. core frequency**

TBD

Figure 3. VLPR mode current vs. core frequency

## 5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for TBD package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	TBD	dB $\mu$ V	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	TBD	dB $\mu$ V	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	TBD	dB $\mu$ V	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	TBD	dB $\mu$ V	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25 °C, f<sub>OSC</sub> = 8 MHz (crystal), f<sub>SYS</sub> = 48 MHz, f<sub>BUS</sub> = 48 MHz

3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	48	MHz	
$f_{BUS}$	Bus clock	—	24	MHz	
$f_{FLASH}$	Flash clock	—	24	MHz	
$f_{LPTMR}$	LPTMR clock	—	24	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	1	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	
$f_{LPTMR}$	LPTMR clock	—	24	MHz	
$f_{ERCLK}$	External reference clock	—	16	MHz	
$f_{LPTMR\_pin}$	LPTMR clock	—	24	MHz	
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz	

*Table continues on the next page...*

## General

Symbol	Description	Min.	Max.	Unit	Notes
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz	
$f_{TPM}$	TPM asynchronous clock	—	8	MHz	
$f_{UART0}$	UART0 asynchronous clock	—	8	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

## 5.3.2 General Switching Specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I<sup>2</sup>C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

## 5.4.2 Thermal attributes

**Table 10. Thermal attributes**

Board type	Symbol	Description	48 LQFP	32 LQFP	32 QFN	24 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	82	88	97	110	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	58	59	34	42	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	70	74	81	92	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	28	36	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	13	18	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	27	26	2.3	3.7	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	8	8	8	10	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 SWD Electricals

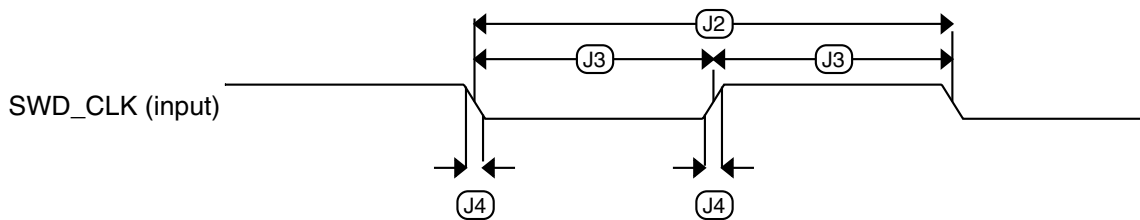
**Table 11. SWD full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

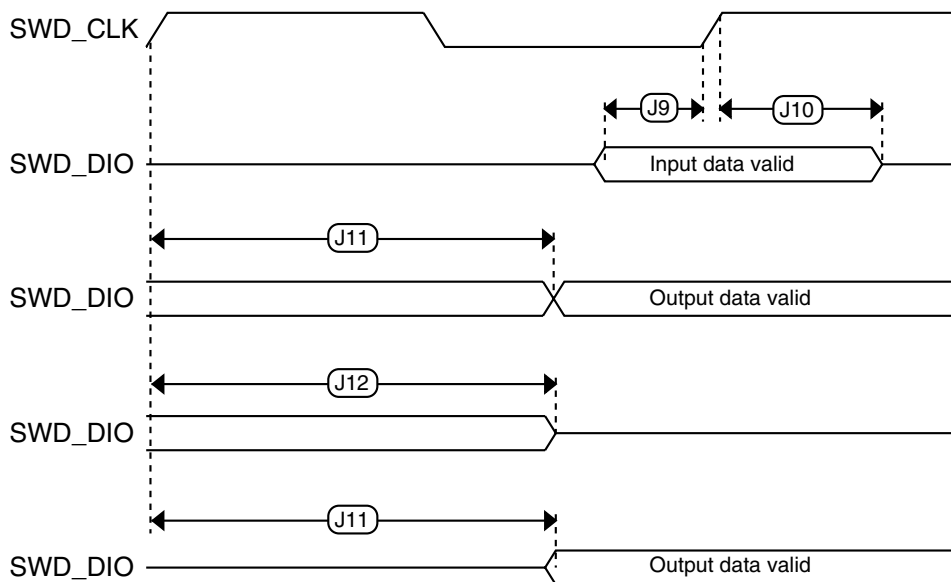
Table continues on the next page...

**Table 11. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns



**Figure 4. Serial wire clock input timing**



**Figure 5. Serial wire data timing**



## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

Table 12. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	32.768	—	kHz		
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	$\pm 0.3$	$\pm 0.6$	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	TBD	% $f_{dco}$	1, 2	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	—	$\pm 0.4$	TBD	% $f_{dco}$	1, 2	
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	4	—	MHz		
$\Delta f_{intf\_ft}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage --- factory trimmed at nominal $V_{DD}$ and 25 °C	—	+1/-2	TBD	% $f_{intf\_ft}$	2	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C	3	—	5	MHz		
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS = 00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) $1280 \times f_{fill\_ref}$	40	41.94	48	MHz	

Table continues on the next page...

**Table 12. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{\text{dco\_t\_DMX32}}$	DCO output frequency	Low range (DRS = 00) $732 \times f_{\text{fill\_ref}}$	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) $1464 \times f_{\text{fill\_ref}}$	—	47.97	—	MHz	
$J_{\text{cyc\_fill}}$	FLL period jitter • $f_{\text{VCO}} = 48$ MHz	—	180	—	ps	7	
$t_{\text{fill\_acquire}}$	FLL target frequency acquisition time	—	—	1	ms	8	

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal  $V_{\text{DD}}$  and 25 °C,  $f_{\text{ints\_ft}}$ .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{\text{dco\_t}}$ ) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

### 6.3.2.1 Oscillator DC electrical specifications

**Table 13. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{\text{DD}}$	Supply voltage	1.71	—	3.6	V	
$I_{\text{DDOSC}}$	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	

Table continues on the next page...

**Table 13. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDOSC</sub>	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C <sub>x</sub>	EXTAL load capacitance	—	—	—		2, 3
C <sub>y</sub>	XTAL load capacitance	—	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub>,C<sub>y</sub> can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used..
4. When low power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 14. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	—	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	—	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 15. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{pgm}4}$	Longword Program high-voltage time	—	7.5	18	$\mu\text{s}$	
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1

1. Maximum time based on expectations at cycling end-of-life.

### 6.4.1.2 Flash timing specifications — commands

**Table 16. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1\text{sec}1\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu\text{s}$	1
$t_{pgm\text{chk}}$	Program Check execution time	—	—	45	$\mu\text{s}$	1
$t_{rd\text{rsrc}}$	Read Resource execution time	—	—	30	$\mu\text{s}$	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu\text{s}$	
$t_{er\text{sscr}}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1\text{all}}$	Read 1s All Blocks execution time	—	—	0.5	ms	
$t_{rd\text{once}}$	Read Once execution time	—	—	25	$\mu\text{s}$	1
$t_{pgm\text{once}}$	Program Once execution time	—	65	—	$\mu\text{s}$	
$t_{er\text{sall}}$	Erase All Blocks execution time	—	55	465	ms	2
$t_{vfy\text{key}}$	Verify Backdoor Access Key execution time	—	—	30	$\mu\text{s}$	1

- Assumes 25MHz flash clock frequency.
- Maximum times for erase parameters based on expectations at cycling end-of-life.

### 6.4.1.3 Flash high voltage current behaviors

**Table 17. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DD\_PGM}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{DD\_ERS}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 6.4.1.4 Reliability specifications

**Table 18. NVM reliability specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvm\text{retp}10\text{k}}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvm\text{retp}1\text{k}}$	Data retention after up to 1 K cycles	20	100	—	years	
$\eta_{nvm\text{cycp}}$	Cycling endurance	10 K	50 K	—	cycles	2

## Peripheral operating requirements and behaviors

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ .

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

#### 6.6.1.1 12-bit ADC operating conditions

Table 19. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> -V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> - V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	3
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	3
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	• 8-/10-/12-bit modes	—	4	5	pF	
R <sub>ADIN</sub>	Input resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance	12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	4
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	5
C <sub>rate</sub>	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

- DC potential difference.
- For packages without dedicated VREFH and VREFL pins,  $V_{REFH}$  is internally tied to  $V_{DDA}$ , and  $V_{REFL}$  is internally tied to  $V_{SSA}$ .
- This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has  $< 8 \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1\text{ns}$ .
- To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
- For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#)

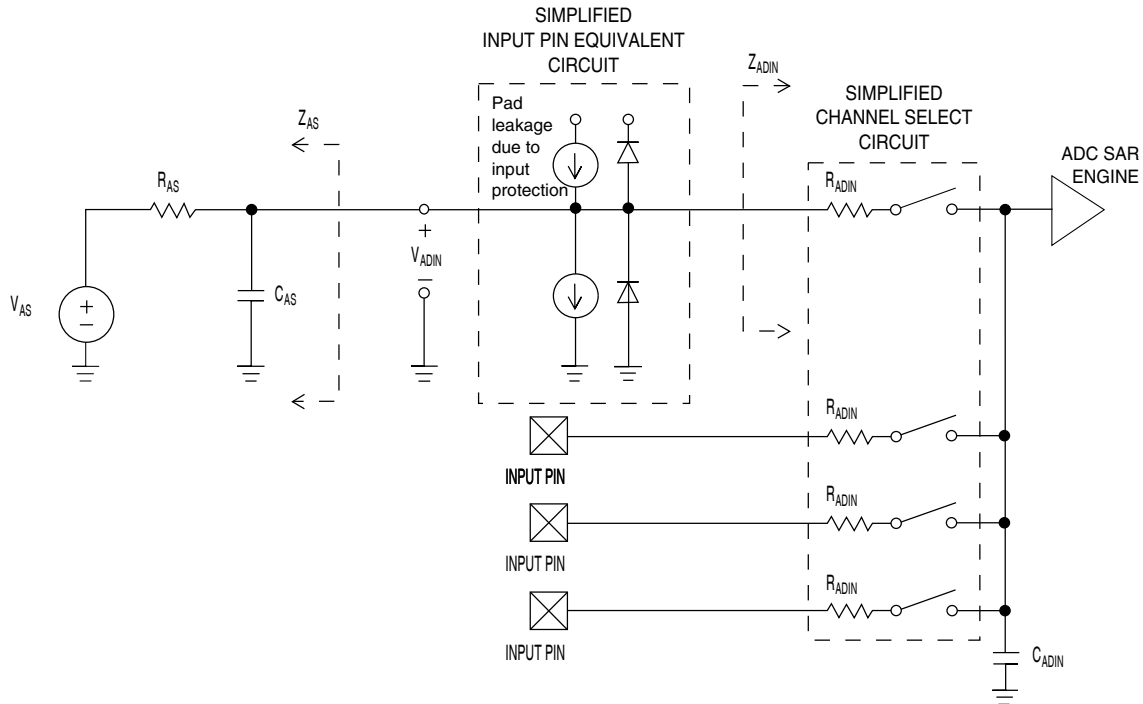


Figure 6. ADC input impedance equivalency diagram

### 6.6.1.2 12-bit ADC electrical characteristics

Table 20. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	<ul style="list-style-type: none"> <li>ADLPC = 1, ADHSC = 0</li> <li>ADLPC = 1, ADHSC = 1</li> <li>ADLPC = 0, ADHSC = 0</li> <li>ADLPC = 0, ADHSC = 1</li> </ul>	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
			2.4	4.0	6.1	MHz	
			3.0	5.2	7.3	MHz	
			4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	$\pm 4$	$\pm 6.8$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	$\pm 0.7$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5

Table continues on the next page...

**Table 20. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±1.0	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
E <sub>FS</sub>	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	-4	-5.4	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ 5
E <sub>Q</sub>	Quantization error	<ul style="list-style-type: none"> <li>12-bit modes</li> </ul>	—	—	±0.5	LSB <sup>4</sup>	
E <sub>IL</sub>	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current  (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	—	1.715	—	mV/°C	
V <sub>TEMP25</sub>	Temp sensor voltage	25 °C	—	719	—	mV	

- All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25°C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 21. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V
I <sub>DDHS</sub>	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	μA
I <sub>DDL</sub>	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	μA
V <sub>AIN</sub>	Analog input voltage	V <sub>SS</sub>	—	V <sub>DD</sub>	V
V <sub>AIO</sub>	Analog input offset voltage	—	—	20	mV

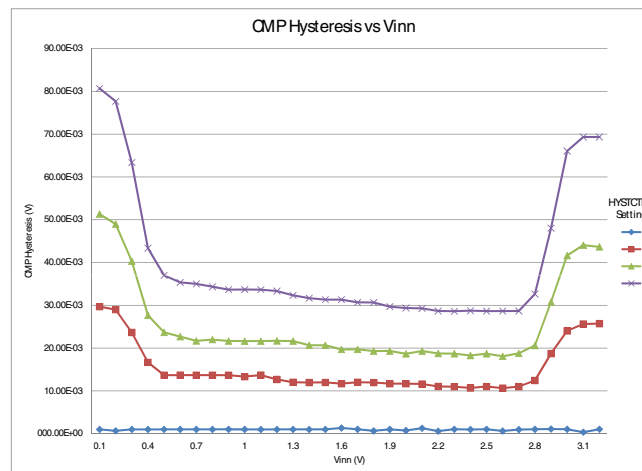
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**Table 21. Comparator and 6-bit DAC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_H$	Analog comparator hysteresis <sup>1</sup>				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu$ s
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu$ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to  $V_{DD} - 0.7$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

**Figure 7. Typical hysteresis vs. Vin level ( $V_{DD} = 3.3$  V, PMODE = 0)**

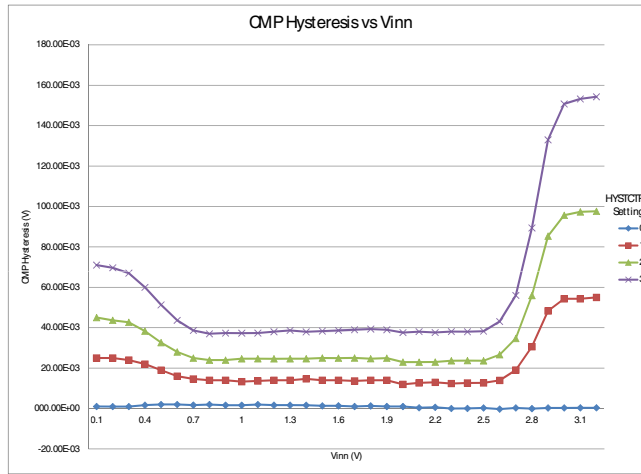


Figure 8. Typical hysteresis vs. Vin level ( $V_{DD} = 3.3\text{ V}$ ,  $\text{PMODE} = 1$ )

### 6.6.3 12-bit DAC electrical characteristics

#### 6.6.3.1 12-bit DAC operating requirements

Table 22. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage		3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$T_A$	Temperature	Operating temperature range of the device		°C	
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or the voltage output of the VREF module (VREF\_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

#### 6.6.3.2 12-bit DAC operating behaviors

Table 23. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	250	μA	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	900	μA	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1

Table continues on the next page...

**Table 23. 12-bit DAC operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	TBD	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	TBD	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance load = 3 k $\Omega$	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu\text{s}$	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4$  V
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0$  V, reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

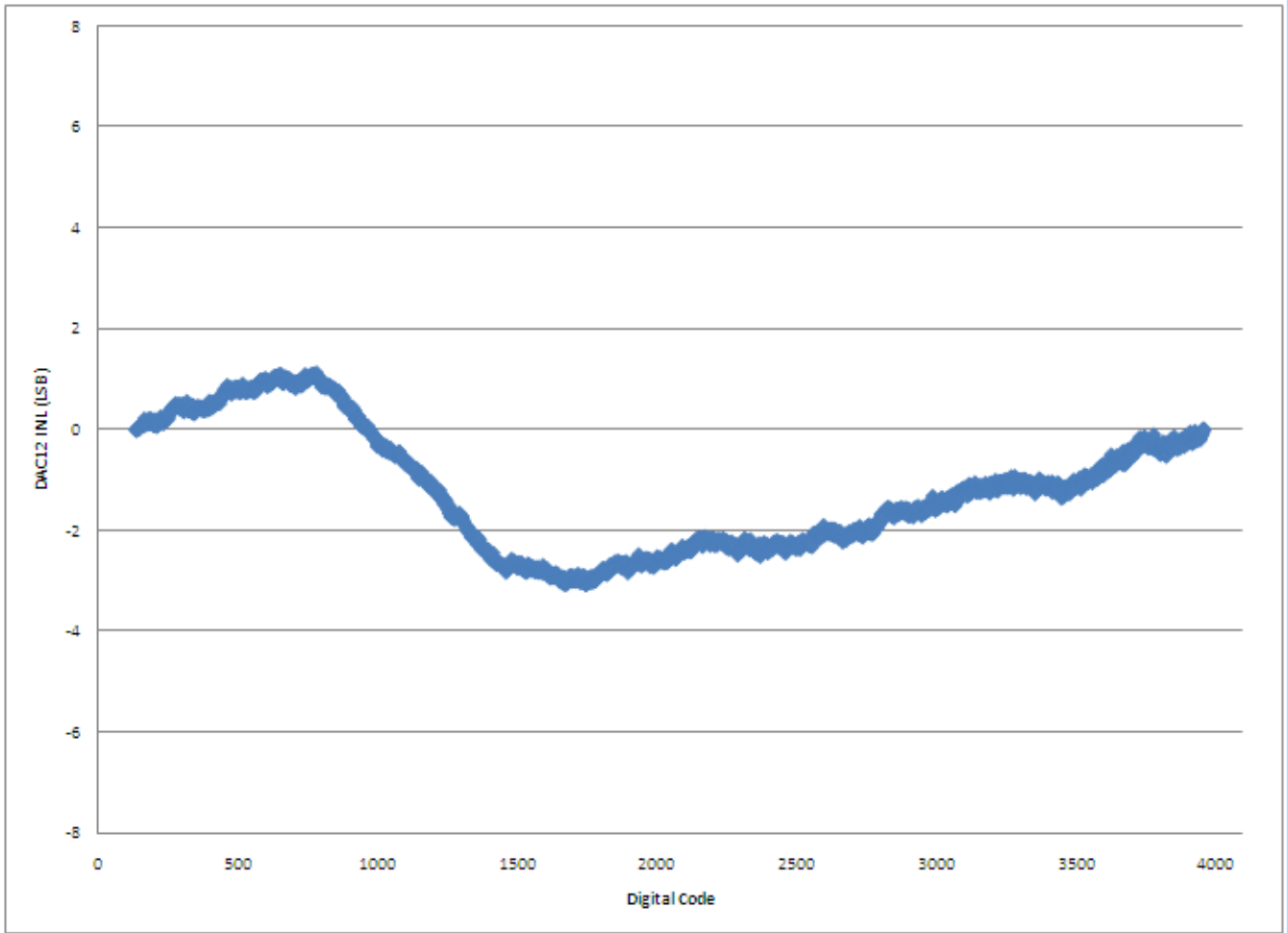


Figure 9. Typical INL error vs. digital code

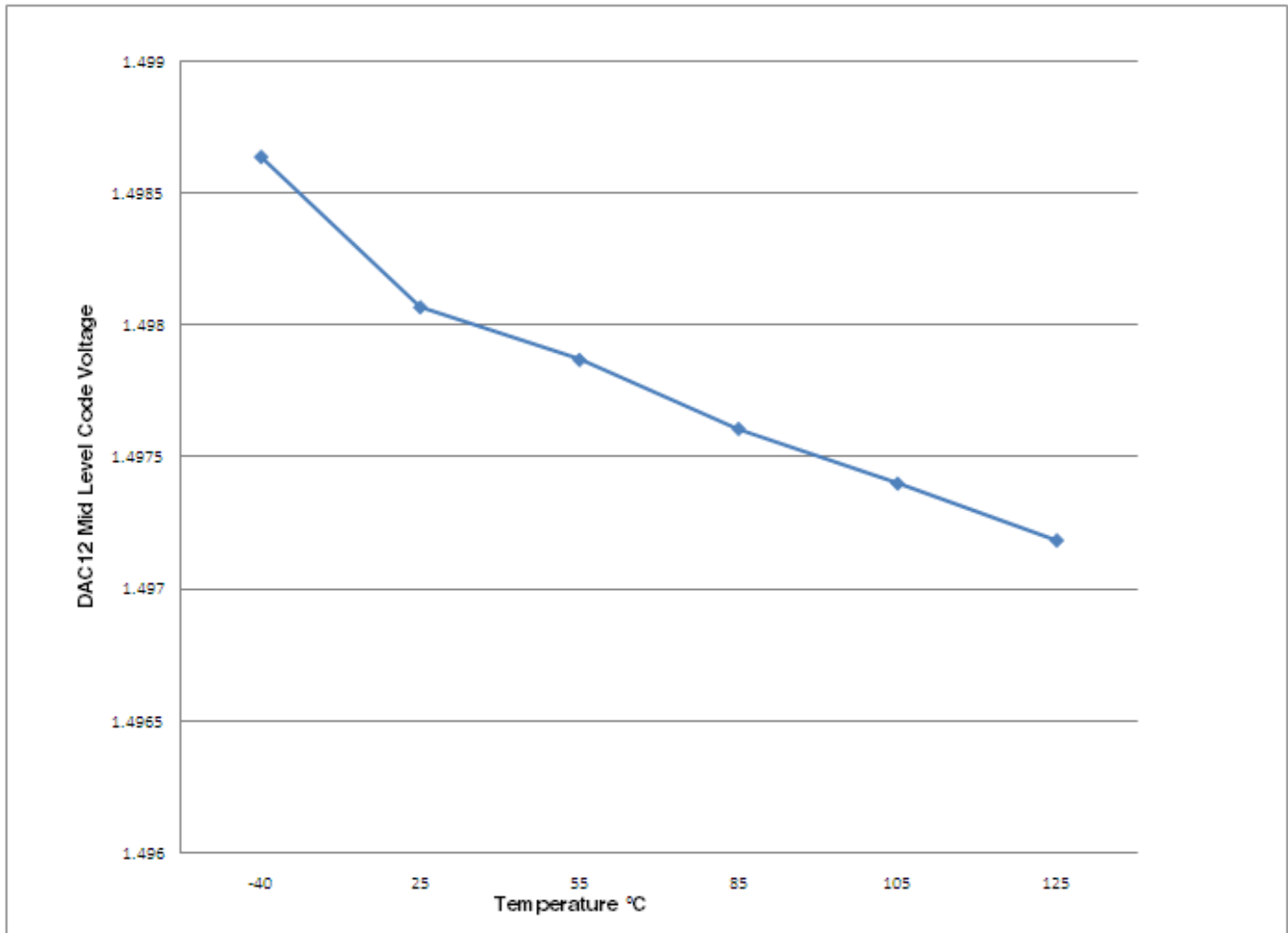


Figure 10. Offset at half scale vs. temperature

## 6.7 Timers

See General switching specifications.

## 6.8 Communication interfaces

### 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

## Peripheral operating requirements and behaviors

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 24. SPI master mode timing on slew rate disabled pads**

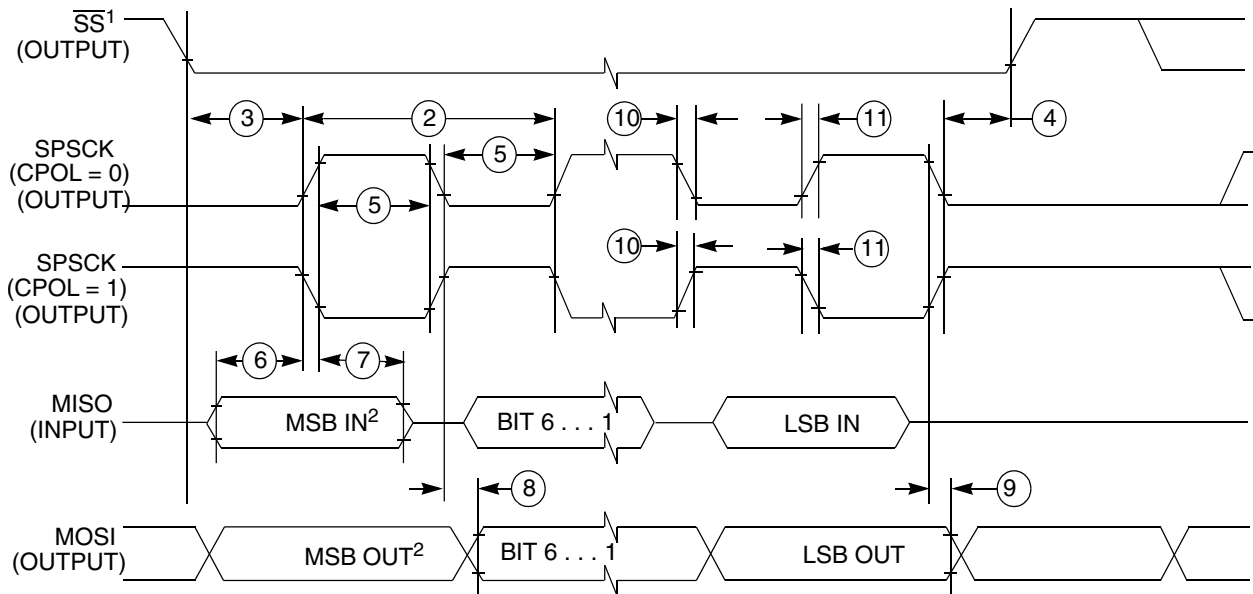
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	16	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	10	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ).
2.  $t_{periph} = 1/f_{periph}$

**Table 25. SPI master mode timing on slew rate enabled pads**

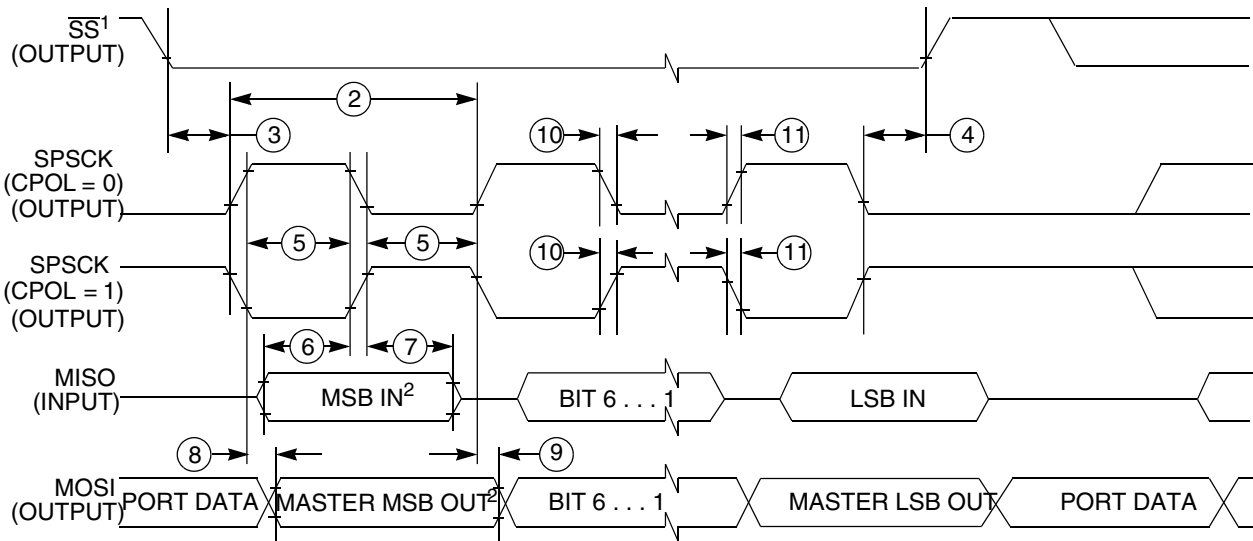
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	96	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	52	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ).
2.  $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 11. SPI master mode timing (CPHA = 0)**



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 12. SPI master mode timing (CPHA = 1)**

**Table 26. SPI slave mode timing on slew rate disabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—

Table continues on the next page...

**Table 26. SPI slave mode timing on slew rate disabled pads (continued)**

Num.	Symbol	Description	Min.	Max.	Unit	Note
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCCK edge)	—	22	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

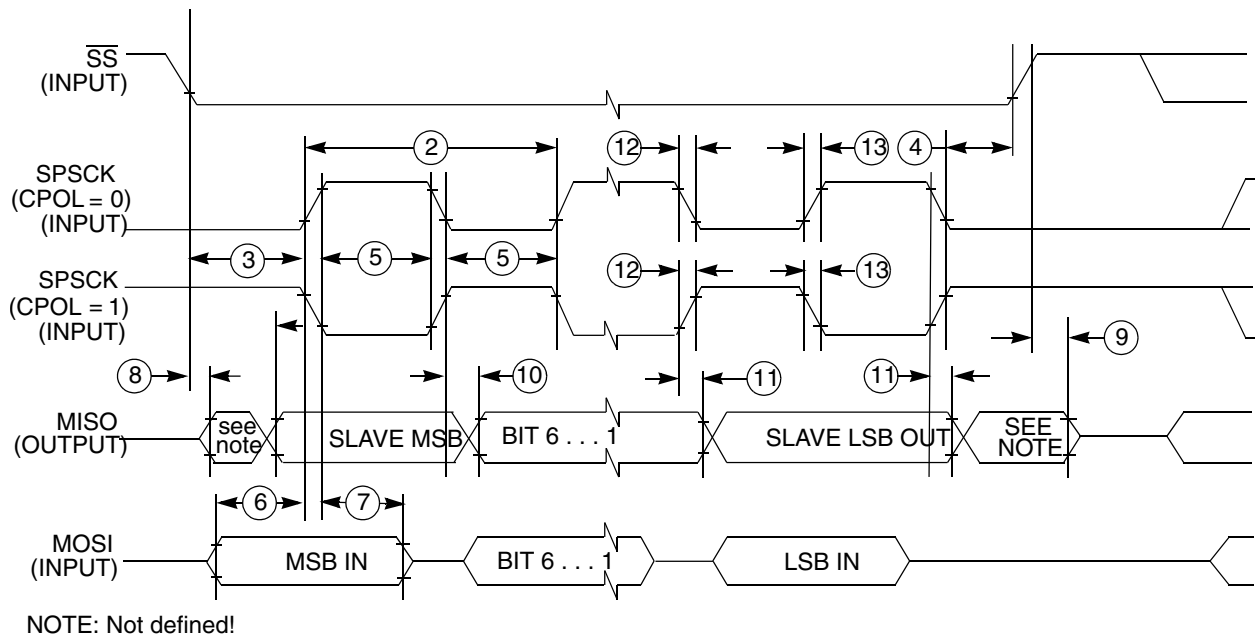
1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Table 27. SPI slave mode timing on slew rate enabled pads**

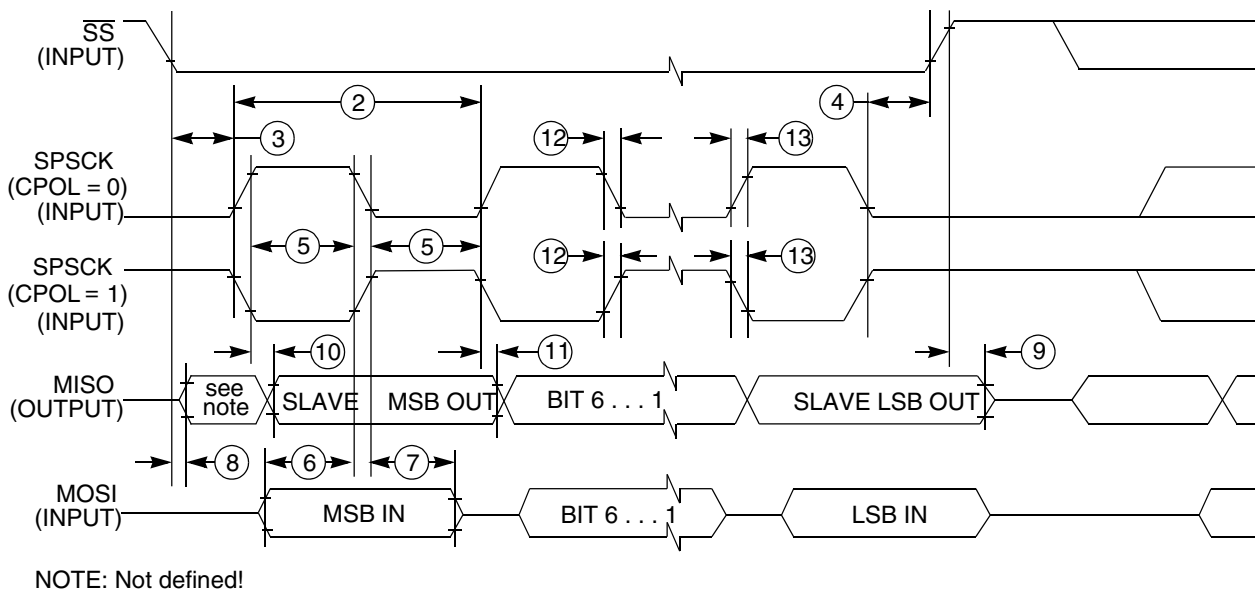
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCCK}$	SPSCCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCCK}$	Clock (SPSCCK) high or low time	$t_{periph} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCCK edge)	—	122	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state





**Figure 13. SPI slave mode timing (CPHA = 0)**



**Figure 14. SPI slave mode timing (CPHA = 1)**

## 6.8.2 I<sup>2</sup>C

See General switching specifications.

## 6.8.3 UART

See General switching specifications.

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

**Table 28. TSI electrical specifications**

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [www.freescale.com](http://www.freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
24-pin QFN	98ASA00474D
32-pin QFN	98ASA00473D
32-pin LQFP	98ASH70029A
48-pin LQFP	98ASH00962A

## 8 Pinout

## 8.1 KL05 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

48 LQFP	32 QFN	32 LQFP	24 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	1	PTB6/ IRQ_2/ LPTMR0_ALT3	DISABLED	DISABLED	PTB6/ IRQ_2/ LPTMR0_ALT3	TPM0_CH3	TPM_CLKIN1
2	2	2	2	PTB7/ IRQ_3	DISABLED	DISABLED	PTB7/ IRQ_3	TPM0_CH2	
3	—	—	—	PTA14	DISABLED	DISABLED	PTA14		TPM_CLKIN0
4	—	—	—	PTA15	DISABLED	DISABLED	PTA15		CLKOUT
5	3	3	3	VDD	VDD	VDD			
6	4	4	3	VREFH	VREFH	VREFH			
7	5	5	4	VREFL	VREFL	VREFL			
8	6	6	4	VSS	VSS	VSS			
9	7	7	5	PTA3	EXTAL0	EXTAL0	PTA3	I2C0_SCL	I2C0_SDA
10	8	8	6	PTA4/ LLWU_P0	XTAL0	XTAL0	PTA4/ LLWU_P0	I2C0_SDA	I2C0_SCL
11	—	—	—	VSS	VSS	VSS			
12	—	—	—	PTB18	DISABLED	DISABLED	PTB18		
13	—	—	—	PTB19	DISABLED	DISABLED	PTB19		
14	9	9	7	PTA5/ LLWU_P1/ RTC_CLK_IN	DISABLED	DISABLED	PTA5/ LLWU_P1/ RTC_CLK_IN	TPM0_CH5	SPI0_SS_b
15	10	10	8	PTA6/ LLWU_P2	DISABLED	DISABLED	PTA6/ LLWU_P2	TPM0_CH4	SPI0_MISO
16	11	11	—	PTB8	ADC0_SE11	ADC0_SE11	PTB8	TPM0_CH3	
17	12	12	—	PTB9	ADC0_SE10	ADC0_SE10	PTB9	TPM0_CH2	
18	—	—	—	PTA16/ IRQ_4	DISABLED	DISABLED	PTA16/ IRQ_4		
19	—	—	—	PTA17/ IRQ_5	DISABLED	DISABLED	PTA17/ IRQ_5		
20	—	—	—	PTA18/ IRQ_6	DISABLED	DISABLED	PTA18/ IRQ_6		
21	13	13	9	PTB10	ADC0_SE9/ TSIO_IN7	ADC0_SE9/ TSIO_IN7	PTB10	TPM0_CH1	
22	14	14	10	PTB11	ADC0_SE8/ TSIO_IN6	ADC0_SE8/ TSIO_IN6	PTB11	TPM0_CH0	
23	15	15	11	PTA7/ IRQ_7/ LLWU_P3	ADC0_SE7/ TSIO_IN5	ADC0_SE7/ TSIO_IN5	PTA7/ IRQ_7/ LLWU_P3	SPI0_MISO	SPI0_MOSI
24	16	16	12	PTB0/ IRQ_8/ LLWU_P4	ADC0_SE6/ TSIO_IN4	ADC0_SE6/ TSIO_IN4	PTB0/ IRQ_8/ LLWU_P4	EXTRG_IN	SPI0_SCK

## Pinout

48 LQFP	32 QFN	32 LQFP	24 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
25	17	17	13	PTB1/ IRQ_9	ADC0_SE5/ TSIO_IN3/ DAC0_OUT/ CMP0_IN3	ADC0_SE5/ TSIO_IN3/ DAC0_OUT/ CMP0_IN3	PTB1/ IRQ_9	UART0_TX	UART0_RX
26	18	18	14	PTB2/ IRQ_10/ LLWU_P5	ADC0_SE4/ TSIO_IN2	ADC0_SE4/ TSIO_IN2	PTB2/ IRQ_10/ LLWU_P5	UART0_RX	UART0_TX
27	19	19	15	PTA8	ADC0_SE3/ TSIO_IN1	ADC0_SE3/ TSIO_IN1	PTA8		
28	20	20	16	PTA9	ADC0_SE2/ TSIO_IN0	ADC0_SE2/ TSIO_IN0	PTA9		
29	—	—	—	PTB20	DISABLED	DISABLED	PTB20		
30	—	—	—	VSS	VSS	VSS			
31	—	—	—	VDD	VDD	VDD			
32	—	—	—	PTB14/ IRQ_11	DISABLED	DISABLED	PTB14/ IRQ_11	EXTRG_IN	
33	21	21	—	PTA10/ IRQ_12	DISABLED	TSIO_IN11	PTA10/ IRQ_12		
34	22	22	—	PTA11/ IRQ_13	DISABLED	TSIO_IN10	PTA11/ IRQ_13		
35	23	23	17	PTB3/ IRQ_14	DISABLED	DISABLED	PTB3/ IRQ_14	I2C0_SCL	UART0_TX
36	24	24	18	PTB4/ IRQ_15/ LLWU_P6	DISABLED	DISABLED	PTB4/ IRQ_15/ LLWU_P6	I2C0_SDA	UART0_RX
37	25	25	19	PTB5/ IRQ_16	NMI_b	ADC0_SE1/ CMP0_IN1	PTB5/ IRQ_16	TPM1_CH1	NMI_b
38	26	26	20	PTA12/ IRQ_17/ LPTMR0_ALT2	ADC0_SE0/ CMP0_IN0	ADC0_SE0/ CMP0_IN0	PTA12/ IRQ_17/ LPTMR0_ALT2	TPM1_CH0	TPM_CLKIN0
39	27	27	—	PTA13	TSIO_IN9	TSIO_IN9	PTA13		
40	28	28	—	PTB12	TSIO_IN8	TSIO_IN8	PTB12		
41	—	—	—	PTA19	DISABLED	DISABLED	PTA19		SPI0_SS_b
42	—	—	—	PTB15	DISABLED	DISABLED	PTB15	SPI0_MOSI	SPI0_MISO
43	—	—	—	PTB16	DISABLED	DISABLED	PTB16	SPI0_MISO	SPI0_MOSI
44	—	—	—	PTB17	DISABLED	DISABLED	PTB17	TPM_CLKIN1	SPI0_SCK
45	29	29	21	PTB13	ADC0_SE13	ADC0_SE13	PTB13	TPM1_CH1	RTC_CLKOUT
46	30	30	22	PTA0/ IRQ_0/ LLWU_P7	SWD_CLK	ADC0_SE12/ CMP0_IN2	PTA0/ IRQ_0/ LLWU_P7	TPM1_CH0	SWD_CLK
47	31	31	23	PTA1/ IRQ_1/ LPTMR0_ALT1	RESET_b	DISABLED	PTA1/ IRQ_1/ LPTMR0_ALT1	TPM_CLKIN0	RESET_b
48	32	32	24	PTA2	SWD_DIO	DISABLED	PTA2	CMP0_OUT	SWD_DIO

## 8.2 KL05 Pinouts

The below figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

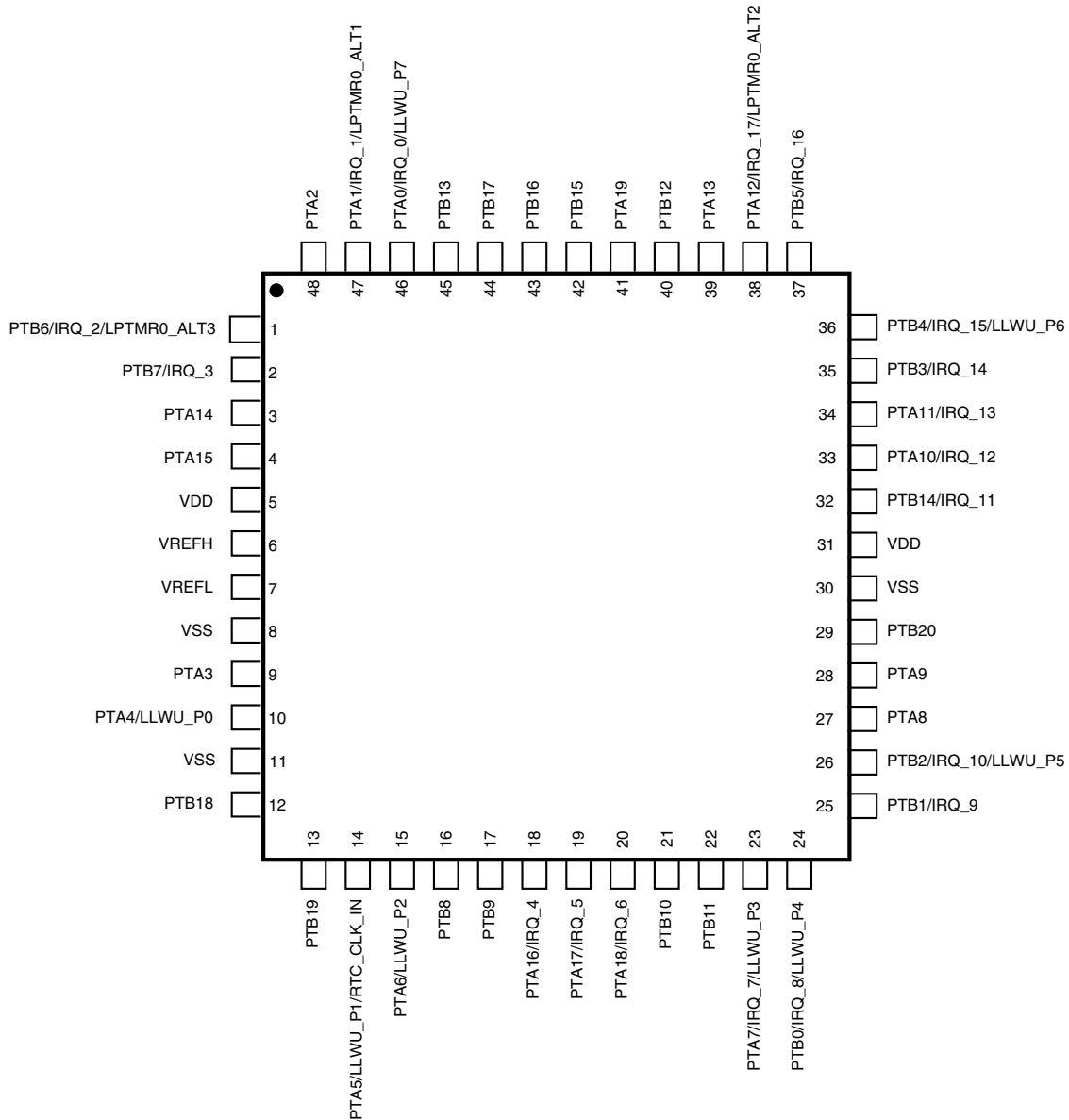


Figure 15. KL05 48-pin LQFP pinout diagram

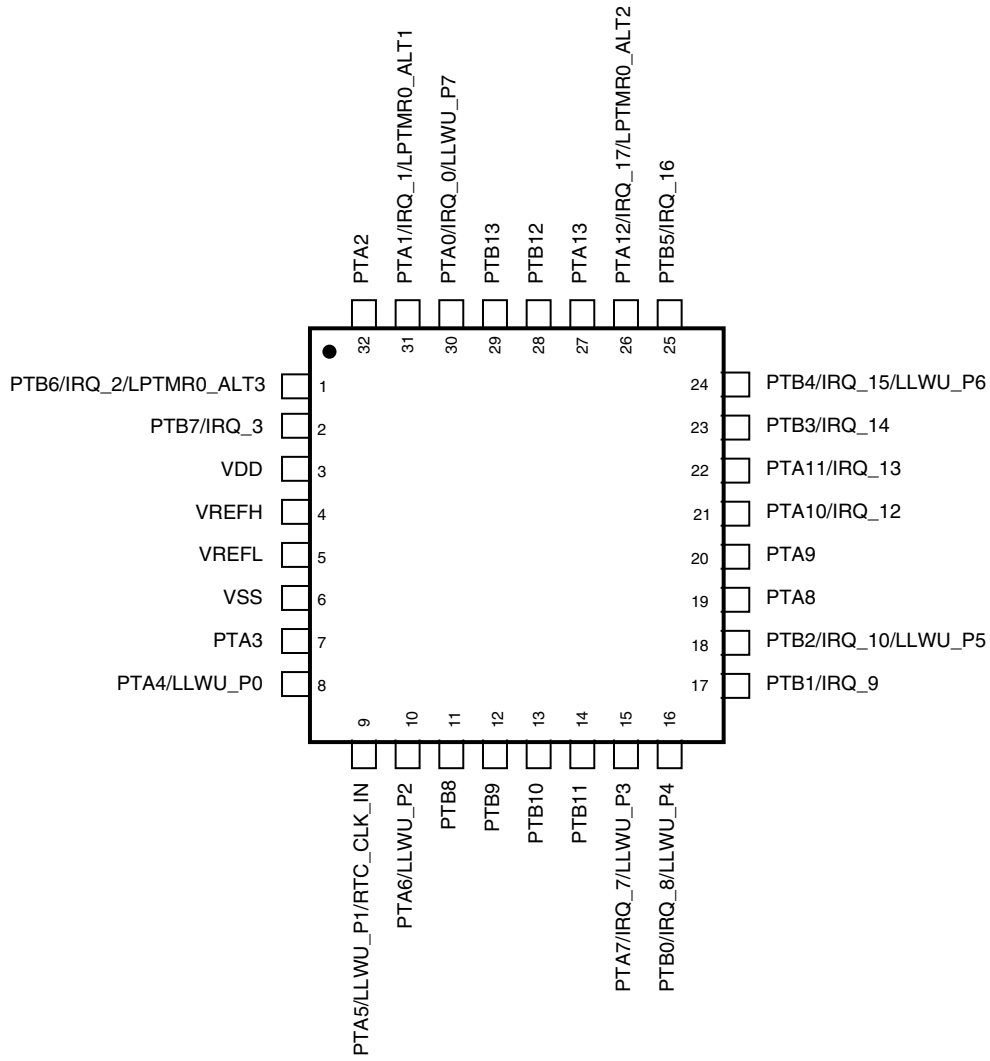


Figure 16. KL05 32-pin LQFP pinout diagram

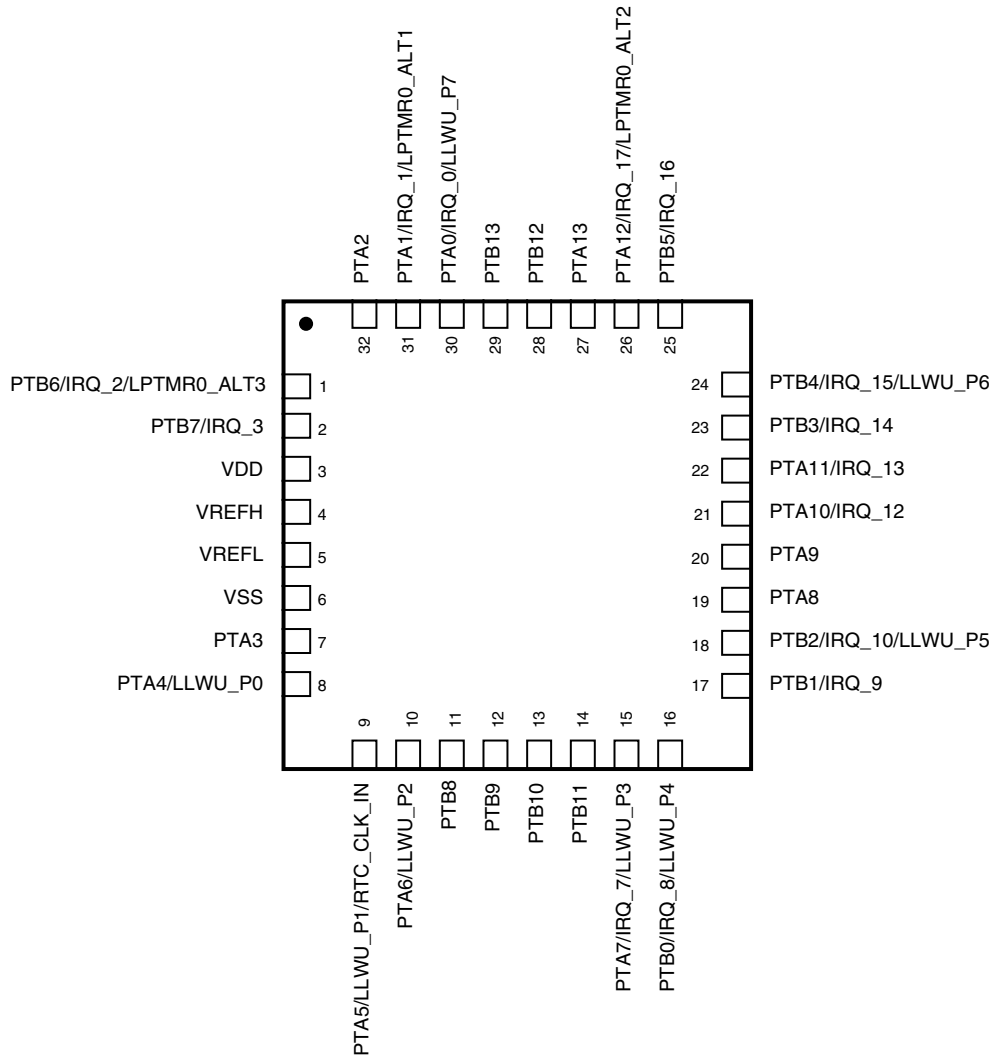


Figure 17. KL05 32-pin QFN pinout diagram

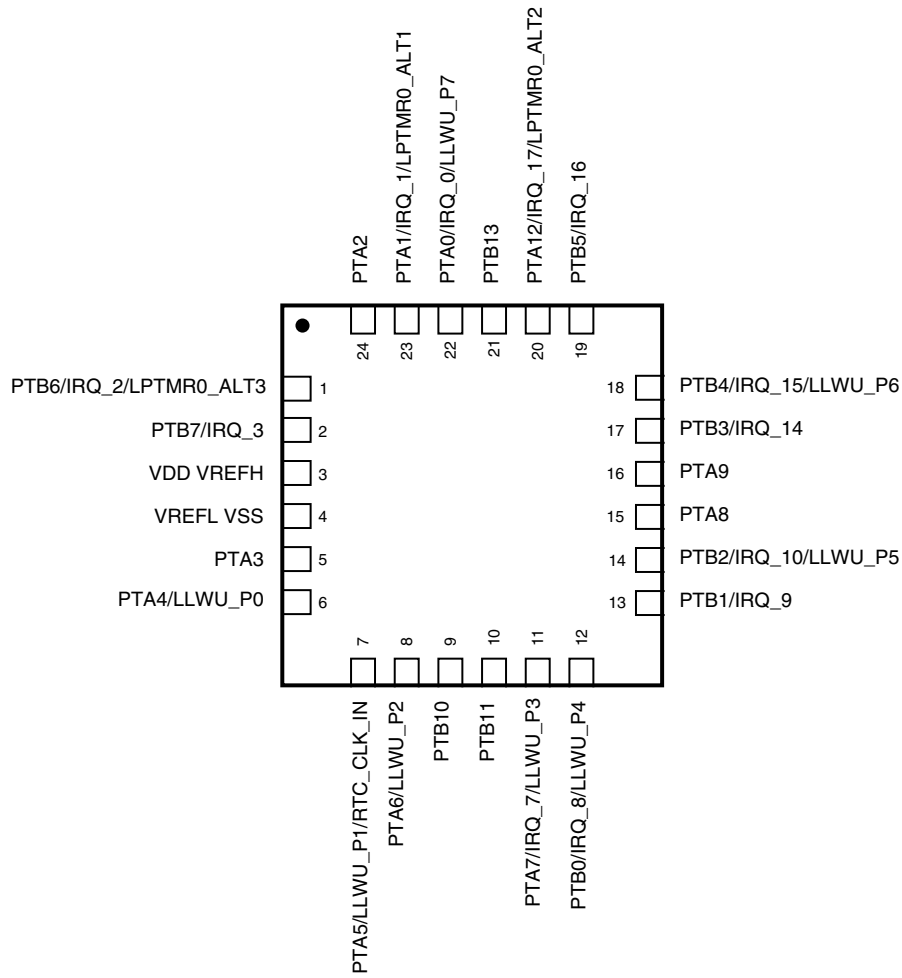


Figure 18. KL05 24-pin QFN pinout diagram

## 9 Revision History

The following table provides a revision history for this document.

Table 29. Revision History

Rev. No.	Date	Substantial Changes
1	7/2012	Initial NDA release.
2	9/2012	Initial public release.



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