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APPLICATION BULLETIN
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PROGRAMMING TRICKS FOR HIGHER CONVERSION SPEEDS UTILIZING DELTA SIGMA CONVERTERS

By Bonnie Baker

Delta-Sigma (ΔΣ) Analog-to-Digital Converters are well known for their innate ability to resolve an analog input signal to very small LSB voltage ranges. The primarily applications for this type of product is in the Industrial Process Control market such as direct transducer interface for pressure, temperature, flow, weigh scales and force measurement systems. In the Instrumentation market, the ΔΣ converter is particularly well-suited for portable applications, such as thermometers, gas analyzers and blood analyzers. At first glance, high resolution doesn't seem to be an important specification for these types of applications. To the contrary, close inspection of these transducer interface circuits divulge a different story. The sensing element's output could be a fairly high voltage (hundreds of mV to several volts), however, the delta output voltages that represent a change in temperature, pressure, light, etc., is usually extremely low, sub-mV or μV. If the dynamic resolution of the A/D converter is relatively high, the total application cost can be lowered. Additionally, the circuit becomes less complex making it easier to design. ΔΣ ADCs are very good in the right application but they do have some disadvantages. The most obvious of these is a limited frequency response. The frequency response is dictated by the output data rate. A greater data rate leads to a higher frequency response but lower effective resolution. Although the ΔΣ converter brings the circuit designer considerably closer to achieving the desired results, expanding the application to include μP implemented bit-shifting or front end analog gain techniques can enhance the resolution even further (refer to AB-107 for more details about front end analog gain). The technique of shifting the output bits of the A/D converter in the μP is not new, however, a revisit is appropriate in lieu of the arrival of the ΔΣ converter, where higher resolution is possible in the conversion process. This Application Bulletin addresses the design trade-off that is taken between resolution and data rates when ΔΣ converters are used. This relationship is examined and techniques such as hardware and software gain are used. These techniques can be used as tools to improve the resolution versus data rate picture. In this Application Bulletin the advantages of software gain emphasized.

The fundamental concept of the original ΔΣ A/D conversion process was based on a single-bit quantizer, rather than multi-bit, as used in architectures such as sub-ranging or successive approximation. Since the first design of the ΔΣ A/D converters front ends have been designed that digitize more than 1-bit of resolution, while tolerating some design trade-offs for the multi-bit approach. The state-of-the-art ΔΣ converter contains a programmable gain amplifier (PGA), a multi-order charge-balancing A/D converter, a calibration μC with on-chip static RAM, a clock oscillator, a programmable digital filter, and a bi-directional serial communications port. The function of the multi-order charge-balancing A/D converter can be conceptualized with the first-order stage shown in the insert in Figure 1. The analog input voltage and the output of the 1-bit DAC is differentiated, providing an analog voltage at X_2. The voltage at X_2 is presented to the integrator. The output of the integrator progresses in a negative or positive direction. The slope and direction of the signal at X_3 is dependant on the sign and magnitude of X_2. At the time the voltage at X_3 equals the comparator reference voltage, the output of the comparator switches from negative to positive or positive to negative, dependent on its original state. The output value of the comparator (X_4) is clocked into the 1-bit DAC, as well as clocked into the digital filter stage. At the time that the output of the comparator switches from a HIGH to a LOW or visa versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage to the difference amplifier. This creates a different output voltage at X_2, causing the integrator to progress in the opposite direction.

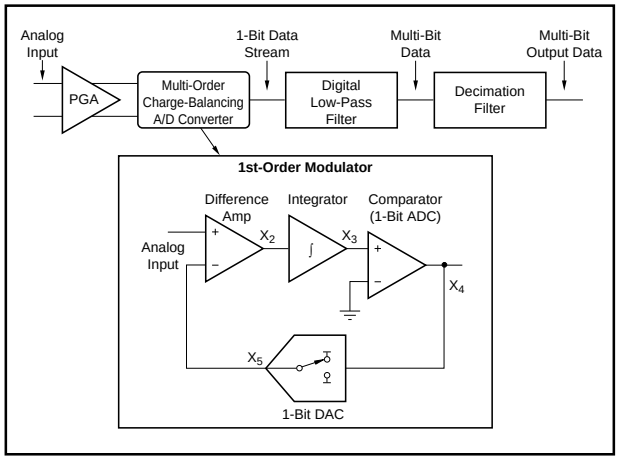

FIGURE 1. A Block Diagram of a Generic ΔΣ A/D Converter. Typically, this class of modulator has an input Programmable Gain Amplifier that conditions the analog input signal. The PGA stage is followed by the multi-order charge-balancing section which performs the first step in low frequency noise reduction and digitizes the signal into a stream of ones and zeros. This stage is followed by a digital low pass filter and finally, a decimation stage. The digital low-pass filter and decimation filter can be combined in some A/D converters, dependent on the design topology used.

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The output of the multi-order charge-balancing converter is a series of digital ones and zeros, which is sent to the digital filter. The digital filter uses an oversampling and averaging algorithm to further process the signal into the higher resolutions. The combination of the digital filter and the decimation filter stages directly affect the resolution and output data rate of the converter.

As mentioned, the output of the charge-balancing converter is a series of digital ones and zeros. The input of the digital filter clocks the charge-balancing converter output state (whether it is a one or zero) and stores the digital data in a FIFO register for further processing. The clock used at this point in the signal path is called the sampling clock. The ratio of the sampling clock and the system clock is typically equal to the oversampling rate divided by a constant particular to the A/D converter. In the case of the ADS1210 and ADS1211, the oversampling rate is also known as the Turbo rate and the A/D constant is 512.

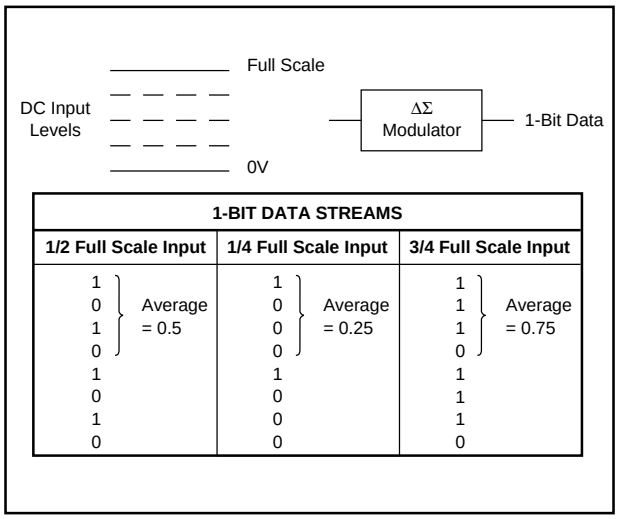
SIGNAL GAIN USING OVERSAMPLING METHODS

A key differentiation of these particular products from the competition is Burr-Brown's proprietary Turbo Mode of operation. In Turbo Mode, the user is allowed to select the oversampling ratio of the input charge-balancing converter. This input stage oversamples at 20kHz, allowing the ADS1210/11 to achieve 21.5 bits at 10Hz. A Turbo Mode 2 oversamples at 40kHz. The effective resolution with respect to frequency is shown in Table I. The benefit of the Turbo Mode function is high resolution at high data rates.

SAMPLE RATE	TURBO 1 (Bits rms)	TURBO 2 (Bits rms)	TURBO 4 (Bits rms)	TURBO 8 (Bits rms)	TURBO 16 (Bits rms)
10Hz	21.5	22	22.5	—	—
20Hz	21	22	22	22.5	—
40Hz	20	21.5	22	22.5	23
50Hz	20	21.5	21.5	22	23
60Hz	19.5	21	21.5	22	23
100Hz	18	20	21	21.5	22.5
1000Hz	10	12.5	15	17.5	20

TABLE I. The effective resolution of the ADS1210/1211 A/D converters is shown in this table. The clock rate for this data was 10MHz, and the number of bits is an rms value. The Turbo (or oversampling ratio) can be increased in order to increase the effective resolution or decreased to improve the sampling rate, which also increases the signal input bandwidth.

Both the digital filter and decimation filter utilize arithmetic tools to filter the digital information into a higher resolution. The most simplistic digital filter is the averaging filter. In this topology, a predetermined number of samples is required to compute the final value. The digital averaging filter waits for its FIFO register to fill with ones and zeros from the charge-balancing converter stage. When the register becomes full, the values in the register are averaged to arrive at the final output value. In order to see this action, consider a DC input level, such as shown in Figure 2. If the input to the ΔΣ charge-balancing converter is 1/2 full scale, the output of the charge-balancing converter would be a steady stream of alternating ones and zeros. Assuming the digital filter is designed to average four samples at a time, the average of four binary numbers resulting from a 1/2 FSR input would be 0.5. When the DC input is changed to 1/4 full scale, the resultant output of the ΔΣ charge-balancing converter would change to a string of the code 1000, as opposed to the previous 1010. The average value of the 1/4 full scale code representation would be 0.25. In this example, four samples of the 1-bit data is averaged, but in fact, any number of samples could be chosen. Accuracy increases with number of samples that are averaged, however, the trade-off for higher accuracy is increased conversion time. This simplistic digital filter can be further enhanced with a rolling average filter or a variety of more sophisticated filters. An in depth discussion of digital filtering can be found in AB-108.



1-BIT DATA STREAMS		
1/2 Full Scale Input	1/4 Full Scale Input	3/4 Full Scale Input
1 } Average = 0.5	1 } Average = 0.25	1 } Average = 0.75
0	0	1
1	0	1
0	0	0
1	1	1
0	0	1
1	0	1
0	0	0

FIGURE 2. This is an illustration of the simplest digital filter, an averaging system. In this filter, the analog signal is clocked into the filter as a series of representative ones and zeros. This example illustrates a 4X averaging filter, where four digits are taken and averaged, giving an overall higher resolution than the original one-bit system. This filter provides a sin(x)/x transfer function which can be used to effectively eliminate line frequency. Although this filter accomplished the task of increasing resolution, it also requires more time than the FIR or IIR style digital filter.

Oversampling, in conjunction with digital filtering, is a technique that is used to achieve increased gain on the analog input signal. For example, a 12-bit A/D converter with a full scale range of 1V would be able to resolve to an LSB of 244μV. If the analog signal were gained with an external gain stage by 4V/V, the output of the 12-bit A/D converter would be able to resolve to a system LSB of 61μV. With an oversampling system, the Signal-to-Noise Ratio

(SNR) is improved as oversampling increases. For an oversampling factor of 4 increase, the conversion process will have a theoretical 6dB or 1-bit improvement in the SNR. Consequently, an oversampling system from 1X to 16X is equivalent to applying a gain of 4 in that the LSB size has changed from 244μV, for that 12-bit A/D converter, to 61μV.

SIGNAL GAIN USING ON-CHIP PGA FUNCTION

The functional elements of a typical ΔΣ A/D converter, such as the ADS1210 and ADS1211, is shown in Figure 3. The input to these converters is differential allowing for the rejection of common-mode voltages. To enhance the accuracy/resolution capability of this type of capability of this

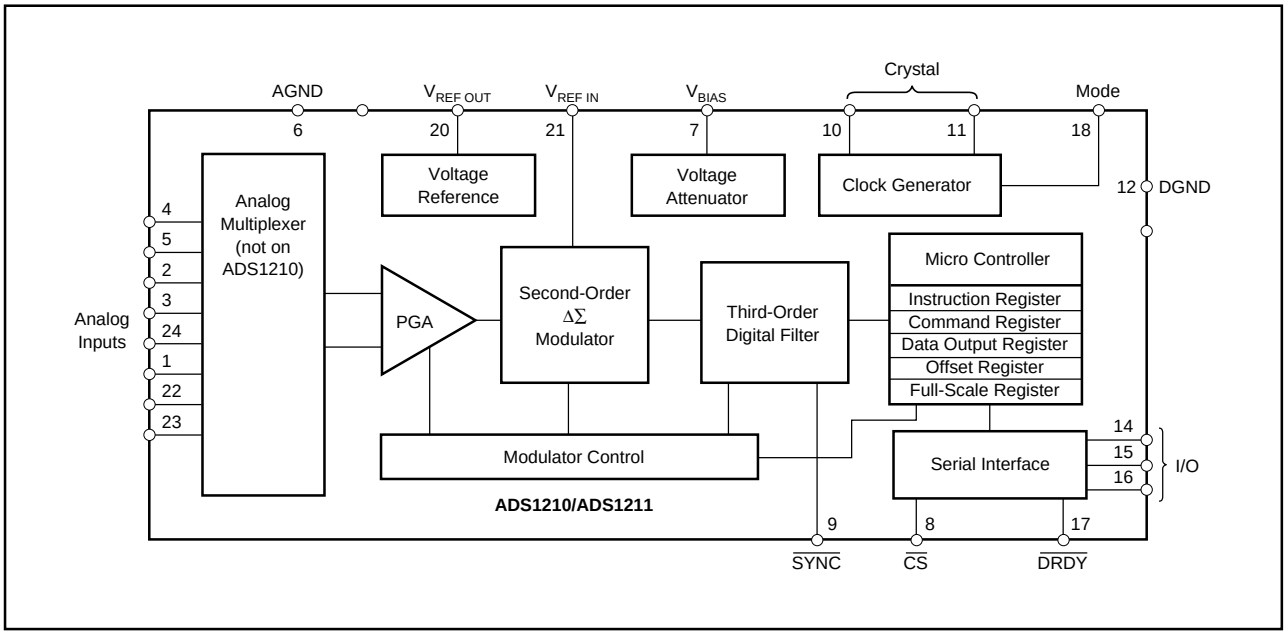


FIGURE 3. Burr-Brown's ADS1210 and ADS1211 are 24-bit, ΔΣ converters which operate from a single 5V supply. The ADS1211 has an input multiplexer to accommodate four differential input sources where the ADS1210 has one differential input. Both have on-chip μC functions such as calibration capability and oversampling. Both converters are easily interfaced with three- or four-wire controllers.

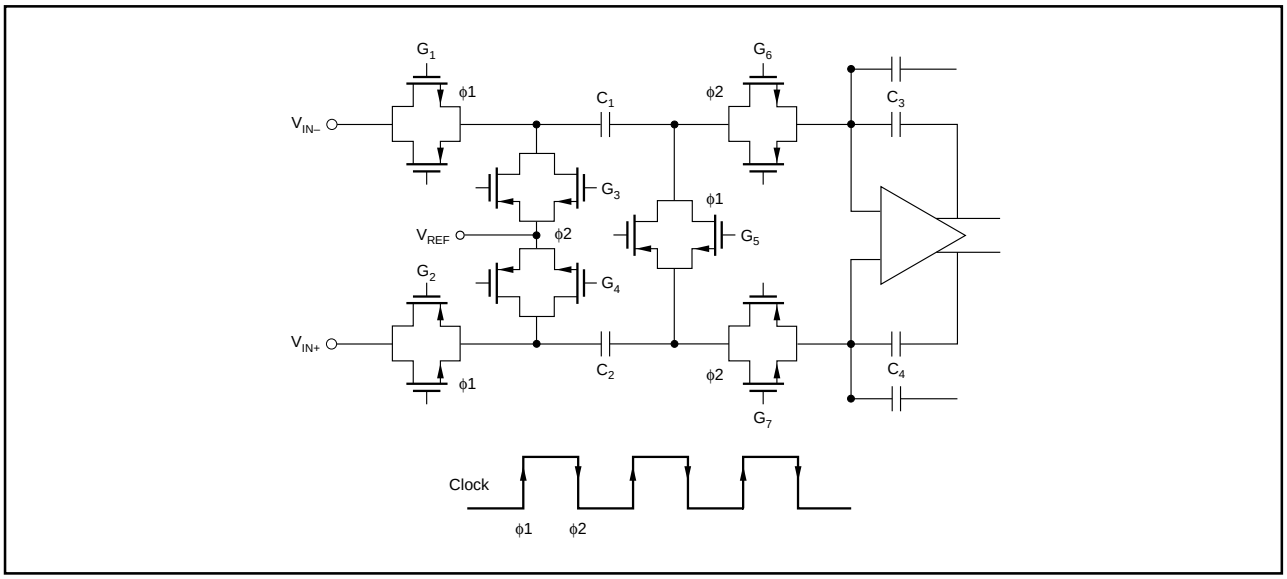


FIGURE 4. The input stage for the ADS1210/1211 uses a switched capacitor topology to sample the signal as well as a perform gain function.

type of converter, the system offsets, as well as the full scale range can be calibrated to desired levels. This is done by using the on-chip μC. The ΔΣ converter, such as the ADS1210 or ADS1211 are precision, wide dynamic range, 24-bit, A/D converters operating from a single +5V supply. The ADS1210 is a single channel A/D converter and the ADS1211 is a 4-channel multiplexed version of the ADS1210. These products offer 3-wire serial interface capability, a command structure and register set to interface to all of the popular microprocessors. Additionally, the differential inputs are useful when a direct connection to transducers is required.

The differential input is gained by the PGA (Programmable Gain Amplifier) stage by a factor of 1, 2, 4, 8 or 16. The basic topology of the PGA stage is a differential switched capacitor amplifier (Figure 4). The switched capacitive topology uses a combination oversampling and capacitor gain to achieve the possible gains of 1, 2, 4, 8, and 16. A simplistic way of looking at the PGA stage is shown in Figure 4. The signal is clocked in on the rising edge of the sampling clock and transferred by the falling edge of the sampling clock to a second group of capacitors. For a PGA gain of one, the next rising clock edge sends the first signal forward to the modulator section of the A/D converter as well as sampling a second input signal. For PGA gains greater than one, say a gain of two, the second rising clock edge does not send the signal forward to the modulator section. The second stage of the PGA retains the original signal and adds it to the second sampled input. In this manner the charge is doubled. At the completion of the second sampling the charge is finally transferred to the modulator section. This concept can easily be extended to gains of 4, 8 and 16. As the gain of the PGA stage increases the number of cycles required to sample the signal also increases.

Maximum Sampling Clock Available	ALLOWABLE PGA GAIN RANGES	TURBO MODE RATE	MODULATOR FREQUENCY
320kHz (10MHz External Clock)	16	1	20kHz
	8	2	40kHz
	4	4	80kHz
	2	8	160kHz
	1	16	320kHz

TABLE II. ADS1210, ΔΣ A/D Converter Gain versus Turbo Mode Trade Off.

Assuming the external clock is a constant of 10MHz, the PGA gain is implemented by increasing the number of samples taken by the input capacitor from 20kHz, for a gain of 1, to 320kHz for a gain of 16. Since the Turbo and PGA functions are both implemented by varying the sampling frequency of either the input capacitors or the modulator output, the multiple of PGA gain and Turbo mode rate is limited to 16. Adjusting the internal gain stage of the ΔΣ converter is yet another technique used in providing appropriate LSB voltage size for the transducer application.

SOFTWARE GAIN

The specifications of the ADS1210 converter performance is similar to other converters on the market, such as Analog Device's AD7712. A comparison of specifications of the ADS1210 and the AD7712 are shown in Table III, but this only shows part of the picture. The ADI product and Burr-Brown's ADS1210 are programmable for both data rate and gain. However, the ADI part is limited in not being able to program its oversampling rate so as the data rate increases, the effective resolution decreases. The ADS1210/11 on the other hand offers Turbo Mode and PGA gain which allows the freedom of programming both the data rate and the effective resolution.

SPECIFICATIONS	ADS1210U	AD7712AR	UNITS
Number of Channels	1	1	
Resolution	24	24	Bits
Full Scale Voltage	10	10	Vp-p
Internal Reference Voltage	2.5	2.5	V
Relative Accuracy	0.0015	0.0015	%
No Missing Codes	24	24	Bits
CMR at 60Hz	100	120	dB
Power CLK = 10MHz	26	30	mW
Resolution at 1kHz Sampling	20	13.5	Bits

TABLE III. Specification comparison of ADS1210 versus AD7712. Both devices are high resolution, ΔΣ A/D Connectors.

The easiest way of showing the advantages of the ADS1210/11 are in charts of effective resolution versus data rate. In Table IV the ADS1210/11 and the AD7712 are shown with various gains against the effective input range and resolution.

The Burr-Brown part focuses on providing a higher resolution at a higher sampling rate rather than gain functionality. At first glance, the specified gain capability of 1, 2, 4, 8, ... 128 of the AD7712 seems fairly impressive. However, once the converter is programmed beyond a gain of 8, the subsequent increases in gain are performed by shifting the data within the registers of the A/D converter. This technique is used by software engineers and typically known as data shifting. By hardware or software data shifting, the dynamic range of the part is not increased but kept constant. Instead, the relative weighting of the data bit is being decreased or in terms of gain—an increase in gain. The same thought process was used with the ADS1210 and ADS1211 but instead of being done in hardware and sacrificing higher effective resolutions, the data shifting techniques were left to the software designer. For example, in Table IV, the LSB weight of the AD7712 for the gains between 4 and 128 is 0.6mV. It is easy to see that as the gain increases AD7712, the effective resolution drops by one bit for every 2X increase in gain. Consequently, for a gain of 128 the effective resolution is 16 bits.

In contrast, the Burr-Brown ADS1210 and ADS1211 leaves the data shifting task to the software designer. With the assumption that the software designer can easily implement this solution to increasing the overall gain of the system, the ADS1210 and ADS1211 are designed to optimize the converter function to achieve the lowest possible LSB voltage. In Table IV, the ADS1210/11 are shown in a Turbo mode of 1 and 2. When the converter is in a Turbo mode of 1 and a PGA gain of 16, the devices surpasses the effective resolution of the AD7712 by four times. In a Turbo mode of 2 and a gain of 8, 22.5-bit resolution is achieved. Implementing software data shifting techniques, and effective gain of 128 can be achieved by combining A/D converter gain shifting techniques, and effective gain of 128 can be achieved by combining A/D converter gain and software bit-shifting. The equivalent full scale voltage of 4.88mV is achieved with the ADS1210 as compared to the AD7712 (Analog Devices) 39mV full scale range.

In your application, four methods of signal gain are possible with the Burr-Brown ADS1210 and ADS1211 ΔΣ converter product line. Two of the methods involve internal gain using the sampling clock to either employ PGA gain on the front end or oversampling after the modulator. The other two methods require external intervention, namely software gain or an input analog gain stage. This Application Bulletin has focused on the fundamental techniques behind software gain. Generally speaking, a combination of PGA and oversampling should be implemented as a first pass attempt to improve the system resolution. If additional gain is required, either software gain of external analog gain are viable options. The software gaining technique is a low cost approach, but the trade-off is increased μC overhead time.

PRODUCT	GAIN	INPUT	EFF RES.	MSB DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	LSB DB0
AD7712	1	5V	21.5	2.5	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	X	X	X
	2	2.5V	21.5	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	X	X	X
	4	1.25V	21.5	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X
	8	.625V	20.5	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X	X
	16	.3125V	19.5	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X	X	X
	32	.15625V	18.5	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X	X	X	X
	64	.078125V	17.5	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X	X	X	X	X
	128	.039V	16.5	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X	X	X	X	X	X	X
ADS1210/11 Turbo 1	1	5V	22	2.5	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	X	X
	2	2.5V	22	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X	X
	4	1.25V	22	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	X	X
	8	.625V	22	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	X	X
	16	.3125V	21	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	X	X	X
ADS1210/11 Turbo 2	1	5V	23	2.5	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	X
	2	2.5V	23	1.25	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	X
	4	1.25V	23	0.625	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	X
	8	.625V	23	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X
	SW Gain 2 X Gain 8 = 16	Equivalent FS 0.3125V	22	0.3125	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X
	SW Gain 4 X Gain 8 = 32	Equivalent FS 0.1562V	21	0.156	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X	
	SW Gain 8 X Gain 8 = 64	Equivalent FS 0.07812SV	20	0.078	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X	X	
	SW Gain 16 X Gain 8 = 128	Equivalent FS 0.039V	19	0.039	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X	X	X	
	SW Gain 32 X Gain 8 = 256	Equivalent FS 0.0195V	18	0.0195	0.009	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.00000015	0.00000007	X	X	X	X	
	SW Gain 64 X Gain 8 = 512	Equivalent FS 0.00976V	17	0.0048	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.0000015	0.00000007	X	X	X	X	X	X	
	SW Gain 128 X Gain 8 = 1024	Equivalent FS 0.00488V	16	0.0024	0.0012	0.0006	0.0003	0.00015	0.000076	0.000038	0.000019	0.000009	0.0000048	0.0000024	0.0000012	0.0000006	0.0000003	0.0000015	0.00000007	X	X	X	X	X	X	X	

TABLE IV. Competitive Analysis—Effective Resolution + Bit Weighting vs Gain.