BURR-BROWN® APPLICATION BULLETIN
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BURR-BROWN SPICE BASED MACROMODELS, REV. F

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INTRODUCTION

Computer based simulation has an importance because it can significantly reduce the development time and therefore speed up the time-to-market process. The increased use of SPICE based simulation software has created a rising demand for accurate models. Such models, or macromodels, should reflect the actual performance of the component, but without carrying the burden of too many circuit details, which can lead to convergence problems. BURR-BROWN has responded to this need and provides macromodels for a broad range of semiconductor products. This Application Bulletin, and the accompanying disk is a collection of SPICE models of BURR-BROWN op amps, difference amps, instrumentation amps, isolation amps, and analog function circuits. There are four different levels of model topologies used, which are:

Level I: Standard Macromodel

Level II: Enhanced Macromodel

Level III: Multi-Pole/Zero Macromodel

Level IV: Simplified Circuit Model

• The standard op amp macromodels were derived using the MicroSim Corporation PSpice® Parts™ simulation software. A detailed description on this macromodel type is given in Section A.

• The second level of macromodel is an enhanced version of the standard model, which is indicated by the suffix "E" in the model's name. This model type is included to offer the circuit designer a model with a higher level of accuracy. See Section B for details.

• The Multiple-Pole/Zero macromodel uses the same input stage as the standard or enhanced op amp macromodel, but has multiple poles and pole/zero pairs in the mid-section. This model has the designation "M", and was used for wide bandwidth op amps and function circuits where this topology showed an advantage over the standard topology. For a detailed description see Section C.

• In some instances, a fourth type of model is available, which are designated by either an "X", "X1", or an "X2" suffix. The model of this level is not a macromodel, but rather a simplified circuit model at the transistor level. The simplified circuit models produce the most accurate simulation results, but because of the complexity, require longer simulation time. See Section D for a detailed discussion on these models.

For a complete overview of all available macromodels on the disk see Table XI on the last page.

DISKETTE INFORMATION

The disk has four different subdirectories, in which the models are organized according to their topology level:

```
A:\
├-- CIR_MOD
├-- ENH_MOD
├-- MPZ_MOD
├-- STD_MOD
```

Here, the Standard macromodels (Level I) are found in the STD_MOD subdirectory. The Enhanced macromodels (Level II) are found in the ENH_MOD subdirectory. The Multi-Pole/Zero macromodels (Level III) are found in the MPZ_MOD subdirectory, and the Simplified circuit models (Level IV) are found in the CIR_MOD subdirectory. Examples of model files are shown in Table I. This application bulletin and the macromodel disk are being revised frequently. To obtain the latest revision please contact your nearest sales office. Each model net-list starts with a header containing the part number, revision information, and the license statement. It should be noted that the disk contains only the net-lists of the macromodels, and does not provide the simulation software that allows the user to run the models. The structure of the net-lists conforms to the standard SPICE format, which most SPICE based simulators will accept. Please refer to the individual software manual if conflicts are encountered. Burr-Brown also welcomes any comments, which may be sent to the Applications Department at the address given above.

FILE NAME	DESCRIPTION
OPA111.MOD	OPA111 Standard Op Amp Macromodel
OPA111E.MOD	OPA111 Enhanced Op Amp Macromodel
OPA671M.MOD	OPA671 Multiple Pole/Zero Macromodel
OPA603X.MOD	OPA603 Simplified Circuit Model

TABLE I. Examples of Files on Macromodel Disk.

PSpice® Parts™, MicroSim Corp.

GENERAL INFORMATION

Throughout this application bulletin and the net-lists of the macromodels, standard definitions and designators are used. As a reference they are listed in the following tables. Table II and Table III specifically refer to the Standard and the Enhanced macromodel only. Listed in Table IV are the definitions for all used component prefixes.

COMPONENT	DESCRIPTION
C_1	Phase-Control Capacitor
C_2	Compensation Capacitor
C_{EE}, C_{SS}	Slew-Rate Limiting Capacitor
D_P	Substrate Junction
E_{GND}	Voltage-Controlled Voltage Source
F_B	Output Device (Controlled by the Current Through V_B, V_C, V_E, and V_{LP}, V_{LN})
G_{11},G_{21}	Input Bias Current Correction
G_A	Interstage Transconductance (Controlled by Differential Voltage at the Input Device Loads)
G_{CM}	Common-Mode Transconductance (Controlled by the Common-Mode Voltage at the Input Device Emitters or Sources)
I_{EE}, I_{SS}	Input Stage Current
H_{LIM}	Voltage-Limiting Device
J_1, J_2	JFET Input Transistors
Q_1, Q_2	Bipolar Input Transistors
R_2	Interstage Resistance
R_{C1}, R_{C2}	Input-Stage Load Resistance
R_{D1}, R_{D2}	Input-Stage Load Resistance
R_{E1}, R_{E2}	Input-Stage Emitter Resistance
R_{EE}, R_{SS}	Input-Stage Current-Source Output Resistance
R_{O1}, R_{O2}	Output Resistors
R_P	Power Dissipation Resistor
V_B	Independent Voltage Source
V_C, D_C	Output Offset Limiter (to V+)
V_E, D_E	Output Offset Limiter (to V–)
V_{LIM}	Output Current Limiting Sensor
V_{LN}, D_{LN}	Negative Supply Limit
V_{LP}, D_{LP}	Positive Supply Limit

TABLE II. Op Amp Macromodel Components for the Standard and Enhanced Macromodels.

BURR-BROWN SYMBOL	MACROMODEL DESIGNATION	DEFINITION
V+, V–	$+V_{PWR}$, $-V_{PWR}$	Positive, Negative Power Supply
	$+V_{OUT}$, $-V_{OUT}$	Max Positive, Negative Output Swing
SR_+	+SR	Positive-Going Slew Rate
SR_-	–SR	Negative-Going Slew Rate
	Pd	Quiescent Power Dissipation
I_B	I_B	Input Bias Current
A_{OL}	Av–dc	DC Open-Loop Voltage Gain
UGBW	F–0dB	Unity-Gain Frequency
CMRR	CMRR	Common-Mode Rejection Ratio
$ø_M$	Phi	Phase Margin at F-0dB (°)
r_O	Ro-dc	DC Output Resistance
z_O	Ro-ac	AC Output Resistance
I_{SC}	Ios	Short-Circuit Output Current
C_C	Cc	Compensation Capacitance

TABLE III. PSpice Parts Inputs for Standard and Enhanced Marcomodels.

PREFIX	DEFINITION
C	Capacitor
D	Diode
E	Voltage-Controlled Voltage Source
F	Current-Controlled Current Source
G	Voltage-Controlled Current Source
H	Current-Controlled Voltage Source
I	Independent Current Source or Stimulus
J	JFET Transistor
Q	Bipolar Transistor
R	Resistor
S	Voltage-Controlled Switch
V	Independent Voltage Source or Stimulus

TABLE IV. Macromodel Component Prefix Definitions.

LIMITATIONS

These macromodels are intended to help designers simulate typical amplifier performance. The macromodels were compiled using data sheet typical specifications. Where data sheet specifications were not available, typical measured values or design values were used. Macromodels were verified with several standard simulations such as gain-phase and large- and small-signal transient response. In some cases, adjustments were made to the macromodels so simulations with the macromodel more closely agreed with actual measured typical performance.

Since these macromodels only simulate the typical performance of certain selected specifications, they will not predict actual device performance under all conditions. Good design practice dictates that, in addition to simulation with macromodels, circuit verification must include:

1) worst case analysis with data sheet minimum and maximum room temperature specifications
2) worst case analysis with variation of specifications over the operating temperature range
3) thorough breadboard evaluation
4) complete prototype characterization

DUAL AND QUAD OP AMPS

All op amps are modeled as single devices. To model duals or quads, use two or four models. Quiescent current for the dual or quad op amp macromodel is the dual or quad op amp quiescent current divided by two or four.

INSTRUMENTATION AMPLIFIERS AND DIFFERENCE AMPLIFIERS

Instrumentation amplifier and difference amplifier macromodels use standard op amp macromodels plus additional components as shown in Figures 1 and 2. There are two types of models used for difference amplifiers. They are the four-resistor difference amplifier and the five-resistor difference amplifier.

FOUR-RESISTOR DIFFERENCE AMPLIFIER

The four-resistor difference amplifier macromodel, used for the INA105, INA106, and the difference amplifier section in all instrumentation amplifier macromodels, is shown in

Figure 1a. The circuit uses an op amp and four matched resistors. If $R_2/R_1 = R_4/R_3$, GAIN = R_2/R_1 and CMR = ∞. To simulate DC CMR error, R_2 is set 0.01% low. CMR for a four resistor difference amplifier is:

$$CMR = -20\ LOG10\ [(\%/100) \bullet R_1/(R_1 + R_2)]$$

Where:

% = % error in any resistor.

With a 0.01% resistor error, DC CMR for the INA105 unity gain difference amplifier is 86dB, and DC CMR for the INA106 gain-of-ten difference amplifier is 100.8dB.

To simulate AC CMR error, a small value capacitor, C_2, is placed in parallel with R_2 to roll-off of CMR with increasing frequency.

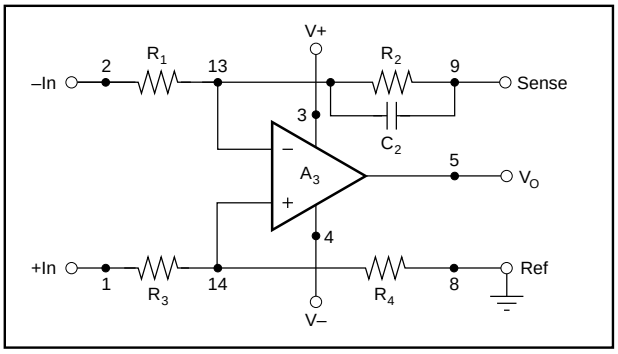


FIGURE 1a. Difference Amp Macromodel and Node Assignments.

FIVE-RESISTOR DIFFERENCE AMPLIFIER

The five-resistor difference amplifier macromodel used for the INA117 is shown in Figure 4b. The advantage of the five-resistor difference amplifier configuration is a boost in input common-mode-voltage range for a given op amp common-mode range. The circuit uses an op amp and five matched resistors. If $(R_2 \parallel R_5)/R_1 = R_4/R_3$, GAIN = R_2/R_1 and CMR = ∞. To simulate DC CMR error, R_4 is set 0.005% low. For errors in R_4, the CMR for a five-resistor difference amplifier is;

$$CMR = -20\ LOG10\ [(\%/100) \bullet R_1/(R_1 + R_4)]$$

Where:

% = % error in R_4

$R_2 \parallel R_5 = R_2 \bullet R_5/(R_2 + R_5)$

With a 0.005% resistor error, DC CMR for the INA117 high common-mode-voltage unity-gain difference amplifier is 86.5dB. Note that unlike the four resistor difference amplifier, the sensitivity of DC CMR to errors in resistor value is different for different resistors.

To simulate AC CMR error, a small value capacitor, C_2, is placed in parallel with R_2 to roll-off of CMR with increasing frequency.

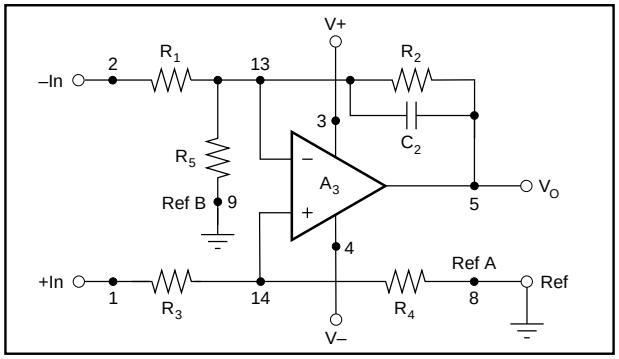


FIGURE 1b. INA117 High Voltage Difference Amplifier Macromodel and Node Assignments.

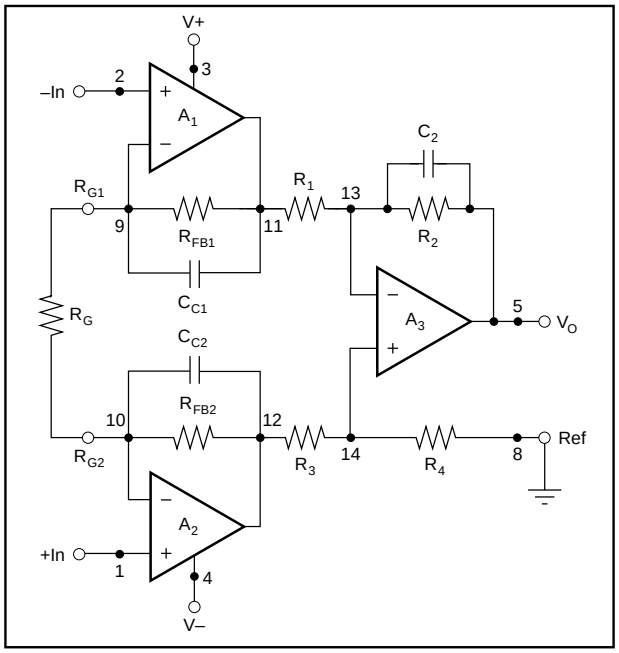


FIGURE 2. Standard Instrumentation Amplifier Macromodel and Node Assignments.

FIGURE	DESCRIPTION
1a	Difference Amp Macromodel Node Assignments
1b	INA117 Difference Amplifier Macromodel
2	Instrumentation Amp Macromodel Node Assignments
3	INA103 Macromodel and Node Assignments
4	INA118 Macromodel and Node Assignments
5	INA110 Macromodel and Node Assignments
6	INA120 Internal Gain Setting Resistor Connections

TABLE V. Figure Reference.

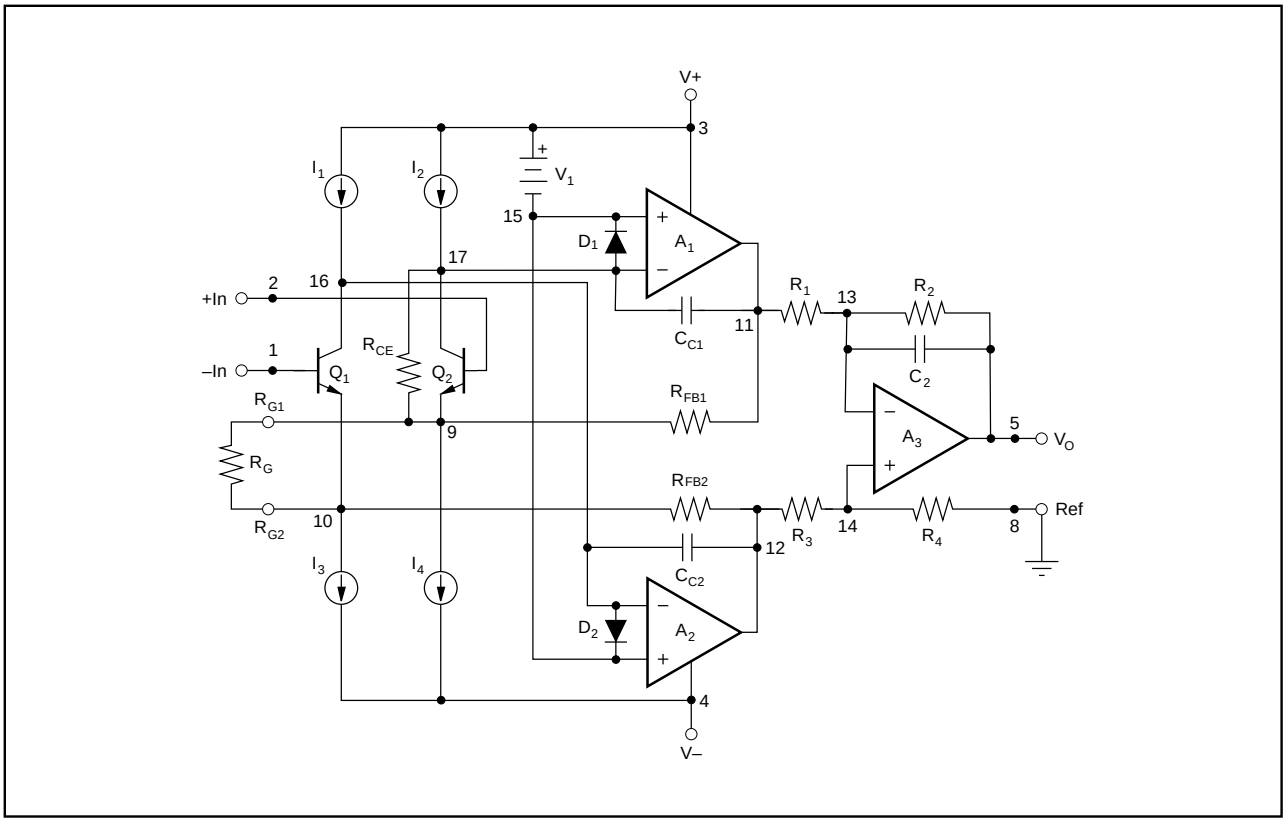


FIGURE 3. INA103 Current-Feedback Instrumentation Amplifier Macromodel and Node Assignments.

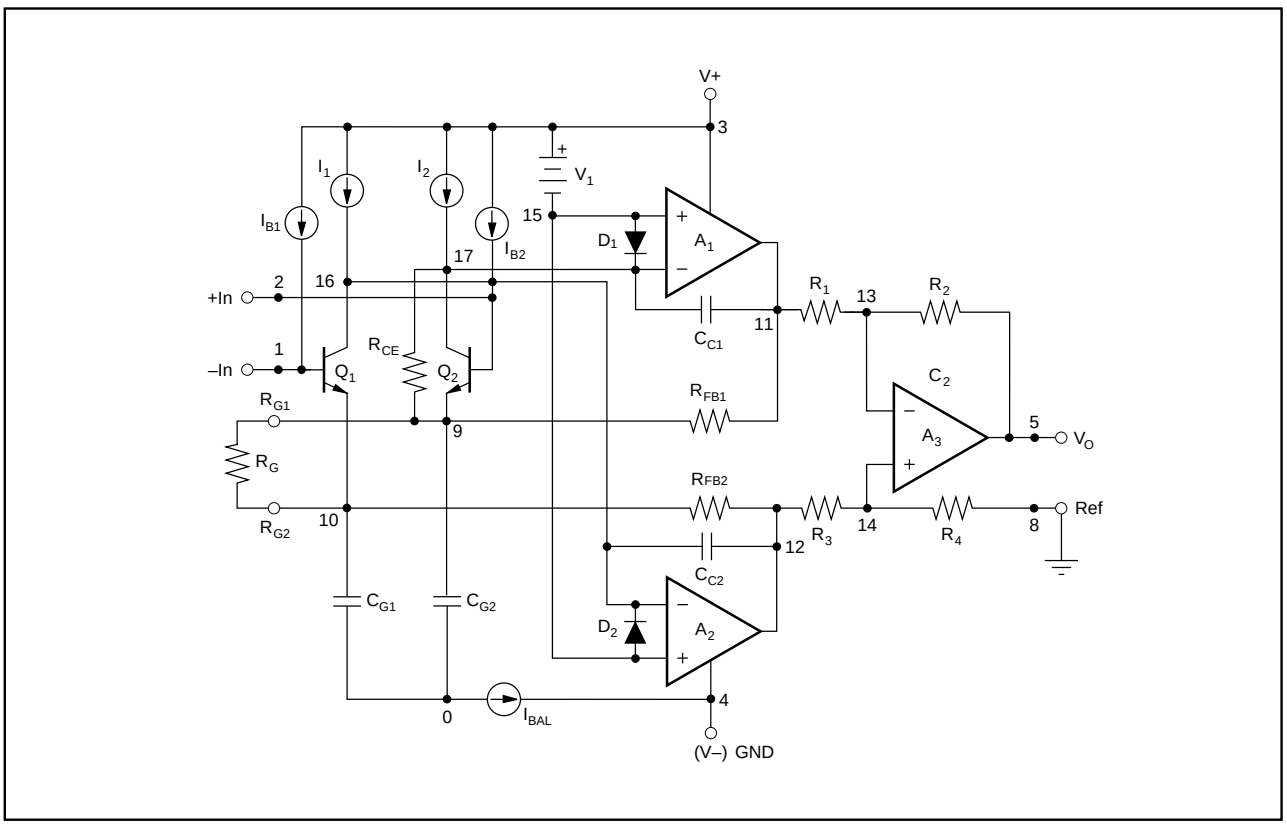


FIGURE 4. INA118 Instrumentation Amplifier Macromodel and Node Assignments.

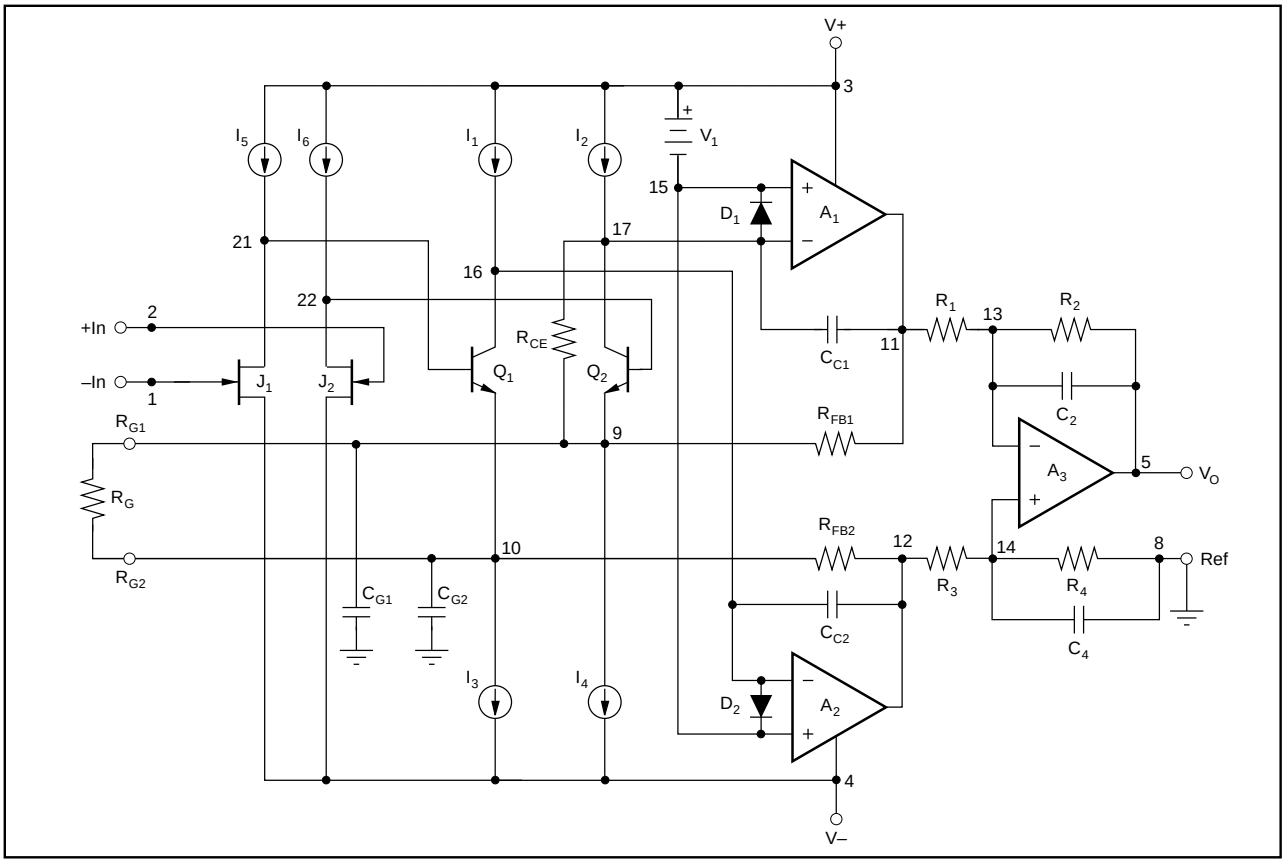


FIGURE 5. INA110 Current-Feedback FET-Input Instrumentation Amplifier Macromodel and Node Assignments.

INA120 INTERNAL GAIN CONNECTIONS[1]

GAIN	CONNECT		
1	G4-G5	G14-G15	
10	G4-G5	G11-G14-G15	
100	G4-G8	G11-G14	G10-G15
1000	G4-G8	G11-G14	G9-G15

NOTE: (1) "G" numbers are also package pin numbers.

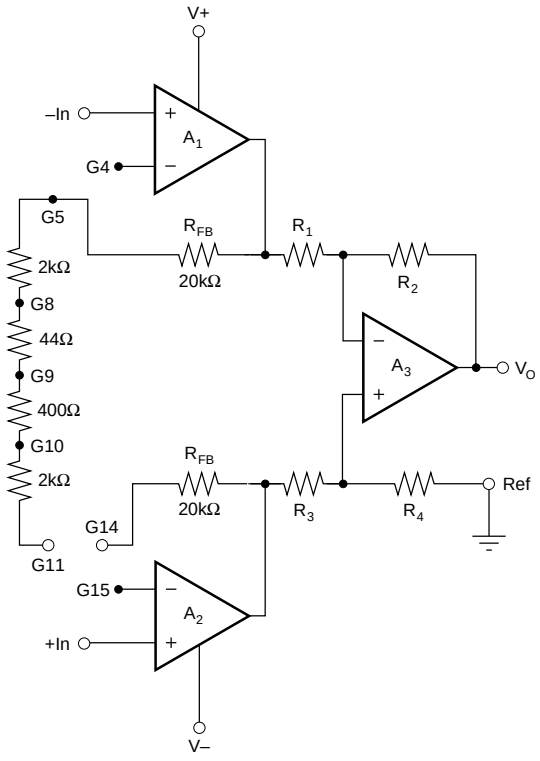


FIGURE 6. INA120 Internal Gain-Setting Resistor Connections.

SECTION A:
STANDARD MACROMODELS

The standard op amp macromodels were created by running the PSpice® Parts™ Simulation software on an IBM-compatible PC. This software uses the standard Boyle op amp model(1). The PSpice manual available from Microsim(2) contains a detailed discussion of each of the elements used in the macromodels.

Op amp macromodels use the node assignments shown in Figures A1 to A6. The FET-input amplifiers using the standard PSpice Parts topology are shown in Figures A3 and A4.

The node assignments for the standard PSpice Part op amp macromodels with bipolar-inputs are shown in Figures A5 and A6. Figure A1 shows the external op amp node assignments. Tables II, III and IV list component prefix designations, macromodel component descriptions, and PSpice INPUT designations used for the standard and enhanced models. The parameters that are modelled by the standard macromodels are listed in Table X.

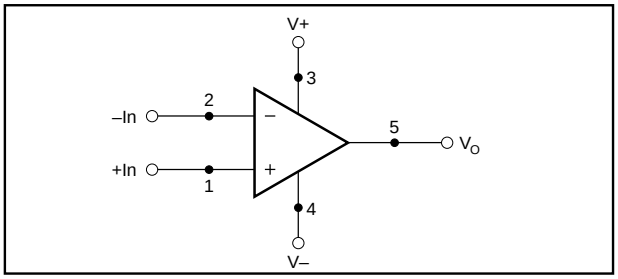


FIGURE A1. Node Assignments for Standard and Enhanced Op Amp Macromodels.

FIGURE	DESCRIPTION
A1	Op Amp Node Assignments
A2	OPTxxx Node Assignments
A3	N-Channel JFET-Input Op Amp
A4	P-Channel JFET-Input Op Amp
A5	NPN Bipolar-Input Op Amp
A6	PNP Bipolar-Input Op Amp

TABLE VI. Standard Macromodels Figure Reference.

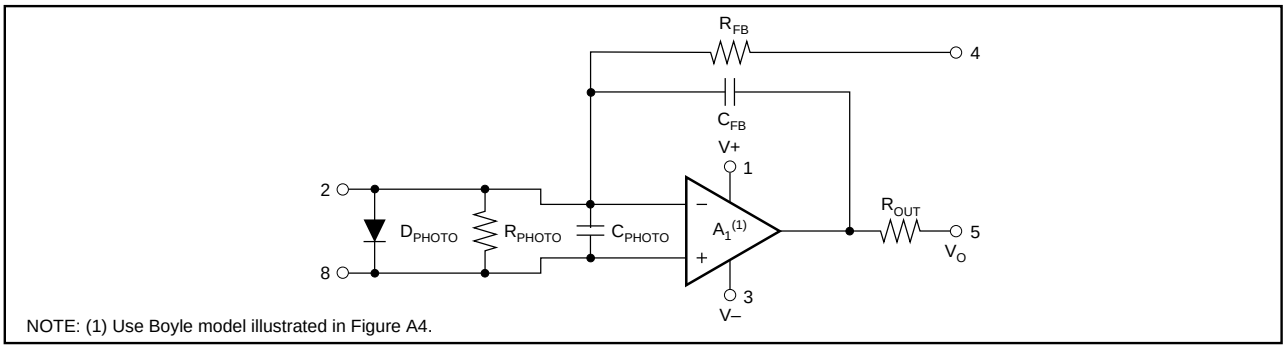


FIGURE A2. OPT–Standard Macromodel.

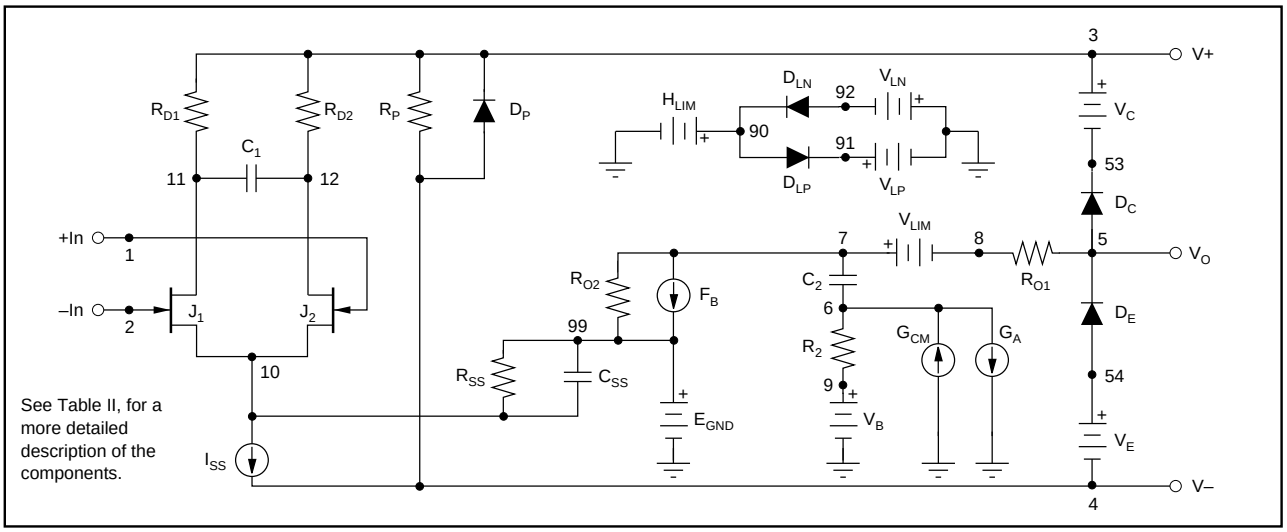


FIGURE A3. N-Channel JFET-Input Op Amp Standard PSpice Parts Macromodel.

(1) For more information, see: G.R. Boyle, B.M. Cohn, D.O. Pederson, and J.E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

(2) MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718 USA, (714) 770-3022, (800) 245-3022.

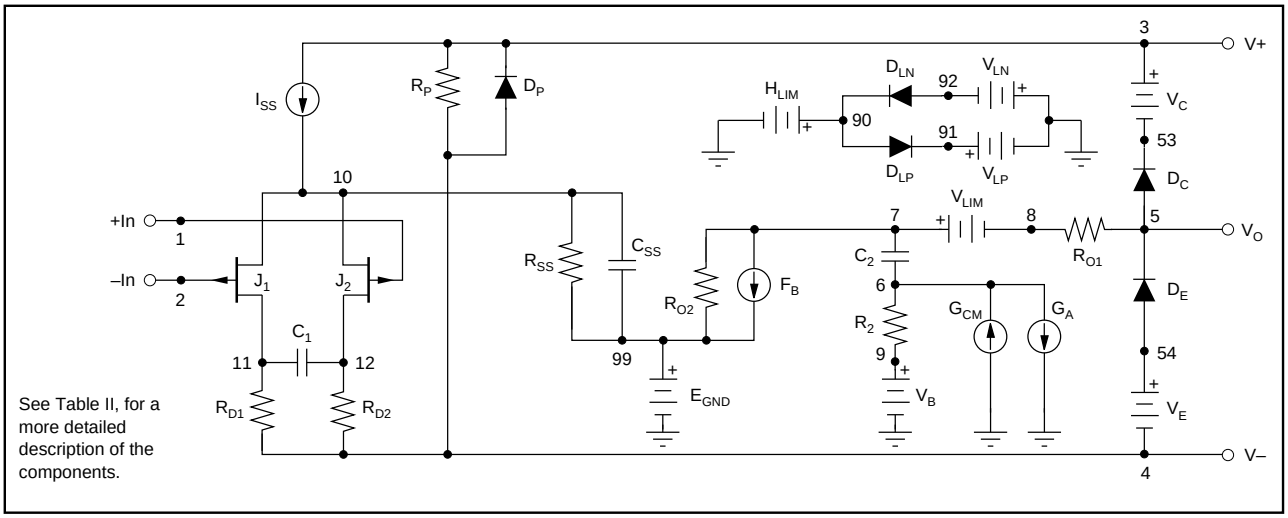


FIGURE A4. N-Channel JFET-Input Op Amp Standard PSpice Parts Macromodel.

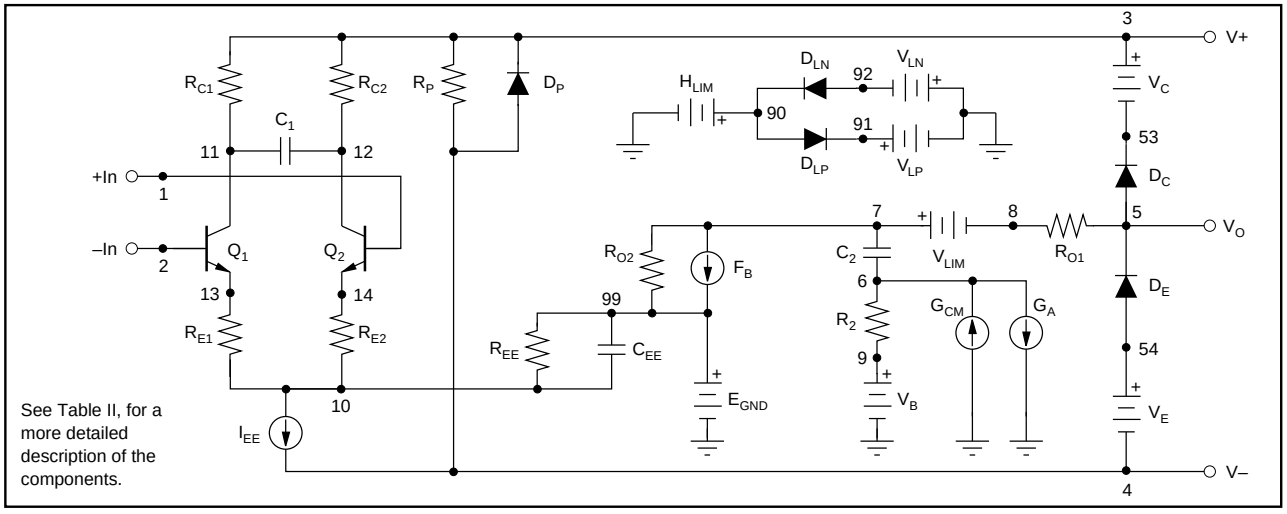


FIGURE A5. NPN-Input Op Amp Standard PSpice Parts Macromodel.

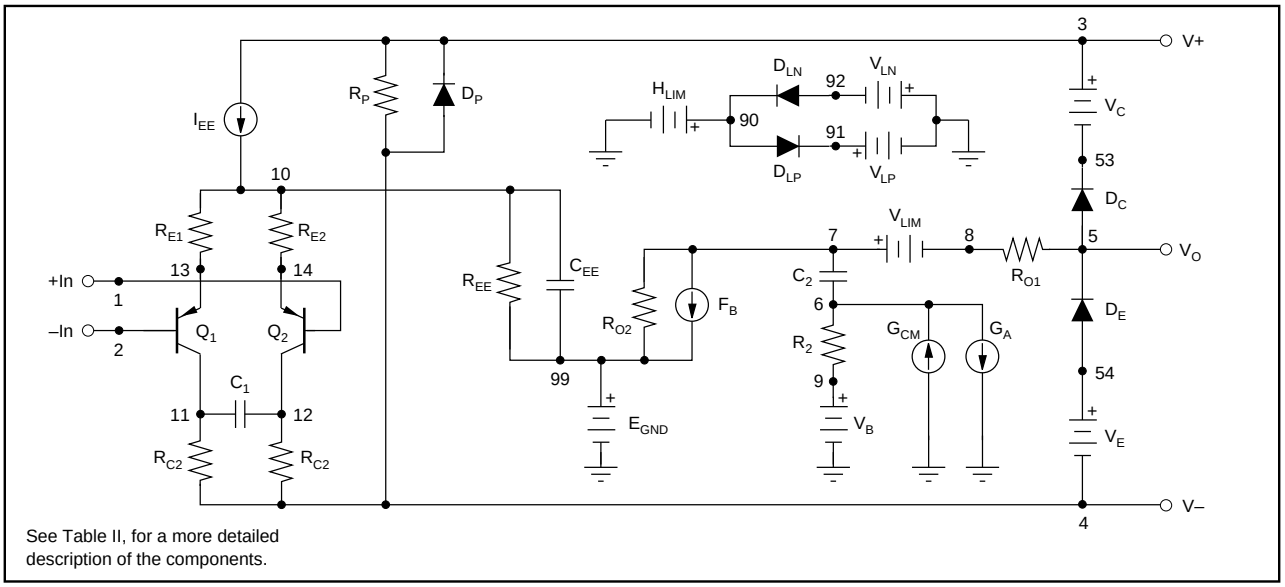


FIGURE A6. PNP-Input Op Amp Standard PSpice Parts Macromodel.

SECTION B:
ENHANCED MACROMODELS

The enhanced version, "E", of the standard PSpice Parts model contains several additional performance features. All of the macromodels using this topology are in the ENH_MOD subdirectory on the disk. The FET-input amplifiers using the standard PSpice Parts topology plus enhancements are shown in Figures B1 and B2. The node assignments for the enhanced op amp macromodels with bipolar-inputs are shown in Figures B3 and B4. Figure A1 shows the external op amp node assignments. Tables II, III, and IV list component prefix designations, macromodel component descriptions, and PSpice INPUT designations used for the standard and enhanced models. The parameters that are modelled by the enhanced macromodels are listed in Table X. Additions and changes to the standard PSpice Parts macromodel to the enhanced version are discussed in the following text.

FIGURE	DESCRIPTION
B1	N-Channel JFET-Input Op Amp
B2	P-Channel JFET-Input Op Amp
B3	NPN Bipolar-Input Op Amp
B4	PNP Bipolar-Input Op Amp
B5	OPA27/37 Input Protection
B6	OPA77/177 Input Protection
B7	INA114/118 Input Protection Circuitry

TABLE VII. Enhanced Macromodels Figure Reference.

Input Current Correction

One feature that Burr-Brown offers with the enhanced model type is accurate simulation of input bias current for N-Channel JFET and P-Channel JFET operational amplifiers. Mathematically, the input bias current for JFET op amps should equal twice the I_S of the JFET model. However, simulation will show that the gate current from J_1 and J_2 in Figures A3 through B2 is between 10 to 20pA larger than expected, depending on the common-mode voltage of the input stage and the magnitude of the supply voltages, if G_{11} and G_{21} are not included in the model. This additional current is generated from the drain-to-gate and source-to-gate nodes of the input FETs of the operational amplifier, which manifests itself as the bias current of the amplifier. The additional current is caused by the Spice default value, GMIN. In this case, 1/GMIN is the impedance between the drain and gate and the source and gate. This is done by Spice to keep the gate node of each FET from floating. The default value, or GMIN is 1E-12Ω. The voltage dependent current sources, G_{11} and G_{21} remove this error current from the model, hence the macromodel models input bias current correctly. This technique is used in all of the FET-enhanced and multiple pole/zero macromodels. To improve simulation accuracy the .OPTIONS statement should include ABSTOL = 100fA or 10fA.

Noise

Most of the enhanced JFET-input macromodels model device current noise and voltage noise. The current noise is modeled using R_{N1}, R_{N2}, R_{N3}, R_{N4}, R_{N5} and R_{N6} to create the noise source and the voltage-dependent current sources, G_{11} and G_{21}, to model the noise on the inverting and non-

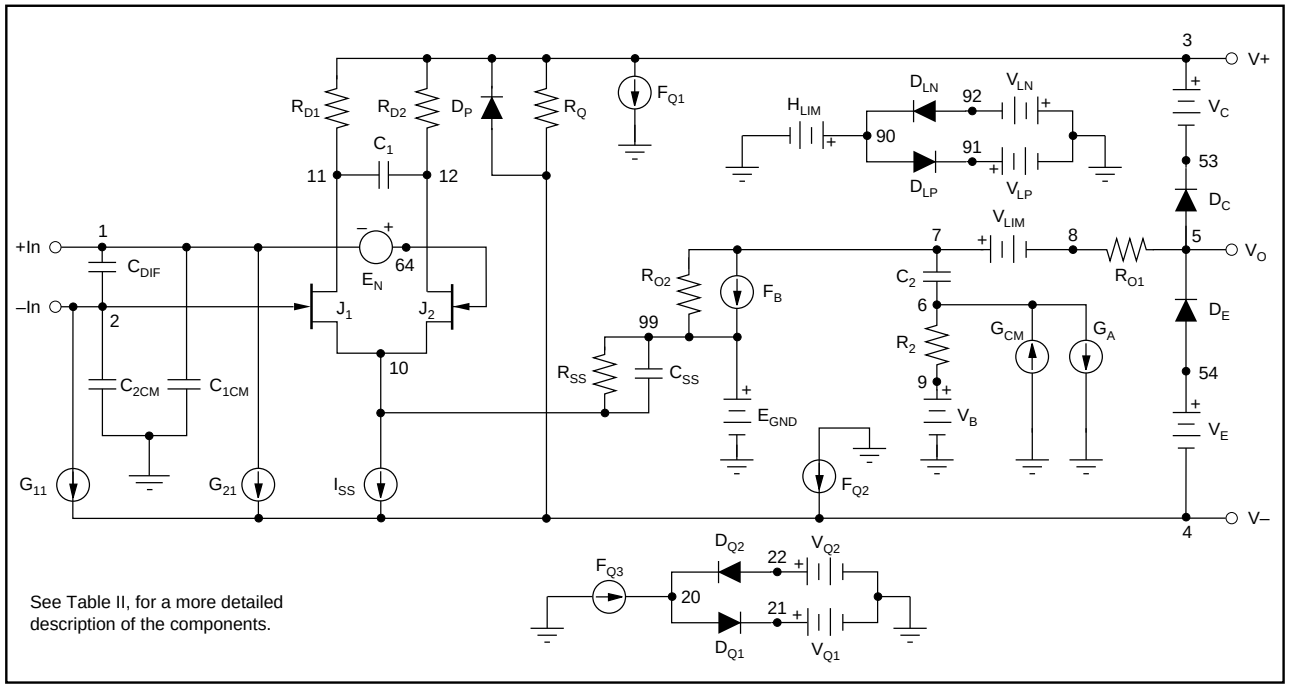


FIGURE B1. N-Channel JFET-Input Op Amp Enhanced PSpice Parts Macromodel.

inverting inputs of the amplifiers. The voltage noise is modelled using D_{N1}, D_{N2}, V_{N1} and V_{N2} to create the noise source and EN to model the noise on the non-inverting input of the amplifiers.

Input Capacitance

Differential and common-mode input capacitors, C_{DIF}, C_{1CM}, and C_{2CM} have been added to the enhanced macromodels. Input capacitance could also be modeled by including capacitor coefficients in the transistor models. Instead, discrete capacitors were used so the comparison to the standard model would be more obvious.

Input Protection Diodes

If an op amp contains input protection diodes, its enhanced op amp macromodel also contains diodes connected between the input pins as shown in Figures B5 and B6, for example.

Quiescent Power

R_P was replaced by R_Q. The value of R_Q is higher. It models only the resistive portion of quiescent current. The current sources described below model the constant portion of the quiescent current. This technique provides a more accurate model of quiescent current vs power-supply voltage.

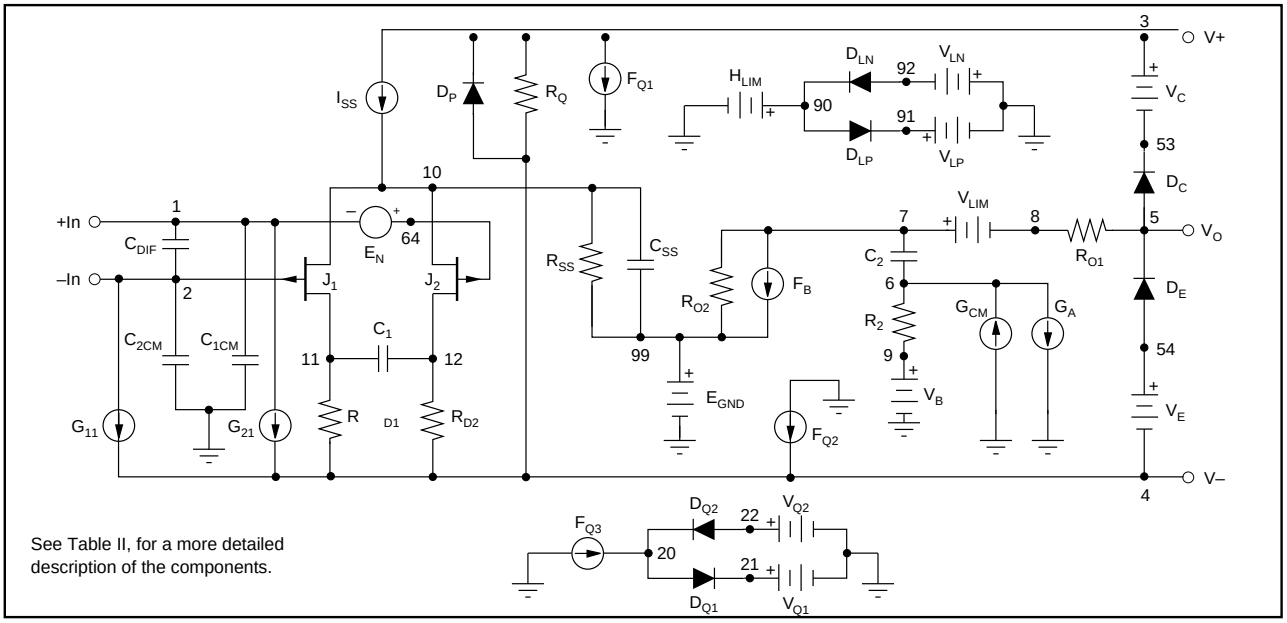


FIGURE B2. P-Channel JFET-Input Op Amp Enhanced PSpice Parts Macromodel.

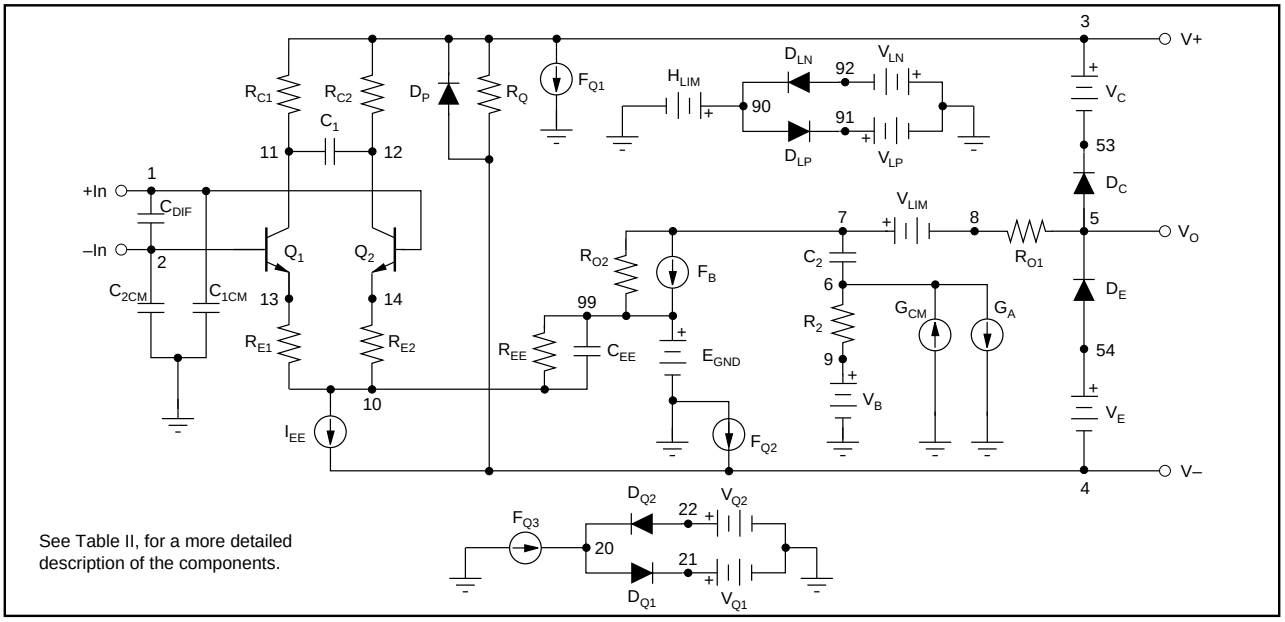


FIGURE B3. NPN-Input Op Amp Enhanced PSpice Parts Macromodel.

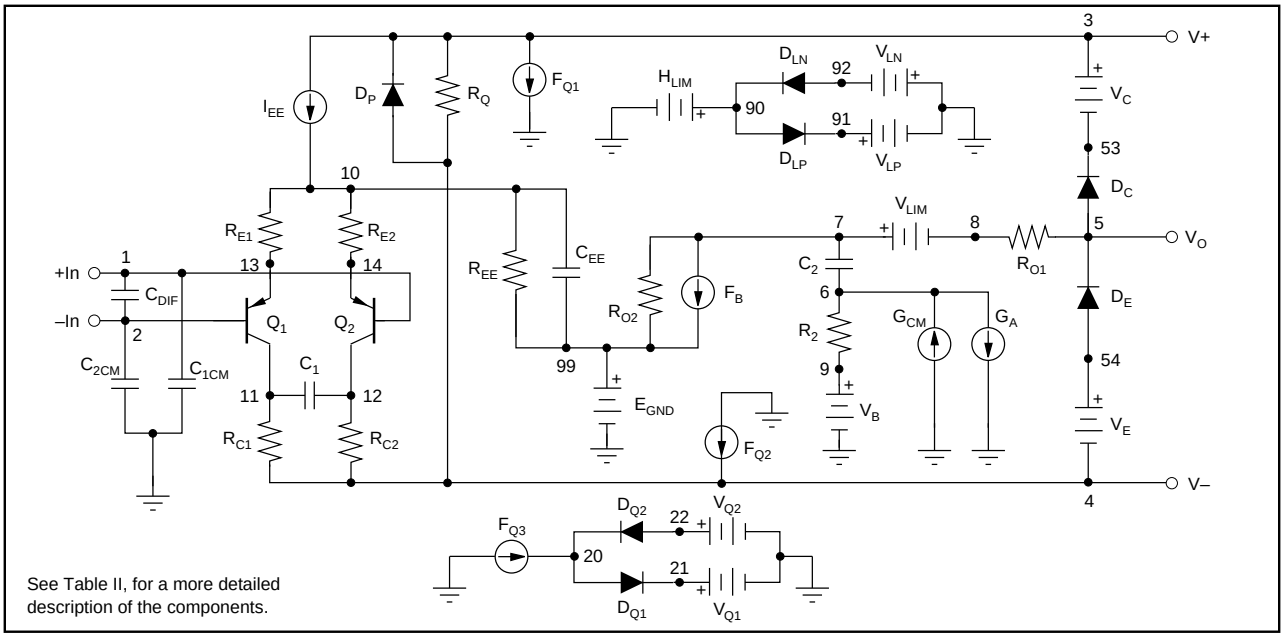


FIGURE B4. PNP-Input Op Amp Enhanced PSpice Parts Macromodel.

Output Current Flowing from the Power-Supply Nodes

A number of components were added so that both load and quiescent current flow from the power supply nodes.

F_{Q3} mirrors the current flowing from V_{LIM}.
Positive current from F_{Q3} flows through D_{Q1} into V_{Q1}.
Negative current from F_{Q3} flows through D_{Q2} into V_{Q2}.
F_{Q1} supplies constant portion of I_Q plus mirrors positive output current, which is measured by V_{Q1}.
F_{Q2} supplies constant portion of I_Q plus mirrors negative output current, which is measured by V_{Q2}.

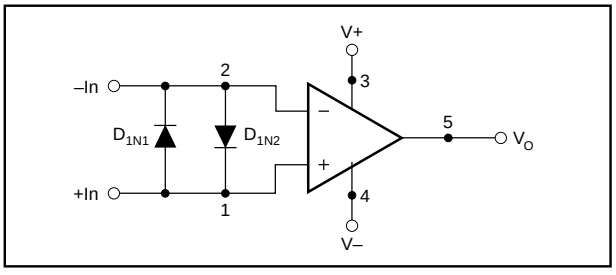


FIGURE B5. Input Protection Diode Circuitry Used on OPA27/37 Enhanced Macromodels.

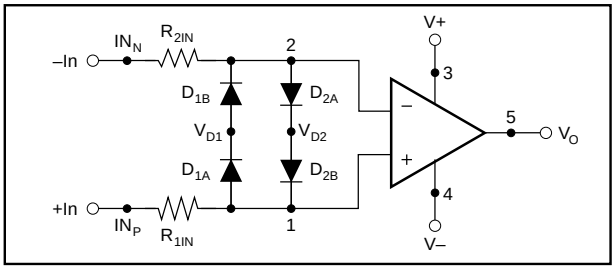


FIGURE B6. Input Protection Circuitry Used on OPA77/177 Enhanced Macromodels.

NOTE: The enhanced op amp macromodels are more complicated and require more simulation time than the standard macromodels, but will provide more accuracy in simulations in some applications.

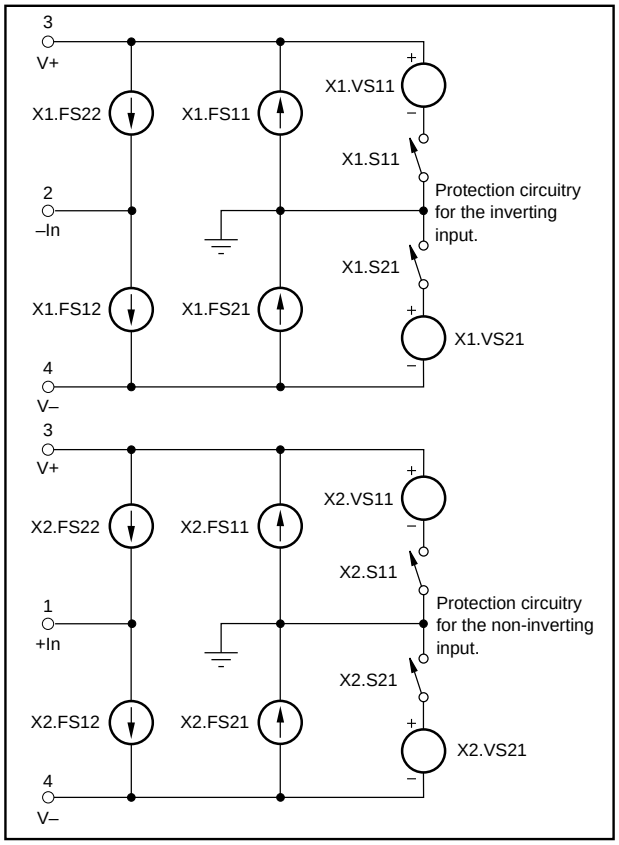


FIGURE B7. Input Protection Circuitry Used on INA114/118 Enhanced Macromodel.

SECTION C: MULTIPLE-POLE/ZERO MACROMODELS

The multiple pole/zero ("M") macromodel allows modeling of more than two poles and any additional zeros in the op amp macromodel. All of the macromodels using this topology are in the MPZ_MOD subdirectory on the disk. The input stage of this model is similar to the standard and enhanced op amp macromodels; however, after the input stage that similarity disappears. By using various circuit topologies the gain stages, pole stages, zero stages and pole/zero stages are constructed. The number of each of these stage types is dependent on the performance characteristics of the amplifier being modelled. An effort is made to match the macromodel performance as closely as possible to the tested gain/phase of the op amp. The output stage also offers improvements in current steering from the supply voltages. This model type is typically used to model high-speed amplifiers; however, it has come in useful when modelling function circuits that require special considerations.

FIGURE	DESCRIPTION
C1	N-Channel JFET–Input Op Amp
C2	P-Channel JFET–Input Op Amp
C3	NPN Bipolar–Input Op Amp
C4	PNP Bipolar–Input Op Amp
C5	Gain-, Pole/Zero, and Output Stages
C6	ACF2101M–Op Amp Section
C7	ACF2101M–Node Assignments
C8	OPA675M/676M–Input Stage
C9	OPA675M/676M–Package and Pad Parasitics
C10	VCA610M–Macromodel

TABLE VIII. Multi Pole/Zero Macromodels Figure Reference.

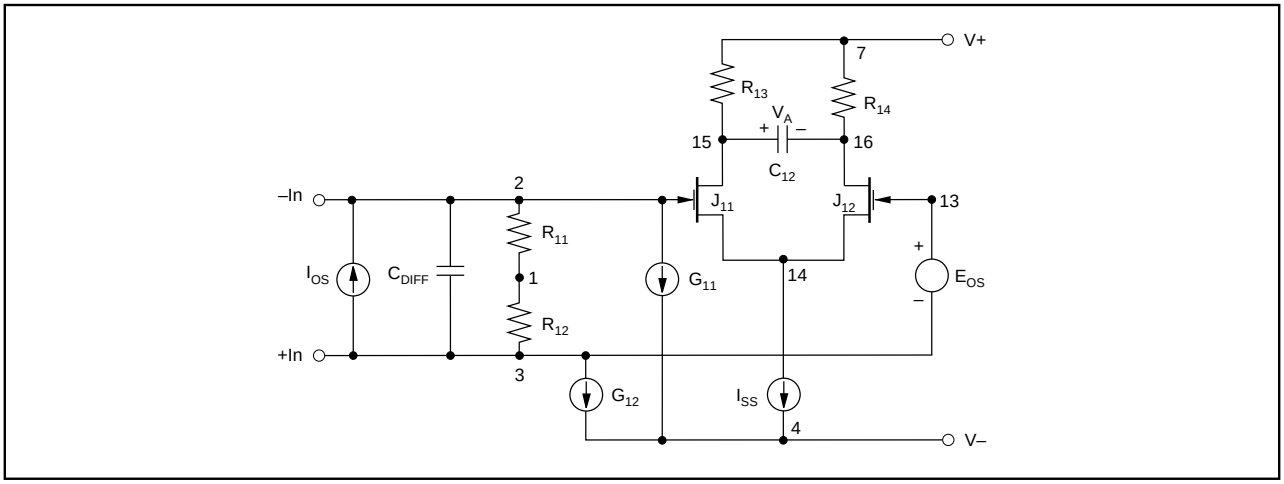


FIGURE C1. Input Stage to the N-Channel JFET-Input Op Amp Multiple Pole/Zero Macromodel.

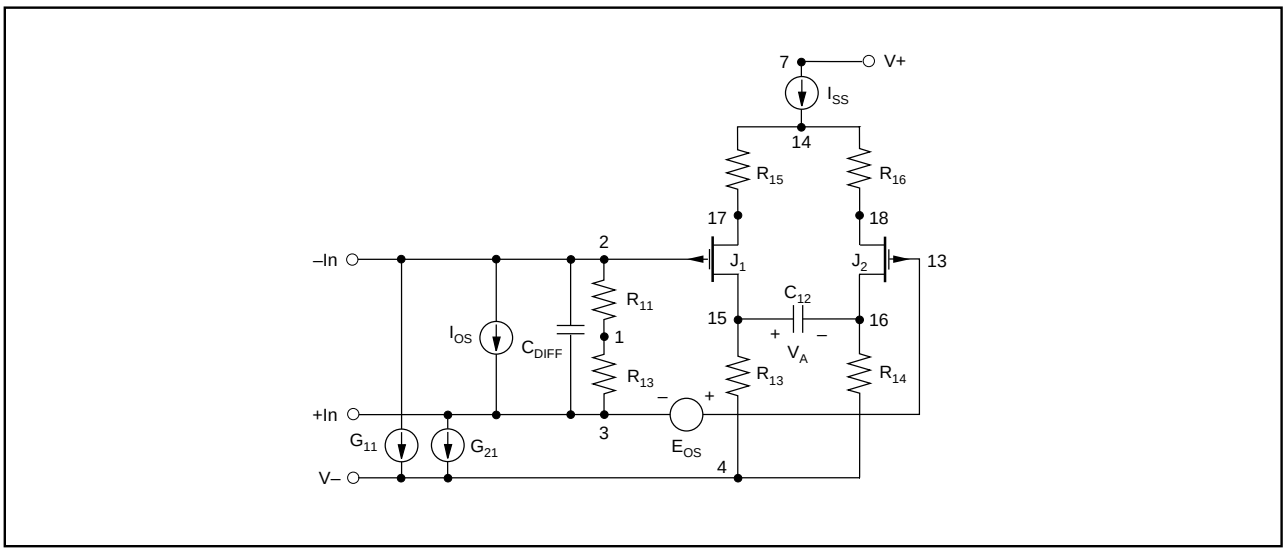


FIGURE C2. Input Stage to the P-Channel JFET-Input Op Amp Multiple Pole/Zero Macromodel.

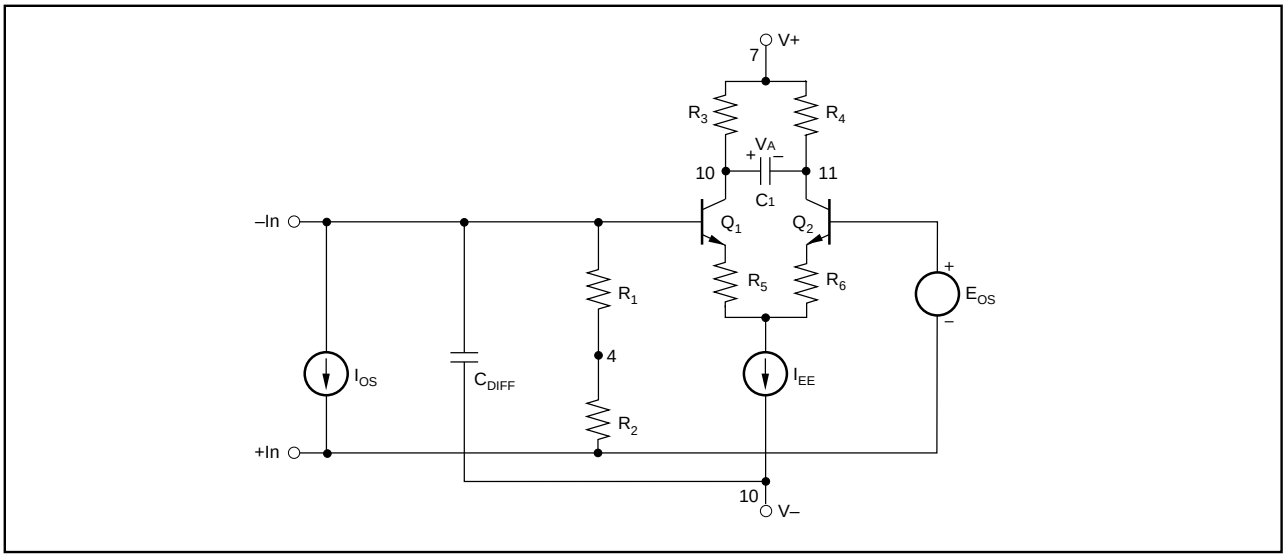


FIGURE C3. Input Stage to the NPN–Input Op Amp Multiple Pole/Zero Macromodel.

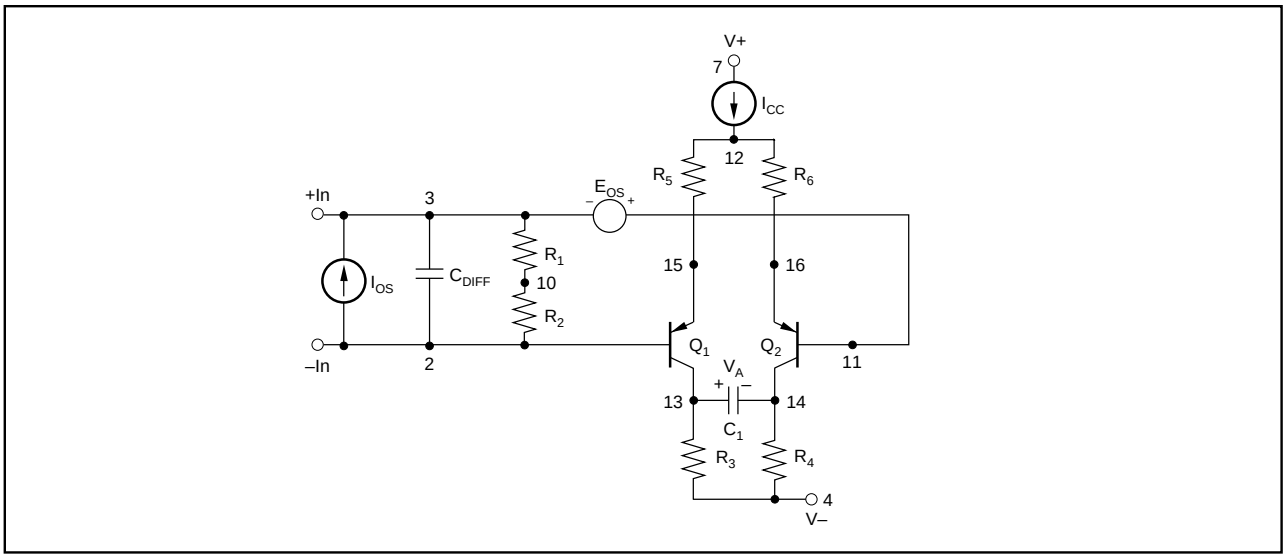


FIGURE C4. Input Stage to the PNP–Input Op Amp Multiple Pole/Zero Macromodel.

The accuracy of this model topology compared to the standard and enhanced model topologies is improved for high speed amplifiers primarily because of the improved gain/phase performance. Assuming no convergence problem exists with the macromodels discussed so far, the time taken for Spice to produce the dc operating point calculation of the multiple pole/zero model is about twice the time required for the standard model. For transient analysis using this model, simulation time can be reduced by using the .OPTION statement to increase the number of transient iterations from 10 to 40. The proper Spice command is:

.OPTIONS ITL4=40

The basic topology of input stages of this op amp model are shown in Figures C1, C2, C3, and C4. The input stage is the only section in the macromodels that differ between the four types of op amps (N-Channel FET, P-Channel FET, NPN Bipolar, and PNP Bipolar). The remainder of the macromodel circuit (gain stages, phase stages, CMRR stage, and output stage) is shown in a generic form in Figure C5. A summary of the parameters modelled is listed in Table X.

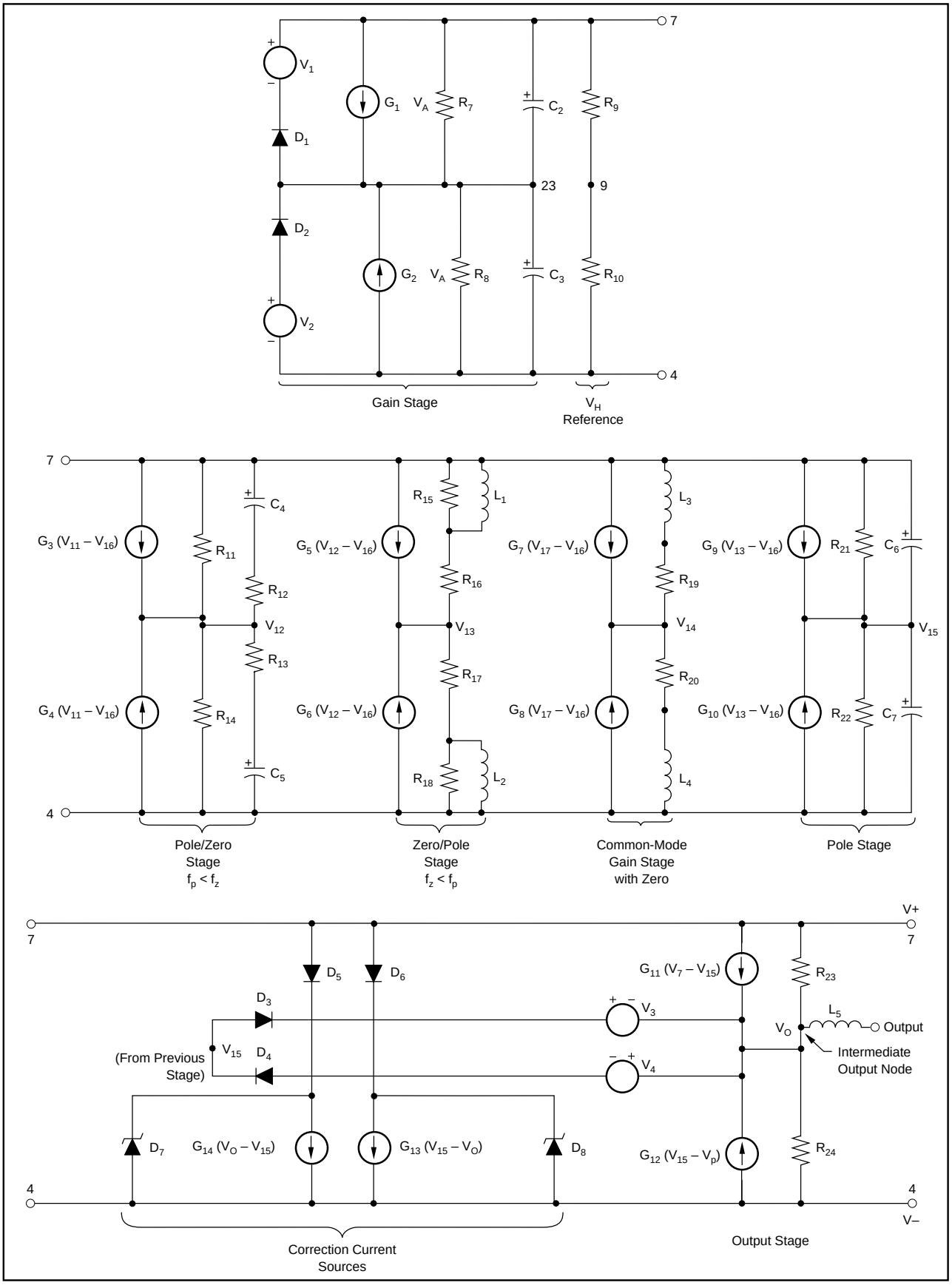


FIGURE C5. Multiple Pole/Zero Macromodel without Input Stage. Refer to Figures C1 Through C4 for Input Stage Topology.

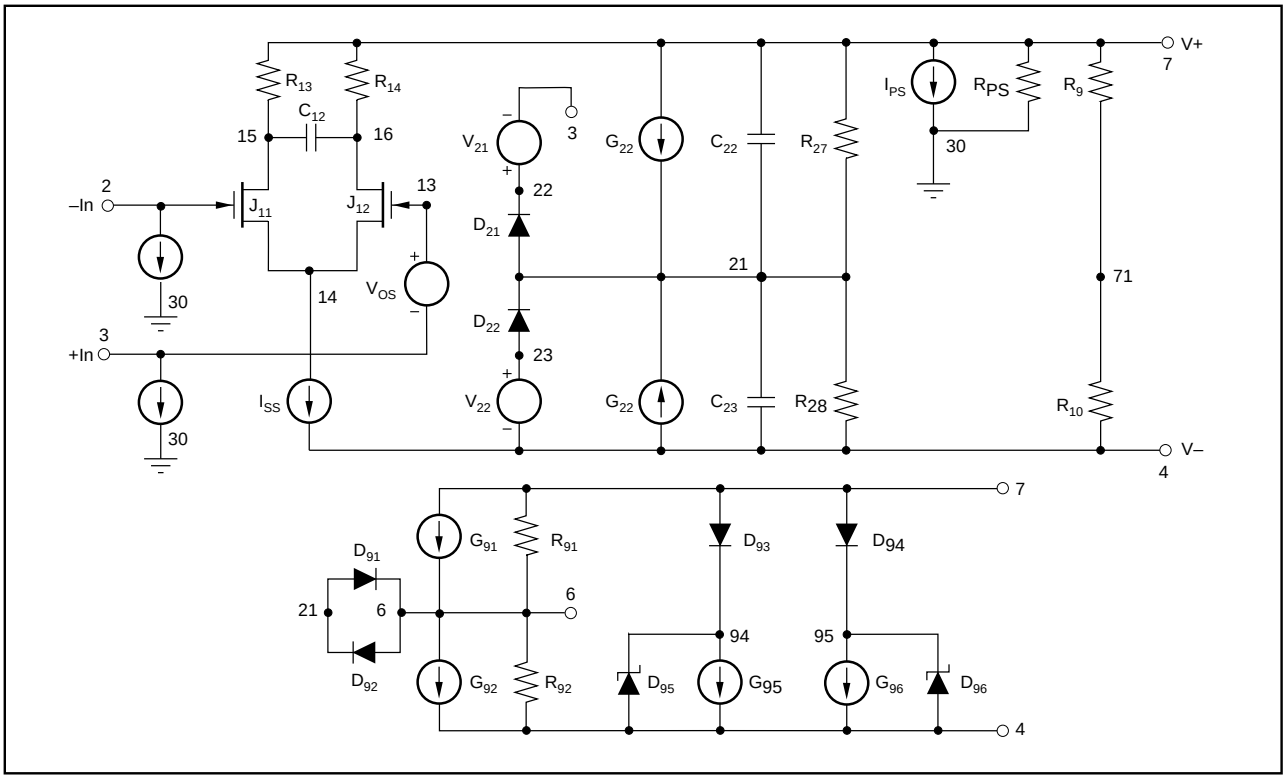


FIGURE C6. Op Amp Section of the ACF2101 Using the Multiple Pole/Zero Macromodel Topology.

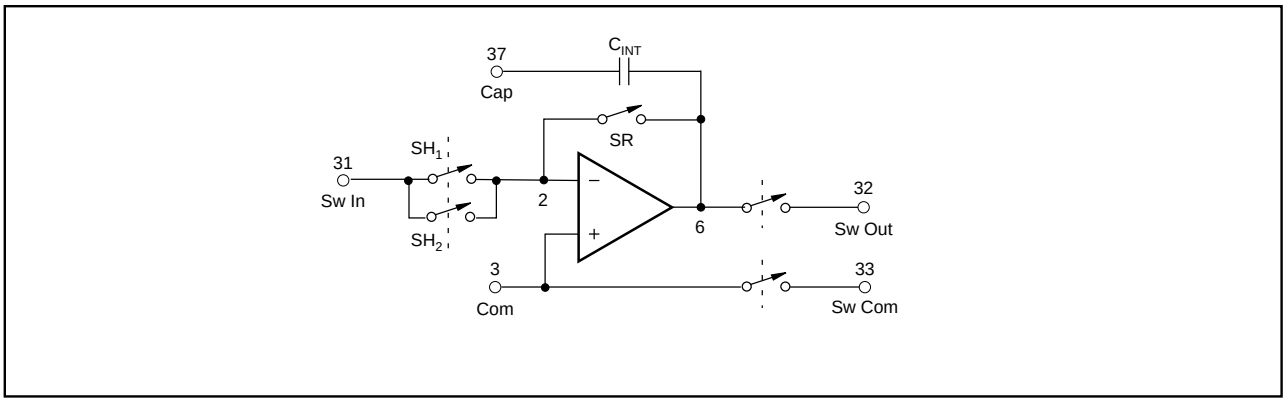


FIGURE C7. Node Assignments for ACF2101 Macromodel.

The multiple pole/zero topology is used to model the op amp section of the ACF2101 switched integrator. The node assignments for this model are shown in Figure C6 and C7. The transient time of the switches (HOLD, RESET, and SELECT) should be programmed to have a slew of 6V/µs. Complying with this requirement will give the user greater success in convergence during transient analysis, and a more accurate emulation of the effect of the 200ns switching speed of the actual switching transistors in the ACF2101. This is easily implemented with the PULSE command in Spice. Also, to insure proper operation, always establish the initial bias point for the transient analysis with RESET and HOLD equal to the potential of COMMON (node 3).

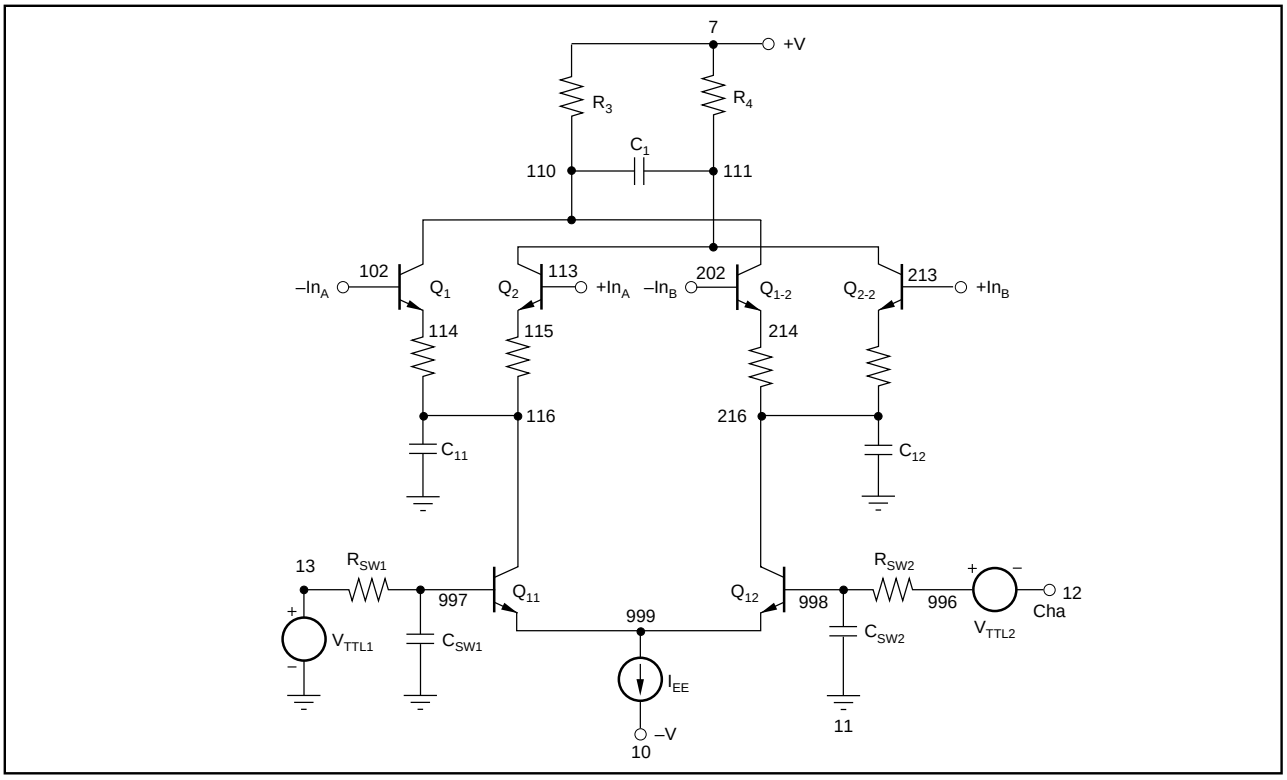


FIGURE C8. Input Stage of the OPA675 and OPA676 Switched-Input Op Amp Using the Multiple Pole/Zero Macromodel Topology.

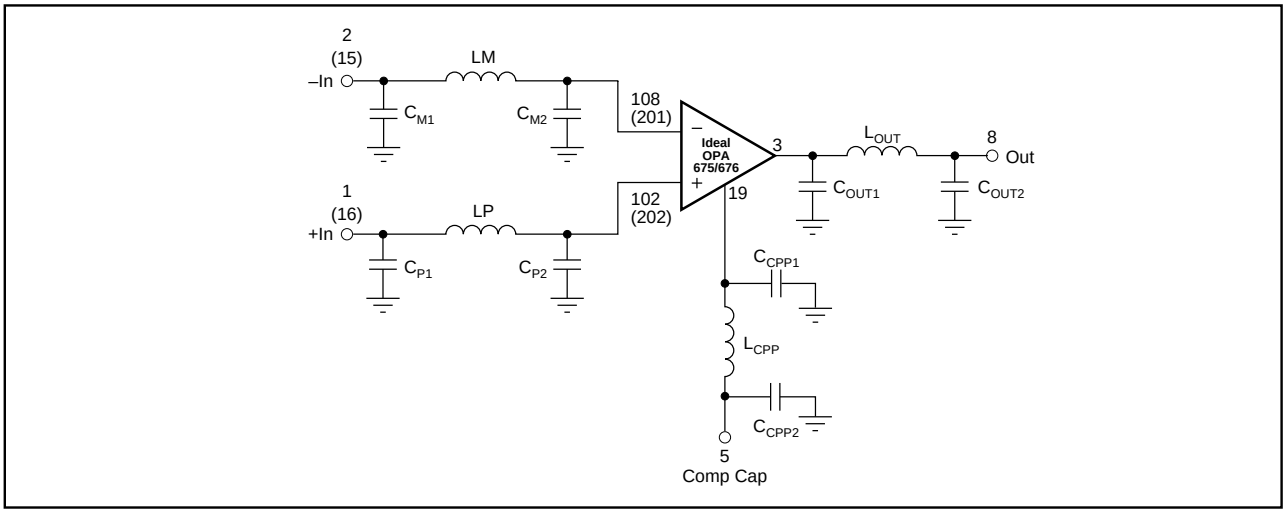


FIGURE C9. Package and Pad Parasitics Modelled by the OPA675 and OPA676 Macromodel.

The OPA675 and OPA676 are wideband op amps with two independent differential inputs (Figure C8). The multiple pole/zero topology is used to model the op amp portion of these switched-input amplifiers. Both amplifiers are identical except for the switch logic. The OPA675 is an ECL-switched device and the OPA676 is a TTL-switched device. Both files will model the device characteristics and package parasitics. If the user is using the product in its die form, the package parasitics no longer apply (Figure C9).

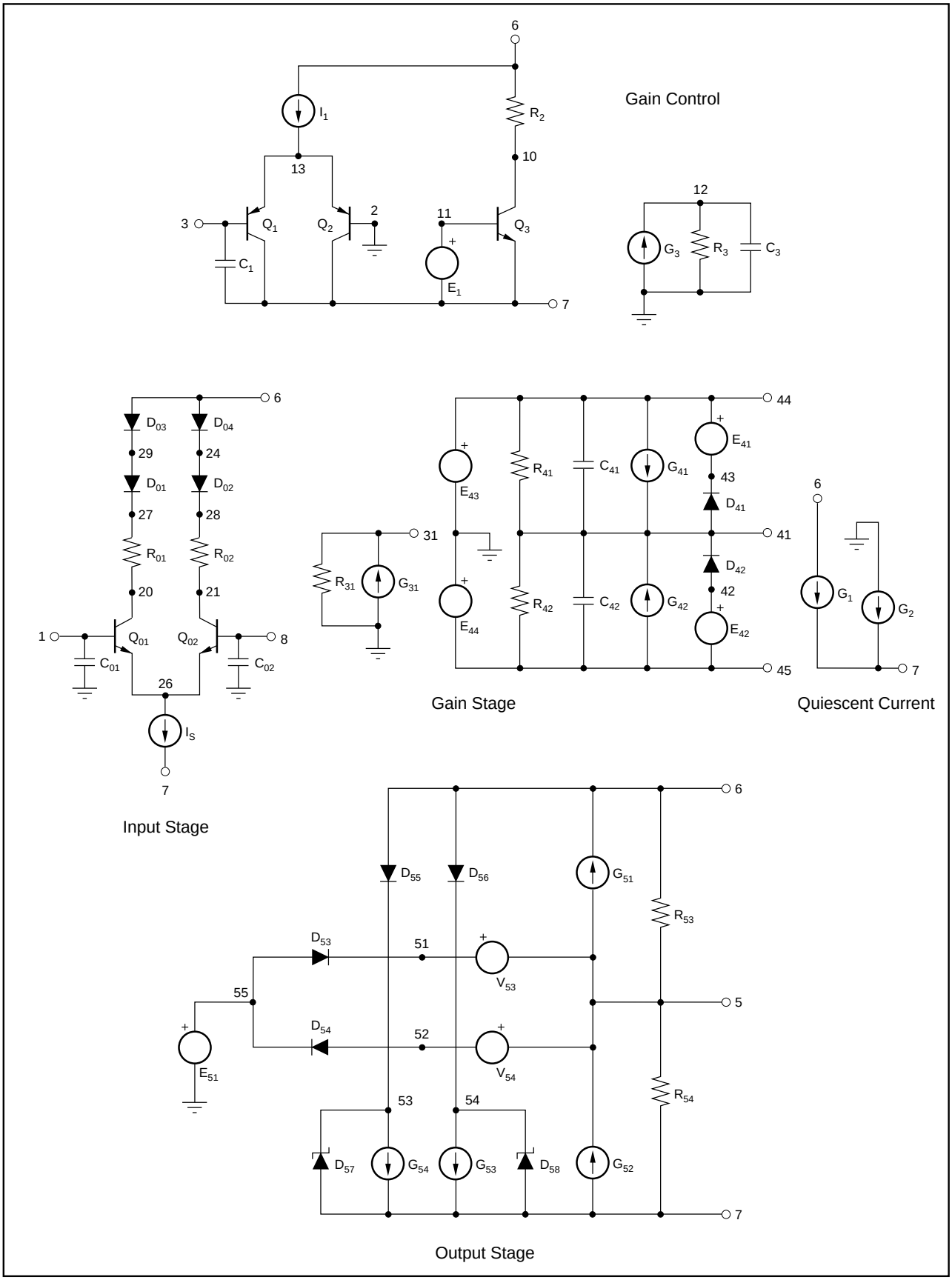


FIGURE C10. VCA610M Voltage Controlled Amplifier using the Multiple Pole/Zero Macromodel Topology.

SECTION D:
SIMPLIFIED CIRCUIT MODELS

As already mentioned the simplified circuit models provide a much different simulation approach, because they do not follow a standard model design. They are micromodels at the transistor level, therefore each model has its individual circuit schematic, which are shown on the following pages. Almost all of the devices of this model level (Level IV) are wideband/high-speed components with bandwidth capabilities of up to 1GHz. Some models have only one simplified circuit model available, and are labeled with the suffix "X". Other models offer two simplified circuit models. In general, the models with an "X1" suffix are of equivalent complexity as the "X" models. They are simpler implementations of the macromodel and will simulate faster; however, the accuracy is not as good as with the macromodels with an "X2" suffix for the same product.

All of these models are found in the CIR_MOD subdirectory on the disk. These models are designed using different topologies than mentioned above and several non-linear elements. Because of the increased number of non-linear elements in these models, the simulation time is longer, but the accuracy is improved.

The wideband operational amplifiers that have simplified circuit macromodels were designed using several subcircuits that allow the user to implement a variety of configurations. The OPA622 is a monolithic amplifier that can be configured as a current-feedback amplifier or a voltage-feedback amplifier. Like typical current-feedback amplifier, the OPA622 has a constant large-signal bandwidth of 280MHz. One would expect that when the OPA622 is configured in a voltage-feedback configuration the bandwidth would change with gain. This is not the case. When the OPA622 is configured as a voltage-feedback amplifier, it will again have a constant bandwidth over a wide gain and output voltage range. In the voltage-feedback mode, the OPA622 offers the speed advantages of current-feedback amplifiers and matched input impedance advantage of the voltage-feedback op amp. The OPA623 is strictly configured as a current-feedback amplifier, using the same internal design as the OPA622.

The OPA660 wideband amplifier offers the user an "ideal transistor" and a buffer. The "ideal transistor" has three terminals available to the user—a high-impedance input (base), a low-impedance input/output (emitter) and the current output (collector). This "ideal transistor", otherwise called an Operational Transconductance Amplifier (OTA), is constructed using several discrete real transistors on the chip to give the user superior gain and temperature performance, hence, the comparison to an "ideal transistor".

Although these transistor level models are more accurate than the other three topology levels used for macromodels on this disk, the user is cautioned that all models are an aid to circuit design and not a suggested replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing. The parameters that are modelled by the transistor level circuit macromodels are listed in Table X.

FIGURE	DESCRIPTION
D1	BUF600/601X1 Circuit Model
D2	BUF600/602X2 Complex Circuit Model
D3	BUF634X Circuit Model
D4	ISO120/121X Circuit Model
D5	ISO130 Circuit Model
D6	MPC100X1 Circuit Model
D7	MPC100X2 Complex Circuit Model
D8	OPA603X Circuit Model
D9	OPA620/621X Circuit Model
D10	OPA622X1 Circuit Model
D11	OPA622X2 Complex Circuit Model
D12	OPA623X1 Circuit Model
D13	OPA623X2 Complex Circuit Model
D14	OPA640X/OPA641X Circuit Model
D15	OPA642X/OPA643X Circuit Model
D16	OPA644X Circuit Model
D17	OPA646X Circuit Model
D18	OPA648X Circuit Model
D19	OPA64x Package and Pad Parasitics
D20	OPA658X Circuit Model
D21	OPA660X1 Circuit Model
D22	OPA660X2 Complex Circuit Model

TABLE VIIII. Simplified Circuit Models Figure Reference.

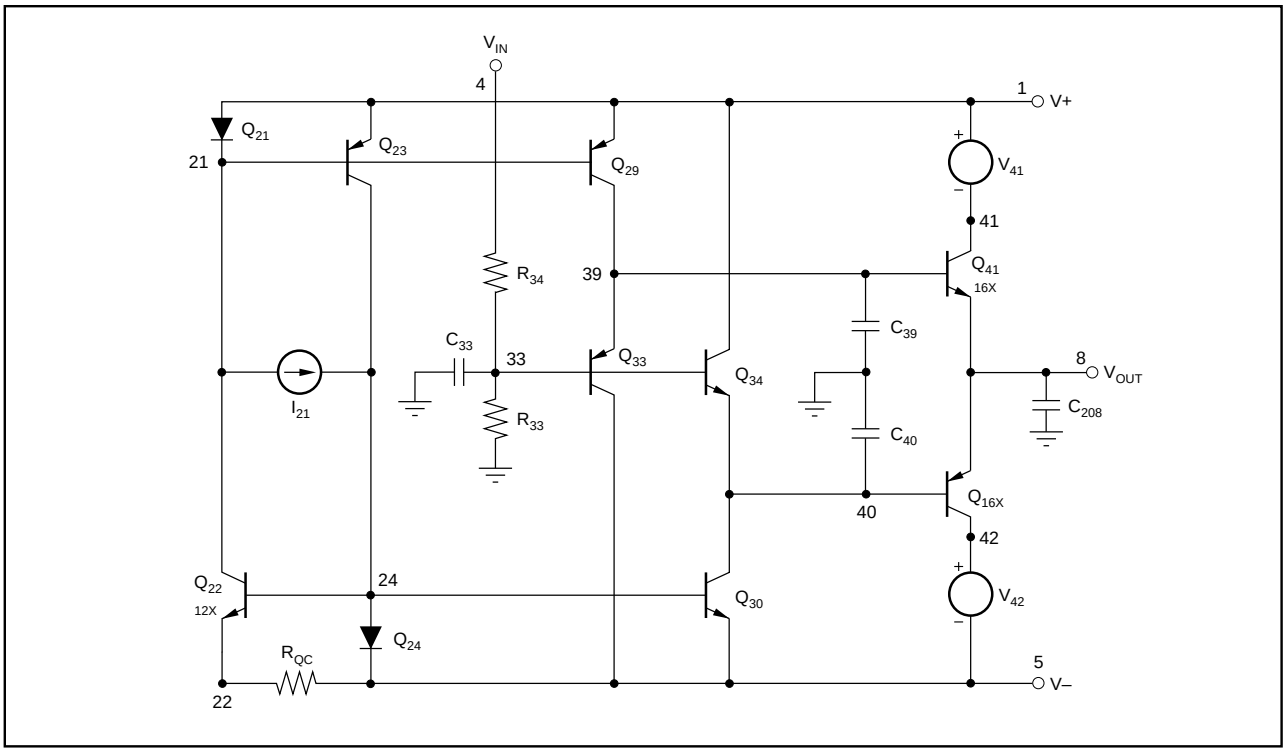


FIGURE D1. BUF600X1 and BUF601X1 Simplified Circuit Macromodel. Compared to Figure D2, this macromodel is less complex with faster simulation times.

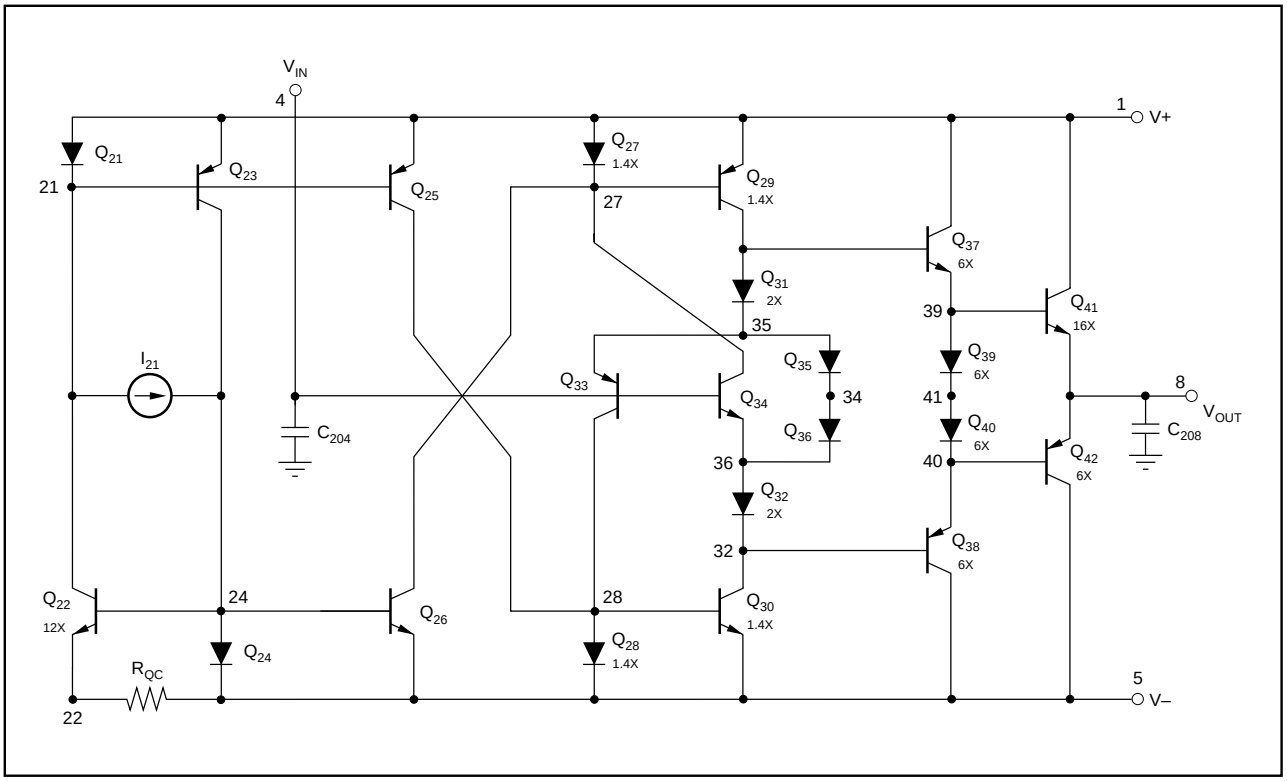


FIGURE D2. BUF600X2 and BUF601X2 Complex Macromodel. Compared to Figure D1, this macromodel is more complex and requires more simulation time.

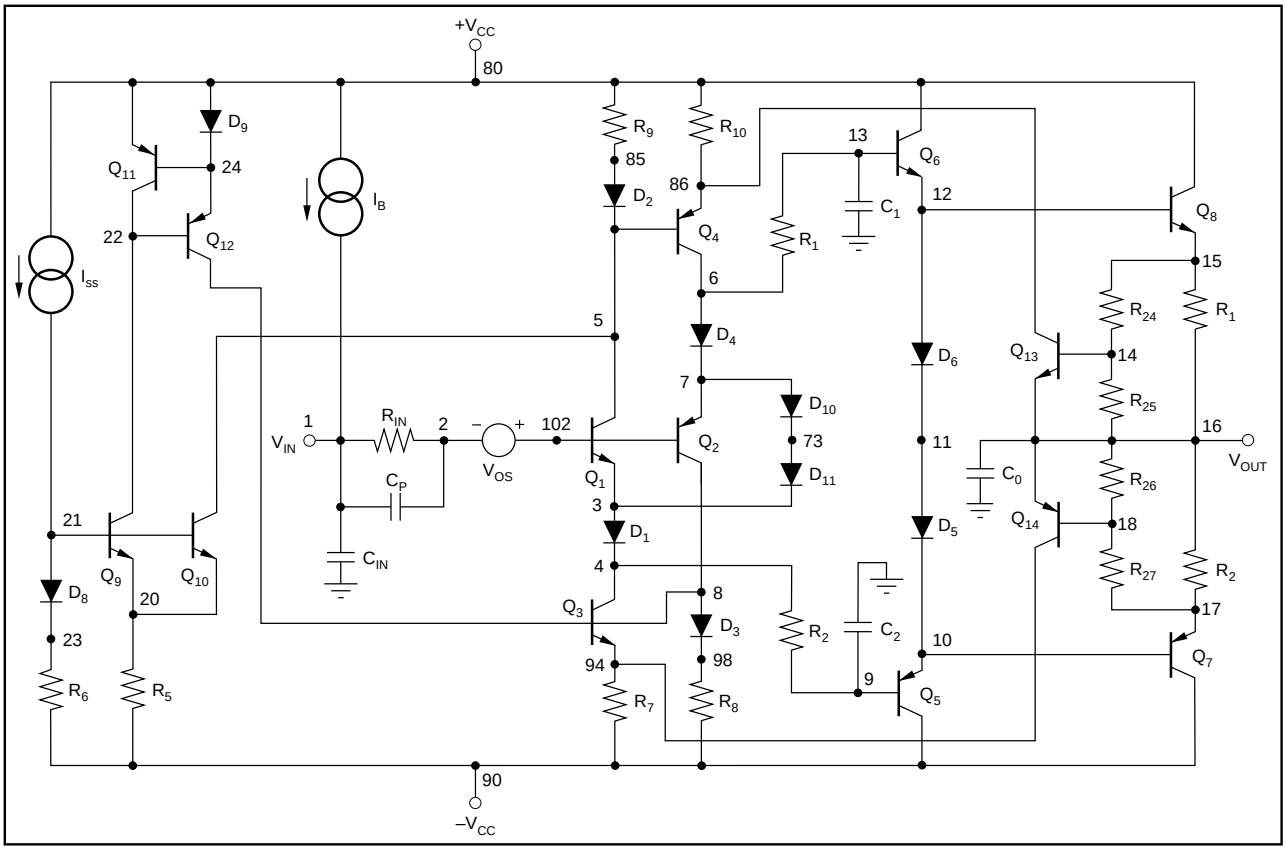
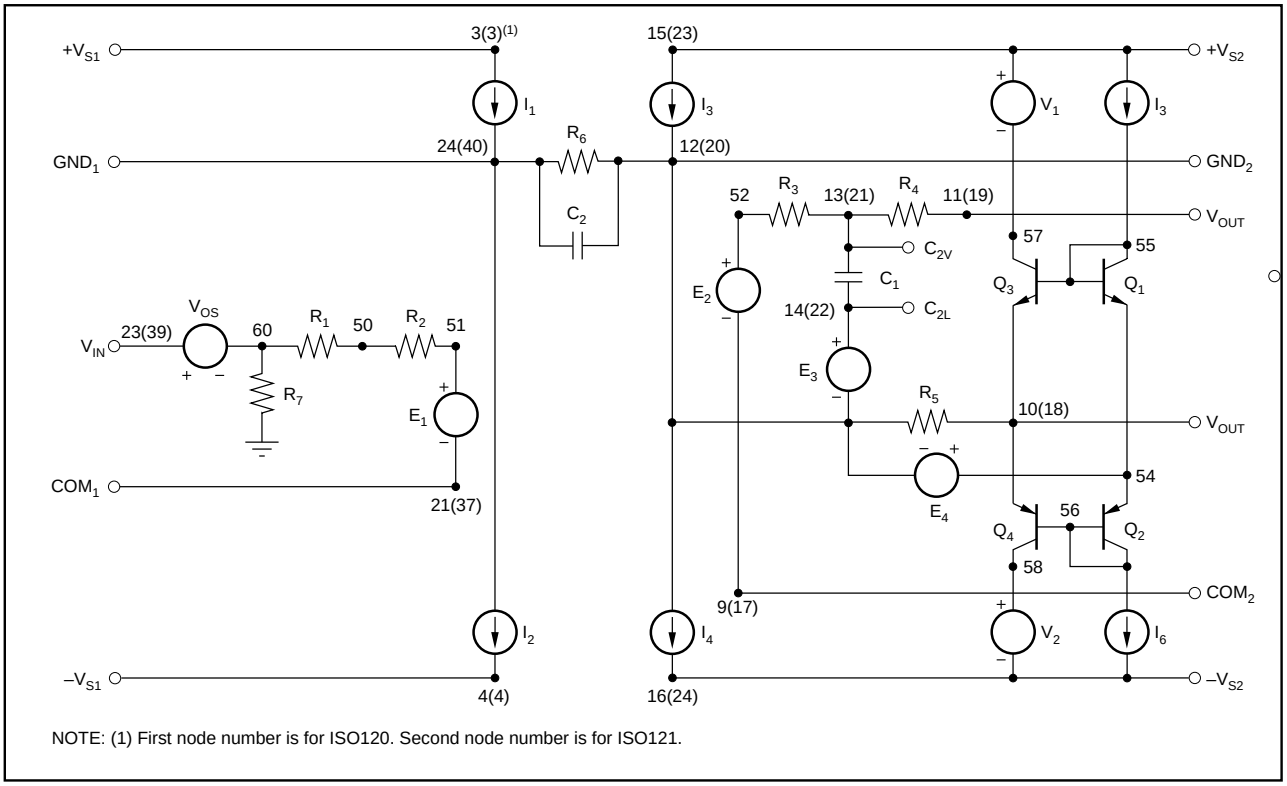


FIGURE D3. BUF634X Simplified Circuit Macromodel.



NOTE: (1) First node number is for ISO120. Second node number is for ISO121.

FIGURE D4. ISO120/121X Isolation Amplifiers Simplified-Circuit Macromodel.

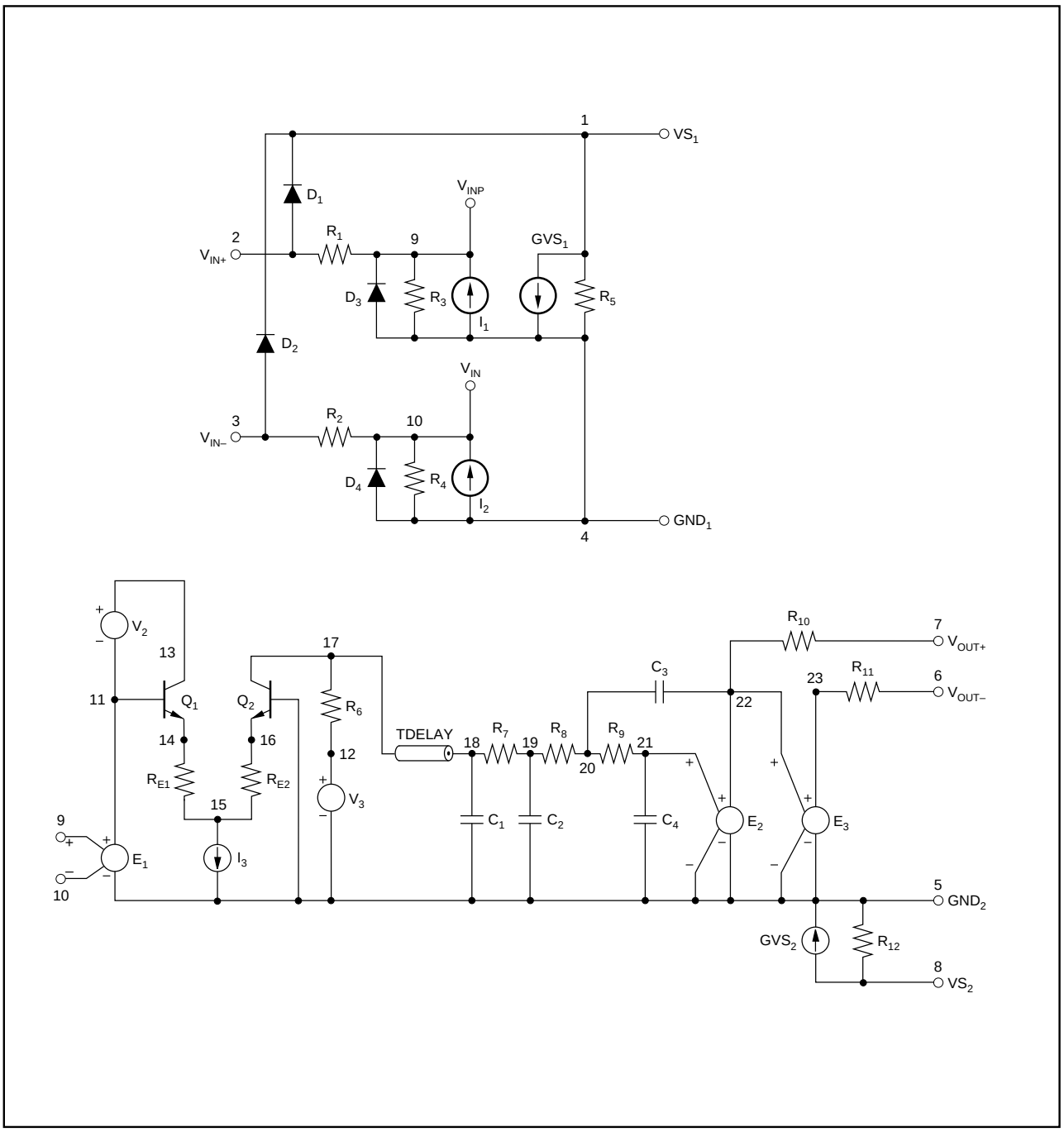


FIGURE D5. ISO130X Simplified-Circuit Model.

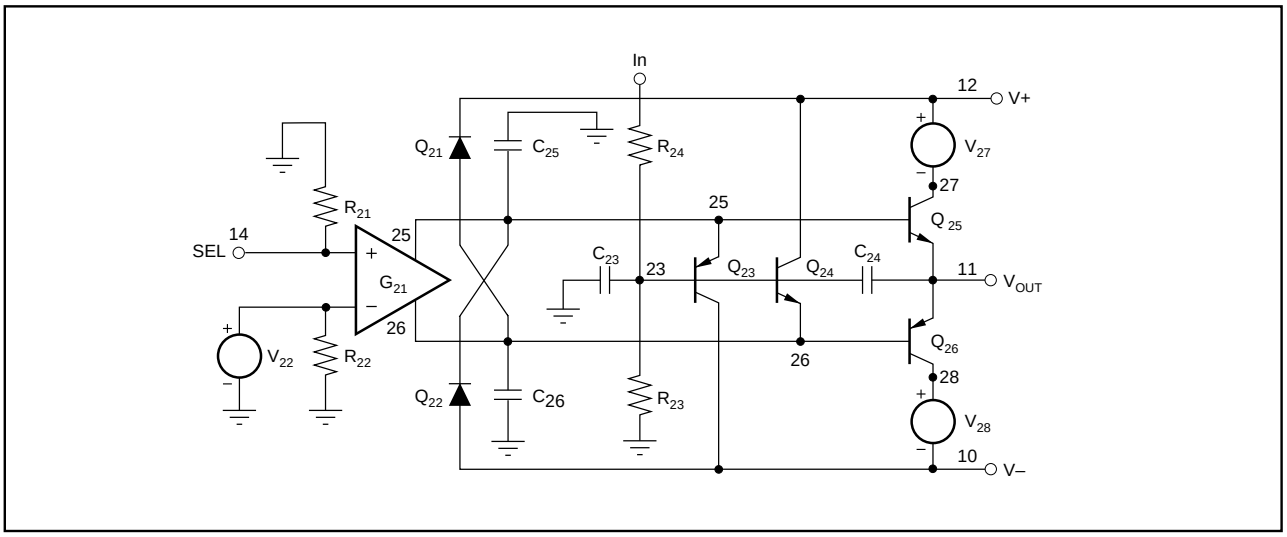


FIGURE D6. MPC100X1 Simplified-Circuit Macromodel. Compared to Figure D7, this macromodel is less complex with faster simulation times. Shown here is only one out of four inputs of the MPC100. However, the same circuit schematic applies to the MPC102X1 and MPC104X1 model.

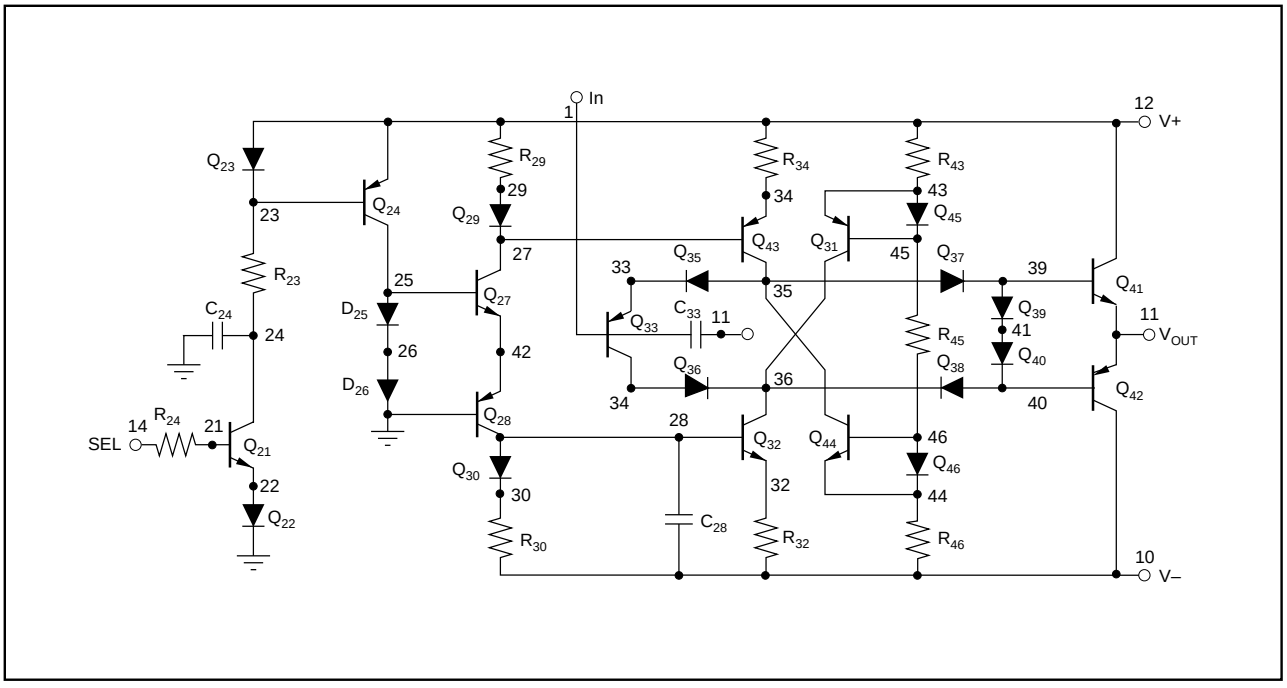


FIGURE D7. MPC100X2 Complex-Circuit Macromodel. Compared to Figure D6, this macromodel is more complex and requires more simulation time. Shown here is only one out of four inputs of the MPC100.

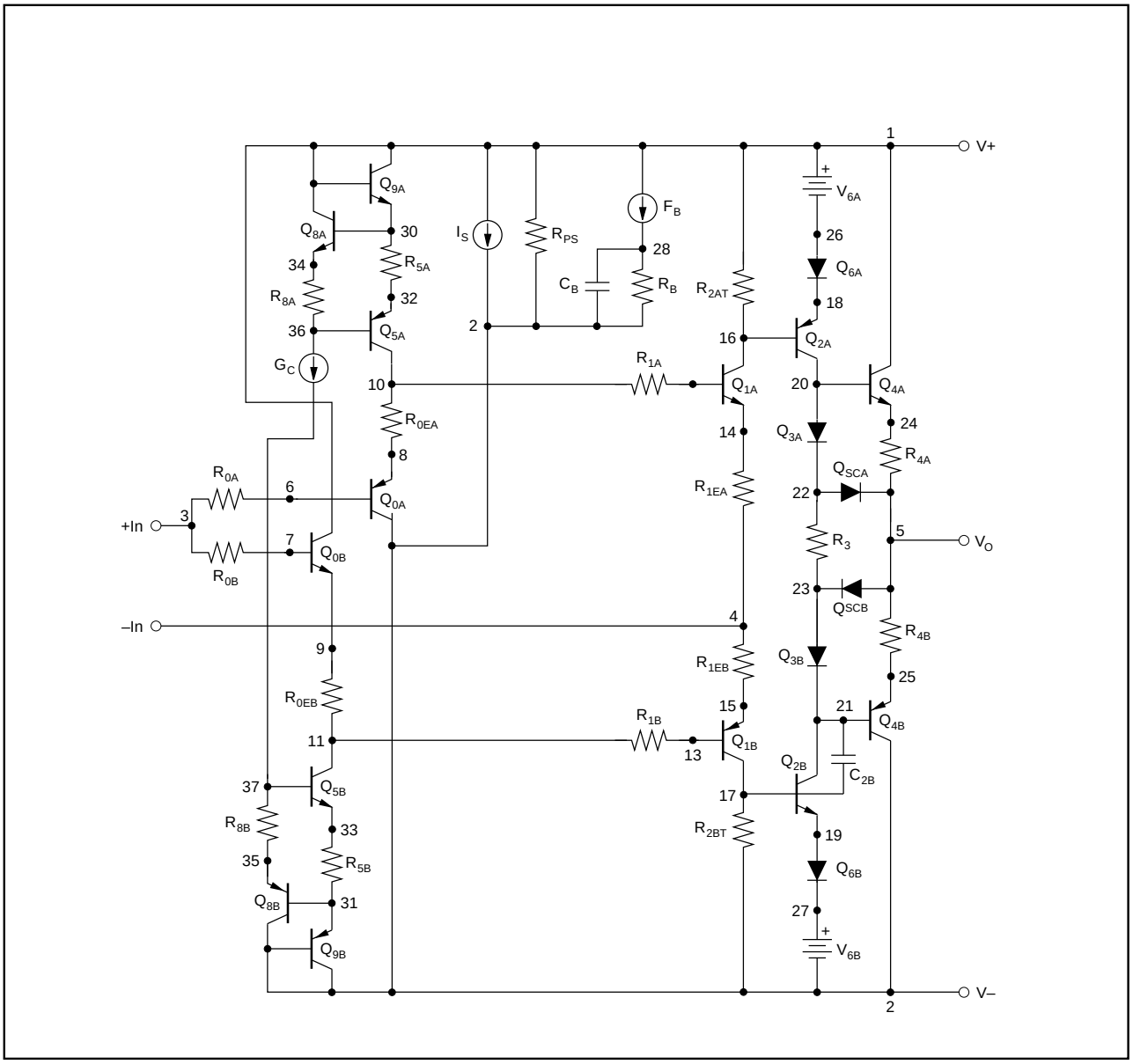
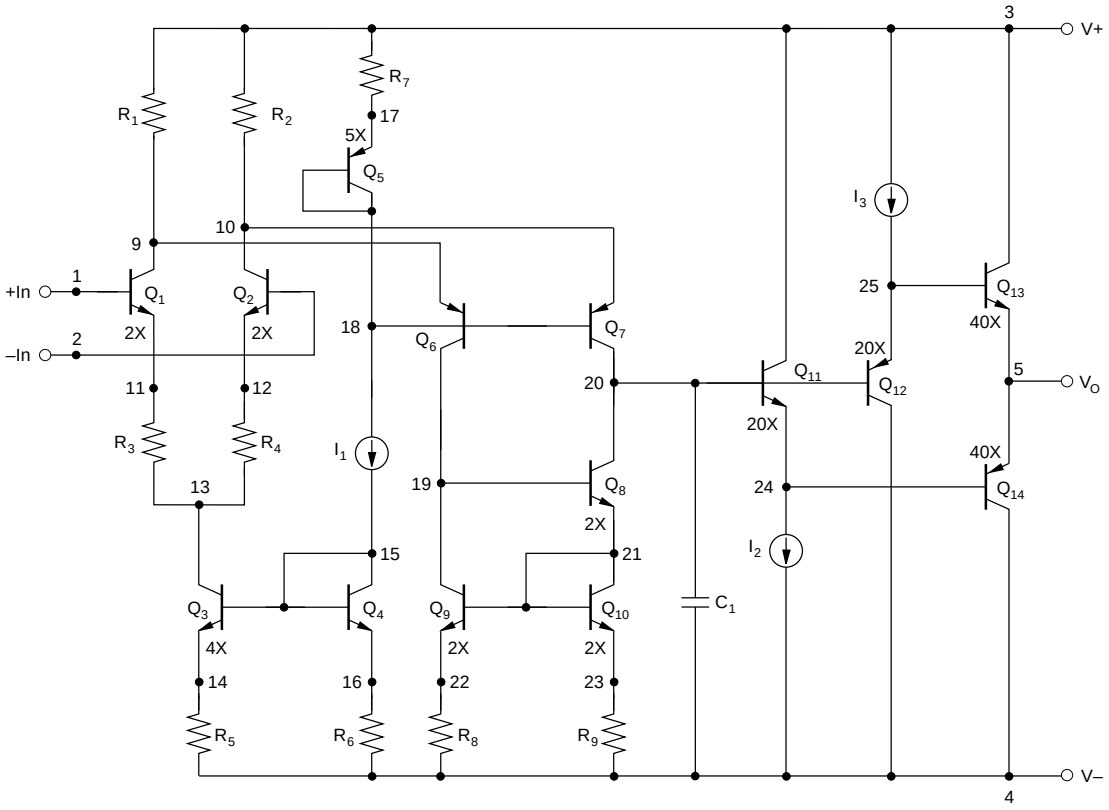


FIGURE D8. OPA603X High Speed Current-Feedback Op Amp Simplified-Circuit Macromodel.



NOTE: OPA620 and OPA621 simplified-circuit macromodels are the same with the following exceptions.

MODEL	C_1 (pF)	I_1 (mA)	I_2 (mA)	I_3 (mA)
OPA620	10	1.1	4	2
OPA621	2	1.3	3.5	3.5

FIGURE D9. OPA620X and OPA621X High Speed Op Amp Simplified-Circuit Macromodel.

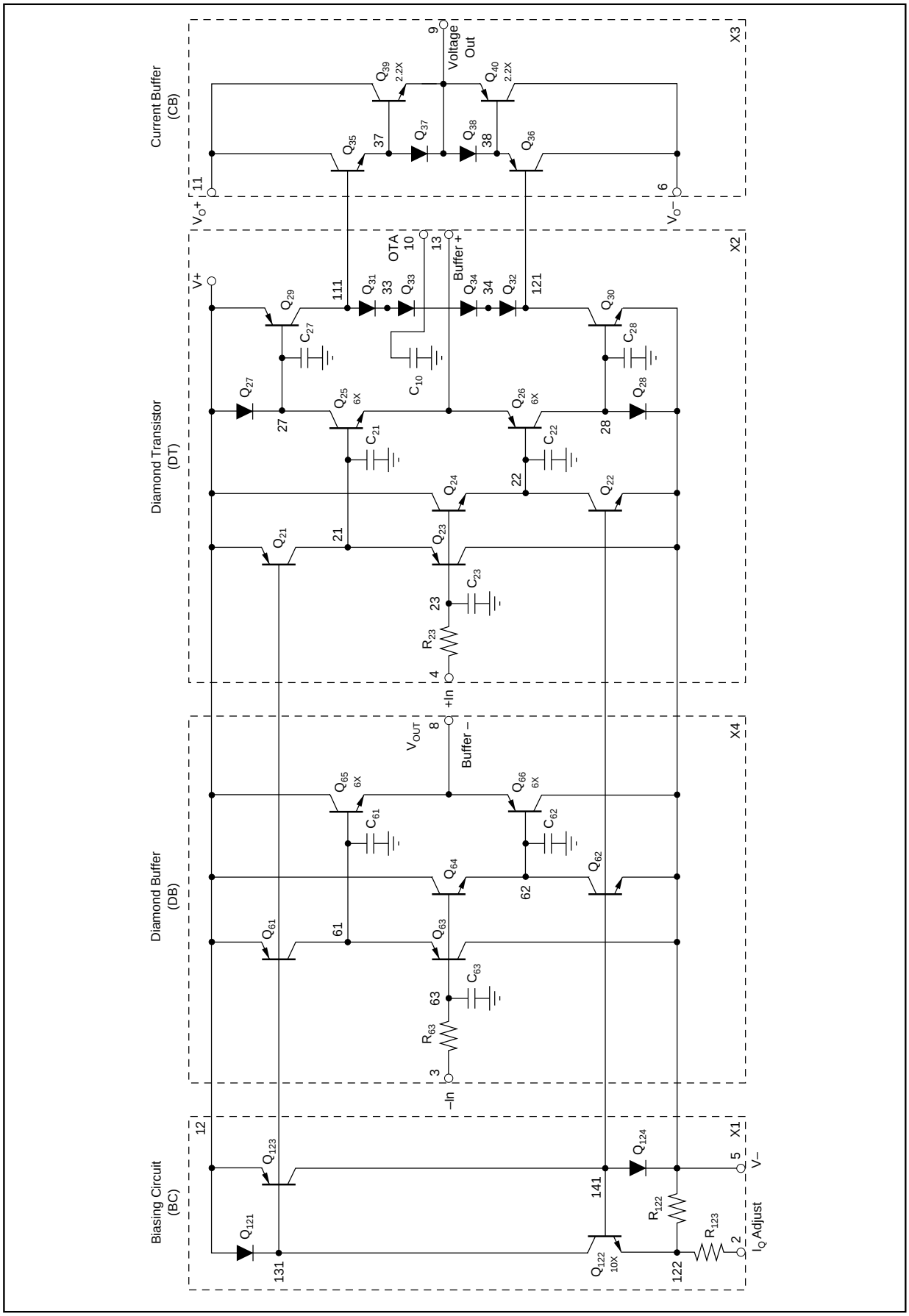


FIGURE D10. OPA622X1 Simplified Circuit Macromodel. Compared to Figure D11, this macromodel is less complex with faster simulation times.

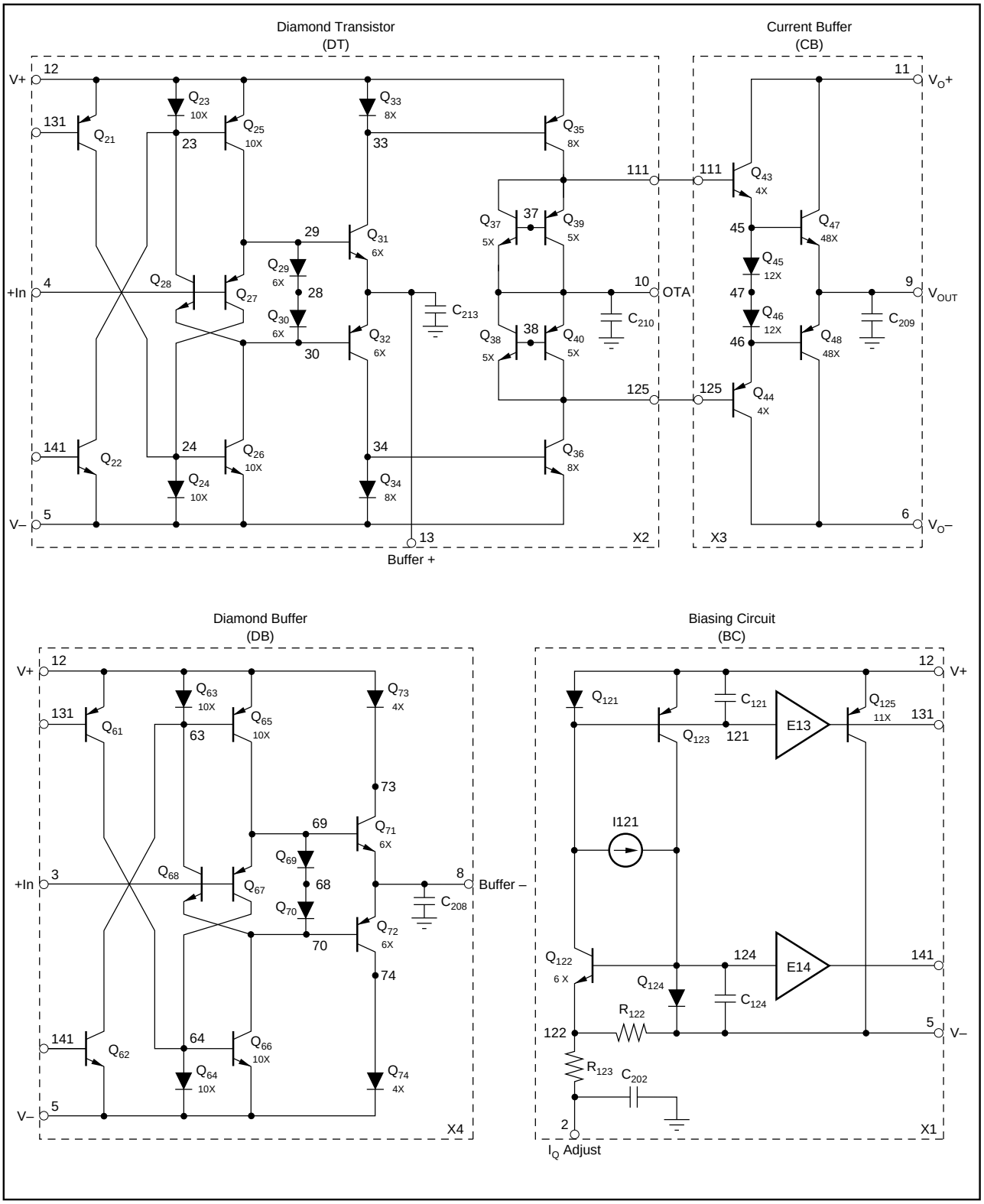


FIGURE D11. OPA622X2 Complex Macromodel. Compared to Figure D10, this macromodel is more complex and requires more simulation time.

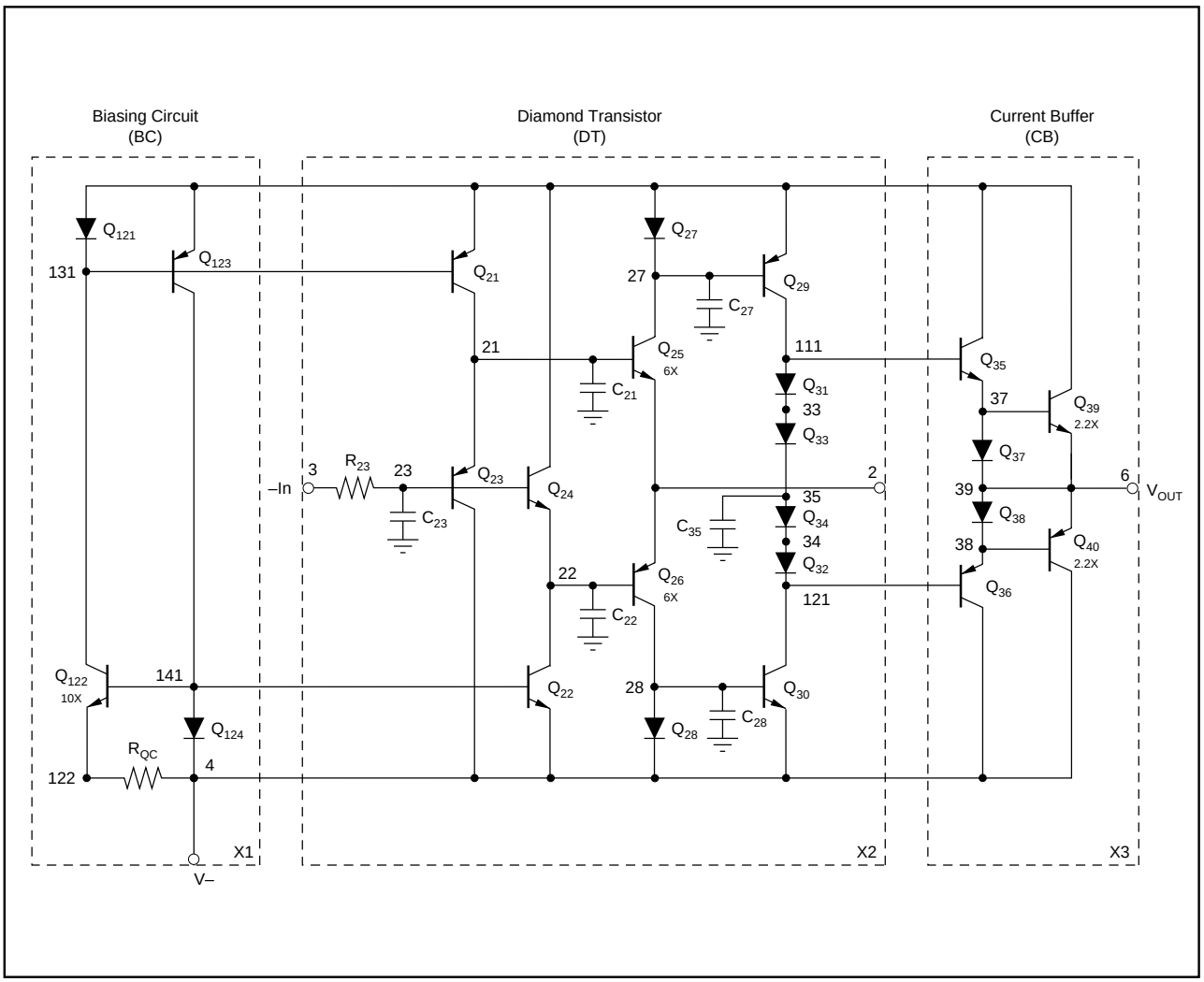


FIGURE D12. OPA623X1 Simplified-Circuit Macromodel. Compared to Figure D13, this macromodel is less complex with faster simulation times.

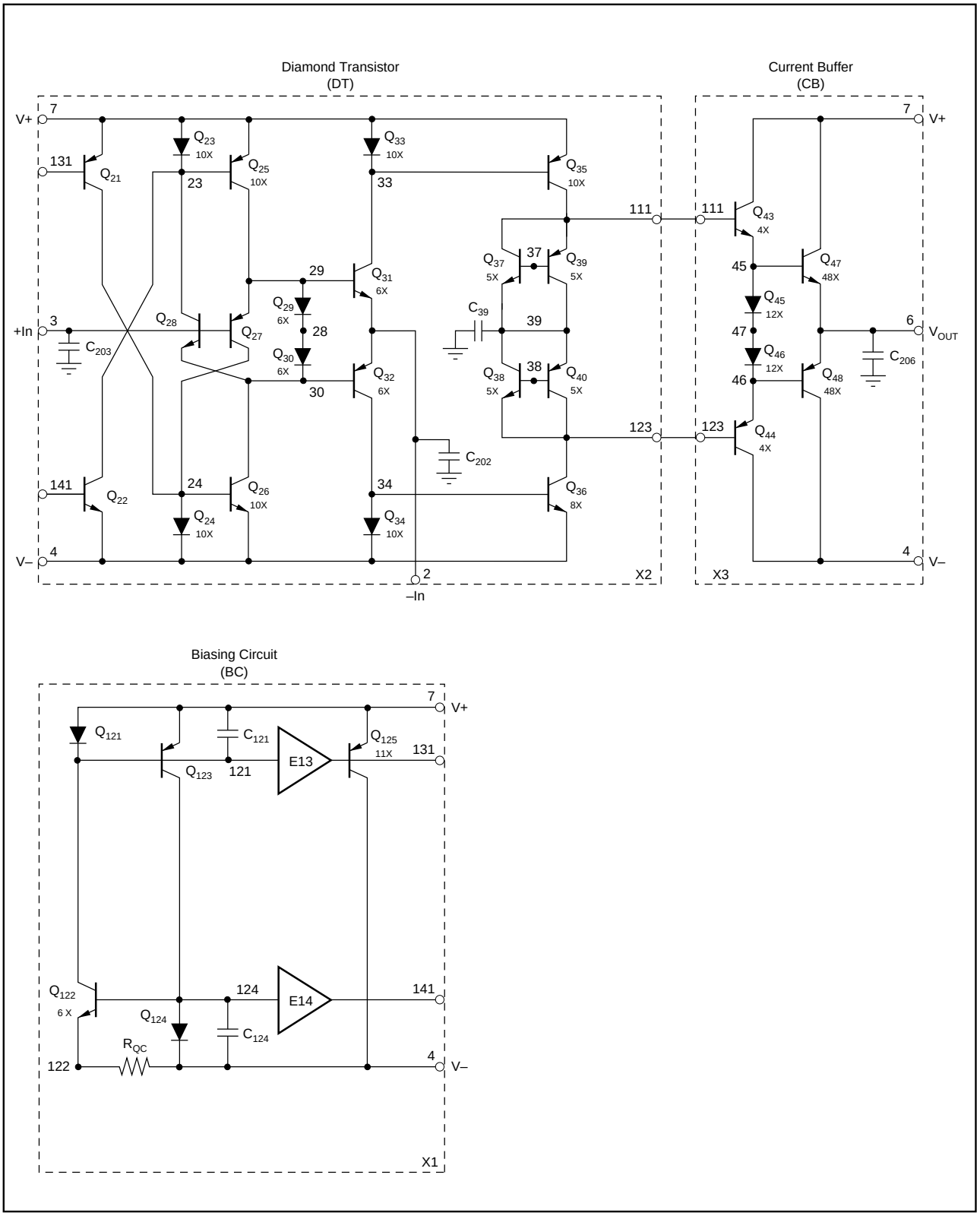


FIGURE D13. OPA623X2 Complex Macromodel. Compared to Figure D12, this macromodel is less complex with faster simulation time.

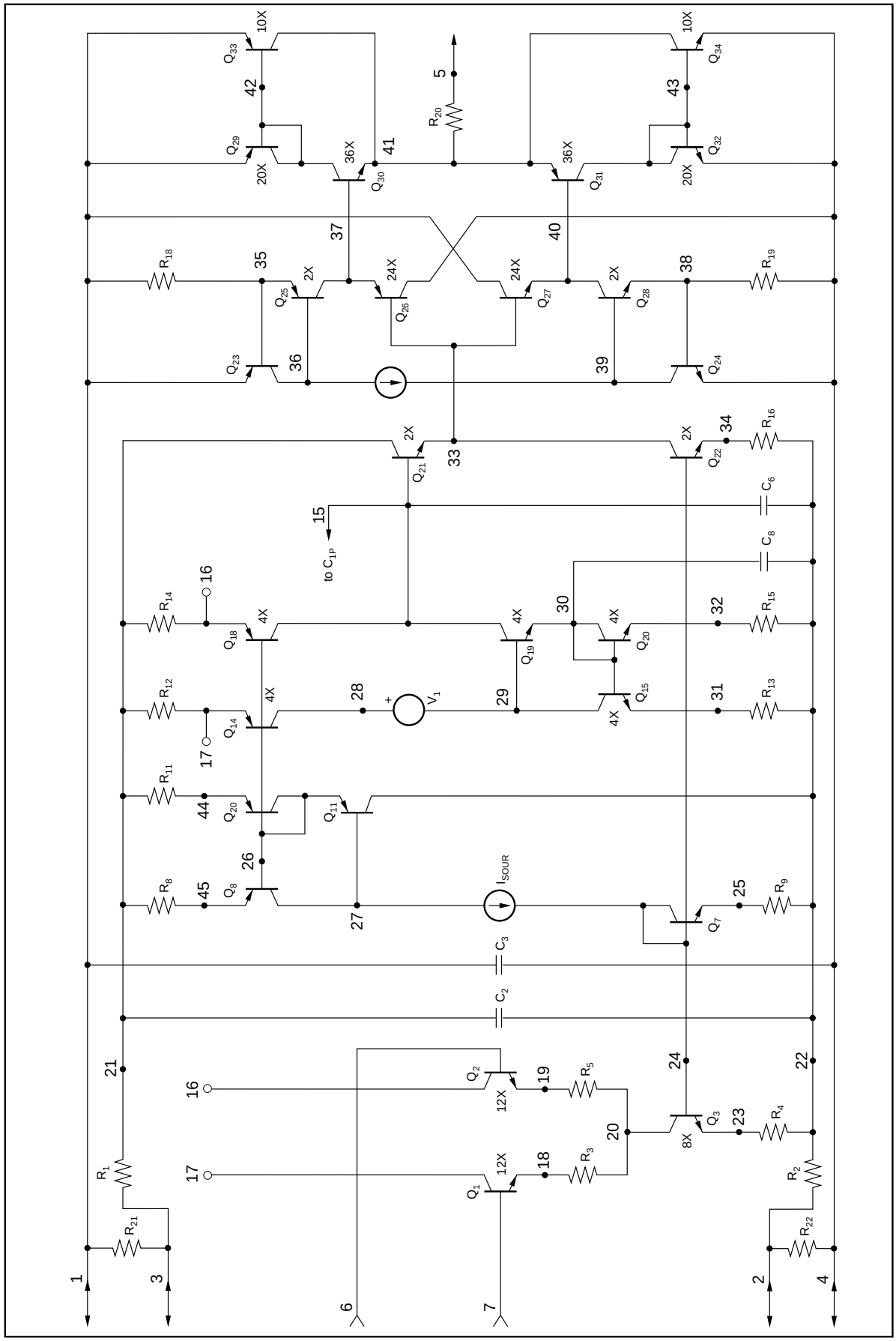


FIGURE D14. OPA640X, OPA641X, Wide Bandwidth Op Amp Simplified-Circuit Macromodel. See Figure D19 for package parasitics.

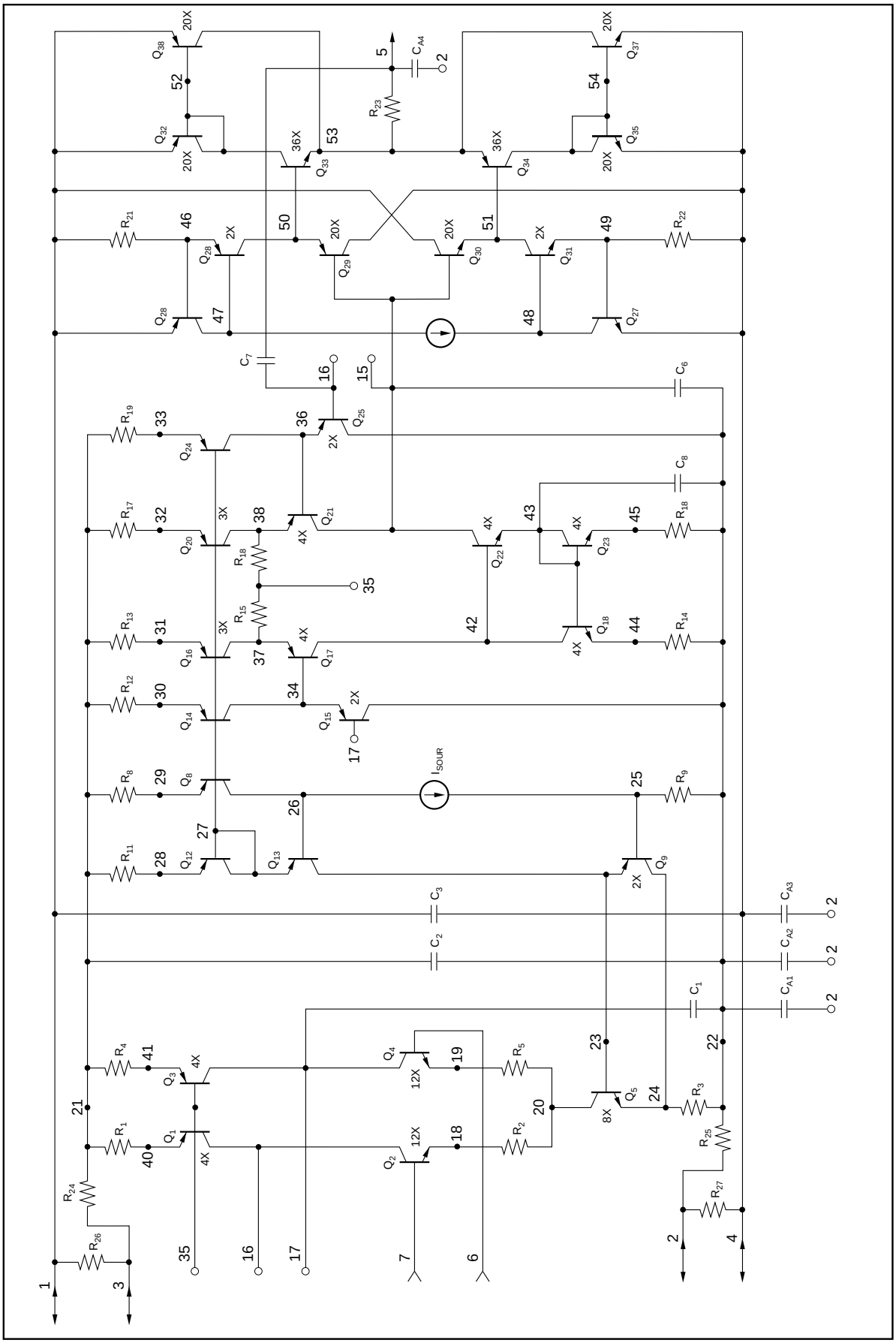


FIGURE D15. OPA642X, OPA643X, Low Distortion, High-Speed Op Amp Simplified-Circuit Macromodel. See Figure D19 for package parasitics.

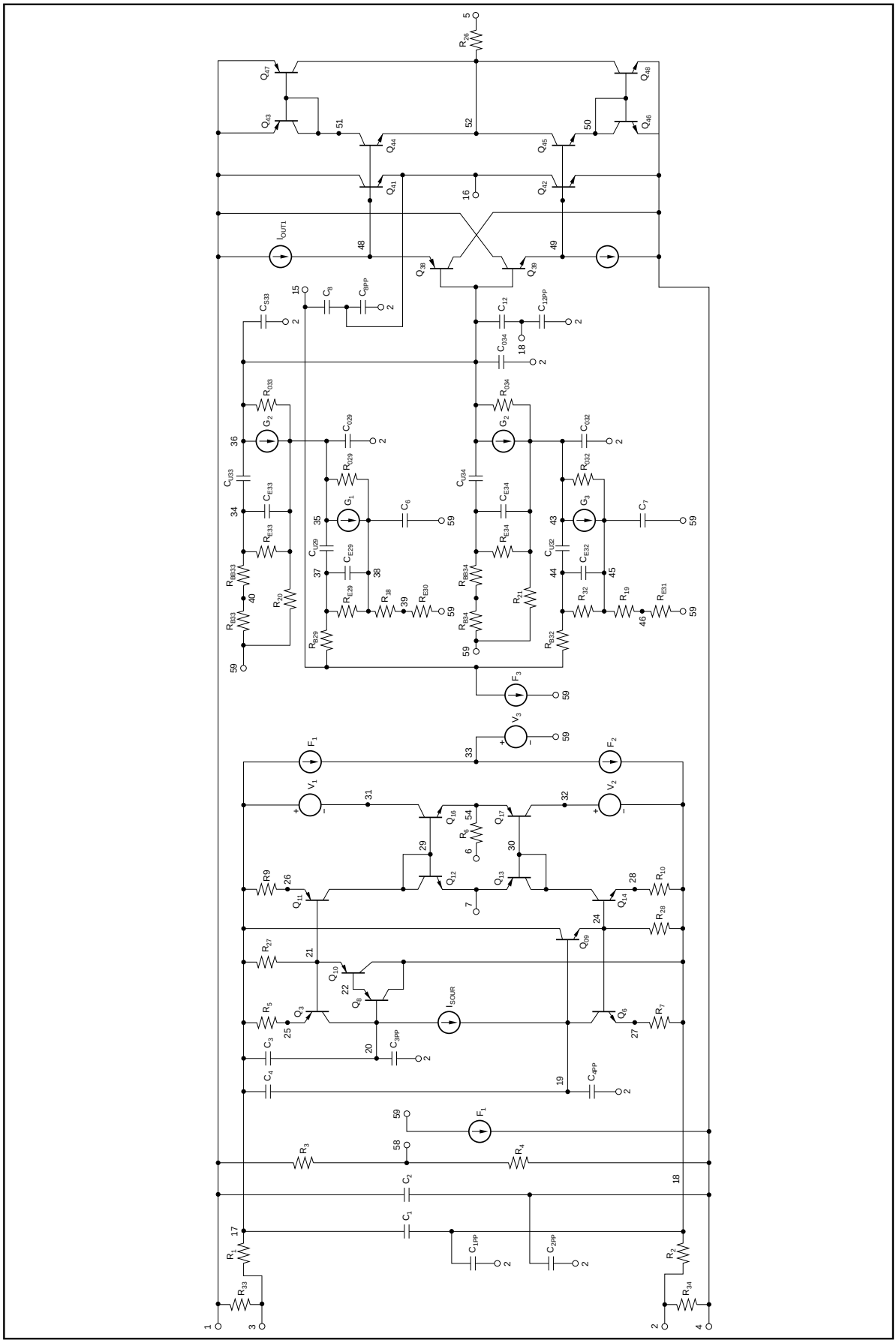


FIGURE 16. OPA644x, High-Speed Op Amp Simplified-Circuit Macromodel. See Figure D19 for package parasitics.

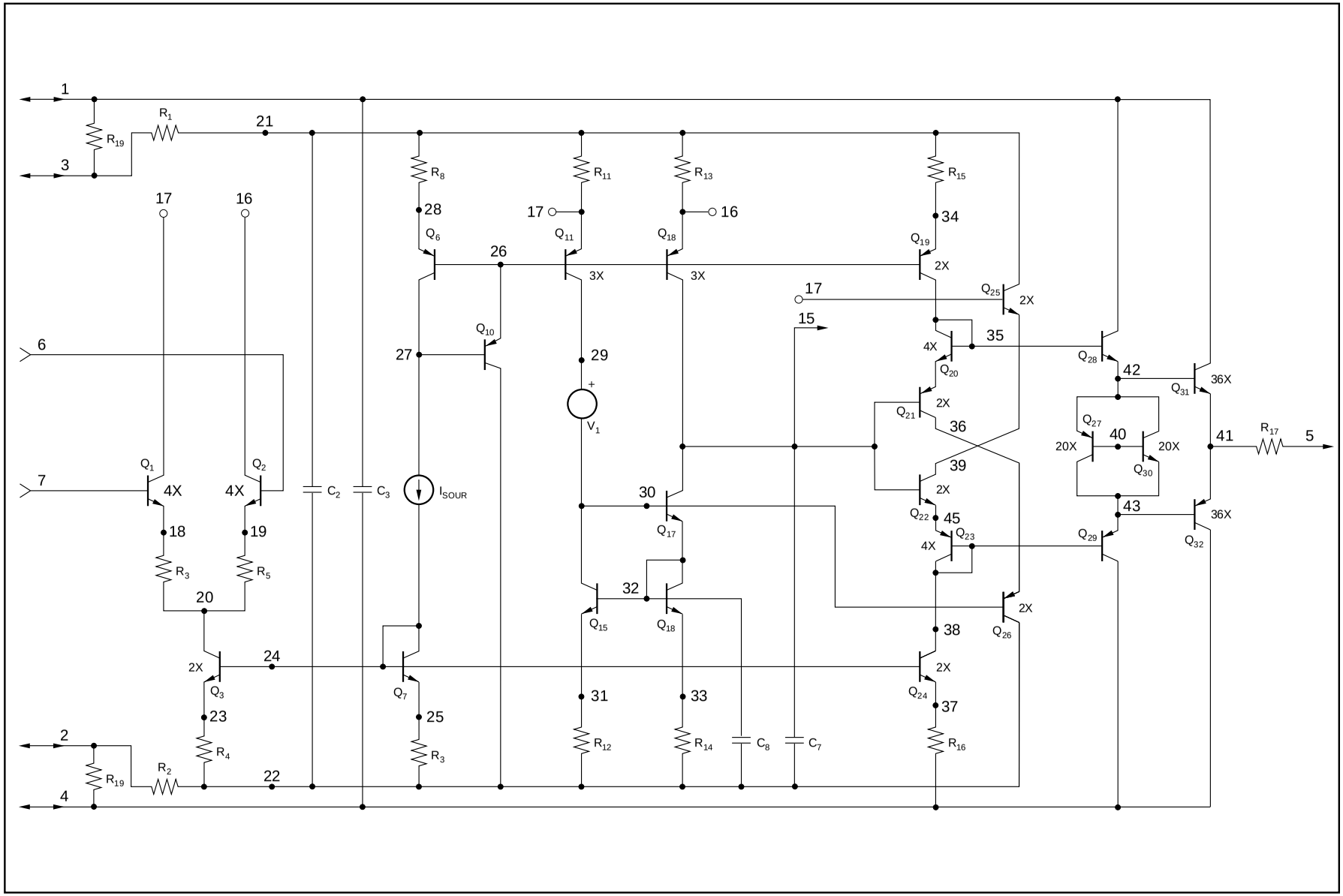


FIGURE D17. OPA646X, Low Power, High-Speed Op Amp Simplified-Circuit Macromodel. See Figure D19 for package parasitics.

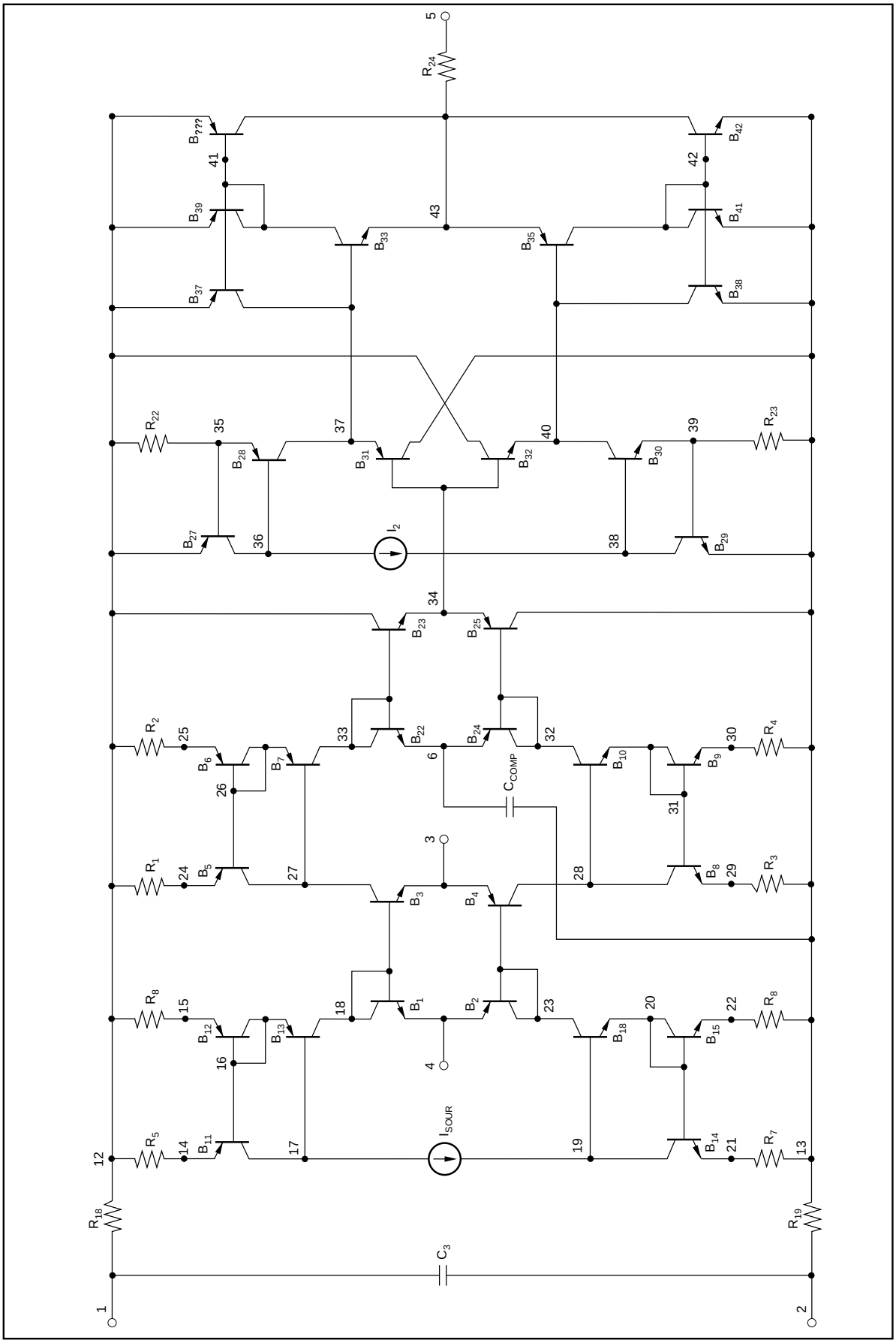


FIGURE D18. OPA648X, High-Speed Op Amp Simplified-Circuit Macromodel.

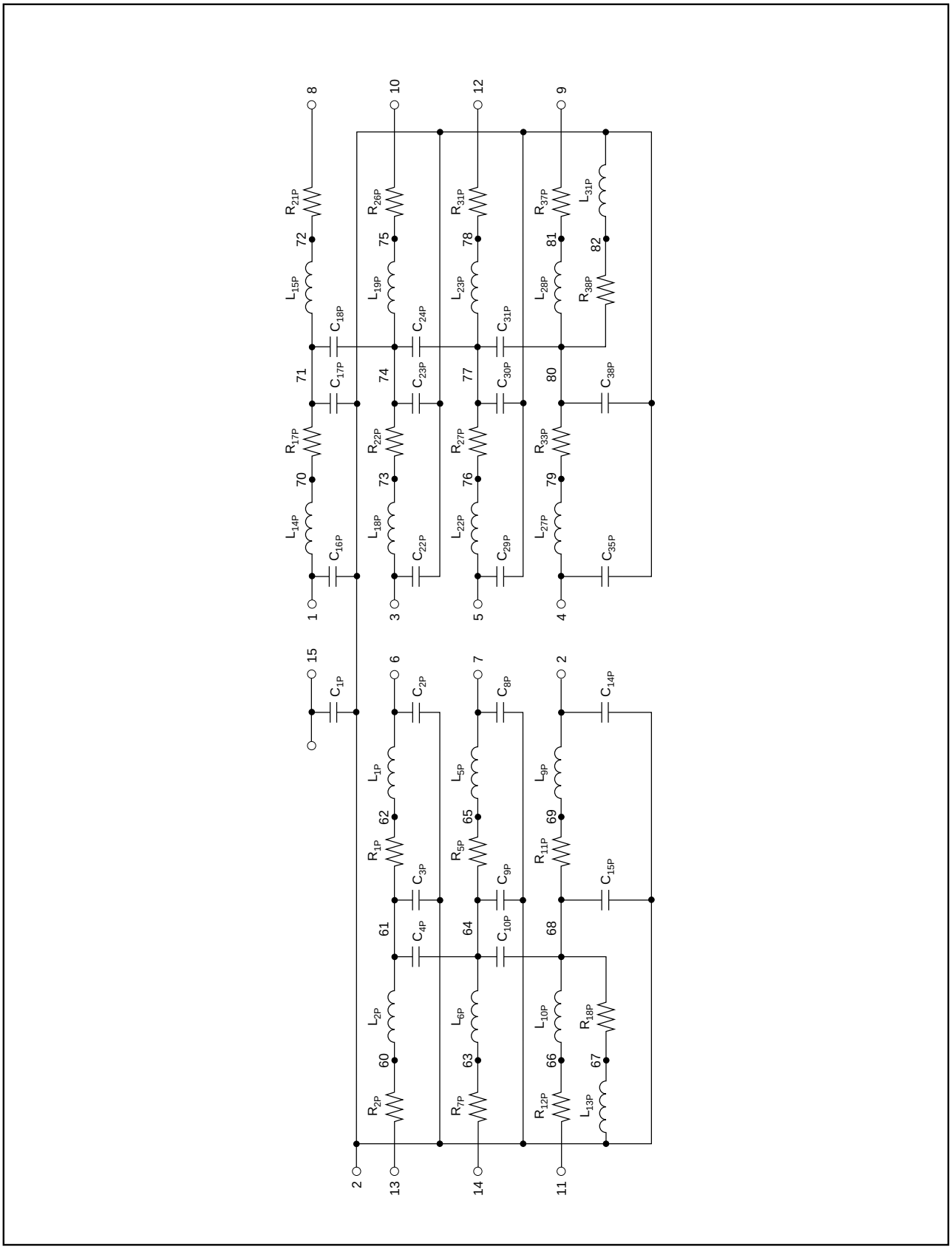


FIGURE D19. Schematic to Model the Pad Parasitics Used for the OPA64X High-Speed Op Amp Series.

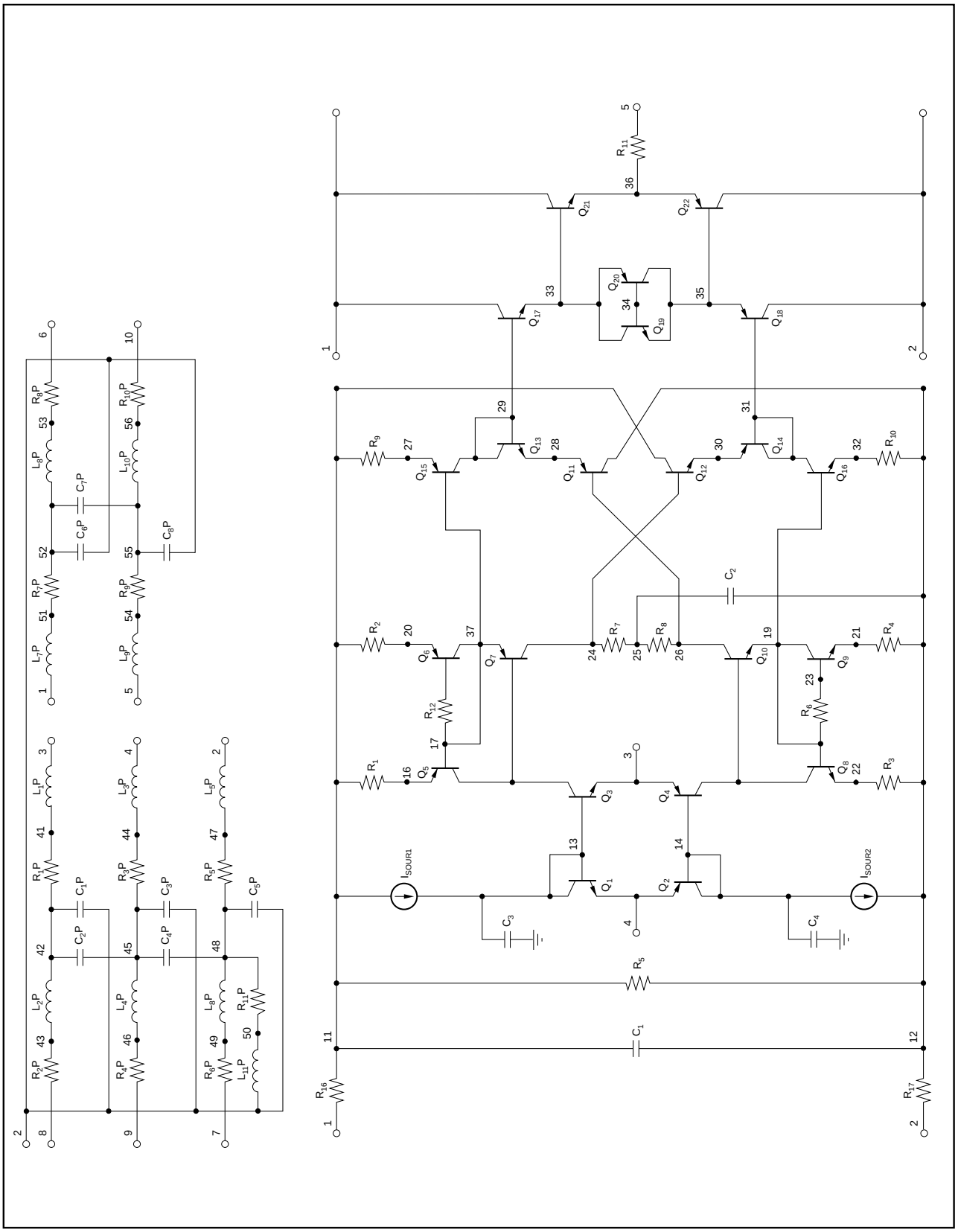


FIGURE D20. OPA658X, OPA2658X and OPA4658 Current-Feedback Wideband Op Amp Simplified-Circuit Macromodel.

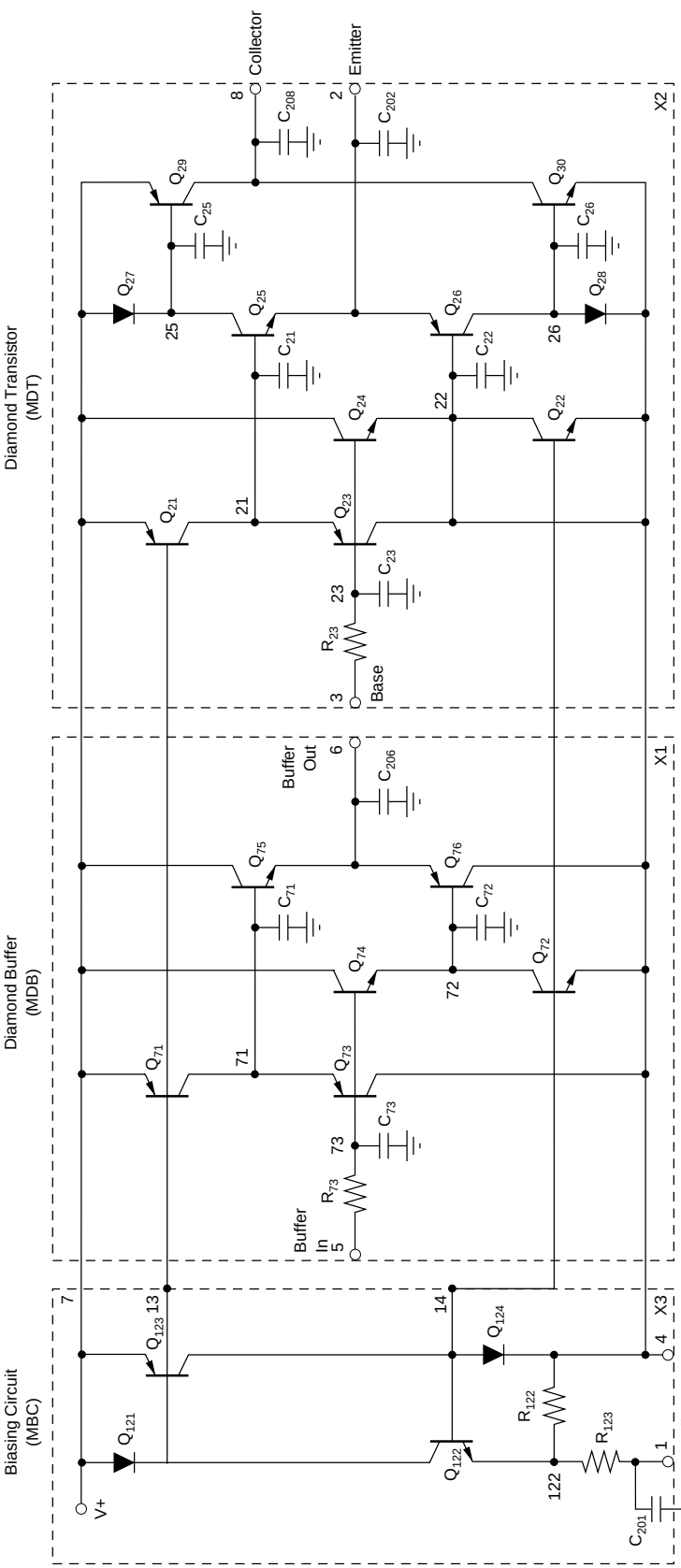


FIGURE D21. OPA660X1 Simplified-Circuit Macromodel. Compared to Figure D22, this macromodel is less complex with faster simulation times.

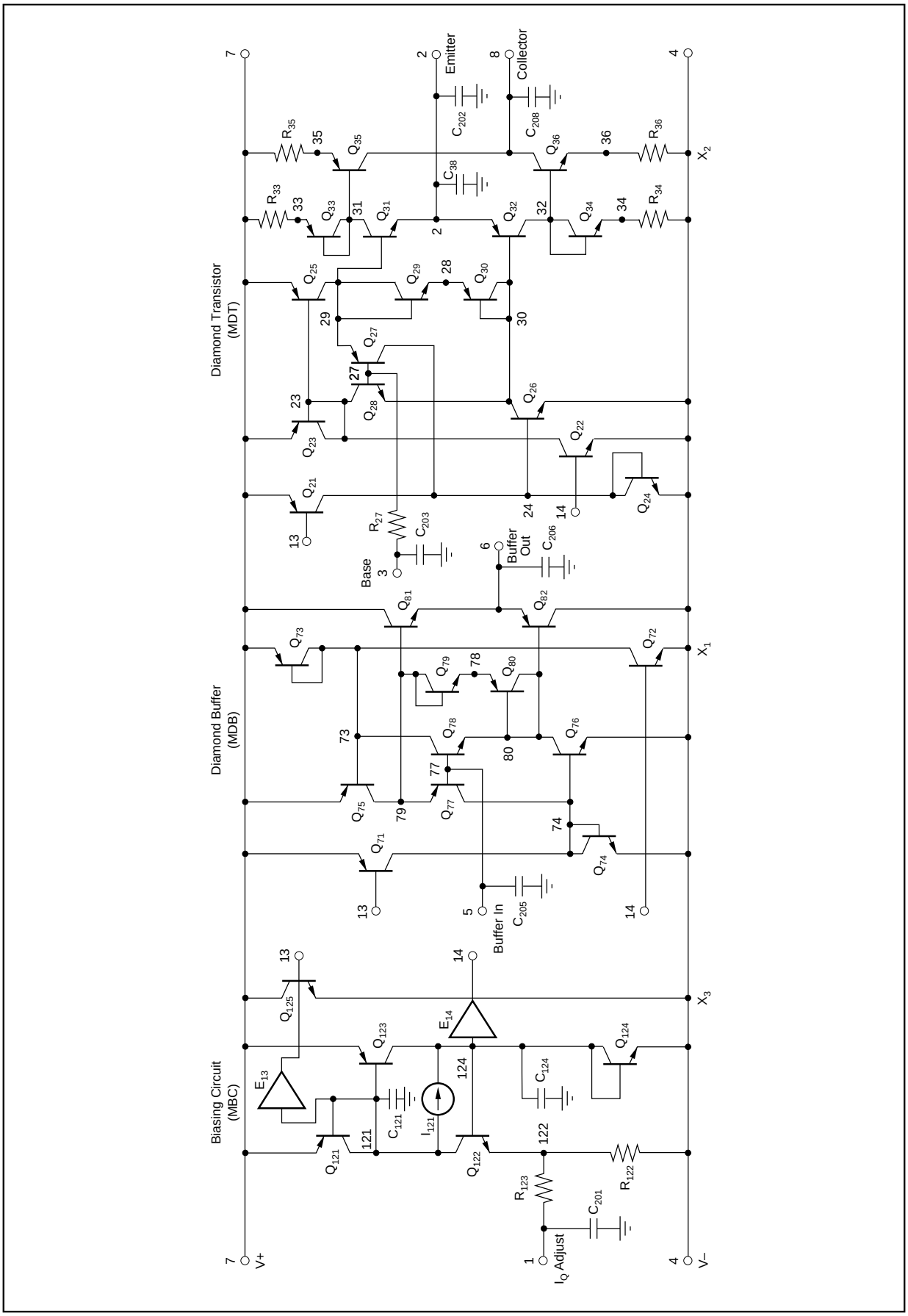


FIGURE D22. OPA660X2 Complex Macromodel. Compared to Figure D21, this macromodel is more complex and requires more simulation time.

MODEL / DEVICE CHARACTERISTICS MODELED	INPUT BIAS CURRENT	INPUT OFFSET CURRENT	OFFSET VOLTAGE	INPUT VOLTAGE NOISE	INPUT CURRENT NOISE	INPUT PROTECTION	INPUT IMPEDANCE	INPUT BIAS CURRENT CORRECTION	OUTPUT RESISTANCE	OUTPUT CURRENT LIMIT	OUTPUT FLOWING FROM POWER SUPPLIES	OUTPUT VOLTAGE SWING	QUIESCENT CURRENT	QUIESCENT CURRENT vs POWER SUPPLY	QUIESCENT CURRENT vs TEMPERATURE	GAIN vs FREQUENCY	GAIN vs TEMPERATURE	PHASE RESPONSE	CMRR vs FREQUENCY	PSRR	PSRR vs FREQUENCY	SLEW RATE	PAD PARASITICS	NO GROUND REFERENCE	COMMENTS	FIGURE
ACF2101M	X	NA	X			X	X	X	X	X	X	X	X	X		X		X				X			7	C6,7
BUF600X1	X	NA					X	NA	X		X	X	X			X		X				X			10, 14	D1
BUF600X2	X	NA		X	X		X	NA	X		X	X	X			X		X		X	X	X			10, 14	D2
BUF601X1	X	NA					X	NA	X		X	X	X			X		X				X			10, 14	D1
BUF601X2	X	NA		X	X		X	NA	X		X	X	X			X		X		X	X	X			10, 14	D2
BUF634X	X						X		X		X	X	X			X		X				X			1	D3
INA101	X								X	X		X	X			X		X	X			X			1	2
INA101E	X					X	X		X	X	X	X	X	X		X		X	X			X			1	2
INA102	X								X	X		X	X			X		X	X			X			1	2
INA102E	X						X		X	X	X	X	X	X		X		X	X			X			1	2
INA103	X							X	X	X		X	X			X		X	X			X			1	3
INA103E	X						X	X	X	X	X	X	X	X		X		X	X			X			1	3
INA105	X								X	X		X	X			X		X	X			X			2	1a
INA105E	X								X	X	X	X	X	X		X		X	X			X			2	1a
INA106	X								X	X		X	X			X		X	X			X			2	1a
INA106E	X								X	X	X	X	X	X		X		X	X			X			2	1a
INA110	X							X	X	X		X	X			X		X	X			X			1	5
INA110E	X						X	X	X	X	X	X	X	X		X		X	X			X			1	5
INA111	X							X	X	X		X	X			X		X	X			X			1	2
INA111E	X						X	X	X	X	X	X	X	X		X		X	X			X			1	2
INA114	X								X	X		X	X			X		X	X			X			1	2
INA114E	X					X	X		X	X	X	X	X	X		X		X	X			X			1	2
INA115	X								X	X			X			X		X				X				2
INA115E	X						X	X	X	X	X		X	X		X		X	X			X				2
INA117	X								X	X		X	X			X		X	X			X			2	16
INA117E	X								X	X	X	X	X	X		X		X	X			X			2	16
INA118	X								X	X		X	X			X		X				X				4
INA118E	X						X		X	X	X	X	X	X		X		X				X				4
INA120	X							X	X	X		X	X			X		X	X			X			1	6
INA120E	X					X	X	X	X	X	X	X	X	X		X		X	X			X			1	6
INA131	X								X	X			X			X		X				X				2
INA131E	X						X	X	X	X	X		X	X		X		X	X			X				2
ISO120X	NA	NA	X				X					X	X			X									4	D4
ISO121X	NA	NA	X				X					X	X			X									4	D4
ISO130X																										D5
MPC100X1				X	X		X		X		X	X	X	X		X		X		X	X	X			14, 10	D6
MPC100X2							X		X		X	X	X	X		X		X				X			14, 10	D7
MPC102X1							X		X		X	X	X	X		X		X				X			14, 10	D6
MPC104X1							X		X		X	X	X	X		X		X				X			14, 10	D6
OPA1013	X								X	X		X	X			X		X				X				A6
OPA1013E	X						X			X	X	X	X	X		X		X				X				B4
OPA111	X							X	X	X		X	X			X		X				X				A4
OPA111E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA121	X							X	X	X		X	X			X		X				X				A4
OPA121E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA124	X							X	X	X		X	X			X		X				X				A4
OPA124E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA128	X						X	X	X		X	X				X		X				X				A4
OPA128E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA129	X						X	X	X		X	X				X		X				X				A4
OPA129E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA131	X						X	X	X		X	X				X		X				X				
OPA131E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				
OPA177	X								X	X		X	X			X		X				X				A5
OPA177E	X					X	X		X	X	X	X	X	X		X		X				X				B6

TABLE X. Parameters Modeled by the Standard, Enhanced, Multiple Pole/Zero, and Simplified Circuit Macromodel.

MODEL / DEVICE CHARACTERISTICS MODELED	INPUT BIAS CURRENT	INPUT OFFSET CURRENT	OFFSET VOLTAGE	INPUT VOLTAGE NOISE	INPUT CURRENT NOISE	INPUT PROTECTION	INPUT IMPEDANCE	INPUT BIAS CURRENT CORRECTION	OUTPUT RESISTANCE	OUTPUT CURRENT LIMIT	OUTPUT FLOWING FROM POWER SUPPLIES	OUTPUT VOLTAGE SWING	QUIESCENT CURRENT	QUIESCENT CURRENT vs POWER SUPPLY	QUIESCENT CURRENT vs TEMPERATURE	GAIN vs FREQUENCY	GAIN vs TEMPERATURE	PHASE RESPONSE	CMRR vs FREQUENCY	PSRR	PSRR vs FREQUENCY	SLEW RATE	PAD PARASITICS	NO GROUND REFERENCE	COMMENTS	FIGURE
OPA2107	X							X	X	X		X	X			X		X				X				A4
OPA2107E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA2111	X							X	X	X		X	X			X		X				X				A4
OPA2111E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA2131	X						X	X	X		X	X				X		X				X				
OPA2131E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				
OPA2541	X							X	X	X		X	X			X		X				X				A4
OPA2541E	X						X	X	X	X	X	X	X	X		X		X				X				B2
OPA2604	X							X	X	X		X	X			X		X				X				A4
OPA2604E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA2604M	X	X	X				X	X	X	X	X	X	X	X		X		X	X			X		X		C2, 5
OPA2658X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X		D20
OPA27	X								X	X		X	X			X		X				X				A5
OPA27E	X					X	X		X	X	X	X	X	X		X		X				X				B4
OPA27M	X	X	X				X		X	X	X	X	X	X		X		X	X			X		X		C3, 5
OPA37	X								X	X		X	X			X		X				X				A5
OPA37E	X					X	X		X	X	X	X	X	X		X		X				X				B4
OPA404	X							X	X	X		X	X			X		X				X				A4
OPA404E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA445	X							X	X	X		X	X			X		X				X				A4
OPA445E	X						X	X	X	X	X	X	X	X		X		X				X				B2
OPA4131	X						X		X	X		X	X			X		X				X				
OPA4131E	X						X	X	X	X	X	X	X			X		X				X				
OPA4658X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X		D20
OPA501	X							X	X	X		X	X			X		X				X				A5
OPA501E	X						X	X	X	X	X	X	X	X		X		X				X				B4
OPA502	X							X	X	X		X	X			X		X				X				A3
OPA502E	X						X	X	X	X	X	X	X	X		X		X				X				B4
OPA511	X							X	X	X		X	X			X		X				X				A4
OPA511E	X						X	X	X	X	X	X	X	X		X		X				X				B2
OPA512	X							X	X	X		X	X			X		X				X				A4
OPA512E	X						X	X	X	X	X	X	X	X		X		X				X				B2
OPA541	X							X	X	X		X	X			X		X				X				A4
OPA541E	X						X	X	X	X	X	X	X	X		X		X				X				B2
OPA602	X							X	X	X		X	X			X		X				X				A4
OPA602E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA603X	X						X		X	X	X	X	X	X		X		X				X		X	9	D8
OPA604	X							X	X	X		X	X			X		X				X				A4
OPA604E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA604M	X	X	X				X	X	X	X	X	X	X	X		X		X	X			X		X		C2, 5
OPA606	X							X	X	X		X	X			X		X				X				A4
OPA606E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA620	X								X	X		X	X			X		X				X				A5
OPA620E	X						X		X	X	X	X	X	X		X		X				X				B4
OPA620X	X	X		X	X		X		X		X		X			X		X				X		X	8	D9
OPA621	X								X	X		X	X			X		X				X				A5
OPA621E	X						X		X	X	X	X	X	X		X		X				X				B4
OPA621X	X	X		X	X		X		X		X		X			X		X				X		X	8	D9
OPA622X1	X	NA					X	NA	X		X	X	X			X		X				X			10, 14	D10
OPA622X2	X	NA		X	X		X	NA	X		X	X	X			X		X	X	X	X	X			10, 14	D11
OPA623X1	X	NA					X	NA	X		X	X	X			X		X				X			10, 14	D12
OPA623X2	X	NA		X	X		X	NA	X		X	X	X			X		X	X	X	X	X			10, 14	D13
OPA627	X							X	X	X		X	X			X		X				X				A4
OPA627E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA628M	X	X	X				X		X	X	X	X	X	X		X		X	X			X		X		C3

TABLE X (cont). Parameters Modeled by the Standard, Enhanced, Multiple Pole/Zero, and Simplified Circuit Macromodel.

DEVICE CHARACTERISTICS MODELED / MODEL	INPUT BIAS CURRENT	INPUT OFFSET CURRENT	OFFSET VOLTAGE	INPUT VOLTAGE NOISE	INPUT CURRENT NOISE	INPUT PROTECTION	INPUT IMPEDANCE	INPUT BIAS CURRENT CORRECTION	OUTPUT RESISTANCE	OUTPUT CURRENT LIMIT	OUTPUT FLOWING FROM POWER SUPPLIES	OUTPUT VOLTAGE SWING	QUIESCENT CURRENT	QUIESCENT CURRENT vs POWER SUPPLY	QUIESCENT CURRENT vs TEMPERATURE	GAIN vs FREQUENCY	GAIN vs TEMPERATURE	PHASE RESPONSE	CMRR vs FREQUENCY	PSRR	PSRR vs FREQUENCY	SLEW RATE	PAD PARASITICS	NO GROUND REFERENCE	COMMENTS	FIGURE
OPA637	X							X	X	X		X	X			X		X				X				A4
OPA637E	X			X	X		X	X	X	X	X	X	X	X		X		X				X				B2
OPA640X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D14
OPA641X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D14
OPA642X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D15
OPA643X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D15
OPA644X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D16
OPA646X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D17
OPA648X	X	X	X	X	X		X	X	X	X	X	X	X			X		X	X	X	X	X	X	X	8, 12	D18
OPA660X1	X	NA					X	NA	X		X	X	X			X		X	X	X	X	X				D21
OPA660X2	X	NA		X	X	X	X	NA	X		X	X	X			X		X	X	X	X	X			10, 14, 5	D22
OPA671M	X	X	X				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		C2, 5
OPA675M	X	X	X				X		X	X	X	X	X	X		X		X	X			X	X	X	6	C8, C9
OPA676M	X	X	X				X		X	X	X	X	X	X		X		X	X			X	X	X	6, 11	C8, C9
OPA77	X								X	X		X	X			X		X				X				A5
OPA77E	X					X	X		X	X	X	X	X	X		X		X				X				B6
OPT101									X	X		X	X			X		X				X				A2
OPT201									X	X		X	X			X		X				X				A2
OPT202									X	X		X	X			X		X				X				A2
OPT209									X	X		X	X			X		X				X				A2
UAF42	X							X	X	X		X	X			X		X				X			3	A4
UAF42E	X						X	X	X	X	X	X	X	X		X		X				X			3	B2
VCA610M	X						X		X	X	X	X	X			X								X	13	C10

COMMENTS: 1. Instrumentation Amplifier. 2. Difference Amplifier. 3. All four op amps in the UAF42 chip are identical. This model only contains one op amp. 4. Also models isolation barrier impedance. 5. Also models enable transient response and the quiescent resistor transient response. 6. Also has the input control switch and models its transient response. 7. Model includes HOLD, RESET and SELECT switches and internal capacitor. 8. Also models total harmonic distortion. 9. Also models bias current vs power supply and bias current vs common-mode. 10. Also models group delay time. 11. Also models TTL switching times. 12. Also models output recovery time. 13. Also models gain control vs frequency. 14. Contact the factory for a more detailed description of this macromodel 800 548-6132 or FAX (602) 746-7852.

TABLE X (cont). Parameters Modeled by the Standard, Enhanced, Multiple Pole/Zero, and Simplified Circuit Macromodel.

PRODUCT NOTES

For more information please refer to the individual data sheet.

ACF2101
SWITCHED INTEGRATOR

The integrator output voltage range is from +0.5V to –10V. The output voltage (V_{OUT}) can be calculated as:

$$V_{OUT} = -\frac{1}{C_{INT}}\int i_{IN}\, dt$$

V_{OUT} = the output voltage of the ACF2101
C_{INT} = the integration capacitor (in farads)
i_{IN} = the input current (in amperes)
dt = the integration time (in seconds)

INA101
INSTRUMENTATION AMPLIFIER

The INA101 contains internal gain-setting feedback resistors;

$$R_{FB} = 20k\Omega$$

When using the metal package (TO-100), these resistors must be used. When using the ceramic or plastic packages, the internal gain-setting feedback resistors may be used, or external feedback resistors may be used.

If the internal resistors are used:

$$GAIN = 1 + (40k/R_G)$$

If external feedback resistors are used:

$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:
R_G = external gain-setting resistor (Ω)
R_{FB} = optional external feedback resistor (Ω)

INA102
INSTRUMENTATION AMPLIFIER

The INA102 contains internal gain-setting and feedback resistors;

$$R_{FB} = 20k\Omega$$

INA102 INTERNAL GAIN-SETTING RESISTORS

R_G (Ω)	GAIN (V/V)
4.444k	10
404	100
40.4	1000

The internal resistors are ratio trimmed to high accuracy and have excellent tracking with temperature for low gain drift. If the internal resistors are used:

$$GAIN = 1 + (40k/R_G)$$

External gain-setting resistors can be used in series with one of the internal gain-setting resistors. If external gain-setting resistors are used:

$$GAIN = 1 + (40k/[R_{GI} + R_{GE}])$$

R_{GI} = One of the three internal gain-setting resistors shown in the table (Ω)
R_{GE} = external gain-setting resistor (Ω)

INA103
INSTRUMENTATION AMPLIFIER

The INA103 contains internal gain-setting and feedback resistors:

$$R_{FB} = 3k\Omega$$
$$R_G = 60.606\Omega \text{ (Gain = 100)}$$

The internal gain-setting feedback resistors may be used, or external feedback resistors may be used.

If the internal resistors are used:

$$GAIN = 1 + (6k/R_G)$$

If external feedback resistors are used:

$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:
R_G = Optional external gain-setting resistor (Ω)
R_{FB} = Optional external feedback resistor (Ω)

INA110
INSTRUMENTATION AMPLIFIER

INA110 INTERNAL GAIN-SETTING RESISTORS

R_G (w)	GAIN (V/V)
4.444K	10
404.04	100
201.0	200
80.16	500

The INA110 contains internal gain-setting and feedback resistors;

$$R_{FB} = 20k\Omega$$

The internal resistors are ratio trimmed to high accuracy and have excellent tracking with temperature for low gain drift. If the internal resistors are used:

$$GAIN = 1 + (40k/R_G)$$

External gain-setting resistors can be used in series with one of the internal gain-setting resistors. If external gain-setting resistors are used:

$$GAIN = 1 + (40k/R_{GI} + R_{GE}])$$

R_{GI} =one of the four above internal gain-setting resistors (Ω)
R_{GE} = external gain-setting resistor (Ω)

INA111
INSTRUMENTATION AMPLIFIER

The INA111 contains internal gain-setting feedback resistors;

$$R_{FB} = 25k\Omega$$

External gain-setting resistors are used to set the gain at:

$$GAIN = 1 + (50k/R_G)$$

R_G = external gain resistor (Ω)

INA120
INSTRUMENTATION AMPLIFIER

The INA120 contains an internal gain-setting and feedback resistor string;

$$R_{FB} = 20k\Omega$$

INA120 INTERNAL GAIN-SETTING RESISTORS

R_G [Ω]	GAIN [V/V]
4000	10
400	100
44	1000

The internal resistors are ratio-trimmed to high accuracy and have excellent tracking with temperature for low gain drift. If the internal gain-setting resistor string is used, it can be connected to the amplifier input terminals to give accurate gains of 1, 10, 100, and 1000. The gain equation is the same as for external gain-setting resistors, but in higher gains, part of the lower gain-setting resistor is added to the feedback resistor so the values shown for R_G can not be inserted directly in the equation—see Figure 10.

The internal feedback resistors can be used with external feedback resistors. If the internal feedback resistors are used with external gain-setting resistors:

$$GAIN = 1 + (40k/R_G)$$

Where:

R_G = optional gain-setting resistor (Ω) connected between G_5 and G_{14} with G_{11} open

External gain-setting and feedback resistors can be used. If external feedback resistors are used:

$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:

R_G = Optional external gain-setting resistor (Ω)

R_{FB} = Optional external feedback resistor (Ω)

OPA111
OPERATIONAL AMPLIFIER

The OPA111 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was used in the macromodel.

OPA121
OPERATIONAL AMPLIFIER

The OPA121 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was used in the macromodel.

OPA660
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

This device includes a voltage-controlled current source and a voltage buffer. The voltage-controlled current source or Operational Transconductance Amplifier can be viewed as an “ideal transistor”. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain tradeoffs to be optimized. Demo boards are available.

OPA675
SWITCHED-INPUT OPERATIONAL AMPLIFIER

The OPA675 is a “classical” high-speed amplifier that has two differential input stages. Each stage is selectable with ECL logic.

OPA676
SWITCHED-INPUT OPERATIONAL AMPLIFIER

The OPA676 is a “clasical” high-speed amplifier that has two differential input stages. Each stage is selectable with TTL logic.

OPA2111
DUAL OPERATIONAL AMPLIFIER

The OPA2111 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was used in the macromodel.

TABLE XI. Content of the Macromodel Disk, Revision F, Listed by Topology Level and Directory. New models in bold.

CONTENT OF MACROMODEL DISK

LEVEL I STD_MOD		LEVEL II STD_MOD		LEVEL III STD_MOD	LEVEL IV STD_MOD	
INA101	OPA404	INA101E	OPA404E		BUF600X1	OPA646X
INA102	OPA445	INA102E	OPA445E	ACF2101M	BUF600X2	**OPA648X**
INA103	OPA501	INA103E	OPA501E		BUF601X1	**OPA650X**
INA105	OPA502	INA105E	OPA502E	OPA27M	BUF601X2	**OPA658X**
INA106	OPA511	INA106E	OPA511E	OPA604M	**BUF634X**	**OPA2658X**
INA110	OPA512	INA110E	OPA512E	OPA628M		**OPA4658X**
INA111	OPA541	INA111E	OPA541E	OPA671M	ISO120X	OPA660X1
INA114	OPA602	INA114E	OPA602E	OPA675M	ISO121X	OPA660X2
INA115	OPA604	**INA115E**	OPA604E	OPA676M	**ISO130X**	
INA117	OPA606	INA117E	OPA606E	OPA2604M		
INA118	OPA620	**INA118E**	OPA620E		MPC100X1	
INA120	OPA621	INA120E	OPA621E	VCA610M	MPC100X2	
INA131	OPA627	**INA131E**	OPA627E		**MPC102X1**	
	OPA637		OPA637E		**MPC104X1**	
OPA27	OPA1013	OPA27E	OPA1013E			
OPA37	OPA2107	OPA37E	OPA2107E		OPA603X	
OPA77	OPA2111	OPA77E	OPA2111E		OPA620X	
OPA111	**OPA2131**	OPA111E	**OPA2131E**		OPA621X	
OPA121	OPA2541	OPA121E	OPA2541E		OPA622X1	
OPA124	OPA2604	OPA124E	OPA2604E		OPA622X2	
OPA128	**OPA4131**	OPA128E	**OPA4131E**		OPA623X1	
OPA129		**OPA129E**			OPA623X2	
OPA131	**OPT101**	**OPA131E**	UAF42E		OPA640X	
OPA177	**OPT201**	OPA177E			**OPA641X**	
	OPT202				OPA642X	
	OPT209				OPA643X	
	OPT211				**OPA644X**	
	UAF42					